Guest Editorial
IEEE 2022 BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium

THE Special Section of the IEEE JOURNAL OF SOLID-STATE CIRCUITS features expanded versions of selected articles presented at the 2022 BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) held in Phoenix, AZ, USA, on October 16–19, 2022. The first three invited papers demonstrate advances in indium phosphide (InP) heterojunction bipolar transistor (HBT) and SiGe BiCMOS clock generation circuits with the highest harmonics frequency 4 THz in silicon IC. Their techniques overcome the limitations of phase locked loop (PLL)-based circuits where output frequency is limited by the maximum oscillation frequency of a VCO. The fourth paper addresses best-in-class linearity along with power efficiency of a single-stage InP HBT power amplifier IC in 27 GHz–48 GHz frequency range employed by 5G wireless systems.

In [A1], Thomas et al. describe how a 1960s idea for harmonics generation with a step-recovery diode is implemented in a standard SiGe process by integrating a p-i-n-diode with a 130-GHz Colpitts oscillator and folded dipole antenna. The chip radiates harmonics power at frequencies up to 4 THz. Their intensity was measured and characterized by the corresponding SNR. It allows to assess its suitability as a silicon-based source for a variety of THz-range applications such as imaging, gas spectroscopy, and Doppler radar.

In [A2], Soylu et al. report two InP HBT 8:1 and 16:1 frequency multipliers aiming at 280 GHz output frequency. The multipliers use cascaded push-push emitter-coupled-pairs serving as balanced frequency doublers with a 1:1 transformer; the 16:1 multiplier has an additional input emitter-coupled push–push doubler with the input generated by a transistor differential input stage.

In [A3], Romstadt et al. present the feasibility of a fully integrated SiGe x12 frequency multiplier chain comprising two frequency doubling and one frequency tripling stage. Each stage uses an architecture that ensures high harmonic rejection at its output and in the end at *D*-band x12 output.

Finally, In [A4], Kobayashi et al. detail a design methodology and a prototype IC of a single-stage 4-way combined power amplifier targeting highest linearity for a selected HBT circuit topology. As a result, the low level of IP3 distortions is achieved without boosting DC power dissipation with superior figure of merit for two-tone IP3 linearity over DC power dissipation.

YURIY M. GRESHISHCHEV
Ciena Corporation
Ottawa, ON K2K 0L1, Canada

APPENDIX: RELATED ARTICLES

[A1] S. Thomas et al., "A 0.4-4 THz p-i-n diode frequency multiplier in 90-nm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, early access, Jul. 4, 2023, pp. 2407–2420.

[A2] U. Soylu, A. Alizadeh, M. Seo, and M. J. W. Rodwell, "280-GHz (×8) frequency multiplier chains in 250-nm InP HBT technology," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Oct. 2022, pp. 191–194.

[A3] J. Romstadt et al., "A 117.5–155 GHz SiGe × 12 frequency multiplier chain with push-push doublers and a Gilbert cell-based tripler," *IEEE J. Solid-State Circuits*, early access, Jun. 22, 2023, pp. 2430–2440.

[A4] K. W. Kobayashi, P. Partyka, T. Howle, T. Sellas, and L. Hayden, "A high linearity Ka-band InP HBT MMIC amplifier with 19.8:1 IP3/Pdc LFOM at 48 GHz," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Oct. 2022, pp. 128–131.

Digital Object Identifier 10.1109/JSSC.2023.3294068

Yuriy M. Greshishchev (Senior Member, IEEE) received the M.S.E.E. degree from Odessa Electrotechnical Institute of Communications, Odessa, Ukraine, in 1974, and the Ph.D. degree in electrical and computer engineering from the Microelectronics Division, Institute of Cybernetics, Kiev, Ukraine, in 1984.

He held a post-doctoral fellow position with the University of Toronto, Toronto, ON, Canada, from 1994 to 1995, where he conducted research on GaAs MESFET wireless circuits. He joined Nortel Networks (now Ciena), Ottawa, ON, Canada, in 1996, where he worked on III–V, SiGe, and CMOS integrated circuits for optical communications. He is currently a Senior Technical Advisor on the Silicon SoC Research and Development Team for optical transport products and a Data Converter Architect for optical communication ASICs. He is the coauthor of three books and more than 50 technical papers and is named on 13 patents in the field of data converters and high-speed circuit design.

Dr. Greshishchev, in 2014, and again in 2016, was nominated to IEEE fellow grade for early work on 10 GB/s SONET SiGe BiCMOS clock and data recovery circuits as well as for the industry's first 40 Gss CMOS 6-bADC and 56GS/s 6-b DAC designs for optical communications. He is a Ciena Distinguished Engineer. He served for the IEEE International Solid State Circuits Conference (ISSCC) International Technical Program Committee (ITPC) from 2001 to 2009. He has been with the IEEE Symposium on Compound Semiconductor Integrated Circuit (CSICS) TPC since 2014 and is now a BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) ExCom Member. For more than two decades, he taught tutorials, and co-organized and participated in High-Speed Circuit Design Forums and Workshops at ISSCC, VLSI Symposium, CSICS, BCICTS, Workshop on Advances in Analog Circuit Design (AACD), and Mead Education. He is a co-recipient of the 2008 IEEE ISSCC Special Topic Evening Award for the topic "Trends and Challenges in Optical Communications Front-End." He was a Guest Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS, December 2005 issue.