A 117.5–155-GHz SiGe ×12 Frequency Multiplier Chain With Push-Push Doublers and a Gilbert Cell-Based Tripler

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***Abstract*— In this work, we present a fully integrated *D*-band ×12 SiGe-based frequency multiplier chain. It comprises two frequency doubling and one frequency tripling stage. Each stage uses an architecture that ensures high harmonic rejection at its output and, thus, ultimately, at *D*-band frequencies. The focus of this work is on describing the generation and propagation of harmonic components in the multiplier chain. Measurements show a maximum output power of 3.5 dBm and a 3-dB bandwidth of 37.5 GHz covering the range from 117.5 to 155 GHz. Over the entire *D*-band, the output power varies by 9 dB. The power consumption equals 0.64 W. The harmonic rejection at the center frequency is approximately 24.5 dBc and within the 3-dB bandwidth, always above 19.5 dBc.**

***Index Terms*— Active balun, *D*-band, frequency doubler, frequency multiplier, frequency tripler, harmonic rejection, push-push doubler, SiGe.**

I. Introduction

AMONG popular alternatives (RFCMOS and Section III-V semiconductors), SiGe BiCMOS has established itself as the preferred technology for *D*-band (110–170 GHz) usage due to its high integration capabilities while still maintaining sufficiently high output power [1]. The use of SiGe in *D*-band applications concerning fields such as data communication, high-resolution imaging, or distance/velocity measurements is presumed to rise significantly. This increase is also attributable to frequency classifications, including the unlicensed 122–123-GHz ISM band, a future potential automotive band [2], and locally (US/U.K./EU) approved industrial frequency bands (>100 GHz) [3].

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A prime example of a high-resolution imaging and distance/velocity measurement system is given in [4], which uses a single reference signal to drive numerous channels in multiple monolithic microwave integrated circuits (MMICs) in a synchronous MIMO configuration. If one were to apply this reference signal directly as a *D*-band signal, high distribution losses in terms of transmission and signal division in conjunction with a more demanding signal generation/less tunable VCO are to be expected [1], [5]. Both culminate in an increased design effort for high-frequency sources compared with similar performing frequency-multiplied lower frequency sources. Hence, the latter is often used despite its higher area consumption. This economic shortcoming can be partially offset using lower cost laminates and cheap commercially available frequency sources. However, a need for spectrally pure, high-performing multiplication stages becomes undeniable, typically met by cascading frequency doubling (x2) and tripling stages (x3).

To accentuate the potential of frequency multipliers regarding spectral purity, output power, and bandwidth, a x12 multiplier chain designed in Infineon's 130-nm SiGe BiCMOS technology B11HFC [6] showcases a cascade of two x2 stages and one x3 stage. The target frequency range corresponds to the *D*-band.

II. System Considerations

When using high multiplication factors, a careful design is essential to reach the desired spectral purity. For each frequency, multiplication generates harmonic components called spurs in addition to the desired harmonic. When multiplying a signal with a frequency f_0, the spurs appear at $h \cdot f_0$, where h is the harmonic number, excluding the desired multiplication factor. A higher factor is needed to reach a desired output frequency with a lower fundamental frequency f_0. The higher the multiplication factor, the lower f_0, and the more spurs appear in or near the target frequency range. Fig. 1 illustrates this relationship, with the hatched area displaying the *D*-band as the target frequency range and differently sized arrows representing either the desired harmonic or its spurs. Since two vastly different multiplication factors, ×4 and ×12, are showcased, the spurs' total number and the frequency difference between neighboring spurs differ

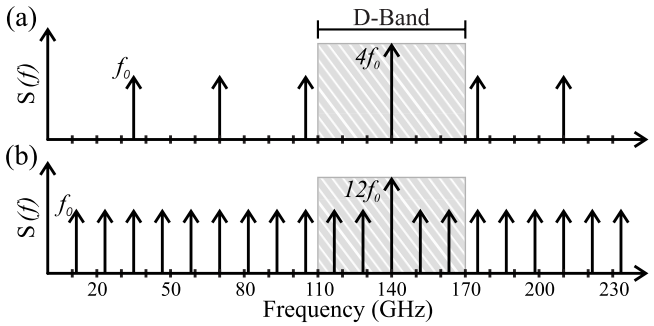

Fig. 1. Harmonics occurring when a 140-GHz signal is generated with (a) ×4 and (b) ×12 multiplication. For higher multiplication factors, more spurs appear in and near the hatched region, illustrating the target frequency range (*D*-band).

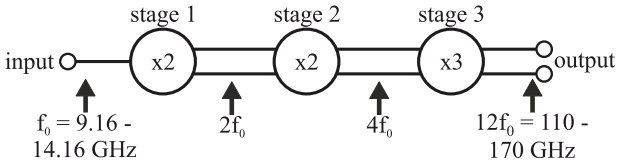

Fig. 2. Simplified block diagram of the ×12 frequency multiplier chain consisting of two frequency doubling and one frequency tripling stage.

substantially. Hence, unwanted harmonic components appear in the target frequency range and cannot be filtered out in the case of ×12 multiplication.

Achieving very high harmonic rejections on a chip is mainly restrained by the reduced quality factors of passives and filters [7] when compared with discrete or waveguide-based components. Nevertheless, through careful design considerations, high spectral purity is accomplished in this work using an ×12 multiplier chain. It consists of a cascade of two ×2 multipliers and one ×3 multiplier in accordance with Fig. 2. While each of those stages exhibits harmonic spurs that may lead to undesired mixing and intermodulation products, high harmonic rejections at the output of each stage diminish the influence.

III. Push-Push Doubler Fundamentals

Push-push doublers are used multiple times in the ×12 multiplier chain for frequency doubling. The theory of these doublers is described in several works. However, they refer only to either small-signal operations [8] or use the idealized assumption that the circuit's load corresponds to an ideal resonator tuned to the 2nd harmonic of the excitation frequency [9]. Hence, we explain the theory for the large-signal operation without an output resonator in the following.

Ideally, a frequency doubler would only double the frequencies applied to its input. However, a push-push doubler has the inherent characteristic of generating additional harmonics. By considering the simplified schematic of a push-push doubler, as shown in Fig. 3, the output voltage is

$$V_{\mathrm{OUT}} = V_{\mathrm{CC}} - R_L \cdot (I_{C1} + I_{C2}). \tag{1}$$

Similar to the derivations in [8] and [9] to determine a push-push doublers' output voltage, using Shockley's equation resolves the currents I_{C1} and I_{C2}

$$I_{C1,2} = I_S \cdot \left(e^{\frac{V_{\mathrm{BE1,2}}}{n \cdot V_T}} - 1\right). \tag{2}$$

Therein, I_S is the reverse bias saturation current, V_T is the thermal voltage, and n is the ideality factor. If the differential monofrequent signal V_{IN} with $f_{\mathrm{IN}} = (\omega_{\mathrm{IN}}/2\pi)$ is applied, the voltages V_{BE1} and V_{BE2} can be expressed by the same Fourier series but with one being delayed by half a period of their fundamental frequency compared with the other one

$$\frac{V_{\mathrm{BE1}}}{nV_T} = \sum_{l=-\infty}^{\infty} c_l \cdot e^{jl\omega_{\mathrm{IN}}t} = \sum_{l\in\mathbb{Z}} c_l \cdot e^{jl\omega_{\mathrm{IN}}t} \tag{3}$$

$$\frac{V_{\mathrm{BE2}}}{nV_T} = \sum_{l\in\mathbb{Z}} c_l e^{jl\omega_{\mathrm{IN}}\left(t-\frac{2\pi}{2\omega_{\mathrm{IN}}}\right)} = \sum_{l\in\mathbb{Z}} (-1)^l \cdot c_l \cdot e^{jl\omega_{\mathrm{IN}}t}. \tag{4}$$

This mathematical approach considers any nonlinearities in V_{BE1} and V_{BE2}. Using the Taylor series of the exponential function for the currents I_{C1} and I_{C2}, the sum $I_{C1} + I_{C2}$ can be expressed with the use of (3) and (4)

$$I_{C1} + I_{C2} = I_S\left(-2 + e^{\frac{V_{\mathrm{BE1}}}{nV_T}} + e^{\frac{V_{\mathrm{BE2}}}{nV_T}}\right) \tag{5}$$

$$= I_S\left(-2 + \sum_{k=0}^{\infty}\frac{1}{k!}\left(\frac{V_{\mathrm{BE1}}}{nV_T}\right)^k + \sum_{k=0}^{\infty}\frac{1}{k!}\left(\frac{V_{\mathrm{BE2}}}{nV_T}\right)^k\right) \tag{6}$$

$$= \sum_{k=1}^{\infty}\frac{I_S}{k!}\left(\left(\sum_{l\in\mathbb{Z}} c_l e^{jl\omega_{\mathrm{IN}}t}\right)^k + \left(\sum_{l\in\mathbb{Z}}(-1)^l \cdot c_l e^{jl\omega_{\mathrm{IN}}t}\right)^k\right). \tag{7}$$

Reducing leads to

$$I_{C1} + I_{C2} = \frac{I_S}{1!}\sum_{l_1\in\mathbb{Z}}\left(1 + (-1)^{l_1}\right)c_{l_1}e^{jl_1\omega_{\mathrm{IN}}t} + \frac{I_S}{2!}\sum_{l_1\in\mathbb{Z}}\sum_{l_2\in\mathbb{Z}}\left(1 + (-1)^{l_1+l_2}\right) \times c_{l_1}c_{l_2}e^{j(l_1+l_2)\omega_{\mathrm{IN}}t} + \cdots \tag{8}$$

Consequently, the sum of the currents is

$$I_{C1} + I_{C2} = \sum_{k=1}^{\infty}\frac{I_S}{k!}\sum_{l\in\mathbb{Z}^k}\left(1 + (-1)^{\sum_{m=1}^{k} l_m}\right) \cdot \left(\prod_{m=1}^{k} c_{l_m}\right)e^{j\left(\sum_{m=1}^{k} l_m\right)\omega_{\mathrm{IN}}t}. \tag{9}$$

By substituting (9) into (1), the output voltage results in

$$V_{\mathrm{OUT}} = V_{\mathrm{CC}} - R_L \cdot \sum_{k=1}^{\infty}\frac{I_S}{k!}\sum_{l\in\mathbb{Z}^k}\left(1 + (-1)^{\sum_{m=1}^{k} l_m}\right) \cdot \left(\prod_{m=1}^{k} c_{l_m}\right)e^{j\left(\sum_{m=1}^{k} l_m\right)\omega_{\mathrm{IN}}t}. \tag{10}$$

Every summand in (10) contributes to one harmonic, whose order is $h = \sum_{m=1}^{k} l_m$. All the summands are multiplied by $1 + (-1)^h$, which equals zero for all odd h. In addition, each summand is multiplied by $(1/k!)$, which results in terms with a large k having only minor influence. Consequently, (10) shows the inherent characteristics of push-push doublers. Only

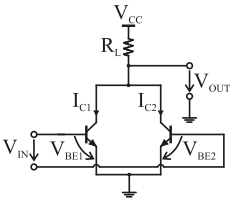

Fig. 3. Schematic of a push-push doubler to explain the principle of operation.

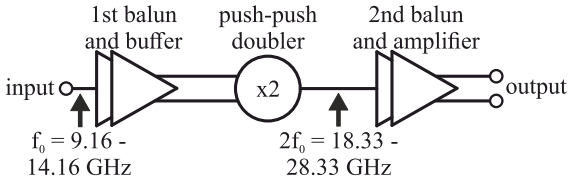

Fig. 4. Block diagram of stage 1. A single-ended input signal is converted into a differential signal through a 1st balun and buffer. This signal is frequency-doubled with a push-push doubler. A 2nd active balun with a subsequent amplifier generates a differential output signal.

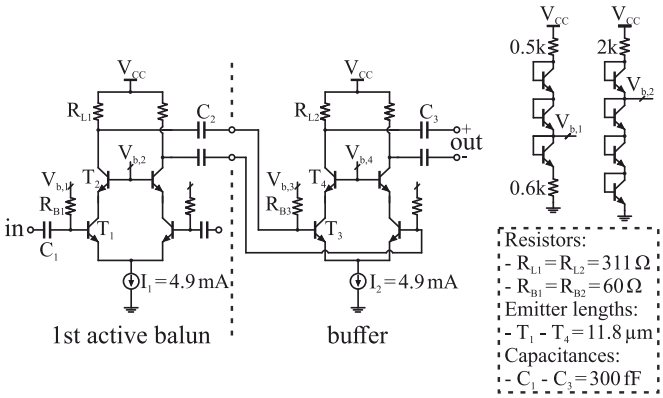

Fig. 5. Stage 1: Schematic of the 1st active balun and buffer. For simplicity, the current mirrors are illustrated as ideal current sources. The bias networks for $V_{b,1}$ and $V_{b,3}$ as well as of $V_{b,2}$ and $V_{b,4}$ are identical.

even harmonics of a differential monofrequent input signal are generated, and the relationship between harmonic number and amplitude is opposing. Therefore, push-push doublers are suited for integration in circuits with cascaded multipliers.

IV. Design and Implementation

A. Stage 1

Fig. 4 illustrates the block diagram of stage 1. This stage's input is single-ended to simplify a possible off-chip signal distribution in a system with multiple MMICs. The 1st active balun and its subsequent buffer convert an input signal into a differential signal and amplify it. Together, both the components take up significantly less area than passive baluns at the corresponding frequencies. Following the 1st balun/buffer sequence, the same reasoning applies for the push-push doubler compared with, e.g., bootstrapped Gilbert cells because they would ideally require a $\lambda/4$-line [10], [11]. Finally, the single-ended and frequency-doubled output signal is converted into a differential signal and amplified by the 2nd active balun and its subsequent amplifier.

For the ensuing simulation results of the first stage, the nominal MMIC supply voltage $V_{CC} = 3.3$ V was used, while −7.5 dBm of the input power was applied with a 50 Ω port. For differential usage, the output was terminated with a 100 Ω

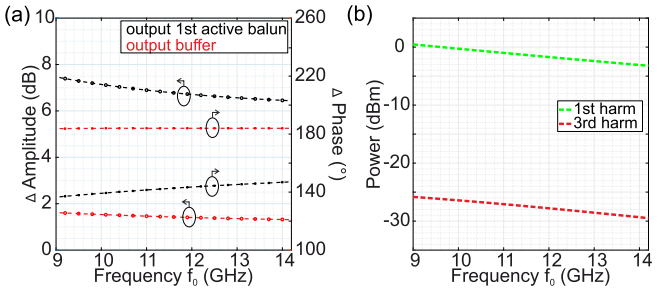

Fig. 6. Sole stage 1 simulation results: (a) Black illustrates the amplitude imbalance and phase difference of the differential signal at the output of the 1st active balun and red at the output of its subsequent buffer. (b) Power of different harmonics at the output of the buffer/input of the push-push doubler (1st harm = signal, min. rejection = 26 dBc).

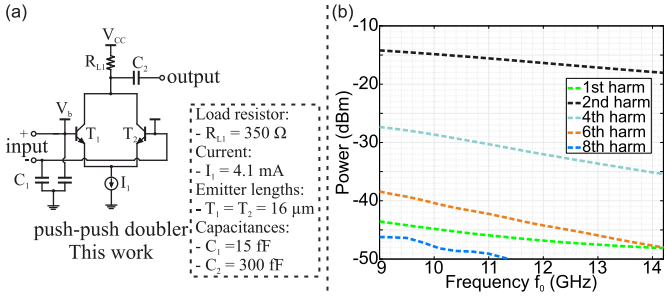

Fig. 7. Sole stage 1 results: (a) Schematic of the push-push doubler designed in this work. (b) Power of different harmonics at the push-push doubler's output (2nd harm = signal, min. rejection = 13 dBc). Due to the inherent behavior of the doubler, mainly even harmonics can be observed.

port. Each plot displaying a single-ended net will henceforth be normalized to 50 Ω, whereas differential nets will have a normalized impedance of 100 Ω. In addition, as for all the simulation results presented in this work, Sonnet EM-verified models were used for the transmission lines.

The circuit diagram of the 1st balun and its subsequent buffer is displayed in Fig. 5. For simplicity, the current mirrors are illustrated as ideal current sources. The buffer amplifies the signal and improves the amplitude imbalance and the phase difference between both parts of the differential signal. Fig. 6(a) shows the simulated amplitude imbalance and phase difference at the output of the 1st active balun and its successive buffer. Prior to the buffer, an amplitude imbalance and phase difference of 6.4–7.5 dB and 136–148°, respectively, are present. The values could be improved with higher impedance bias networks or a current source at the common-base node of the cascode stage. However, almost constant values of 1.45 dB and 184° are yielded at the output of the buffer. Aside from the showcased parameters, the spectral purity is presented in Fig. 6(b), which shows the relationship between the power of all the relevant harmonics, in this case, the 3rd and the 1st. From it, a minimum rejection of at least 26 dB can be determined.

For the push-push doubler designed in this work [Fig. 7(a)], the inherent characteristics according to (10) can be observed in Fig. 7(b). Mainly even harmonics are generated, and the relationship between harmonic number and amplitude is opposing. While the 4th harmonic has a minimum difference of at least 13 dB from the 2nd harmonic, the 6th harmonic already has a difference of over 24 dB. The 1st harmonic also appears in the output spectrum since the input signal of

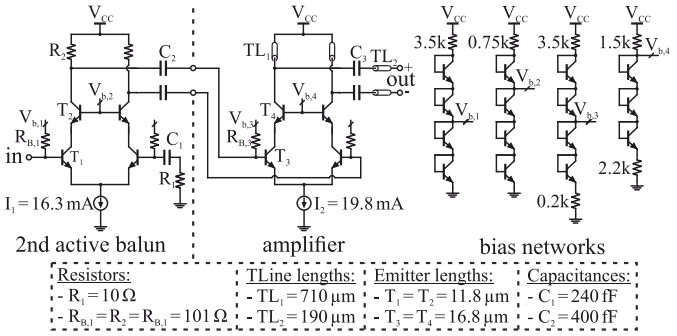

Fig. 8. Stage 1: Schematic of the 2nd balun and its subsequent amplifier. The architecture is comparable to Fig. 5. For simplicity, the current mirrors are illustrated as ideal current sources. The amplifier's transmission-line-based load introduces a filter characteristic.

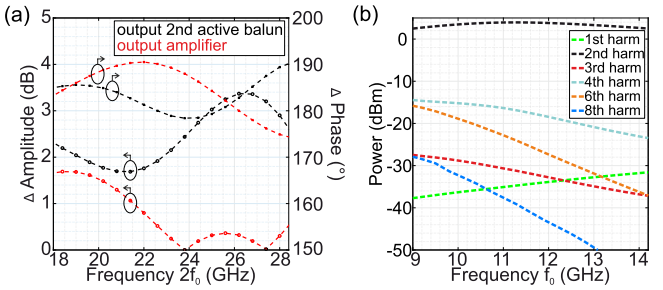

Fig. 9. Sole stage 1 simulation results: (a) Black illustrates the amplitude imbalance and phase difference of the differential signal at the output of the 2nd active balun and red at the output of its subsequent amplifier. (b) Power of different harmonics at the output of the amplifier/stage 1 (2nd harm = signal, min. rejection = 17 dBc).

the doubler is not ideally differential [Fig. 6(a)]. A crucial difference between the doublers in Figs. 3 and 7(a) is that the latter uses a current source, which is realized as a current mirror. This was used because it offers the advantage of setting a more stable operation point. Assuming that the current source would force a constant output current, a frequency-doubled output signal would not occur. However, this is not the case because both the transistors in the current mirror and the transistors in the differential pair have parasitic capacitances to ground. This makes the principle of operation between the doublers in Figs. 3 and 7(a) comparable.

To provide a differential signal with increased power to the next stage, the 2nd active balun and its subsequent amplifier, shown in Fig. 8, are used. To estimate the quality of the differential signal, Fig. 9(a) displays the amplitude imbalance and phase difference at the output of the 2nd active balun and its subsequent amplifier. Especially the amplitude imbalance between both parts of the differential signal is improved by the amplifier.

For the center frequency, the imbalance changes from >3 dB at the input to <0.4 dB at the output of the amplifier. Furthermore, Fig. 9(b) indicates that the 3-dB bandwidth of the amplifier's output signal exceeds the frequency range while providing a maximum power of 4 dBm to the second stage.

The amplifier's load TL_1, which is a transmission line, introduces a filter characteristic because it realizes a frequency-dependent impedance. Its length of 710 μm corresponds to an electrical length of about $(\lambda/10)$ at the center frequency of the desired 2nd harmonic and acts inductive. For frequencies in the approximate range from 51 GHz to 102 GHz, the corresponding electrical length roughly changes from $(\lambda/4)$ to $(\lambda/2)$, which leads to the transmission line characteristic approaching lower impedance values for higher frequencies. This is particularly apparent in the decreasing power of the 6th and 8th harmonics with an increase in frequency. In addition, the minimum rejection of the spurs to the 2nd harmonic is enhanced from 13 dBc at the output of the doubler to 17 dBc at the amplifier's output.

B. Stage 2

This stage also realizes frequency doubling and could have been realized with a mixer requiring two input signals for both its RF and LO, a modified mixer architecture as is the case with the bootstrapped Gilbert cells, or a push-push doubler. An architecture with a push-push doubler was chosen since such a doubler mainly generates even harmonics of all the applied input signal frequency components, as shown in (10).

One concept to obtain a differential output signal is to use a balun at the output of the doubler. However, for this stage, a different concept is used. As the block diagram in Fig. 10 illustrates, the input signal is converted into an IQ signal through a poly-phase filter (PPF). To compensate for the losses of the PPF, a preamplifier to each of the following push-push doublers is used in both the I and Q paths. Note that the components in both the paths have an identical design. The frequency-doubled single-ended output signals of both the doublers considered together result in a differential signal.

The concept of frequency doubling through IQ signal generation, however, results in a high harmonic rejection differential output signal [8]. For example, assume that the output voltage of one doubler is $V_{\mathrm{OUT},I}$ and that of the other is $V_{\mathrm{OUT},Q}$, respectively. Consequently, the differential output voltage is

$$V_{\mathrm{Diff}} = V_{\mathrm{OUT},Q} - V_{\mathrm{OUT},I}. \tag{11}$$

Assuming the in-phase voltages are covered by (3)–(10) and $V_{\mathrm{OUT},I}$ is given by (10), the quadrature voltages are

$$\frac{V_{\mathrm{BE1},Q}(t)}{nV_T} = \sum_{l\in\mathbb{Z}} c_l e^{jl\omega_{\mathrm{IN}}\left(t-\frac{2\pi}{4\omega_{\mathrm{IN}}}\right)} = \sum_{l\in\mathbb{Z}} (-j)^l \cdot c_l e^{jl\omega_{\mathrm{IN}}t} \tag{12}$$

$$\frac{V_{\mathrm{BE2},Q}(t)}{nV_T} = \sum_{l\in\mathbb{Z}} c_l e^{jl\omega_{\mathrm{IN}}\left(t-\frac{6\pi}{4\omega_{\mathrm{IN}}}\right)} = \sum_{l\in\mathbb{Z}} j^l \cdot c_l e^{jl\omega_{\mathrm{IN}}t}. \tag{13}$$

Performing calculations similar to (5)–(10), (12) and (13) result in

$$V_{\mathrm{OUT},Q} = V_{\mathrm{CC}} - R_L \cdot \sum_{k=1}^{\infty} \frac{I_S}{k!} \sum_{l\in\mathbb{Z}^k} \left(j^h + (-j)^h\right) \cdot \left(\prod_{m=1}^{k} c_{l_m}\right) e^{j\left(\sum_{m=1}^{k} l_m\right)\omega_{\mathrm{IN}}t}. \tag{14}$$

Substituting (10) and (14) into (11) leads to the output voltage

$$V_{\mathrm{Diff}} = R_L \sum_{k=1}^{\infty} \frac{I_S}{k!} \sum_{l\in\mathbb{Z}^k} \left(1 - j^h + (-1)^h - (-j)^h\right) \cdot \left(\prod_{m=1}^{k} c_{l_m}\right) e^{jh\omega_{\mathrm{IN}}t}. \tag{15}$$

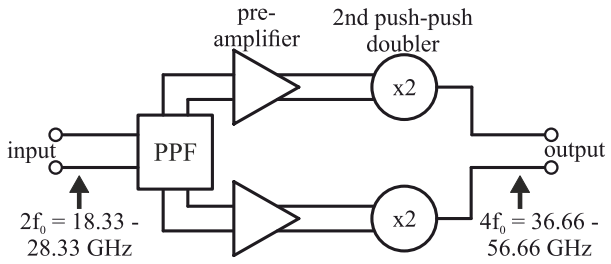

Fig. 10. Block diagram of stage 2. A PPF generates an IQ signal, which is frequency-doubled by push-push doublers, resulting in a differential output signal.

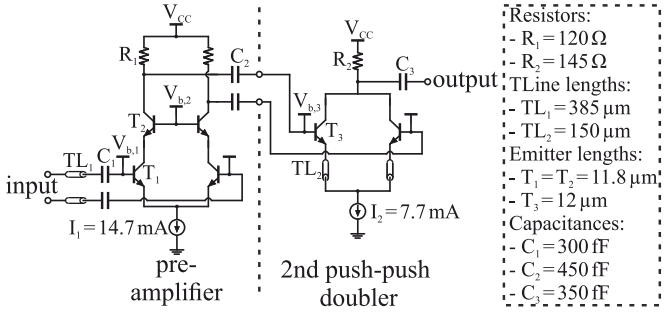

Fig. 11. Stage 2: Schematic of the 2nd balun and its preamplifier. Both the components are used in both the I and Q paths.

Analyzing (15), $1 - j^h + (-1)^h - (-j)^h$ reveals that only summands where $h = 2 + 4p, p \in \mathbb{Z}$ are nonzero. Consequently, not all even harmonics are present in the differential signal, but every 2nd even harmonic is eliminated. Hence, with the architecture chosen for stage 2, the 4th harmonic, which a push-push doubler inherently generates and is also its dominant spur, does ideally not appear. This is also the main advantage of the used concept compared with a frequency doubling concept, with one push-push doubler and a subsequent balun.

The generated IQ signals of the PPF do not necessarily have the same amplitude or exhibit a phase difference of precisely 90°. To estimate the influence of these nonidealities, the amplifier and subsequent doubler are considered first. Fig. 11 shows the circuit diagrams of both the components. Due to the connection between the PPF and the preamplifier, the amplifier possesses a 385-μm differential transmission line at its input. Furthermore, akin to the doubler in stage 1, the 2nd push-push doubler has a current source to set a stable operation point.

Stage 2 is first simulated without the PPF to determine the aforementioned influence. Instead, a 100-Ω port is applied at each preamplifier input and the differential output. The ports at the inputs always provide an added input power of −8 dBm. Fig. 12(a) shows the output power of the desired harmonic and its 4th harmonic rejection versus the phase difference of the input signals at the center frequency. Both are presented for an amplitude imbalance of the differential input signals of 0 and 1 dB, respectively. The output power and 4th harmonic rejection are maximum if the ports generate an ideal IQ signal. The output power varies by less than 1.2 dB for a phase difference in the range of 60°–120°. In the case of no amplitude imbalance, the 4th harmonic rejection is greater than 30 dBc in the range of 77°–103°. Both the output power and

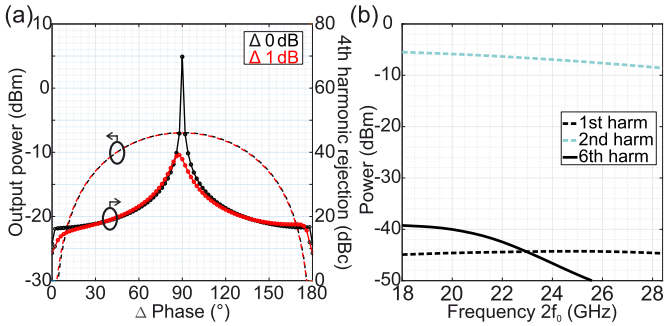

Fig. 12. Sole stage 2 simulation results excluding the PPF. Instead, an input signal is applied at each preamplifier input. (a) Output power and 4th harmonic rejection over the phase difference between both the input signals for an amplitude difference of 0 and 1 dB. (b) Power level of different harmonics for an ideal IQ input signal (2nd harm = signal, min. rejection = 33.7 dBc).

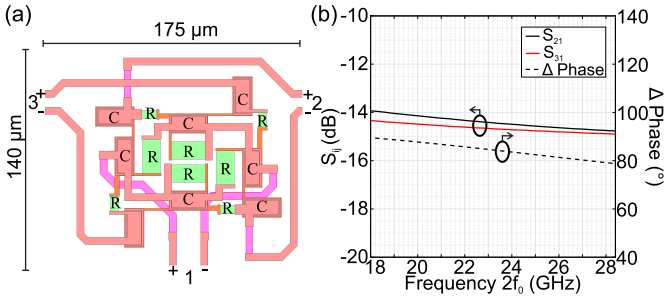

Fig. 13. Stage 2: (a) Layout of the PPF. For better illustration, the ground plane is hidden. (b) Sonnet EM-simulated insertion losses and phase difference between both the differential outputs of the filter.

the rejection are insensitive to amplitude imbalance. To show that no other spurs with relevant power occur, Fig. 12(b) displays the output power of the most significant harmonics for an ideal IQ input signal. The output power of the desired 2nd harmonic is in the range of −9.4 to −5.5 dBm over the entire bandwidth and always provides a harmonic rejection greater than 33.7 dBc.

The layout of the two-stage PPF is inspired by [12] and resembles a ring structure, as depicted in Fig. 13(a). TaN resistors and MiM capacitors, which are both located within the upper layers of the metal stack, were used for the layout. Fig. 13(b) shows the simulation results of the depicted layout obtained using Sonnet EM. The insertion losses S_{21} and S_{31} amount to 14.5 dB on average and their difference never exceeds 0.5 dB. In the worst case, the phase difference between the differential output signals has a maximum deviation of 13° from the ideal IQ value. However, the layout of the PPF might be prone to process variations. Therefore, a Monte Carlo simulation of the PPF was performed to be able to determine their influence. Due to the scope of the Monte Carlo simulation, the PPF was simulated with lumped-element models for the resistors and capacitors instead of with Sonnet EM. The corresponding results for the amplitude imbalance and phase difference are shown in Fig. 14. Process variations in 3σ can result in a phase difference of about 78° at the center frequency, and thus a 4th harmonic rejection of about 28 dBc [see Fig. 12(a)]. The results of the PPF, obtained with Sonnet EM, are used in all the following simulations.

Fig. 15 shows the simulation results of the second stage, where an input signal with a power of 3 dBm is fed to

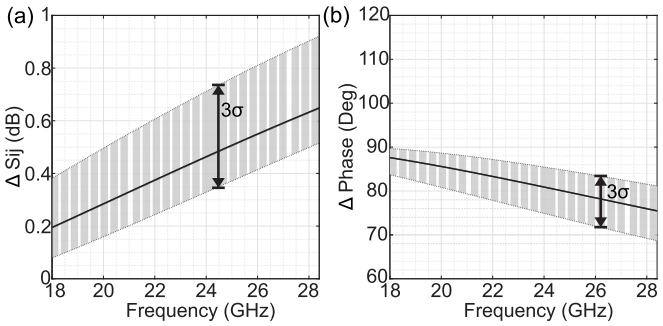

Fig. 14. Stage 2: Monte Carlo simulation regarding process variations in the PPF. For the resistors and capacitors, lumped-element models were used. (a) Difference of the insertion losses $S_{21,\mathrm{dB}}$ and $S_{31,\mathrm{dB}}$ and (b) phase difference between the differential output signals.

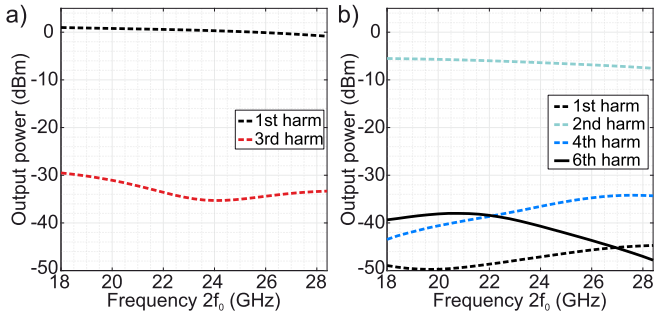

Fig. 15. Sole stage 2 simulation results: Power level of different harmonics at (a) preamplifier output/2nd push-push doubler input (1st harm = signal, min. rejection = 30.5 dBc) and (b) output of stage 2 (2nd harm = signal, min. rejection = 26.7 dBc).

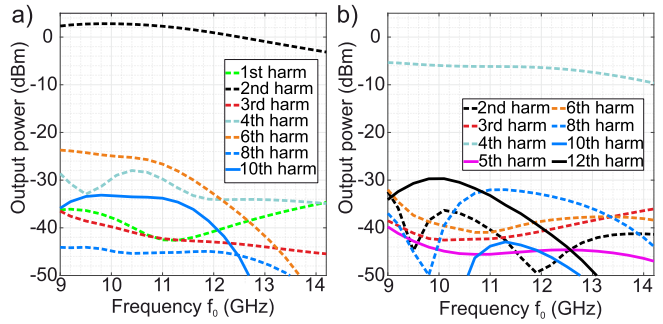

Fig. 16. Simulation results including stage 1 and stage 2: Power level of different harmonics at (a) preamplifier output/2nd push-push doubler input (2nd harm = signal, min. rejection = 25 dBc) and (b) output of stage 2 (4th harm = signal, min. rejection = 23.7 dBc).

the input of stage 2/the PPF. The output power of relevant harmonic signal components at the output of one preamplifier is illustrated in Fig. 15(a), and the power at the differential output of the stage is shown in Fig. 15(b). At the output of the amplifier, the 3rd-order intermodulation product occurs with a minimum rejection of 30.5 dBc to the desired signal component. Due to frequency doubling, the desired 2nd and undesired 6th harmonics occur at the output of stage 2. As the signals generated by the PPF are not ideal, the 1st and especially the 4th harmonics also appear with a relevant maximum power of −46 dBm and −35 dBm, respectively. This results in a minimal harmonic rejection of 26.7 dBc.

However, these results are obtained by applying an ideal input signal, which is not the case considering that stage 1 provides a signal with multiple harmonics at its output,

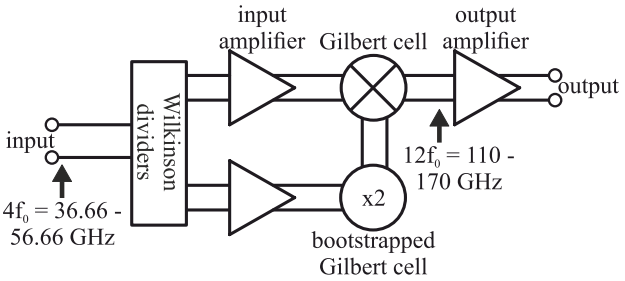

Fig. 17. Block diagram of stage 3. Two signal paths that lead to a Gilbert cell are generated using two Wilkinson dividers. In one of the two paths, the frequency is doubled, resulting in a frequency-tripled output signal.

as shown in Fig. 9(b). To evaluate how stage 1 and stage 2 interact, both the stages are connected to each other. The according simulation results are displayed in Fig. 16. Here, an input power of −7.5 dBm was applied with a 50-Ω port to the input of stage 1. The output of stage 2 was terminated with a differential 100-Ω port. At the output of the preamplifier and at the output of stage 2, significantly more harmonics than in the sole stage 2 simulation results depicted in Fig. 15 are present. By comparing the stage 2 input signal in Fig. 9(b) with an output signal of one preamplifier in Fig. 16(a), it is noticeable that mostly the same harmonics occur and that the minimum harmonic rejection increased by 8 dB. The rejection has increased due to the frequency-dependent insertion losses of the PPF and frequency-dependent amplification of the preamplifier. The output signal of stage 2, as illustrated in Fig. 16(b), contains a large number of harmonics, e.g., caused by intermodulation and mixing in active components. Nevertheless, even harmonics are mainly prevalent in the output spectrum due to the push-push doublers in both the stages.

C. Stage 3

By means of stage 3, frequency tripling is achieved. One way to realize a frequency tripler is to apply a large input signal to an active component/amplifier to generate harmonics of the input frequency. The 3rd harmonic at the output of such a harmonic-based frequency tripler is then amplified and all other harmonics are filtered out. An example of this is given in [13]. Operating transistors in the large-signal regime, however, requires a meticulous design because effects such as self-biasing or power-dependent impedances must be considered. Consequently, a broadband design of such a circuit is very challenging. Therefore, a different multiplication scheme based on the Gilbert cells is used instead. Fig. 17 illustrates the corresponding block diagram.

Using two identical Wilkinson dividers, the differential input is divided into two paths. One divider, whose layout is based on lumped elements as in [14], and the magnitude of its relevant S-parameters are illustrated in Fig. 18.

Up to frequencies of about 120 GHz, the magnitudes of S_{21} and S_{31} are each above −4 dB. Both the paths created by the Wilkinson dividers lead to a Gilbert cell. To ensure that a frequency-tripled signal is obtained at the output of the Gilbert cell, a frequency doubler is placed in one of the two paths. The architecture of a bootstrapped Gilbert cell was

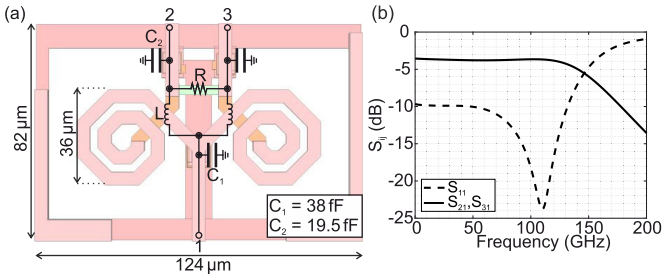

Fig. 18. Stage 3: (a) Layout of the lumped element Wilkinson divider and (b) magnitude of its *S*-parameters (simulated with Sonnet EM).

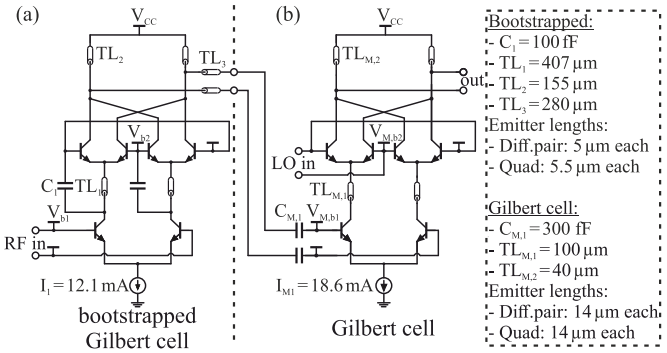

Fig. 19. Stage 3: Schematics of (a) frequency doubler realized as a bootstrapped Gilbert cell and (b) mixer realized as the Gilbert cell.

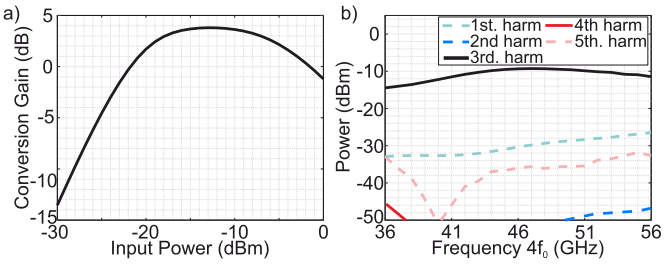

Fig. 20. Sole stage 3 simulation results excluding the output amplifier with (a) conversion gain at the center frequency and (b) harmonics at the Gilbert cell output for an input power of −13 dBm (3rd harm = signal, min. rejection = 15.5 dBc).

chosen for the frequency doubler. Since the signal frequencies in this stage are higher than in the previous stages, the required $\lambda/4$ line is less area-demanding than before. In addition, a bootstrapped Gilbert cell may exhibit gain and thus might increase the gain of the whole stage. As depicted in the schematic in Fig. 19, the bootstrapped Gilbert cell is connected to the RF input of the Gilbert cell. An amplifier precedes each frequency converter. The inputs of both the amplifiers are isolated from each other through the Wilkinson dividers. Both the amplifiers are in a fully differential cascode architecture with a resistive load and provide a wideband signal with sufficient power to their respective subsequent frequency converter.

To characterize the described frequency tripling architecture, the input of both the Wilkinson dividers and the output of the Gilbert cell are terminated with a 100-Ω port. Fig. 20(a) shows the corresponding conversion gain. It exceeds 0 dB even at input powers below −20 dBm and reaches a peak value of 3.8 dB at an input power of −13 dBm. In addition, the Gilbert cells' output provides a variation

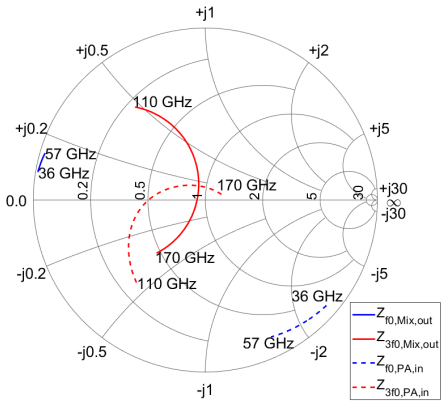

Fig. 21. Stage 3 simulation results: Smith chart illustrating the output impedance of the Gilbert cell (solid lines) and the input impedance of its subsequent amplifier (dashed lines). Impedances are shown in blue for the frequency range of the fundamental (36–57 GHz) and in red for the desired 3rd harmonic (110–170 GHz).

in output power below 5.3 dB over the frequency range considered in Fig. 20(b). The minimum 1st and 5th harmonic rejection equals 15.5 and 20.5 dBc, respectively. The 1st and 3rd harmonics would provide the same output power when assuming an ideal mixer instead of the Gilbert cell. However, the load of the Gilbert cell is realized by transmission lines. As a result, the load possesses a frequency dependence and therefore realizes a lower impedance for lower frequencies. The frequency-dependent load leads to the output impedance of the Gilbert cell being significantly lower at low frequencies. An illustration of this is given in Fig. 21, showing a Smith chart including the Gilbert cell's output impedance and its subsequent amplifier's input impedance for both the 1st and 3rd harmonics. The output match of the Gilbert cell at the desired 3rd harmonic has a significantly better match to an impedance of 100 Ω.

The amplifier is located at the output of the MMIC. It has a transmission-line-based load and is used to increase the output power of the broadband signal provided by the Gilbert cell. As can be seen in Fig. 21, the Gilbert cells' output and amplifiers' input are highly mismatched regarding the 1st harmonic.

For a final compact representation of all the stages, the circuits' complete block diagram with its most important quantities is shown in Fig. 22.

V. Measurement Results

A. Measurement Setup

Fig. 23 shows the measurement setup for the output power and the output spectrum of the ×12 multiplier chain. The chip input was fed by a Keysight PSG signal generator and a 40A GS Picoprobe. Accordingly, the only difference between the setups is present at the chip's output. The power was measured using a *D*-band Infinity waveguide GSG probe from FormFactor, a VDI Erickson PM5B power meter, and a taper. Two measurements with different setups were performed with a UXA spectrum analyzer from Keysight to determine high-frequency harmonic components. To measure spectral components in the *D*-band, an Infinity waveguide GSG probe, a WR6.5 SAX from VDI, and a 20-dB attenuator were used.

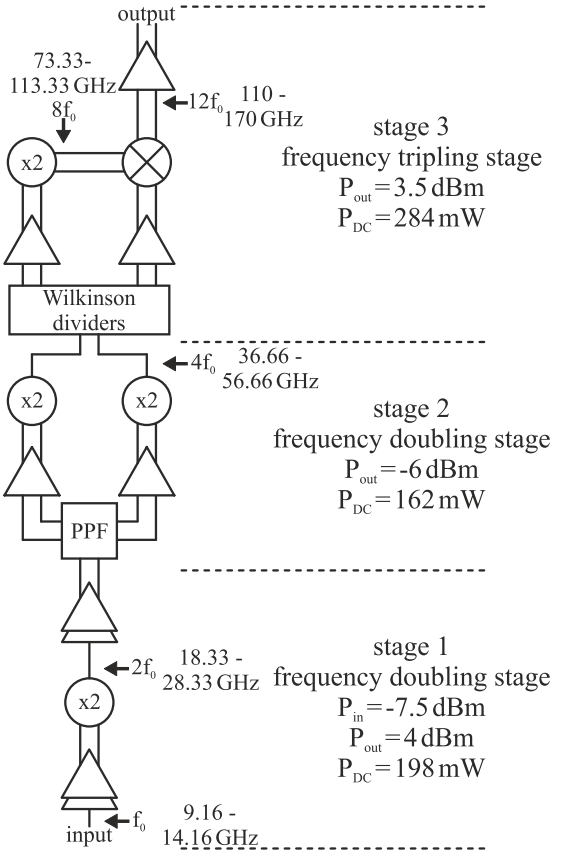

Fig. 22. Block diagram of the ×12 frequency multiplier chain.

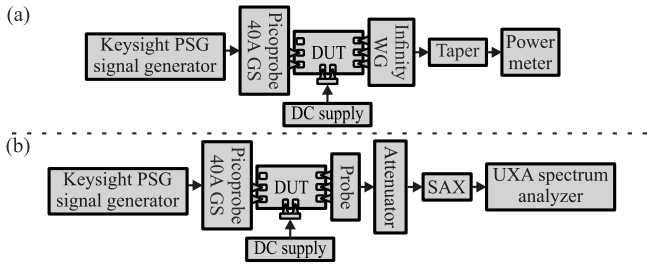

Fig. 23. Measurement setup of (a) output power and (b) spectrum. The spectrum was measured twice, once with *D*-band and once with *G*-band (140–220 GHz) equipment at the MMIC output.

For the frequency range of 140–220 GHz, a T-Wave 220 GSG probe from FormFactor and a WR5.1 SAX from VDI with its corresponding 20-dB attenuator were used instead.

B. Results

A chip micrograph of the ×12 multiplier chain with an overlay of the block diagram is given in Fig. 24. The current consumption and power consumption were determined to be 195 mA and 0.64 W, respectively.

The measured and simulated power of the output signal is shown in Fig. 25. Due to the single-ended equipment used for measurement, a 3-dB correction was applied. Any losses incurred by the probe and waveguide were also considered through de-embedding. A comparison of the simulation and measurement results reveals a high degree of agreement up to frequencies of 160 GHz. The 3-dB bandwidth of the system

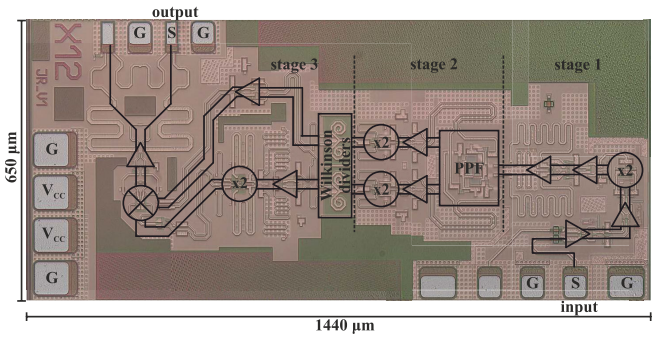

Fig. 24. Micrograph the ×12 multiplier chain with an overlay of the block diagram.

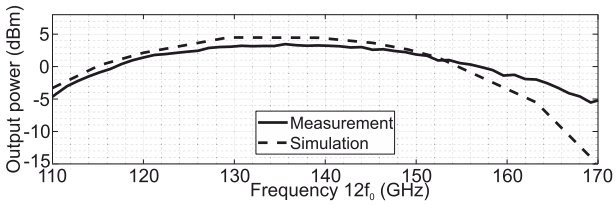

Fig. 25. Simulated and measured output power of the ×12 multiplier chain at an input power of −7.5 dBm.

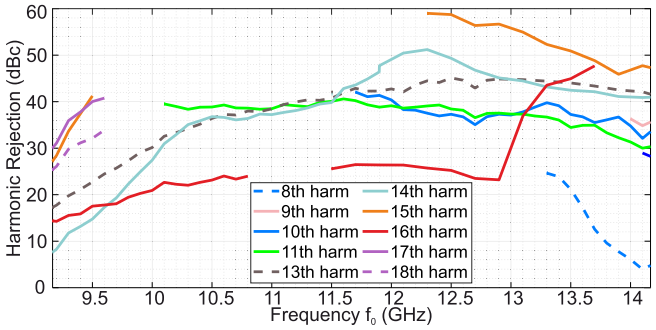

Fig. 26. Measured rejection of harmonics at the ×12 multiplier chain output over the input frequency at an input power of −7.5 dBm.

was determined to be 37.5 GHz, with a center frequency of 136.25 GHz. The output power displays a deviation of 9 dB across the entire *D*-band and a maximum output power of 3.5 dBm.

As illustrated in Fig. 26, a harmonic rejection at the center frequency of approximately 24.5 dBc is demonstrated. For input frequencies ranging from 9.25 to 13.8 GHz, the harmonic rejection exceeds 10 dBc. In comparison to Fig. 20(b), significantly more harmonic signal components are present at the output because the signal at the input of stage 3 is not monofrequent [see Fig. 16(b)]. Especially, the 6th and 8th harmonics, resulting from the inherent characteristics of the push-push doublers, lead to additional intermodulation products. As a result, the 14th and 16th harmonics are observed at the output of the ×12 multiplier. Alongside these harmonics, the 8th harmonic exhibits comparatively low rejection, particularly at high frequencies. Above an input frequency of 13.8 GHz, the rejection is less than 10 dBc. As the frequency decreases, however, the rejection increases. It is thus expected that the 8th harmonic has a rejection higher than 25 dBc at input frequencies below 13.3 GHz. Due to the

TABLE I
COMPARISON OF *D*-BAND FREQUENCY MULTIPLIER CHAINS WITH A MULTIPLICATION FACTOR OF FOUR OR HIGHER

Ref.	Technology (nm)	xN	Frequency (GHz)	BW_{3dB} (GHz)	Conversion Gain (dB)	$P_{out,max}$ (dBm)	Min. Rejection at f_{center} (dBc)	Min. Rejection in BW_{3dB} (dBc)	Area (mm^2)	P_{DC} (mW)
[15]	130 SiGe	x4	110-135	25	1.4	2.7	30	21	0.42	45.2
[16]	130 SiGe	x4	129-171	44/42/44	5.5/4.5/3.2	2.2	32.5	21.5	0.61	100
[17]	130 SiGe	x4	124-132.5	8.5	3	4.4	-	-	0.66	115
[11]	130 SiGe	x4	100-140	40	26	4	-	-	0.45	132
[18]	130 SiGe	x5	114-126	12	-11	-3.8	42	35	0.86	59
[19]	120 SiGe	x6	112-145	33	1	4.5	19	10	0.55	310
[20]	250 InP	x6	100-125	25	-10.5	-3.5	9.5	6	0.46	20
[21]	250 InP	x6	139-179	40	-2	4.6	19	13	0.58	100
[22]	130 SiGe	x8	110-140	30	15	5.4	39	38	0.47	170
[23]	130 SiGe	x8	114-151	37	-	-7.4	21	13	4.34	1518
[23][1]	130 SiGe	x8	119-150	31	-	-4.7	34.5	26	4.34	1518
[24][1]	130 SiGe	x8	111.5-154	42.5	-	4.6	32.5	14	4.34	1904[2]
[25]	28 CMOS	x9	135-155	7.8/13.5/20	6.7/4.2/1.7	7.1	16.5 (sim.)	15.5 (sim.)	2.03[3]	77
[26]	65 CMOS	x9	117-129.3	12.3	-4	6.3	29	25.5	0.49	328
This work	130 SiGe	x12	117.5-155	37.5	19	3.5	24.5	19.5	0.94	640

[1]Octupler is part of a 4-channel transceiver MMIC. [2]Standalone, the inserted quadruper consumes 561 mW. [3]Area includes an on-chip antenna.

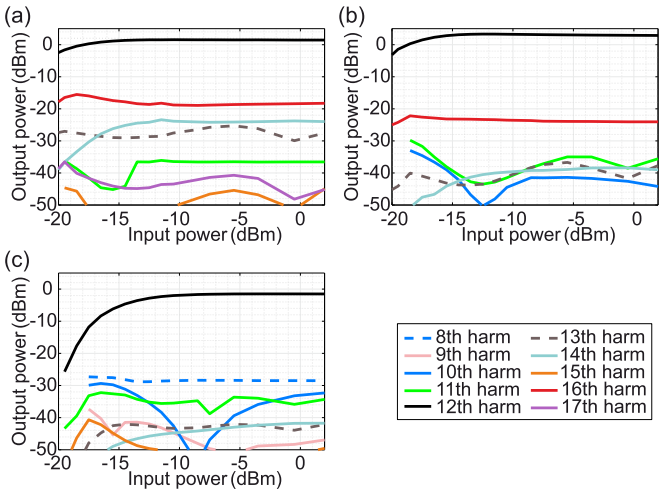

Fig. 27. Measured ×12 multiplier chain output power of different harmonics over the input power. (a) Input frequency f_0 = 10 GHz. (b) Input frequency f_0 = 11.67 GHz. (c) Input frequency f_0 = 13.33 GHz.

limitations and changes in measurement equipment, gaps in the curves of some harmonics can be observed. Fig. 27 shows the output power of different harmonic signal components versus the input power for three different input frequencies. According to Fig. 27(b), the maximum observed gain is 19 dB. For the most part, the input power has little effect on harmonic rejection and output power. For input powers above −15 dBm, the performance of the ×12 multiplier chain only changes marginally.

Different *D*-band frequency multiplier chains are considered in Table I. The ×12 multiplier chain presented in this work provides a comparably high 3-dB bandwidth. The output power is in the same order of magnitude as that of the other multiplier chains. Regarding the power consumption of frequency multiplier chains with a factor of 8 or higher, the ×12 multiplier chain consumes above average. The harmonic rejection at the center frequency and within the 3-dB bandwidth is competitive to all the multiplier chains despite the higher multiplication factor.

VI. CONCLUSION

This article presented an ×12 multiplier chain based on two frequency doubling stages and one frequency tripling stage. For each stage, an architecture was chosen that is suitable in terms of area consumption and also generates an output signal with a high harmonic rejection.

The 1st stage is based on active baluns and a push-push doubler. According to the presented push-push doubler theory, even harmonic spurs are mainly prevalent at the stages' output. For the 2nd stage, an architecture with a PPF and two push-push doublers was chosen. A mathematical derivation and the corresponding simulations of the circuit show that, for example, the 4th harmonic of the input signal does ideally not occur at the output. Adopting this architecture, the 2nd stage generates an output signal with a high harmonic rejection of at least 23.7 dBc. The 3rd stage realizes frequency tripling using one bootstrapped Gilbert cell and one mixer implemented as a Gilbert cell. This architecture enables a robust design compared with the harmonic-based frequency triplers, which operate in the large-signal regime. The Gilbert cell provides a wideband output signal and, due to its architecture, a minimum harmonic rejection of more than 15 dBc.

On account of the design of each stage, the ×12 multiplier chain generates a wideband *D*-band output signal with a high harmonic rejection. Measurements show a maximum output power of 3.5 dBm and a 3-dB bandwidth of 37.5 GHz. At the center frequency, which is 136.25 GHz, the minimum harmonic rejection equals 24.5 dBc. Even though the multiplier chain has a higher multiplication factor than other *D*-band multiplier chains, the results indicate a competitive performance. Regarding the usability of the multiplier chain in MIMO systems with multiple channels, it must be individually assessed whether the power consumption of 0.64 W is of concern.

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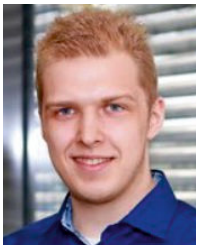

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