Design Aspects of Single-Ended and Differential SiGe Low-Noise Amplifiers Operating Above $f_{max}/2$ in Sub-THz/THz Frequencies

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***Abstract*— This article presents a single-stage single-ended (SE) and a multistage pseudo-differential cascode low-noise amplifiers (D-LNA) with their center frequencies at 235 and 290 GHz, respectively. Both low-noise amplifiers (LNAs) are designed beyond half of the maximum frequency of oscillation (f_{max}) in 130-nm SiGe BiCMOS technology with f_t/f_{max} of 300/450 GHz. Implications of gain-boosting and noise reduction techniques in cascode structure are analyzed and it is observed that beyond $f_{max}/2$, these techniques do not provide desired benefits. The single-stage SE LNA is designed to ascertain the theoretical analysis, and the same analysis is further implemented in staggered tuned four-stage LNA. Single-stage SE LNA provides a small signal gain of 7.8 dB at 235 GHz with 50 GHz of 3-dB bandwidth by consuming 18 mW of power. Four-stage differential LNA gives 12.9 dB of gain at center frequency 290 GHz and 11.2 dB at 300 GHz by drawing 68 mA current from the 2-V supply. The 3-dB bandwidth of differential LNA is measured to be 23 GHz. Noise figure measurements of both LNAs are performed using a gain-method technique with their measured noise figure values of 11 and 16 dB, respectively. This work successfully demonstrates the possibility of using a Si-based process to implement amplifiers beyond $f_{max}/2$. To the authors' best knowledge, the four-stage differential LNA achieves, without any gain-boosting technique, the highest gain at 2/3(f_{max}) with decent noise figure performance in SiGe technology.**

***Index Terms*— High current model (HICUM), low-noise amplifiers (LNAs), maximum frequency of oscillation (f_{max}), receivers, SiGe BiCMOS integrated circuits, sub-THz and THz integrated circuits, vertical bipolar intercompany model (VBIC).**

I. Introduction

FUTURE high-speed wireless technologies are dependent on the sub-THz and THz band of electromagnetic spectrum [1], [2], [3], [4]. In this aspect, IEEE 802.15.3d-2017 proposes the use of a sub-THz frequency range for point-to-point communication for data rates up to 100 Gb/s [5]. RF front-end design in the WR3.4 waveguide band (220–330 GHz) is very promising for future high-speed communication [6]. It has been analyzed that indoor range for radio link can be achieved at 300 GHz with decent antenna gain and quite moderate noise figure [7].

Consistent advancement in SiGe BiCMOS technology makes it a promising candidate to implement the sub-THz transceiver system [8], [9]. However, as discussed in [10], due to low gain and high noise figure offered by the Si-based semiconductor technologies in the sub-THz frequencies range, the mixer-first receiver is a common architecture in the sub-THz/THz transceiver system. This makes it suitable for a system with low SNR requirements with simple modulation techniques. An LNA-first receiver is required to fulfill the high SNR criterion. With their limited speed or maximum frequency of oscillation (f_{max}), new circuit topologies for low-noise amplification are being explored beyond the 200-GHz frequency range. Often in cascode and common base (CB) topologies, an inductor, as a positive feedback element is used to boost the power gain of the amplifier [11], [12], [13], [14], [15], [16], [17], [18], [19]. In [20], [21], [22], [23], [24], [25], and [26], the power gain of the amplifier is enhanced close to its unilateral gain by eliminating the reverse path using a lossy passive feedback network, and the feedback network is optimized to boost the power gain close to maximum achievable gain (G_{max}). However, previous art does not mention the impact of a lossy passive network on the noise figure of the amplifier. On the other hand, [27] presents the use of a recursive approach to optimize the Z-embedding to boost the gain. It also discusses the gain versus noise figure tradeoff when using the embedding technique. In [28], a theoretical study of a lossless feedback network of a low-noise amplifier (LNA) is analyzed without practical implementation. Spasaro et al. [29] provide a systematic method to make a compromise between gain and noise for a case where the matching network is lossy. The gm-boosting technique is also used to increase the overall power gain of the amplifier [30], [31], [32], [33], [34], [35]. Techniques mentioned in these works do not only enhance the power gain, but also reduce the noise contribution by the amplifier. However, the aforementioned work is done at frequencies much below the $f_{max}/2$ mark. In [35] and [36], SiGe BiCMOS technology achieves speed (f_{max}) of the transistor as high as 600 and 700 GHz, respectively. Due to their circuit operation below $f_{max}/2$, the amplifier offers relatively improved performance compared to the other state-of-the-art.

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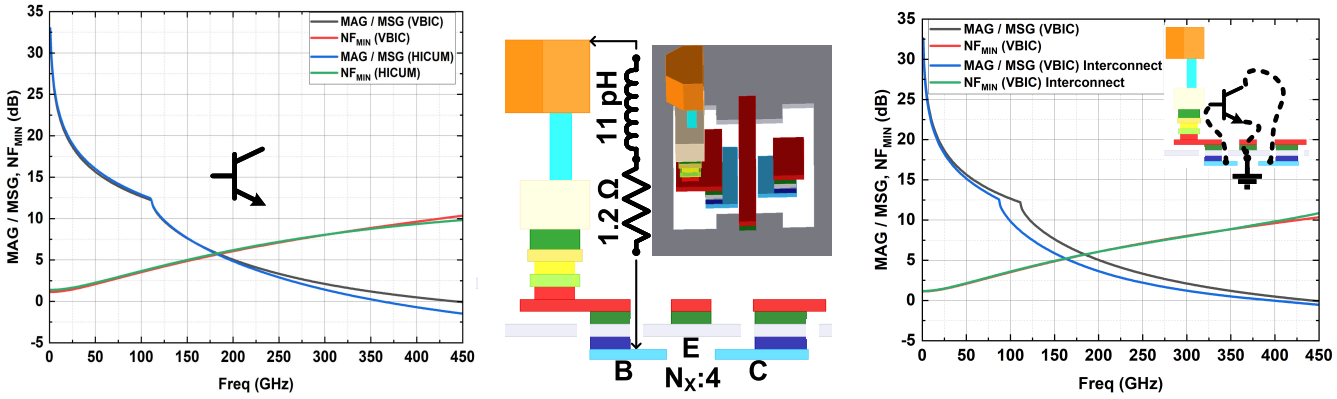


(a) (b) (c)

Fig. 1. (a) MAG/MSG and minimum noise figure (NF_{min}) of VBIC and HICUM models of SiGe HBT with a number of emitters (N_X) = 4. (b) Metal interconnect from M1 to TM2 and its parasitics. (c) MAG/MSG and NF_{min} of the VBIC model of SiGe HBT after metal interconnect.

This article presents two LNAs, which are operating beyond $f_{max}/2$. One is a single-ended (SE), single-stage amplifier, and the other is a four-stage differential amplifier operating at center frequencies of 235 and 290 GHz, respectively. This article expands the work on a four-stage LNA originally presented in [37] by providing its theoretical background. Theoretical analysis is done on the SE cascode amplifier operating beyond $f_{max}/2$. It clearly points out that the well-known g_m-boosting and noise-reduction technique using the base inductor at the CB transistor and the series inductor between the CB and common emitter (CE) transistor of cascode amplifier are not useful when operating beyond $f_{max}/2$. To ascertain the theoretical analysis, a single-stage amplifier was designed just above the $f_{max}/2$ frequency range. Second, a four-stage differential amplifier was designed at two-third of f_{max} using the same theoretical analysis by using the advantage of the differential design. Implementation of these two LNAs shows the opportunity to implement LNA-first receiver operating above $f_{max}/2$ frequency range in the 220–330-GHz band. In addition, the noise figure measurement technique, for frequency bands where commercial noise sources are not available, is presented.

The rest of the article is organized as follows. Section II describes aspects of the semiconductor technologies used to implement the low-noise amplifiers. Here, impacts of interconnect on the speed of transistors are also explained with the relative performance of VBIC and HICUM models of the heterojunction bipolar transistor (HBT) beyond $f_{max}/2$. Section III investigates sizing and gm-boosting of transistors, stability criterion, and noise reduction technique for the simple cascode topology. Subsequently, Section IV presents the design and implementation of both the SE and differential LNAs based on the analysis explained in previous sections. In Section V, small-signal, large-signal, and noise figure measurement setups are depicted. Here, measurement and simulated results are discussed and compared with the state-of-the-art. Finally, Section VI concludes the work.

II. Technology and Layout Description

The circuit is designed and fabricated with SG13G2 SiGe BiCMOS technology by innovation for high performance microelectronics (IHP) with f_t/f_{max} of 300 GHz/450 GHz [8]. The back-end-of-line (BEOL) of the process consists of 7 all-aluminum metal layers with five thin (M1–M5) and two thick (TM1–TM2) layers. A metal–insulator–metal (MIM) capacitor, having density of 1.5 fF/um^2, is formed using TM1 and M5 metal layers.

For circuit simulation, PDK offers a vertical bipolar intercompany model (VBIC) and high current model (HICUM/L2.3) of SiGe HBT with emitter area of 0.9 × 0.07 um^2. It is often recommended to use VBIC where a large number of HBTs are to be used and HICUM for high current operation [38]. In the PDK, HBTs are characterized below 100 GHz, and their performance is extrapolated to a higher frequency. Till the frequency of characterization, VBIC and HICUM models are well matched on various performance parameters. In order to design circuits at and above $f_{max}/2$, maximum available gain (MAG) and minimum noise figure (NF_{min}) of a single HBT with emitter area of 4 × 0.9 × 0.07 um^2 are plotted as shown in Fig. 1(a). It is observed that simulated NF_{min} of VBIC and HICUM models are well matched until given maximum frequency of oscillation (f_{max}) of 450 GHz. On the other hand, MAG of VBIC- and HICUM-modeled HBT start to deviate from each other around $f_{max}/2$ onward. HBT is biased for peak f_{max} with a collector current of 9 mA, where VBIC and HICUM models predict f_{max} of 441 and 362 GHz, respectively.

To design RF circuits, top metal layers are often used as reference planes to connect transistors with other parts of circuitry using interconnects. Parasitics of interconnects further lower f_{max} value from what technology offers at the transistor level. Consequently, interconnects are often optimized to compensate for the reduction in RF performance [39]. As shown in Fig. 1(b), parasitic inductance and resistance of interconnect are calculated between ports at the base (metal 1) of the HBT and the extrinsic connection at top metal 2 using following equations:

$$L_{EFF} = \frac{\mathrm{Im}\left(y_{11}^{-1}\right)}{\omega} \quad (1)$$

$$R_s = \mathrm{Re}\left(y_{11}^{-1}\right) \quad (2)$$

where y_{11} is obtained from the EM simulation of the interconnects. f_{max} of HBT is mostly affected by the base resistance (R_B) and collector–base capacitance (C_{CB}) [38]. R_B is

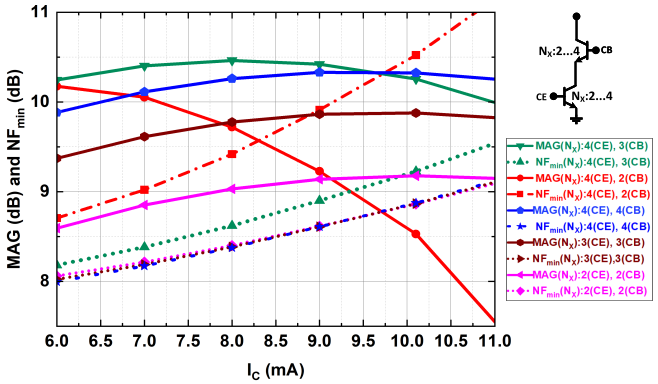


Fig. 2. Simulated MAG and NF_{min} versus bias current (I_C) for different combinations of CE and CB SiGe HBT sizes of the cascode amplifier. Bias current corresponding to peak f_{max} of HBT sized $N_X = 2$, 3, and 4 are 4, 6, and 9 mA, respectively.

combination of both intrinsic base resistance (r_{bi}) of HBT and series resistance (R_s) of interconnect at the base of HBT. Here, L_{EFF} is absorbed in the external matching networks, so only R_s and C_{CB}, caused by interconnects, mostly affect f_{max} of HBT. As shown in Fig. 1(b), by using stair-like interconnects from M1 to TM2 and large number of parallel vias, C_{CB} and R_s are minimized. Consequently, as shown in Fig. 1(c), f_{max} of HBT, with top metal 2 as a reference plane, is reduced by 44 GHz from 441 to 397 GHz which is less than that reported in [13]. On the other hand, NF_{min} of single HBT remains the same due to a relatively lower value of series resistance ($R_s = 1.2\ \Omega$) with respect of intrinsic base resistance ($r_{bi} = 22\ \Omega$).

III. Single-Stage SE Cascode Amplifier

A. Biasing and Sizing of HBTs

Cascode amplifiers offer higher gain, good isolation, higher output impedance, higher stability than CE topology, and better noise performance when compared to CB [17], [40]. Beyond $f_{max}/2$ frequency, the gain of the amplifier drops significantly which necessitates the operation of the cascode structure at a relatively high collector current. To make a balanced choice for a good gain and decent noise figure beyond $f_{max}/2$ frequencies, in the SE cascode amplifier, different combinations of transistor sizes were simulated over various collector currents (I_C). Here, N_X which implies a number of emitter fingers are varied to change the size of the transistor. It can be seen in Fig 2 that CE with $N_X = 4$ and CB with $N_X = 3$ combination gives better gain than other combinations but the poorest NF_{min}. On the other hand, CE with $N_X = 4$ and CB with $N_X = 4$ combination gives the best gain and the lowest NF_{min} over other combinations at higher current. A combination consisting of CE with $N_X = 4$ and CB with $N_X = 2$ suffers from the mismatch of required bias current corresponding to peak f_{max}. This leads to a fall in MAG and a rise in NF_{min}. Considering this, further design analysis is performed with cascode topology having both CE and CB HBTs with $N_X = 4$.

B. G_m-Boosting

To boost the gain of cascode structure, various techniques have been proposed where G_m-boosting is achieved either by an inductor at the base of the CB transistor (L_B) and/or by an inductor between the CE and CB transistors of the cascode (L_C) [11], [12], [13], [14], [15], [16], [17], [18], [30], [31], [32], [33], [34], [35]. However, previous works are implemented at frequencies below $f_{max}/2$. In [35], L_C- and L_B-based analytical study is presented near $f_{max}/3$ frequency range. Unfortunately, [35] had a few typos in the equations of G_m and pole frequencies. We correct them here and extend the analysis of effects of L_C and L_B to frequencies beyond $f_{max}/2$.

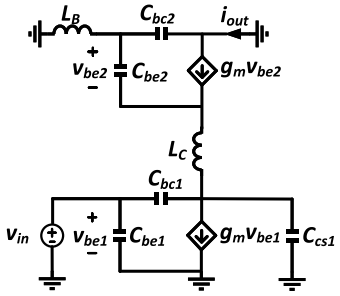


Fig. 3. Simplified small-signal model of the cascode amplifier for transconductance (G_m) equation.

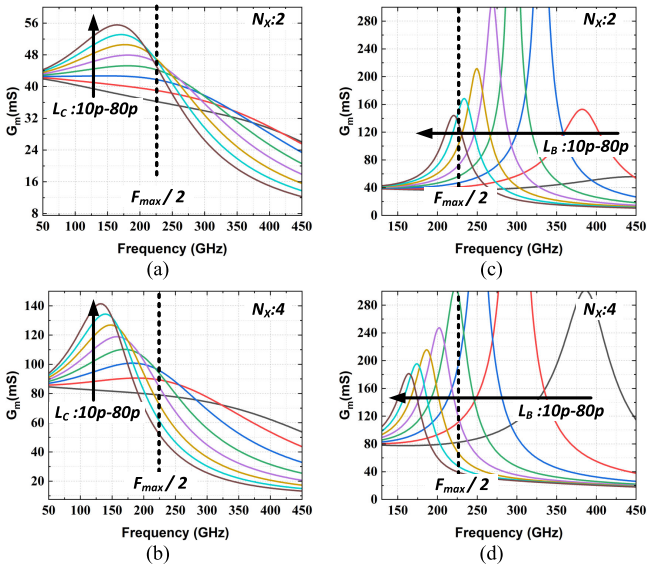


Fig. 4. Magnitude of G_m of ideal the cascode amplifier with HBT size of (a) $N_X = 2$ and parameterized with L_C, where $L_B = 0$, (b) $N_X = 4$, and parameterized with L_C, where $L_B = 0$, (c) $N_X = 2$ and parameterized with L_B, where $L_C = 0$, and (d) $N_X = 4$ and parameterized with L_B, where $L_C = 0$. Here, L_C and L_B are varied from 10 to 80 pH with a step size of 10 pH. All HBTs are biased at their peak f_{max}.

A simplified small-signal model of cascode structure with extrinsic inductors (L_C and L_B) is shown in Fig. 3. G_m of the cascode structure can be expressed as follows:

$$G_m = \frac{i_{out}}{v_{in}}\bigg|_{v_{out}=0}. \tag{3}$$

G_m-boosting using only L_C is analyzed and total G_m can be expressed as follows:

$$G_m = \frac{\text{AC}}{j\omega B + C\left(1 - \left(\frac{\omega}{\omega_1}\right)^2\right)} \tag{4}$$

where ω is the operating frequency and A, B, C, and ω_1 are given by the following equations:

$$A = g_{m_1} - j\omega C_{bc_1} \tag{5}$$

$$B = C_{bc_1} + C_{cs_1} \tag{6}$$

$$C = g_{m_2} + j\omega C_{be_2} \tag{7}$$

$$\omega_1 = \sqrt{\frac{1}{L_C(C_{bc_1} + C_{cs_1})}}. \tag{8}$$

It can be seen in Fig. 4(a) and (b) that due to L_C and corresponding capacitors, overall transconductance (G_m) of cascode peaks at pole frequency ω_1. As L_C goes up, it shifts the peak downward which restricts the use of the higher values of L_C to boost the gain of cascode topology at a higher frequency.

Similarly, G_m-boosting is analyzed using inductor L_B which is expressed by the following equation:

$$G_m = \frac{g_{m_2}A\left(1 - \left(\frac{\omega}{\omega_2}\right)^2\right) - jA\omega^3 L_B C_{be_2} C_{bc_2}}{j\omega B\left(1 - \left(\frac{\omega}{\omega_3}\right)^2\right) + C\left(1 - \left(\frac{\omega}{\omega_2}\right)^2\right)} \tag{9}$$

where the pole frequencies ω_2 and ω_3 are given by the following equations:

$$\omega_2 = \sqrt{\frac{1}{L_B C_{bc_2}}} \tag{10}$$

$$\omega_3 = \sqrt{\frac{1}{L_B(C_{be_2} + C_{bc_2})}}. \tag{11}$$

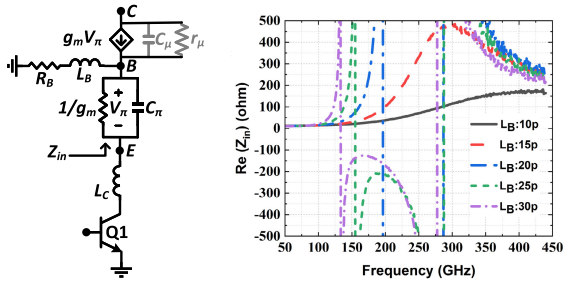
Similarly, as shown in Fig. 4(c) and (d), resonance peak, caused by L_B and corresponding capacitors, shifts downward as L_B values goes up. Here, the movement of G_m peaking is relatively larger than that caused by inductor L_C. This makes larger values of L_B unsuitable for gain boosting at higher frequencies, as well.

It can also be seen from Fig. 4 that intrinsic capacitances of CE and CB transistors increase with the size of transistors, which further shifts the resonance peaks to lower frequencies. Consequently, transistor with $N_X = 4$ with same value of L_C and L_B, which offers higher G_m than that of $N_X = 2$, witnesses G_m-boosting relatively at lower frequencies. This further restricts the applicability of G_m-boosting using L_C and L_B at and beyond $f_{max}/2$ in cascode amplifiers.

C. Stability Criteria

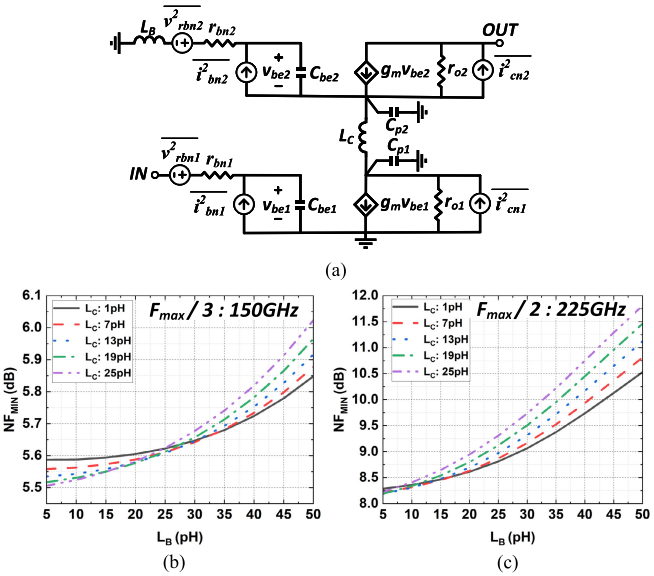
Inductor L_B at the base of the CB transistor of cascode introduces positive feedback to enhance the gain. This also leads to potential instability in the circuit. This can be analyzed by looking into input impedance in Fig. 5(a). The real part of the input impedance, as given by the following equation, should be positive to avoid potential instability in a cascode circuit:

$$\Re\{Z_{in}\} = \frac{\omega^2\left(R_B^2 C_\pi^2 - g_m L_B C_\pi\right) + g_m}{\omega^2 C_\pi^2 + g_m^2}. \tag{12}$$



(a) (b)

Fig. 5. (a) Simplified small-signal model of the cascode amplifier for input impedance equation for stability. (b) Re(Z_{in}) versus frequency for different values of L_b.



(a) (b) (c)

Fig. 6. (a) Simplified small-signal model of the cascode amplifier with its noise sources. (b) Minimum noise figure (NF_{min}) versus L_B parameterized over L_C at $f_{max}/3$. (c) NF_{min} versus L_B parameterized over L_C at $f_{max}/2$. All HBTs are biased at their peak f_{max}.

As shown in Fig. 5(b), as L_B increases, the real part of the input impedance tends to be negative. It can also be seen that as L_B value increases, Re(Z_{in}) becomes negative at lower frequencies. Fig. 5(b) depicts potential instability for L_B beyond 15 pH. It is important to note that HBT models are characterized below the 100-GHz frequency range, so careful selection of L_B value is to be done by operating away from the edge of potential instability. To design LNAs beyond $f_{max}/2$ frequency range, L_B less than 15 pH avoids potential instability.

D. Noise Analysis

In [30], [31], [35], and [41], an inductor between the CE/source and the CB/gate of the cascode network is utilized to minimize the noise figure of the circuit, where L_C is tuned to resonate away the parallel capacitances at the collector of the CE transistor (C_{p1}) and the emitter of the CB transistor (C_{p2}). Total noise figure can be defined by (13) where thermal noise contribution of bases (r_{bn1}, r_{bn2}) and shot noise currents (i_{bn1}, i_{cn1}, i_{bn2}, and i_{cn2}) of the CE and CB transistors are

included [41]

$$F_{\text{total}} = 1 + F_{r_{\text{bn1}}} + F_{i_{\text{bn1}}} + F_{i_{\text{cn1}}} + (F_{r_{\text{bn2}}} + F_{i_{\text{bn1}}} + F_{i_{\text{cn2}}})\left(1 + \left(\frac{1 - \left(\frac{\omega}{\omega_0}\right)^2}{\omega g_{m_2} L_c}\right)\right) \quad (13)$$

where

$$\omega_0 = \sqrt{\frac{1}{(C_{p1} || C_{p2}) L_c}}. \quad (14)$$

Equation (13) gives a good idea about a method where a series/parallel inductor could help to minimize the overall noise figure of the cascode amplifier. However, to avoid analytical complexity, it does not take the simultaneous role of L_B into account. Nonetheless, the contributions of L_B and L_C on the noise performance of the cascode amplifier can be analyzed in simulation. A small-signal model of cascode with its noise sources is shown in Fig. 6(a), where both L_B and L_C are simultaneously taken into consideration. As shown in Fig. 6(b) and (c), NF_{min} is plotted at $f_{\text{max}}/3$ and $f_{\text{max}}/2$, respectively. Here, NF_{min} is depicted over various L_B values with parameterized L_C and it can be observed that NF_{min} behaves differently at $f_{\text{max}}/3$ and $f_{\text{max}}/2$. At $f_{\text{max}}/3$, NF_{min} reduces with increasing L_C until certain values of L_B. On the other hand, at $f_{\text{max}}/2$, L_C does not really contribute in lowering the value of NF_{min}. So, G_m-boosting using L_C does not really help in noise figure reduction at and above $f_{\text{max}}/2$ and higher L_B leads to higher noise figure as well.

It is important to note that the device interconnect from lower metal layers to the top layer circuit exhibits a noticeable amount of inductance. So, it is very difficult to implement the cascode amplifier without some inductance (L_B) at the base of the CB transistor. This inevitably, at sub-THz, nullifies the benefit of using L_C as a noise reduction element in the cascode amplifier circuit where the frequency of operation is at or beyond $f_{\text{max}}/2$.

IV. LNA Design Above $f_{\text{MAX}}/2$

Based on the previous analysis, it is observed that with the proper values of L_B and L_C and sizing of the transistor G_m of the cascode amplifier can be boosted which can help to achieve higher gain. However, it has also been observed that there is a tradeoff between the gain and the noise figure of the cascode amplifier operating at and above $f_{\text{max}}/2$. Although there is the scope of gain boosting using L_B above $f_{\text{max}}/2$ frequency range but beyond a certain value of L_B, it clearly shows that LNA might suffer from potential stability. Taking this into consideration, an SE-LNA at 235 GHz and differential LNA at 290 GHz are designed and the same is discussed in the following subsections IV-A and IV-B, respectively.

A. SE Cascode LNA at 235 GHz

SE-LNA is designed at the center frequency of 235 GHz which is 10 GHz above $f_{\text{max}}/2$ of SiGe BiCMOS technology with f_t/f_{max} of 300/450 GHz. As shown in Fig. 7(a), SE-LNA is designed using a single-stage cascode topology. Here, VBIC model of HBTs (Q1 and Q2), with emitter area of

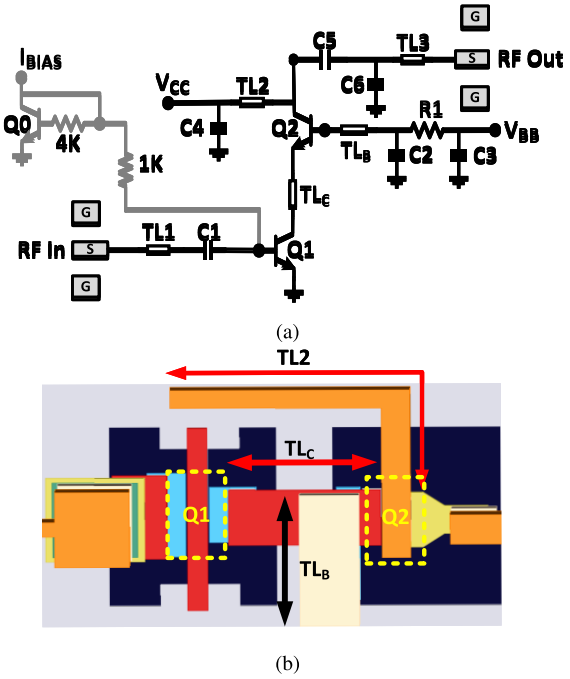


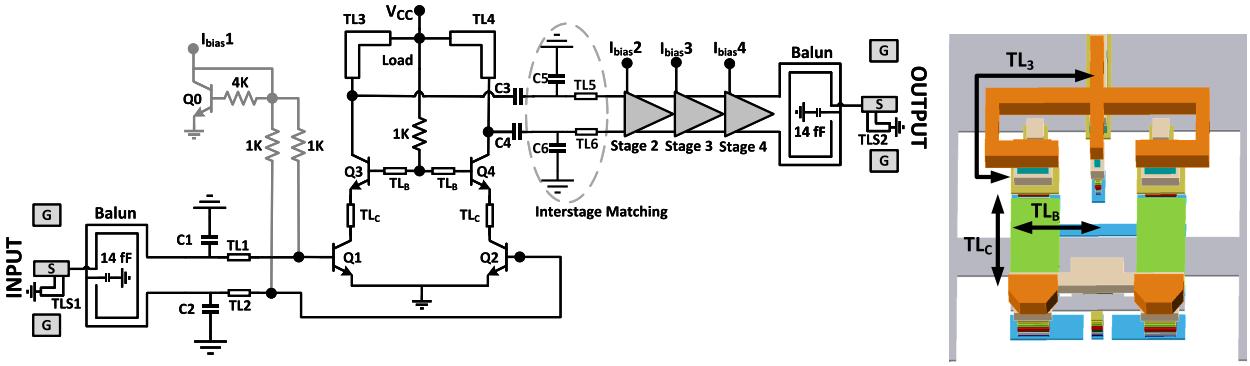
Fig. 7. (a) Simplified schematic of the SE single-stage cascode LNA. (b) Top view of the core layout of the cascode structure.

$4 \times 0.9 \times 0.07$ um^2, is used for simulation. A current mirror is used to bias the amplifier. Transistors are biased at their peak f_{max} with a collector current of 9 mA. As shown in Fig. 7(b), L_B and L_C are implemented using transmission lines TL_B and TL_C, respectively, and via stacks. First, L_B is optimized using transition vias from M1 to TM1 and a 5-μm-wide and 20-μm-long TL_B. The total inductance of 15 pH, for the minimum possible noise figure, is implemented by this structure. Subsequently, L_C is implemented using transition vias from M1 to M3, TL_C using M3 and transition vias from M3 to M2. TL_C is implemented by a 7-μm-wide and 15-μm-long M3 line. At and above $f_{\text{max}}/2$, L_C does not really help to reduce the noise figure, its dimensions are kept at the minimum possible length with 7 pH of overall inductance. The load of SE-LNA is implemented using a 2-μm-wide and 35-μm-long TM2 line which is connected to a 2-V supply.

The input of SE-LNA is conjugate matched to 50-Ω ground-signal-ground (GSG) pads using a 100-fF coupling cap (C1) and a 2-μm-wide and 5-μm-long transmission line TL1. The inductance caused by transition vias from M1 of the base of the transistor to M5 also plays a role in input matching. Input matching is compromised to avoid loss in the matching network and to achieve higher gain. C5 (10 fF) acts as a coupling cap at the output. The output of the LNA is matched to 50-Ω GSG pads using an LC matching network which is implemented using an MIM capacitor (C6 = 14 fF) and a 4-μm-wide MS line (TL3 = 30 μm). MIM capacitors (C2, C3, and C4) of 1 pF are used as decoupling capacitors. R1 (2 KΩ) is used to isolate dc from RF.

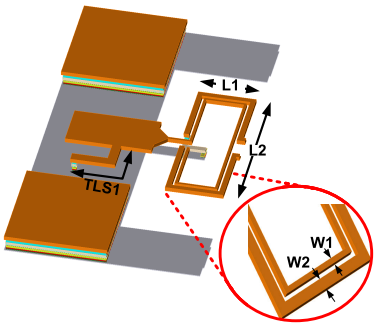
B. Four-Stage 290-GHz Differential Cascode LNA (D-LNA)

A four-stage D-LNA, with pseudo-differential cascode topology, is designed at a center frequency of 290 GHz which

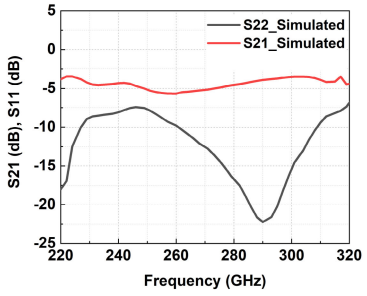


(a) (b)

Fig. 8. (a) Simplified schematic of the four-stage differential LNA. (b) Top view of the core layout of differential cascode structure.

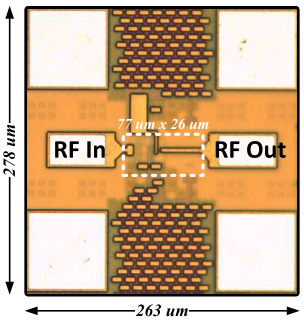


(a)

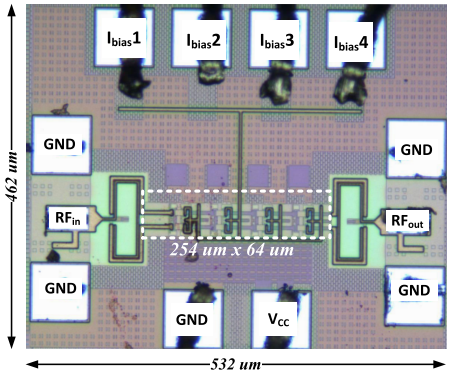


(b)

Fig. 9. (a) Layout of balun. (b) Simulated S-parameters of back-to-back balun structure.



(a)



(b)

Fig. 10. Chip microphotograph of (a) SE-LNA at 235 GHz and (b) D-LNA at 290 GHz.

is near $2/3(f_{max})$. Here, fundamental design methods are the same as explained in Sections II and III. D-LNA is designed in the following two steps.

1) Active Cell of LNA: The active cell of LNA is designed using Nx = 4 sized HBTs for both CE and CB transistors of cascode LNA. Each HBT is biased, using a current mirror, at a collector current of 8.5 mA, which is slightly lower than the collector current corresponding to peak f_{max}. As shown in Fig. 8(a) and (b), L_B and L_C are implemented using transmission lines TL_B and TL_C, respectively, and via stacks. TL_B is implemented using a 1.4-μm-wide and 10-μm-long M1 layer transmission line which provides 6.5 pH of inductance. Similarly, TL_C is implemented using a 7-μm-wide and 10-μm-long transmission line using M4 which incurs 5 pH of inductance. Inductance due to TL_B and TL_C lines are kept as low as possible to have a lower noise figure because around 290 GHz impact of L_B and L_C is not beneficial as far as simultaneous gain boosting and noise figure reduction is concerned. The load line of LNA is implemented using a C-shaped center taped 2-μm-wide TM2 transmission line which is connected to a 2-V supply line. Both TL3 and TL4 are 26-μm long. This active cell of the LNA is replicated in all four stages. Coupling capacitors (C3, C4 = 10 fF) are used at the output of each active cell to isolate the dc current of each stage.

2) Matching Network and Balun: The input matching network is designed to conjugately match the input of the first stage to the output of the input balun using an LC network.

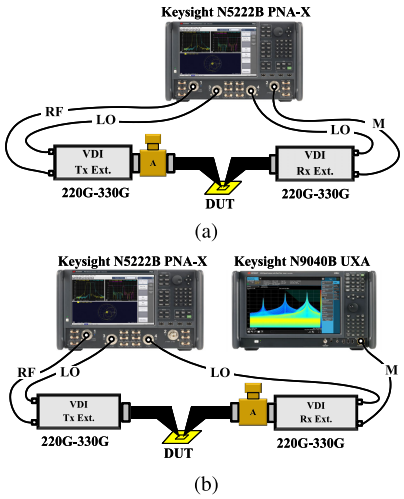


Fig. 11. (a) Small-signal measurement setup. (b) Large-signal measurement setup.

As shown in Fig. 8(a), L-shaped matching network consists of transmission lines (TL1 and TL2 = 34 μm) and MIM capacitors (C1 and C2 = 6 fF). Similarly, the output matching network of the last stage is designed. Interstage matching is achieved using a similar L-shaped matching network consisting of transmission lines (TL5 and TL6 = 30 μm) and MIM capacitors (C6 and C7 = 5 fF). Interstage matching networks, between the stages, are stagger-tuned to achieve the wideband frequency response.

As shown in Fig. 9(a), an edge-coupled Marchand balun is implemented to convert a differential (balanced) signal into an SE (unbalanced) signal. To achieve less amplitude and phase imbalance, asymmetric widths of the inner and outer rings of the balun are used to achieve large even and odd mode ratios. The widths of the rectangular-shaped inner and outer rings (L1 = 45 and L2 = 116 μm) of balun are 2 and 4 μm, respectively. The thickest top metal layer (TM2) is used to achieve minimum insertion loss. The minimum possible gap between two TM2 layers (2 μm) is kept to achieve maximum coupling between the both inner and outer rings. The outer ring of the balun is capacitively shorted to the ground with 14 fF of MIM capacitance which is tuned to minimize the phase imbalance. The SE output of the balun is directly connected to a 50-Ω GSG pad. A 7-μm-wide short-circuit stub with a length (TLS1) of 46 μm is placed at the center of the GSG pad which helps to resonate away the pad capacitance to have close to 50-Ω pad impedance, which also facilitates the ESD protection. As shown in Fig. 9(b), back-to-back EM-simulated insertion loss of pad-connected input and output baluns is less than 5 dB with good matching at the desired bandwidth.

V. Measurement Results

The chip microphotographs of SE-LNA and D-LNA are shown in Fig. 10. The dimensions of SE-LNA is 263 × 278 um^2 with core area of 77 × 26 um^2 and dimensions of D-LNA is 532 × 462 um^2 with core area of 254 × 64 um^2.

A. Small- and Large-Signal Measurement

Both small- and large-signal measurements are carried out on an on-wafer THz probe station. For small-signal measurements, as shown in Fig. 11(a), a Keysight's PNA-X N5222B is used where VDI's WR3.4 CW frequency extenders facilitate the measurement in the 220–330-GHz frequency range.

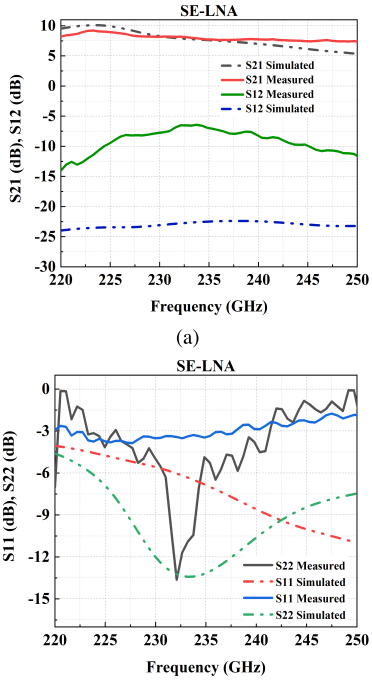


Fig. 12. Simulated and measured small-signal behavior of SE-LNA. (a) S21 and S12 (dB). (b) S11 and S22 (dB).

A transmit (Tx) extender, which can both transmit and receive RF power, is placed at the input port of LNA to measure input return loss (S_{11}) and forward gain (S_{21}). On the other hand, receive (Rx) extender only downconverts the received signal. So, to make a measurement of output return loss (S_{22}) and reverse gain (S_{12}), the LNA chip is rotated. To perform small-signal measurements, an external waveguide attenuator (VA-010E/G from Elmika UAB) is placed at the output of the Tx extender which helps to attenuate the output power of the Tx extender. All on-wafer measurements include the GSG pads for both LNAs. Thru-reflect-line (TRL) calibration is performed using a separate calibration substrate.

In Fig. 12, the measured S-parameters of SE-LNA are compared with the simulated results. In measurement, SE-LNA is biased at a 2-V supply with a bias current of 9 mA. At 235 GHz, SE-LNA has 7.8 dB of gain with a 3-dB bandwidth of 50 GHz. As part of the 3-dB bandwidth of SE-LNA lies below 220 GHz (outside WR3.4 waveguide band extenders), BW is approximated using simulated results. SE-LNA has a peak gain of 9.2 dB at 223 GHz. In comparison to simulated results, measured S12 is increased due to the close proximity of input and output THz probes. Input matching was compromised to have a minimum loss at the input matching network which further deteriorates in measurements without affecting the forward gain of the SE-LNA. It can be observed that the S21 response of SE-LNA is intrinsically wideband because, unlike [11], [12], [13], [14], [15], [16] where S21 response is relatively narrow band due to gain-boosting,

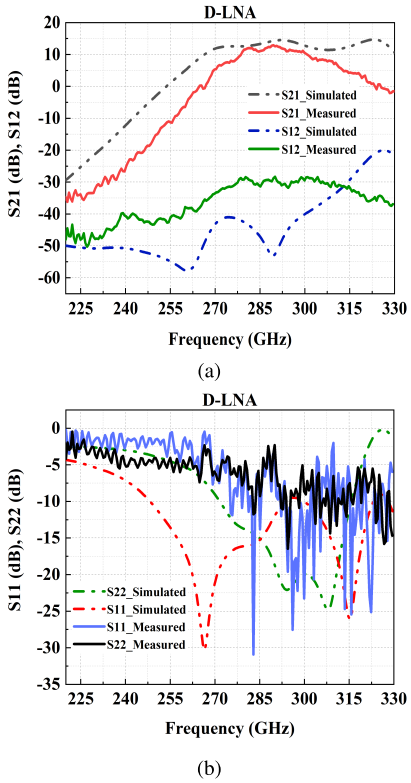


Fig. 13. Simulated and measured small-signal behavior of D-LNA. (a) S21 and S12 (dB). (b) S11 and S22 (dB).

gain-boosting using inductor (L_B) at the base of the CB transistor of cascode is avoided. Output return loss is decently matched with that of simulated results.

All stages of D-LNA are biased from a 2-V supply with a total current of 68 mA. As shown in Fig. 13(a), D-LNA measures 12.9 dB of peak gain at 290 GHz with 3-dB bandwidth of 23 GHz. At 300 GHz, LNA achieves 11.2 dB of gain. The discrepancies between measured and simulated gain response could be explained by the fact that all stages of D-LNA are not EM-simulated as a single block which, unlike measurements, does not fully capture mutual coupling effects between the stages. Due to extra loss incurred by the external attenuator on the reflected signal, measured input and output return loss (S11 and S22) are noisy which is more prominent at higher frequencies.

Fig. 11(b) depicts the large signal measurement setup. Here, Keysight's N5222B vector network analyzer is used to drive VDI's WR3.4 CW frequency extenders. The output power of the Tx frequency extender is varied by changing its input RF power which is provided by the network analyzer itself. However, as mentioned in [42], it is observed that the Tx frequency extender offers a very small linear range of operation. Nonetheless, the output power of the Tx frequency extender was sufficient enough to drive the LNA into compression. As presented in [37], LNA's input 1-dB compression point is −9.0 dBm.

B. Noise Figure Measurement

Noise sources for the WR-3.4 waveguide band are not available. Consequently, a complex setup such as the hot and cold method, where liquid nitrogen is used for cold temperature, is used to determine the noise figure of device under test (DUT) [40], [45]. To avoid such complexity, a well-known gain method is used to perform NF measurements. Noise figure measurement setup, as shown in Fig. 14(a), uses Keysight's E8257C signal generator to provide the LO signal to the VDI's modulated frequency extender (SAX). The downconverted IF signal is further amplified with the help of auxiliary LNA which raises the band-limited noise signal above the noise floor of Keysight's N9040B UXA signal analyzer.

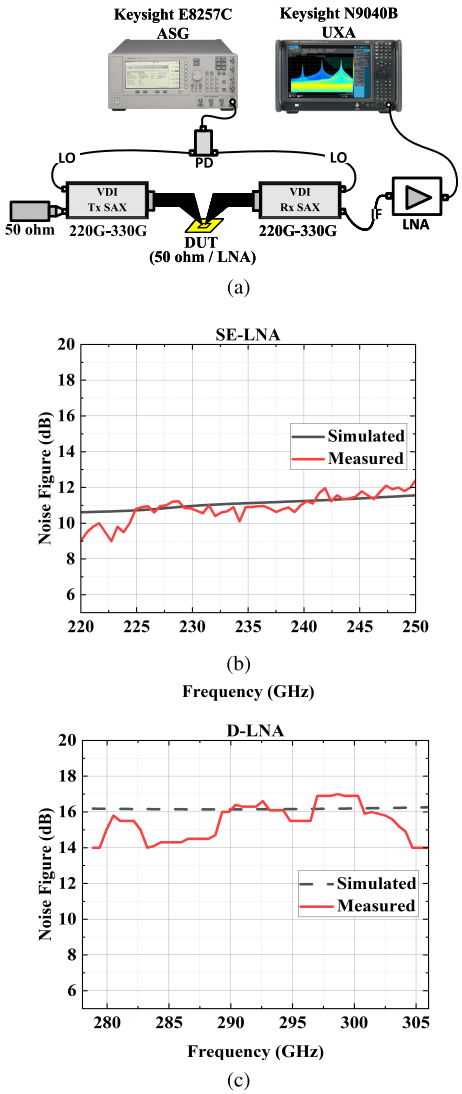


Fig. 14. (a) Noise figure measurement setup. (b) Simulated and measured noise figure of SE-LNA. (c) Simulated and measured noise figure of D-LNA.

The noise figure of DUT can be calculated by the following equation:

$$\mathrm{NF_{CAS}} = P_{N_{\mathrm{OUT}}} - (-174 + 10\log_{10}\mathrm{BW} + \mathrm{Gain_{CAS}}). \quad (15)$$

Here, $\mathrm{NF_{CAS}}$ is the cascaded noise figure of the DUT, probes, Rx SAX module, and auxiliary LNA. To calculate the NF of LNA, the gain and NF of all other components are to be known. First, NF of the Rx SAX module is estimated by calculating $\mathrm{NF_{CAS}}$ using (15) where DUT is 50 Ω GSG load on calibration substrate. Then, the NF of the Rx SAX module is

TABLE I
SUMMARY OF THE IMPORTANT PERFORMANCE PARAMETERS AND COMPARISON WITH RELATED WORKS

	This work	**This work**	[18]	[24]	[43]	[36]	[12]	[44]
Technology	130 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe
f_t/f_{max} (GHz)	300/450	300/450	300/550	220/280	350/550	470/700	300/500	300/500
Frequency (GHz)	235	290/300	252	173	275	291	245	245
Topology	CC[a], SE[c] (1 stage)	CC[a], Diff. (4 stages)	CC[a], Diff. (3 stages)	CE[b], SE[c] (3 stages)	Common Base (8 stages)	CC[a], Diff. (3 stages)	CC[a], Diff. (5 stages)	Common Base (4 stages)
Gain Boosting Technique	No	No	Yes	Yes	Yes	No	Yes	No
Gain (dB)	7.8	12.9/11.2	21.5	18.5	10	10.1	18	12
3-dB BW (GHz)	50	23	11	8.2	7	68	8	25
NF (dB)	11[e]	16[e]	-	-	18[d]	11[d]	11[e]	11.3[e]
Input-Referred P_{1dB} (dBm)	-14.0[d]	-9.0	-20	-10	-10	-15.6	-	-
P_{diss} (mW)	18	136	149	42	122.7	119	303.4	28
Area (um^2)	263 X 278	532 X 462	580 X 290	865 X 465	1065 X 355	700 X 380	360 X 430	420 X 460

[a] Cascode. [b] Common Emitter. [c] Single Ended. [d] Simulated. [e] Measured.

calculated using the Friis equation of the cascaded noise figure with known values of noise figure and gain/loss of probes and auxiliary LNA. Similarly, the NF of LNA is estimated by terminating LNA's input with a 50-Ω probe. In this case, the Tx SAX module's IF input is terminated with 50 Ω.

The measured average noise level of the measurement system was −131.5 dBm/Hz, when the Rx probe was terminated to 50 Ω calibration substrate termination. Similarly, the same noise level was observed when LNA was off, in cases, where the Rx extender with the probe was connected to powered down LNA with and without the Tx extender probe connection to LNA input. Fig. 14(b) and (c) depicts the simulated and measured noise figures comparison for SE-LNA and D-LNA, respectively. It can be seen that the simulated and measured noise figures are in close agreement with each other. Noise figures for SE-LNA are measured over 220–250 GHz and for D-LNA from 279 to 306 GHz. The measured noise figure of SE-LNA is around 11 dB and of D-LNA is around 16 dB. It is observed that the noise spectrum, near the lower and upper end of the frequency band of WR 3.4 waveguide performance varies. Consequently, the noise figure, around 220 GHz and above 300 GHz, is more susceptible to discrepancies. At the same time, the noise figure at midband frequencies of the WR 3.4 band waveguide is more accurate.

Table I compares the performance of state-of-the-art LNAs operating in the sub-THz/THz frequency range. It can be seen that D-LNA performs better than [43], where the center frequency is half of the maximum frequency oscillation with 8 common-base stages with 10 dB of gain and 18 dB noise figure. It can also be seen that the majority of the work has been done either below or close to half of the maximum frequency of oscillation. In [18] and [24], the operating frequency is above half of $f_{\max}$ with good gain which is more focused on gain-boosting without mentioning their noise performance. On the other hand, SE-LNA and D-LNA are operating beyond half of $f_{\max}$ with high gain and comparable noise figures.

VI. CONCLUSION

A single-stage SE and a four-stage differential LNA are implemented beyond $f_{\max}/2$ in 130-nm SiGe BiCMOS technology with $f_t/f_{\max}$ of 300/450 GHz. Gain boosting and noise reduction techniques are analyzed to see their feasibility on LNAs operating near the maximum frequency of oscillation. It is observed that these techniques start to show their limitation beyond the $f_{\max}/2$ range where a tradeoff between gain boosting and noise reduction techniques is found. Without any gain boosting and noise reduction technique, SE-LNA with single-stage achieves 7.8 dB gain at 235 GHz with 11 dB of noise figure and D-LNA offers 12.9 dB of gain at 290 GHz and 11.2 dB at 300 GHz with 16 dB of noise figure. A well-known gain method is used to measure the noise figure of LNAs at the THz frequency range. This work proposes the possibility of LNA-first receiver architecture operating near the maximum frequency of oscillation for future wireless communication.

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