Chip-to-Chip Interfaces for Large-Scale Highly Configurable mmWave Phased Arrays

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***Abstract*— This article presents a chip-to-chip (C2C) interface for constructing reconfigurable phased arrays to be used in fifth-generation (5G)/sixth-generation (6G) wireless systems. The C2C interface further facilitates building phased array panels by allowing the use of grid-based PCB routing, thus providing flexibility in the system design. An eight-element RFIC capable of handling two independent data-streams is fabricated using 45-nm CMOS technology. The RFIC incorporates four C2C interfaces operating at 27 GHz, two C2C interfaces operating at 9 GHz, and a complex baseband (BB) with single-sided bandwidth in excess of 400 MHz. The architecture is tested by flip-chip bonding two fabricated RFICs on an eight-layer Megtron 7 PCB. In this article, only the receiver path of the RFIC and the phased array is described. Performance of both the single RFIC and the combination using the 27-GHz C2C interface is demonstrated using conductive and over-the-air (OTA) measurements. OTA measurements are conducted using 5GNR FR2 OFDM waveforms with a signal bandwidth of up to 800 MHz. The measured RF to BB conversion gain for a single element is larger than 23 dB and the minimum measured noise figure (NF) is 6.2 dB. The nominal dc power consumed by the receiver per element per stream is 116.5 mW. The RFIC occupies a normalized area per element per data stream of 2.7 mm^2. The RFIC is capable of supporting dual-polarized antennas or in a large-scale panel utilizing the same antenna elements to two independently weighted data streams as part of the hybrid beamforming architecture.**

***Index Terms*— Chip-to-chip (C2C), CMOS SOI, fifth generation (5G), millimeter-wave, mmWave receiver, phased array, sixth generation (6G).**

I. Introduction

FIFTH generation (5G) and the upcoming sixth generation (6G) networks promise to provide higher data rates and reliable, low latency, and power efficient wireless connectivity [1], [2]. In order to achieve these goals, scalable, reconfigurable, power efficient, and large phased arrays with multiple antenna elements are proposed [3]. Link analysis for both 5G [4] and 6G [5] indicates a need for high antenna gain i.e., a large number of phased array elements even for single links. Moreover, hybrid beamforming has emerged as a popular phased array transceiver architecture in terms of beamforming flexibility and power consumption for arrays supporting a multiplicity of orthogonal data streams in base stations. In other words, the next-generation phased array system should be scalable, support multiple beams, and be reconfigurable at runtime. This not only helps in improving the power efficiency, but it can also help in intelligently creating beam patterns with reduced sidelobe levels, thus reducing interference to other users [6].

Provided the motivation, these requirements have been addressed in the literature by creating phased arrays in the following three ways.

1) Single RFIC with large number of antenna elements [7], [8], [9], [10], [11], [12], [13].
2) Tiling multiple RFICs and electrically connecting them via different methods such as discrete power combiners and splitters, single wire interface, coaxial cable, and high density interconnect interposers [14], [15], [16], [17], [18], [19], [20], [21], [22].
3) Utilizing hybrid beamforming [23], [24], [25], [26], [27], [28], [29], [30], [31].

Creating a single RFIC with a large number of elements is prone to yield problems and is generally more complex to design and verify. Focusing on the method of creating the phased array via tiling, a distinction can be made between different designs based on how the desired analog signals are routed and coherently combined. Below are the main methods.

1) Symmetrical tree-like routing and combining at RF, IF, or baseband (BB) using passive or active combiners shown in Fig. 1(a) and used for example, in [15], [16], [18], [19], [20], and [21].
2) Point-to-point routing with matched lines shown in Fig. 1(b) and used, for example, in [17] and [22].

The benefit of symmetrical tree-like routing is that it is easier to tile given the symmetrical nature, which further reduces the calibration complexity. At the same time, it incurs larger path loss compared to point-to-point routing.

Hybrid beamforming has been proposed as a solution to process many independent beams in phased arrays [32], [33], [34], [35], [36]. Depending on the context, very different approaches and architectures have been proposed from

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sub-array based to fully connected analog multiple-input–multiple-output (MIMO) solutions. Large-scale solutions are typically based on multiple parallel and independent RF sub-arrays and beam-based processing is done in the digital domain with the limited field of view of each sub-array. MIMO-like fully connected, i.e., cross-coupled arrays, have been limited to a relatively small number of symmetrically combined signal paths in the RF domain or to slightly larger analog combining matrices within one chip. RF or analog-based hybrid beamforming has recently been proposed in chip-scale combining architectures in [24], [25], [26], [27], [28], [29], [30], and [31]. A common concern regarding these designs is that they are not easy to scale up and they require a sophisticated LO distribution network.

Based on the above discussion, the main conclusion is that in the current phased array designs scaling is addressed by employing either tree-like combining/distribution network or point-to-point routing. These methods, although assists in reducing the calibration complexity, however, make changing the number of elements for one stream difficult. Furthermore, for fully connected hybrid implementations, even though the number of elements participating in one stream can be changed easily, the existing implementations do not allow for scaling the architecture to the larger number of antennas. The main motivation of this research is to develop an antenna array architecture that not only allows dynamic reconfiguration of a large antenna array but also provides scalability, with the goal to provide a way to implement complex patterns supporting multiple beams flexibly, as proposed, for example, in [6].

Keeping these goals in mind, a phased array RFIC architecture is proposed and an RFIC is designed and fabricated utilizing multiple chip-to-chip (C2C) interfaces which are combined via grid-based routing. Symmetrically combining IF signals via C2C interfaces have been previously published in [21] and [23]. The proposed RFIC can be tiled in both vertical and horizontal directions on a PCB with antennas on the other side, thus, creating a panel with multiple rows and columns. The proposed architecture not only allows us to easily scale the panel but also to dynamically re-configure it by selecting antennas from any row or column for combining. The architecture also simplifies scaling in the case of hybrid beamforming, allowing C2C connections through specific interfaces at several frequencies and directions. Different routing strategies are illustrated and compared in Fig. 1 and Table I.

The proposed RFIC is designed and fabricated using GlobalFoundaries 45 -nm PDSOI technology. It contains four mmWave C2C interfaces, two IF C2C interfaces, and utilizes grid-based routing, thus simplifying the PCB design and allowing the selection of any antenna from any RFIC to form a desired beam shape as in [6]. The LO is routed in a daisy-chained manner, further reducing the PCB complexity. The daisy-chaining of LO is previously utilized in [18]. The fabricated RFIC supports signal combining at three different frequencies: RF, IF, and BB. In addition, it allows two different data streams to be handled simultaneously. Utilizing two of these RFICs, a phased array receiver is created and tested.

TABLE I
DIFFERENT ROUTING STRATEGIES

Technique	Pros	Cons
Symmetrical tree-like routing	easier to scale via tiling, lower calibration overhead	larger routing losses, difficult to change number of elements in a stream
Point-to-point routing	lower routing losses, lower calibration overhead	difficult to scale via tiling, difficult to change number of elements in a stream
Grid based routing	lower routing losses, easier to scale via tiling, easier to change number of elements in a stream	higher calibration overhead

In Section II, the system architecture is discussed in detail. Architecture and circuit design details of the implemented RFIC supporting this system architecture are described in Section III. Characterization results of the single RFIC and a two RFIC receiver phased array are presented in Section IV and the conclusions are drawn in Section V.

II. RE-CONFIGURABLE PHASED ARRAY ARCHITECTURE

A. System Architecture

The block diagram of the proposed phased array system is shown in Fig. 2. The system consists of a total of $M \times N$ RFICs arranged in a 2-D grid of M rows and N columns. Each RFIC is connected to multiple antennas via its front-end (FE) antenna ports, and to its immediate vertical and horizontal neighbors via the C2C interfaces, shown in red and blue in Fig. 2, respectively. Here, the antenna can be a single patch antenna or a small sub-array driven by one FE. The horizontal C2C interface operates at mmWave frequencies and vertical at IF. Hence, this architecture does not employ a tree-like passive combining with on-PCB power combiners [15], [16], but proposes a more flexible row and column-based combining method. The vertical and horizontal C2C interfaces could be designed to operate on the same frequency (mmWave or IF). However, isolation is improved on the PCB when vertical and horizontal C2C interfaces are operating at different frequencies. All C2C interfaces support simultaneous input and output signal flow.

Based on the number of logical streams that the system is configured to provide, multiple external BBs can be connected at different points in the $M \times N$ grid. Using the C2C interfaces, BB connections can be logically routed on the perimeter of the array. Fig. 2 shows a system with two external BB via RFICs $U_{1,1}$ and $U_{M,N}$, thus, being able to support two independent data streams as an example. Furthermore, it also depicts one viable way to distribute the connected RFICs to form two streams (shown in red and green color).

Since each RFIC has been envisioned with IF and BB mixers for two-stage sliding-IF down conversion, the LO also needs to be routed to each RFIC. In each column, LO is distributed in a daisy-chained fashion. Depending on the floor-planning, the LO can enter the grid from a synthesizer either via the first row or the Mth row. Given the regularity of the

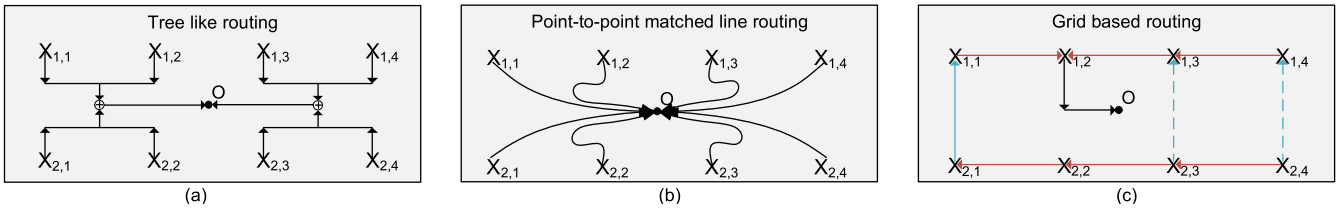


Fig. 1. Comparison between different signal routing topologies, X marks the source and O marks the end summing point. (a) Tree-like routing along with passive combiners. (b) Point-to-point lines of a matched length. (c) Grid-based routing.

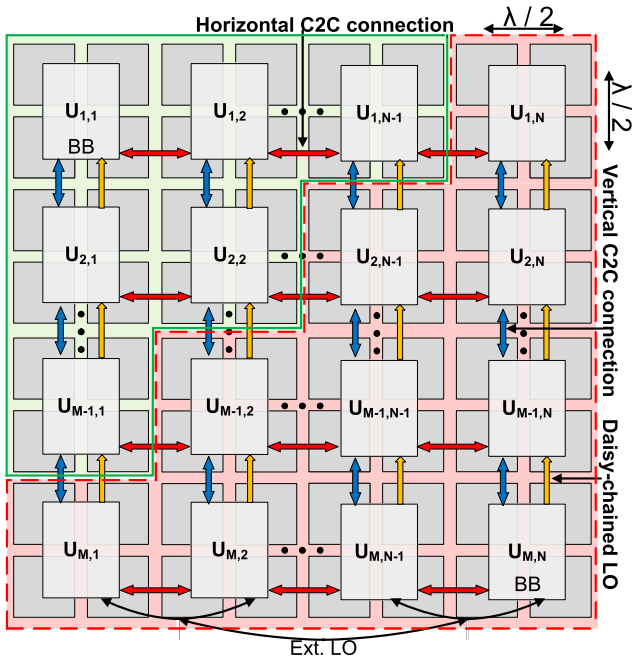


Fig. 2. $M \times N$ grid of RFICs along with vertical and horizontal C2C connections, $\lambda/2$ spaced patch antennas, and daisy-chained LO. Also shown is one possible way to create two non-overlapping logical streams (marked red and green). Red and blue bi-directional arrows represent the vertical and horizontal C2C connections, respectively. Orange-colored uni-directional arrows represent the LO.

structure, from a manufacturing standpoint, it responds well to scaling via tiling.

In this architecture, antenna combining can be achieved dynamically at four levels. At the first level, each RFIC locally combines signals from antennas connected to its FEs. The second level of combining involves the horizontal C2C interface. Here, the aggregated signal, after the local combining, can be coherently combined with the input signal of the horizontal C2C interface, which can be propagated further via the output port of the C2C interface. Thus, the second level of combining allows combination over a row in the grid. This second-level aggregated signal, after the frequency conversion, can then be used for a third level of combining using the vertical C2C interface. The combination via vertical C2C interface behaves similar to the horizontal combining. Thus, the third level of combining allows combination over a column in the grid. The fourth level of combining can be done either in analog or digital BB as proposed in [29]. This architecture provides the following advantages.

1) Flexibility of coherently combining antennas without requiring a tree-like symmetrical routing.
2) Dynamic combination of antennas from different rows and columns, thus, allowing changing of beam patterns and beam properties like inter-beam interference at runtime.
3) Avoiding the losses of passive combining by utilizing active combining.

B. Asymmetrical Combining

The second and third levels of combining, which this architecture proposes, utilize the on-PCB C2C transmission lines. Even though the RFICs are distributed in a regular grid structure, in order to reduce the losses of routing and passive combining, the routing is not done in a fully symmetrical tree-like fashion. Thus, for coherent summation over the row, while using the horizontal C2C interface, the extra time delay caused by the PCB transmission lines has to be compensated. Similarly, extra time delay has to be compensated for coherent summation over a column using the vertical C2C interface. Furthermore, as the LO is actively distributed in a column, there will be a phase difference between the LO signal received by the different RFICs in a column. The LO phase difference across a column can be compensated either by utilizing phase shifters in the LO path or by providing an additional phase shift to all the FEs in the particular RFIC.

In order to compensate for the excess chip-to-chip time delay in the second and third levels of combining, an active vector summing phase shifter (VSPS) is used. Moreover, utilizing a VSPS for compensating a time delay is a band-limited operation and has some effect on the beam pointing accuracy of the beamformer when the fractional bandwidth is high enough [37], [38]. The extent of these effects is demonstrated in Section IV. It should be noted that the asymmetry makes the beam synthesis more complex and thus requires advanced beam management schemes in signal processing.

C. Dynamic Reconfigurability

Dynamic reconfigurability refers to the fact that the RFICs and thus antennas, can be combined dynamically. Fig. 2 shows the complete grid being split into two streams along the diagonal i.e., RFICs labeled $U_{M-1,1}$, $U_{M-2,2}, \ldots, U_{2,N-2}$, and $U_{1,N-1}$, are part of the upper diagonal area for the stream marked with a green background. For a given number of BB streams, these boundaries are programmable and can be varied when needed. This functionality is achieved by pairing the C2C interface with a switchable many-to-many routing matrix. The routing matrix is in principle a collection of multiple active splitters and combiners. The only thing

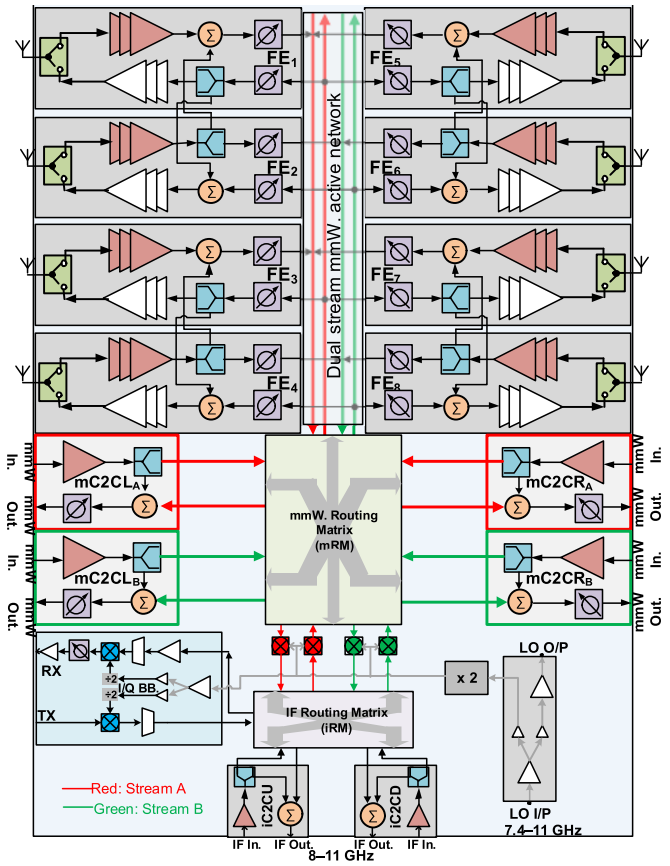


Fig. 3. Simplified block diagram of the implemented mmWave RFIC with eight FEs, two logical mmWave streams, four mmWave C2C interfaces, and two IF C2C interfaces. The placement of different blocks in the figure is according to the floor plan of the RFIC. Red and green colored lines represent the signal path for streams A and B, respectively. Other colors are for visual clarity.

limiting the flexibility is the number and locations of BB inputs and outputs. This reconfigurability allows for tailoring of the vertical and horizontal resolutions of the beam at will.

III. RFIC Design

In this section, the design choices and the internal structure of the implemented RFIC are described.

A. RFIC Architecture

A simplified block diagram of the implemented RFIC is shown in Fig. 3. It is a sliding IF architecture that contains all components from mmWave FEs to an analog BB. As seen, the RFIC contains several blocks including eight FEs ($FE_{1–8}$) which can be combined to form a max of two logical streams, a dual stream mmWave active combining network, a dual stream mmWave routing matrix (mRM), four mmWave C2C interfaces ($mC2CL_{A–B}$ and $mC2CR_{A–B}$), two IF C2C interfaces (iC2CU and iC2CD), a complex BB, an IF routing matrix (iRM), active and passive mixers, frequency multiplier, divider, and LO buffers for internal LO distribution and daisy-chaining.

Each FE has a TRX switch, PA, LNA, two VSPSs, and to support different operating modes, an active combining block, and an active splitter. On the receiver side of the FE, a single-ended RF signal enters from the antenna port and goes to the TRX switch, which directs the signal toward a three-stage LNA. The second stage of the LNA converts the single-ended signal to a differential and the rest of the processing happens on this differential signal. Depending on the physical number of the FE, the LNA is followed either by an active splitter or a combiner. All odd numbered FEs ($FE_{1,3,5,7}$) have an active combiner and even numbered FEs ($FE_{2,4,6,8}$) an active splitter. The last block in the RX chain, before the signal is combined with other FEs using an active combiner is an active VSPS. This VSPS is responsible for beam-steering.

Similarly, at the transmitter side of the FE, a differential signal enters an active VSPS which is followed by either an active splitter or a combiner depending on the physical number of the FE. The signal enters a multistage differential PA whose last stage also performs differential to single-ended conversion, before feeding it to the TRX switch. As this article is focused on the receiver side, there is no additional description related to the TX chain.

The RFIC supports two operating modes for the combination of the local FEs. In mode I, odd-numbered FEs ($FE_{1,3,5,7}$) are combined to form stream A (red colored lines in Fig. 3) and even-numbered FEs ($FE_{2,4,6,8}$) combine together to form stream B (green colored lines in Fig. 3). In this mode, the cross-connection between the neighboring FEs is turned off. This mode is designed for handling dual-polarized antennas or in general for supporting two independent sub-arrays. Thus, the two independent mmWave streams can correspond to vertical and horizontal polarization data, for example. In this mode, the RFIC can handle a total of eight antennas or sub-arrays. In mode II, or hybrid mode, the TRX switch and LNA of the odd-numbered FEs ($FE_{1,3,5,7}$) are turned off and the cross-connection between the neighboring FEs is turned on. This allows to generate two differently oriented spatial streams from the same antenna, allowing the RFIC to handle four antennas or sub-arrays. These two modes are shown in Fig. 4.

After combining, the RX side of the two mmWave streams ends up at the mRM. The mRM also interfaces with the four C2C interfaces ($mC2CL_{A–B}$ and $mC2CR_{A–B}$) and the mmWave-IF mixers. Both mmWave streams are handled independently of each other in the mRM. A detailed signal flow diagram of the mRM for one stream is shown in Fig. 5. Description of the signal labels of Fig. 5 can be seen from Table II. All the combiners and splitters used in the mRM are active in nature and can be turned on or off independently via digital controls. The independent controls allow a plethora of combinations for the signal paths, but only a selected few of these combinations are listed below.

1) *swMode I:* This mode is suitable for routing the signal to other RFICs via the mmWave C2C interfaces. In this mode, the combined signals of the local FEs are routed toward the output interface of any of the two (left or right side) mmWave C2C interfaces. The local BB is turned off. The RFIC does not perform any second-level combining. It is demonstrated in Fig. 5 using red dashed lines.

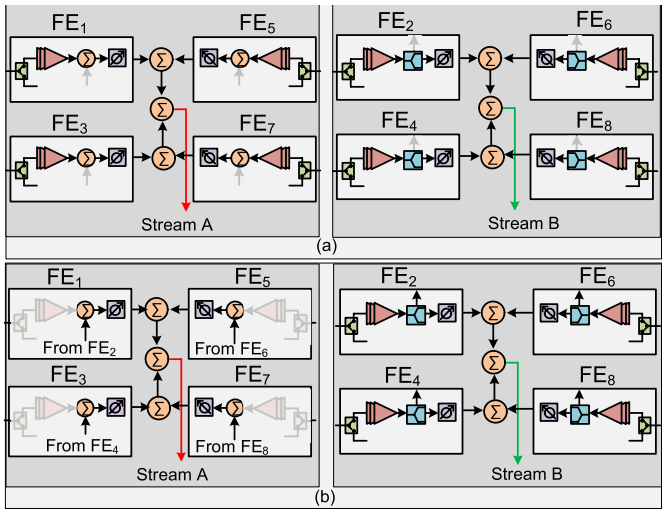


Fig. 4. Simplified block diagram depicting the two operating modes related to mmWave combining of the local FEs. (a) Mode I (dual-polarized antennas). (b) Mode II (hybrid and two independently weighted outputs from the same antenna element). In the latter, the LNA outputs (FE_2, FE_4, FE_6, and FE_8) are fed also to the adjacent front-ends (FE_1, FE_3, FE_5, and FE_7) where they can be weighted to point to different directions.

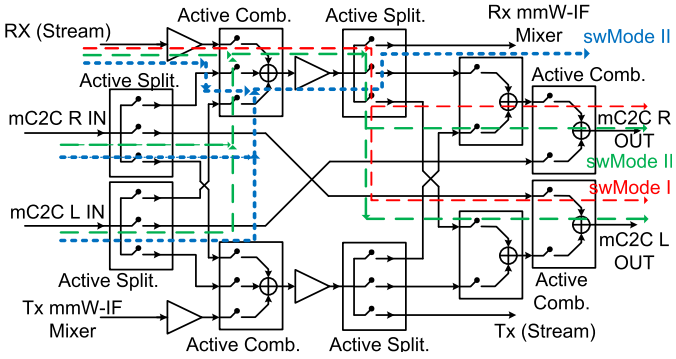


Fig. 5. Simplified block diagram of the mRM depicting the signal flow for one stream. Different colored dashed lines show the signal path for a few of the different modes. Signal labels used here are summarized in Table II.

2) *swMode II:* This mode is suitable for RFICs that are not on the edge of a panel. Here, the local signal is first combined with the input signal from any of the two mmWave C2C interfaces and the combined signal is routed toward the output interface of any of the mmWave C2C interfaces. Here too, the local BB is turned off. This mode differs from swMode I in that here the second level combining happens.
3) *swMode III:* This mode is useful for routing the combined signal toward the IF processing. In this case, the local signal is first combined with the input signal from any of the two mmWave C2C interfaces just like in swMode II. However, instead of going outside of the RFIC, this combined signal is routed toward the mmWave-IF mixer.
4) *swMode IV:* This is a debug bypass mode useful for testing. Here, the signal does not take part in any combination and just flows from the left or right input side (mC2C L/R IN) to the left or right output side (mC2C L/R OUT).

After the mRM and the mmWave-IF mixers, the signal path enters iRM. The iRM is similar in functionality to mRM with the differences being in the operating frequency and number of streams handled, as iRM can handle only one stream at a time. The iRM interfaces with two IF C2C interfaces, mmWave-IF mixers, and the complex analog BB.

TABLE II
mmWAVE ROUTING MATRIX SIGNAL DESCRIPTION

Signal Name	Description
RX (stream)	combined RX local stream signal.
TX (stream)	common TX local stream signal.
RX mmW-IF Mixer	mmWave input signal to the down-conversion mixer.
TX mmW-IF Mixer	mmWave output signal from the up-conversion mixer.
mC2C R IN	mmWave input signal from the right side mC2C interface.
mC2C L IN	mmWave input signal from the left side mC2C interface.
mC2C R OUT	mmWave output signal to the right side mC2C interface.
mC2C L OUT	mmWave output signal to the left side mC2C interface.

The first level of frequency conversion happens via the mmWave-IF mixers, which are active double-balanced Gilbert cell-based mixers. The second level of frequency conversion happens via passive IF-BB mixers. Given the single stream handling in the IF domain, the RFIC has only one complex BB and one set of IF C2C interface (iC2CU and iC2CD).

The RFIC employs a sliding IF architecture. Every RFIC gets an external local oscillator (LO) signal of frequency 7.4–11 GHz (f_{lo}), and doubles it internally via a multiplier to 14.8–22 GHz. The input RF signal is at $3f_{lo}$, and the IF is at f_{lo}. The internally generated $2f_{lo}$ is used to generate quadrature LO at f_{lo} for IF-BB conversion via a divider. These mixing stages are enabled only when needed in the architecture.

The horizontal C2C interfaces have a VSPS at the output point for compensating the excess C2C time delay. The vertical C2C interfaces do not have any VSPS, thus, for coherent summation over different columns, combined row output has to be rotated using the VSPS in the FEs. Furthermore, to minimize the phase noise, there is no VSPS for the LO input. Thus, the LO phase difference also has to be accounted for via the FEs' VSPS.

B. RFIC Circuit Details

1) TRX Switch: The TRX switch utilizes quarter-wave transmission lines, which are implemented here using lumped components. Grounding shunt switches are used in order to improve the isolation. The design is similar to the front-end switch as shown in [39], but with single-ended topology and omission of series switches for simplicity. The schematic of the implemented TRX switch is shown in Fig. 6.

For the TX shunt switch, oxide breakdown is circumvented by stacking five transistors in series. In the off-mode, they generate a capacitive voltage divider and pass a 15-dBm output signal without breakdown or additional distortion.

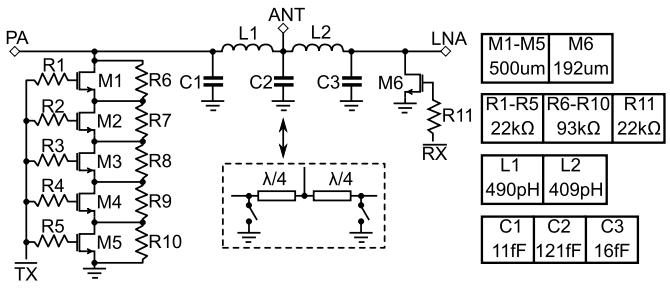


Fig. 6. Circuit diagram of the TRX switch.

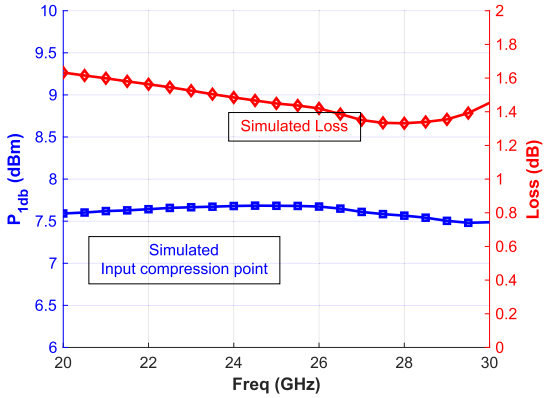


Fig. 7. Simulated loss and input compression of the TRX switch in the receive mode.

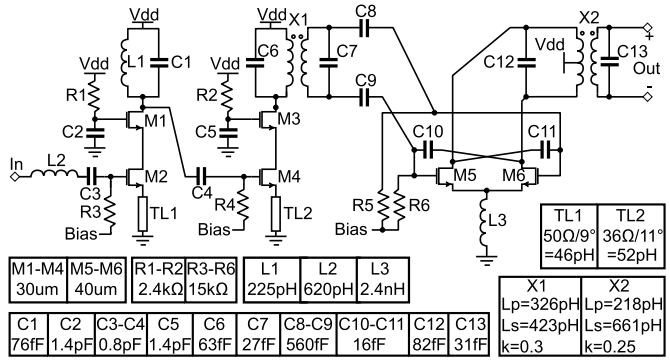


Fig. 8. Circuit diagram of the three-stage LNA.

The simulated input compression point and loss of the switch in the receive mode are plotted in Fig. 7.

2) LNA: The schematic of the LNA is shown in Fig. 8. Input is matched for minimum noise with a series inductor (L_2) and degeneration inductor implemented with a transmission line (TL_1). Transistor width of 30 μm is chosen as a compromise between low noise and power dissipation. Component values are optimized to have a bandpass response from 24 to 29-GHz band. The LNA does not have a dedicated gain control, but adjusting the bias provides more than a 20-dB gain control range.

3) Vector Summing Phase Shifter: All of the phase shifters used in this RFIC are active in nature. The VSPS used here is based on the similar circuit presented in [40].

The VSPS used in the C2C interfaces and the FEs differ from each other in their output stage. As the VSPS in FEs drives internal active blocks, the output driver is a fixed gain differential amplifier. However, in the case of C2C interfaces, the output stage has to drive a 100 Ω differential load, thus, a larger variable gain amplifier is used.

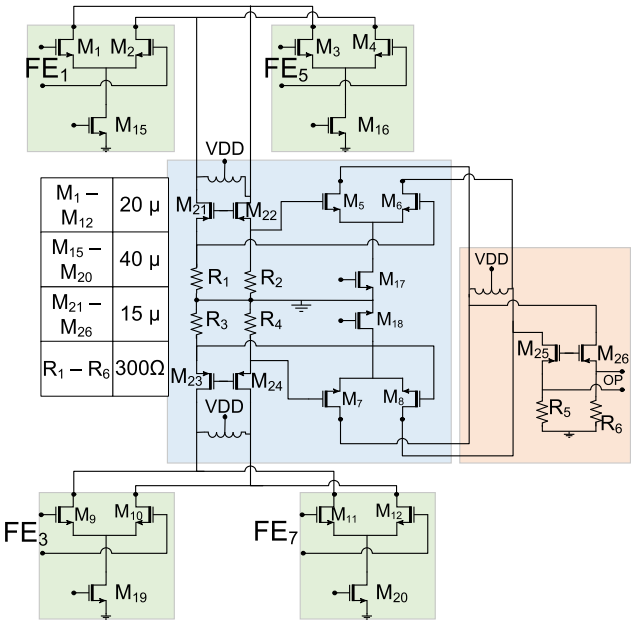


Fig. 9. Circuit diagram for the mmWave distribution network used for combining the receiver side mmWave RF signals from the FEs. Circuit for only stream A is shown.

The VSPS provides up to 0.5° of phase resolution at maximum amplitude and about 10 dB of usable gain control range with a somewhat reduced phase resolution.

4) mmWave Active Distribution Network: The mmWave signals from the FEs are combined together first in the distribution network. Throughout the RFIC, signals are combined in the current domain. The technique used for the same is to first convert the voltage signal to the current one via a g_m stage, transport it to the common point of combining via differential co-planar lines and do the summing and conversion to voltage domain via a folded-cascode type low-ohmic receiver. The signal combination for the four FEs happens in two stages. In the case of stream A, at the first level, FE_1 and FE_3, and FE_5 and FE_7 are combined. These two combined signals are then combined with each other. The circuit for combining four sources into one output is illustrated in Fig. 9. A similar structure is used for stream B.

The g_m stages are implemented using a standard differential amplifier with switchable bias controls. The bias control is used for turning off inputs that are not participating in the summation. The low-ohmic folded-cascode receiver performs resistive matching and isolation of the nodes at the same time. Co-planar lines are designed using the top two copper layers. They are built by repeatedly tiling the structures shown in Fig. 10. In order to keep the routing complexity manageable, a fixed BEOL metal layer is used depending on the routing direction i.e., the top copper layer is used for creating the co-planar lines that are traversing in the horizontal direction, and the penultimate copper layer is used for vertical routing.

5) mmWave Routing Matrix: The mRM is responsible for the second level of combining and moving the RF signals around to support reconfigurability. The simplified schematic is shown in Fig. 11. A single combiner is used to combine the differential RF currents coming from the FEs, right side

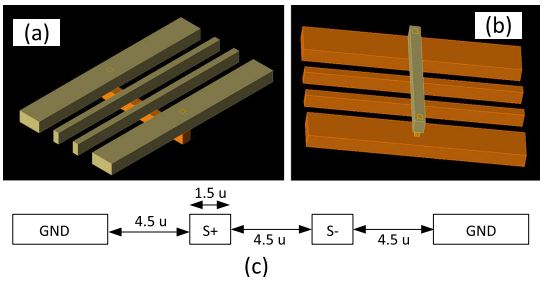


Fig. 10. One segment of the co-planar lines used for transporting RF currents. (a) Line traversing in the vertical direction. (b) Line traversing in the horizontal direction. (c) Distance between the conductors.

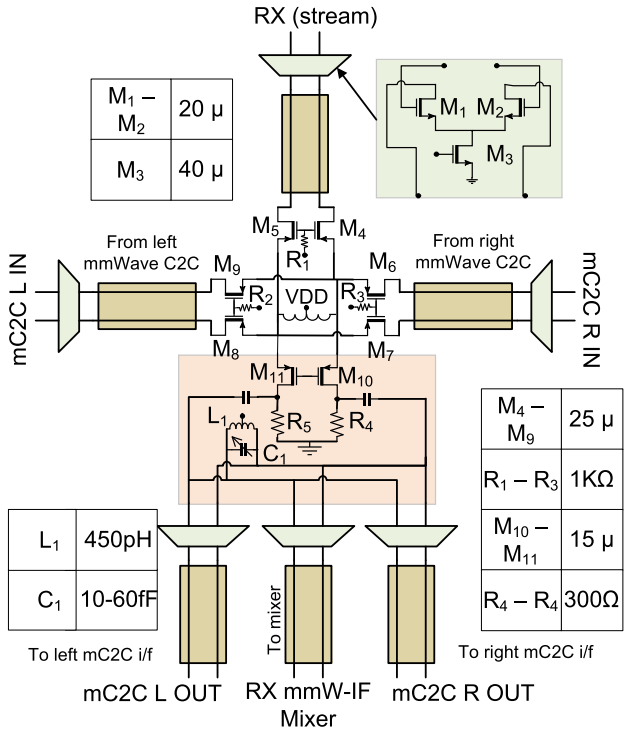


Fig. 11. Circuit diagram for one stream of the mRM. Only the receive side is shown here.

mmWave C2C interface, and left side mmWave C2C interface. Each path has a PMOS switch to isolate the unwanted path. These RF currents sum up at the folded cascade-based combiner, which then, in turn, drives three different g_m stages which are routed toward the mmWave mixer, left side mmWave C2C interface and right side mmWave C2C interface.

6) IF Routing Matrix: The iRM is responsible for the third level of combining. It interfaces with mmWave-IF mixers, RFIC C2C interfaces, and the BB. The simplified schematic is shown in Fig. 12. A single folded cascade-based combiner is used to combine the differential IF currents coming from the mmWave mixers, up side IF C2C interface, and down side IF C2C interface. The g_m stages providing these IF currents have independent biasing. After summation, the signal is routed toward local BB and IF C2C interfaces via g_m stages.

7) mmWave Chip-to-Chip Interface: Each RFIC has four C2C interfaces operating in the mmWave frequencies and is arranged on the left and right sides of the RFIC. These are used for interfacing with other RFICs and thus play an important role in providing reconfigurability. Furthermore, to aid the

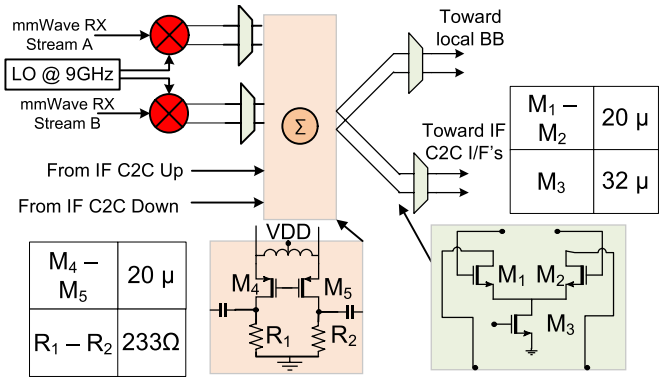


Fig. 12. Circuit diagram for the receiver part of the iRM.

testing capability of the C2C interfaces, a loop-back mode is implemented.

A C2C interface has differential inputs and outputs. At the input side, there is a common-source true differential amplifier with a tail inductor. The simulated differential gain of the input amplifier is around 15 dB. Input matching is done by a combination of a shunt inductor and shunt resistors. This is done to provide wideband matching and burn any reflected signal when the interface is off. The resistors, however, do degrade the NF a bit. On the output side, there is a VSPS which is used to compensate for the C2C propagation delay effects before combining neighboring RFICs. At the output of the VSPS, to provide coarse gain control, there are two independent common-source amplifiers with a transformer as a load. The secondary side of the transformer is connected to the output C4 bumps.

8) LO Distribution: The RFIC gets an external differential LO signal via either a synthesizer (LMX2594) mounted on the PCB or a signal generator. The input LO is buffered using a tuned common-source amplifier and then split into two paths, with one path going out of the RFIC and the other going toward a multiplier. The LO signal going out of the RFIC is daisy-chained vertically. Internally, the LO is multiplied by a differential digitally controlled injection locked doubler that has a 3 dB tuning range from 14 to 20 GHz with 0 -dBm input power [41]. The doubled LO is routed to both mmWave-IF mixers and via a divide-by-two circuit to the IF-BB mixers.

9) mmWave-IF Mixer: A Gilbert cell-based active mixer is used to down-convert the mmWave signal to IF. The schematic for the same can be seen in Fig. 13. Both inductors, L_m and L_{cm}, suppress the even-mode harmonics of the LO and RF signals, improving IIP2.

10) Analog Baseband (Receiver): A simplified schematic for the analog BB is shown in Fig. 14. Besides the mixer for down-converting IF to BB, it also includes a frequency divider, LO drivers for the mixer, a vector modulator (VM), and a self-biased inverter-based transimpedance amplifier (TIA). The VM is present because multiple RFICs can be weighted and combined using the BB.

From IF to BB down-conversion, along with VM, is implemented via a constant-Gm VM topology [42]. Here, current combining via TIA is used instead of charge-sharing as utilized in conventional design. The low impedance node at

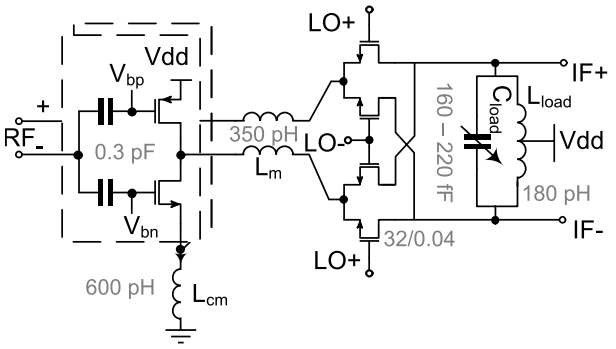


Fig. 13. Down-conversion mmWave-IF Gilbert cell mixer.

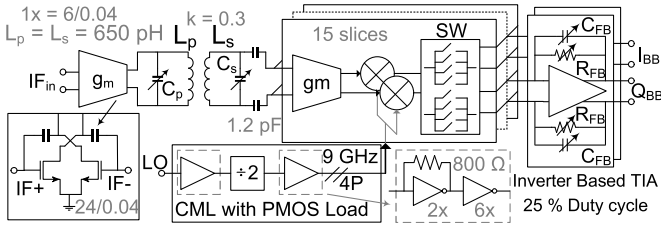


Fig. 14. IF to BB RX block diagram.

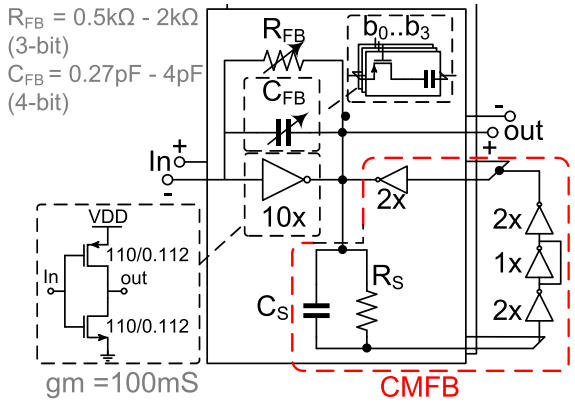


Fig. 15. Self-biased inverter-based TIA with CMFB.

the TIA input further provides frequency range extension [43]. The TIA is implemented using self-biased inverter amplifiers with common-mode feedback (CMFB) [44], and its schematic can be seen in Fig. 15. Transistors with long channel lengths ($L = 0.112\ \mu$m) are employed to achieve large TIA open-loop gain. Both the feedback resistor (R_{FB}) and capacitor (C_{FB}) of the TIA are implemented in a programmable way to provide gain and bandwidth variability. In order to drive the large capacitive load of the VM, a g_m stage along with a transformer is used. Two lumped capacitors of values 400 and 300 fF, along with variable switch-capacitors from 26 to 208 fF, have been added to the primary and secondary side of the transformer, respectively.

The VM is implemented by combining 15 identical slices. The schematic of a single slice is shown in Fig. 16. Each slice contains a self-biased pseudodifferential g_m, a double-balanced passive mixer, and static reconfiguration switches steering the transconductor current in order to provide a phase shift. The VM slices are dc-coupled and the source and drain terminals of the mixer switches are biased at half of the supply via the self-biased TIA and g_m stages. LO level shifter, as shown

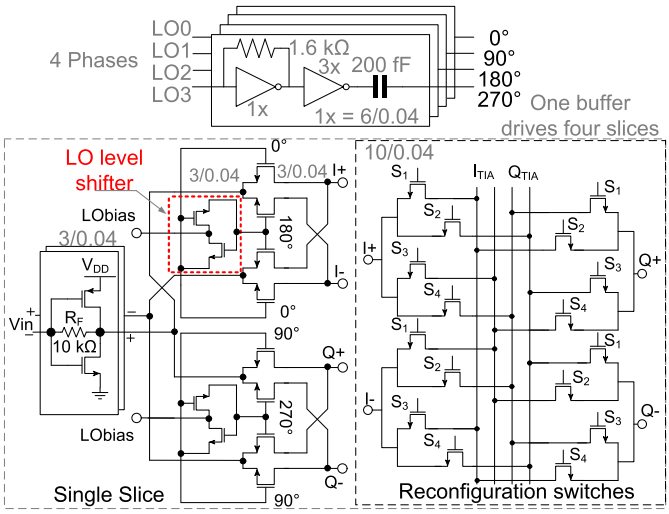


Fig. 16. Single slice and LO buffer stage for driving four slices.

in Fig. 16, is used to increase the gate voltage of the mixer switches.

The I/Q clock generation is done via the current mode logic divider with PMOS load. It divides the multiplied-by-2 clock by 2 and generates the four phases with a 50% duty cycle. The 25% duty cycle clock is generated using the AND gate logic.

C. Receiver Partitioning

Simulated performance for the single receiver chain is shown in Fig. 17. Here, the signal is going from the input of the FE to the BB output. Connection points to and from the mmWave C2C signal path and IF C2C path is also marked. Simulated data for the gain, input compression point ($\mathrm{IP}_{1\,\mathrm{dB}}$), and NF for the FE are shown at two different bias configurations. It can be seen from the figure that the linearity for the single receiver chain is limited by the large FE gain. Furthermore, in the minimum gain case, the mixer and the downstream blocks become the bottleneck for linearity. Extrapolating from this data, the estimated $\mathrm{IP}_{1\,\mathrm{dB}}$ for combining four FEs will be in the range from -64 to -44 dBm. From the noise perspective, the large gain of the FE effectively dominates the NF.

Similarly, simulated receiver parameters of mmWave C2C interface and IF C2C interface are shown in Figs. 18 and 19, respectively. The gain of these interfaces is designed to be low and just enough to overcome the PCB path losses. Looking at the NF of the output end of the mmWave C2C interface, it can be seen that it is large. This is largely because of two reasons, the first one is the presence of a VSPS. The second reason is related to the signal combiner that is just before the VSPS. It is combining the signal coming from the local loop-back and the debug bypass from the mRM. Both of these paths are debug paths and at the combining end, share the biasing with the main path. Thus, even though the source g_m stages which are providing the debug currents can be turned off, because of the shared biasing control, the combiner is still receiving noise from these paths. The output side of the IF C2C does not have a VSPS nor a debug bypass current. It has to be noted that the VSPS in the mmWave C2C interface can be moved

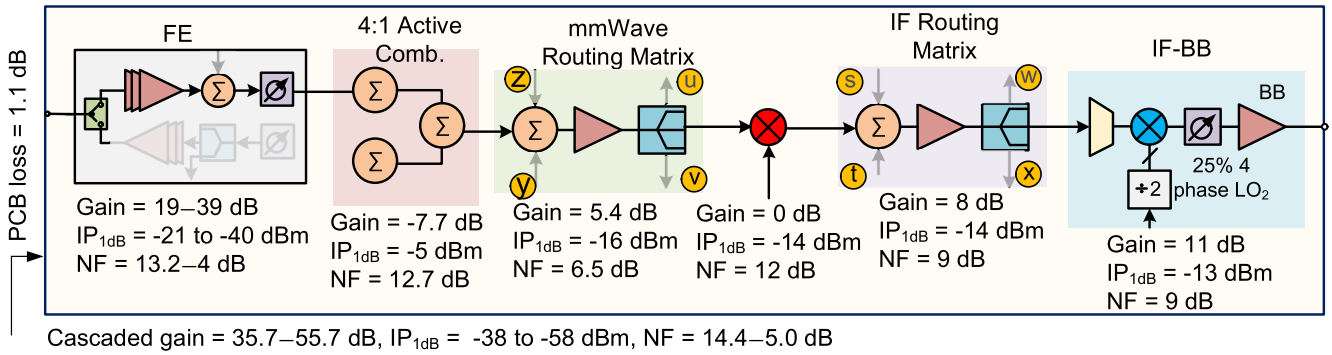


Fig. 17. Simulated receiver parameters for the single chain when the mmWave signal is propagating from one FE to the BB of the same RFIC. Estimated $IP_{1\,dB}$ while combining four FEs will be in the range from −64 to −44 dBm.

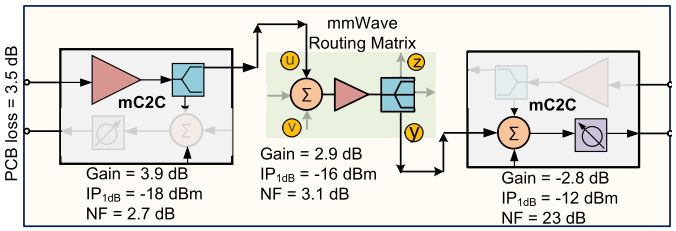


Fig. 18. Receiver parameters for the signal path between the mmWave C2C interfaces.

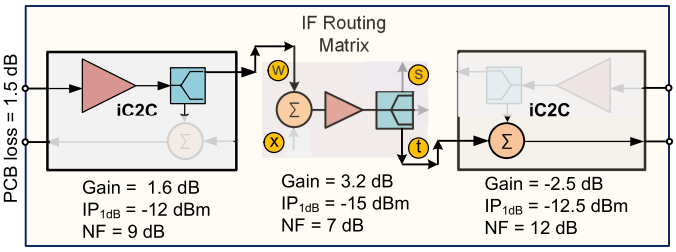


Fig. 19. Receiver parameters for the signal path between the IF C2C interfaces.

to the LO path without impacting the system functionality. However, keeping it here keeps the system logically organized. This design decision, however, forces a compromise in noise while helping in the testing of the prototype.

Large gain of the FEs, along with the limited linearity of the mixers, results in reduced dynamic range in case of high input power levels. As shown later in EVM variation measurements, with efficient gain control this problem can be overcome even for high-order modulations in the case of a single RFIC. However, when combining many antennas over several RFICs, limited dynamic range becomes a bottleneck. This may require a revised gain partitioning along with a re-design of the key building blocks based on tighter linearity specifications. Circuit design techniques such as current bleeding and derivative superposition [45] can be used to improve linearity. It should be noted that the issue of limited linearity when combining many antenna elements, is not just inherent to the presented architecture. It equally plagues the conventional corporate-fed arrays as it depends mostly on the number of antenna elements being combined.

TABLE III
DC POWER CONSUMPTION

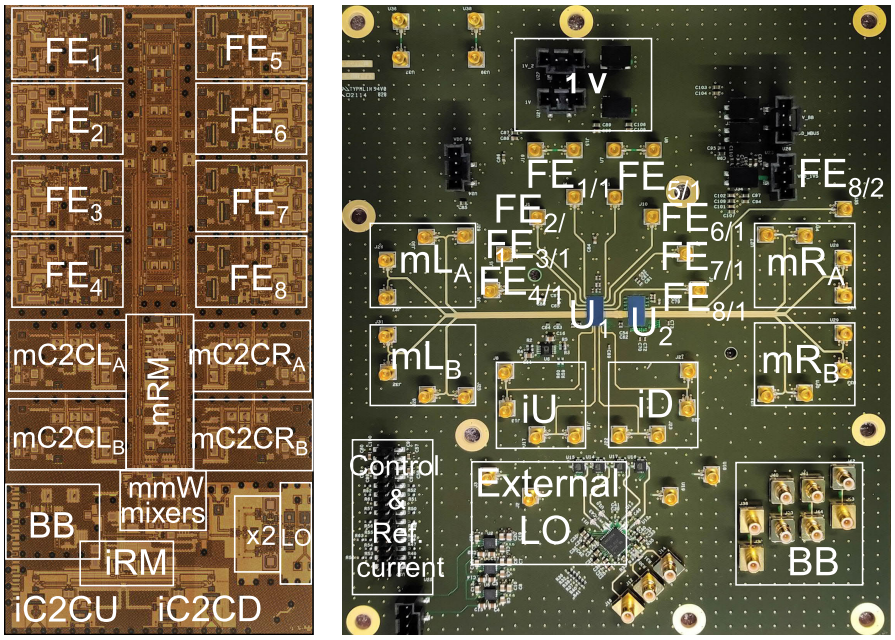
Block	Mode	Power Consumed (mW)
FE	Normal mode	60.1
	Hybrid mode	66.5
mmWave Routing Matrix (mRM)[a]		47
mmWave chip-to-chip interface (mC2C)	Input	15.4
	Output	70.7
IF chip-to-chip interface (iC2C)	Input	17.7
	Output	17.1
Mixer	mmWave to IF	8.5
BB[b]	RX	132.6
LO [c]		37.6
Four antennas combined at BB / per antenna	Single RFIC	116.5
Eight antennas combined at BB / per antenna	Two RFICs via mmWave C2C interface	105
	Two RFICs via BB	116.6

[a] Single stream.
[b] Includes consumption of divider and LO buffers for the passive IF to BB mixers. [c] Includes consumption of multiplier.

IV. EXPERIMENTAL RESULTS

RFIC is fabricated using GlobalFoundries 45-nm CMOS SOI technology. The micrograph is shown in Fig. 20(a). The overall dimensions of the RFIC are 4.4 × 8 mm. Dimensions of a single FE are 1.6 × 0.9 mm. Normalized area per element per stream is estimated to be 2.7 mm^2, calculated similarly as in [24]. DC power consumed by the various blocks from 1-V supply is shown in Table III. As seen from Table III, in terms of power consumption, combining multiple antennas to one BB by using a C2C interface is more efficient than external combining via multiple BBs. The normalized power consumption will further decrease as the number of antenna elements combined via the C2C interface increase.

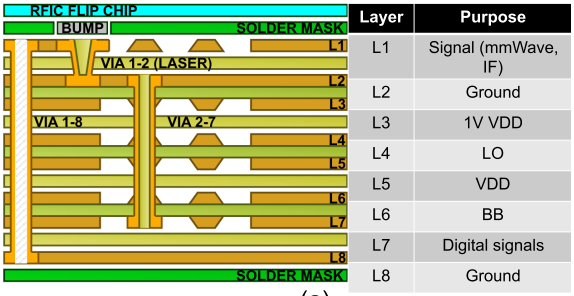
The PCB used for measurements is shown in Fig. 20(b). It is an eight-layer board manufactured using Panasonic's Megtron7 substrate ($\varepsilon_r = 3.34$). The cross section of the PCB along with the PCB layer usage can be seen from Fig. 21(a). The RFICs are flip-chips and are directly bonded to the PCB. Controlled collapse chip connection (C4) of size 73 μm with a minimum pitch of 150 μm are used. PCB footprint of the RFIC is shown in Fig. 21(b). Simulated isolation between different mmWave PCB ports was found to be in excess of 30 dB. The PCB has two RFICs U_1 and U_2.



(a) (b)

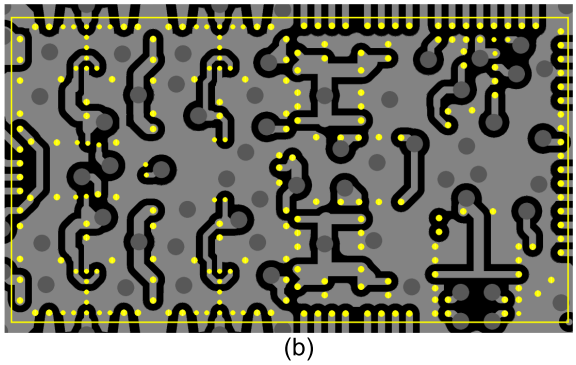
PCB Label	Description
U_1, U_2	Two RFICs
$FE_{1/1}$, $FE_{2/1}$…$FE_{8/1}$	SMPM ports connected to FEs of RFIC U_1.
$FE_{8/2}$	SMPM port connected to eighth FE of RFIC U_2.
mL_A, mL_B	SMPM ports for left side mmWave C2C i/f. Connected to U_1.
mR_A, mR_B	SMPM ports for right side mmWave C2C i/f. Connected to U_2.
iU, iD	SMPM ports connected to Up and Down direction IF C2C i/f. Both are connected to U_1.

Fig. 20. (a) Micrograph of the manufactured RFIC. Total silicon area occupied by the RFIC is 35.2 mm^2. (b) Test PCB with two RFICs, U_1 and U_2, connected using the mmWave C2C interface. RFIC U_2 is used specifically for verifying the C2C interface functionality. In order to differentiate between FEs connected to the two RFICs, the corresponding PCB ports are labeled with the RFIC number in the subscript.



Layer	Purpose
L1	Signal (mmWave, IF)
L2	Ground
L3	1V VDD
L4	LO
L5	VDD
L6	BB
L7	Digital signals
L8	Ground

(a)



(b)

Fig. 21. (a) Cross section of the eight-layered Megtron 7 PCB along with the layer usage. (b) PCB footprint of the RFIC, dots in yellow show the location of the C4 bumps.

The RFICs are further connected to each other via their right and left mmWave C2C interfaces, respectively. All FEs of U_1 are connected to the subminiature push-on micro (SMPM) connectors. However, due to area limitations only FE_8 of RFIC U_2 is connected to an SMPM connector, while the other FEs are permanently terminated with a 50-Ω resistor. For the same reason, the IF C2C interfaces and BB interfaces of only the RFIC U_1 are connected to external connectors. PCB ports marked mL_A and mL_B are connected to the left side stream A and stream B mmWave C2C interface ($mC2CL_A$ and $mC2CL_B$) of RFIC U_1, respectively. Likewise, PCB ports mR_A and mR_B are connected to the right side stream A and stream B mmWave C2C interface ($mC2CR_A$ and $mC2CR_B$) of RFIC U_2, respectively. PCB ports labeled iU and iD are connected to the upside and downside of the IF C2C interface (iC2CU and iC2CD) of RFIC U_1, respectively. It has to be noted that the length of the PCB line connecting $FE_{8/2}$ is about 44 mm longer than the PCB lines used for connecting $FE_{1–8/1}$ to their corresponding FEs on U_1. Furthermore, it is almost ten times longer than the RFIC-to-RFIC interconnect. This needs to be taken into account when beam pattern measurements are performed. Unless otherwise specified, the reference plane for all the measurements is set at the input of the PCB connectors, i.e., connector losses and PCB line losses are part of the measured results.

A. Conductive Measurements

Frequency responses are measured from different mmWave inputs both with fixed LO (BB response) and variable LO (RF response). Fig. 22(a) shows the high side BB gain a response from different inputs. The output is taken only from the I branch of the BB. A four-port VNA along with an external LO generator is used for the measurements. Here, the mRM of RFIC U_1 is operating in swMode III and RFIC U_2 is operating in swMode I, as defined in Section III-A. Furthermore, FE_8 of both U_1 and U_2 have been measured in normal mode (mode I) and hybrid mode (mode II). Fig. 22(a) shows that in all of the modes, there is roughly 47 dB of gain from input of the FEs to the output of RFIC U_1 BB. The solid lines show the gain when the VNA input port is on the FE_8 of RFIC U_2 and the dashed lines show the gain when the input port is connected to

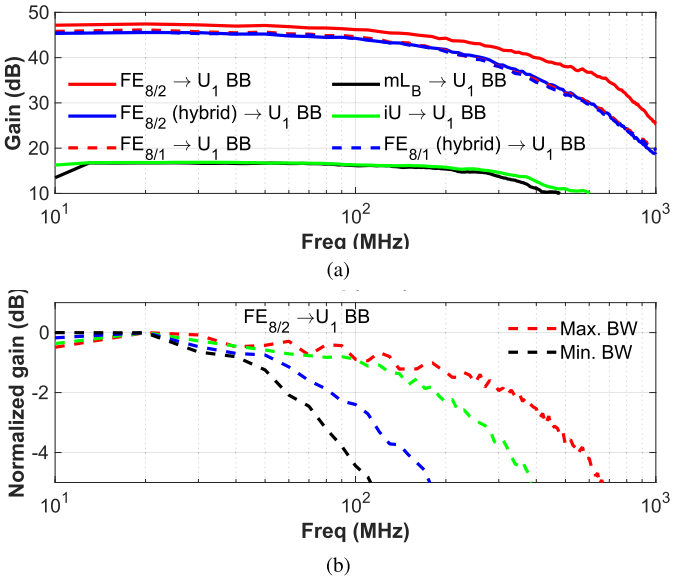


Fig. 22. (a) High side BB response from different FE inputs. (b) Normalized gain for different bandwidth settings. All measurements are done with a fixed LO frequency of 9 GHz, i.e., a carrier frequency of 27 GHz. The results are from the I branch of RFIC U_1 BB.

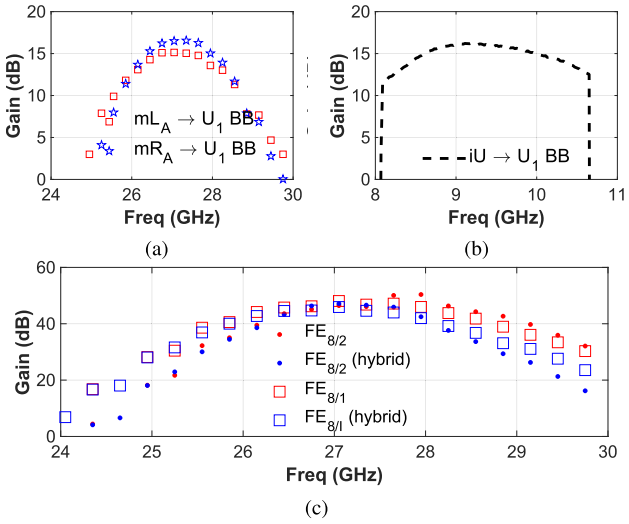


Fig. 23. RF gain from different inputs measured at a fixed BB output frequency of 50 MHz. (a) RF gain from the mmWave C2C interface. (b) RF gain from IF C2C interface. (c) RF gain from different FE inputs.

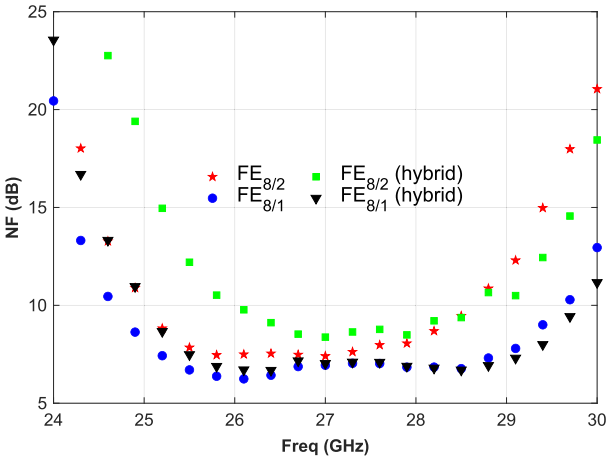


Fig. 24. FE's NF measured at a fixed BB output frequency of 100 MHz. BB on RFIC U_1 is used and mmWave C2C interface is used for routing $FE_{8/2}$ toward RFIC U_1's BB.

the FEs of RFIC U_1. For both U_1 and U_2, the gain difference between the two FE modes (mode I and mode II) is less than 1 dB. The gain difference between the two RFICs is less than 2 dB which can be corrected via either the gain control in the C2C interface or the LNA bias settings. Furthermore, there is around 17 dB of gain from both the mmWave C2C interface and from the IF C2C interface to the BB. The input frequency for the mmWave inputs is varied from 27 to 30 GHz. In the case of the IF input, the input frequency is varied from 9 to 12 GHz. The LO frequency is kept constant at 9 GHz. Fig. 22(b) shows the normalized gain for one of the FE inputs in order to showcase the bandwidth variation capabilities of the RFICs BB. It can be seen from the figure that the BB bandwidth can be varied from 80 to 430 MHz, depending on the bandwidth of the received modulated signal.

The RF response from different inputs down-converted to a fixed BB frequency of 50 MHz is shown in Fig. 23. The frequency for the mmWave input is varied from 24 to 30 GHz. Looking at the RF response from the mmWave C2C interface in Fig. 23(a), it can be seen that the gain difference between the left (from mL_A to RFIC U_1 BB) and the right (from mR_A to U_1 BB) side path is around 1.5 dB. The RF response for the IF C2C interface is presented in Fig. 23(b). The input is connected to the up-direction IF PCB port (iU) and is varied from 8 to 11 GHz. Besides the peak RF gain of 16 dB, the figure also shows the combined locking range of the frequency multiplier and divider, which is 8.1–10.7 GHz. RF response from $FE_{8/1}$ to $FE_{8/2}$ in both normal (mode I) and hybrid mode (mode II) can be seen from Fig. 23(c).

The measured noise figure (NF) at a fixed BB frequency of 100 MHz is shown in Fig. 24. The figure shows the NF for both $FE_{8/1}$ and $FE_{8/2}$ in both normal (mode I) and hybrid mode (mode II). Keysight UXA N9040B along with a broadband noise source (346CK01) is used for measuring the NF. The simulated losses of the PCB lines are calibrated. The minimum NF value of 6.2 dB occurs at 26 GHz. Looking at the simulated NF presented in Section III-B10, there is a 1.2 dB difference compared to the measured results. A small part of it can be attributed to the inaccuracies in the measurement setup. Another reason is related to the simplifications done in the simulation setup.

Given the single-ended nature of the FEs and their large gain, there can be significant coupling between different FEs. Furthermore, based on the coupling mechanism and phase, its value can be dependent on the phase shift provided by the VSPS. To verify this, coupling between adjacent FEs (FE_1 and FE_2, FE_3 and FE_4, and so on) and facing FEs (FE_1 and FE_5, FE_2 and FE_6, and so on) is measured as a function of phase shift provided by one of the VSPS. The worst-case coupling measured is of the order of -30 dB.

In order to understand the combined behavior of noise, linearity, and gain of the input stage, multiple noise and compression measurements are done using different bias settings for the LNA. For these measurements, $FE_{2/1}$ of RFIC U_1 is the input port and differential output is taken from the mmWave C2C interface mL_A. The combined results are

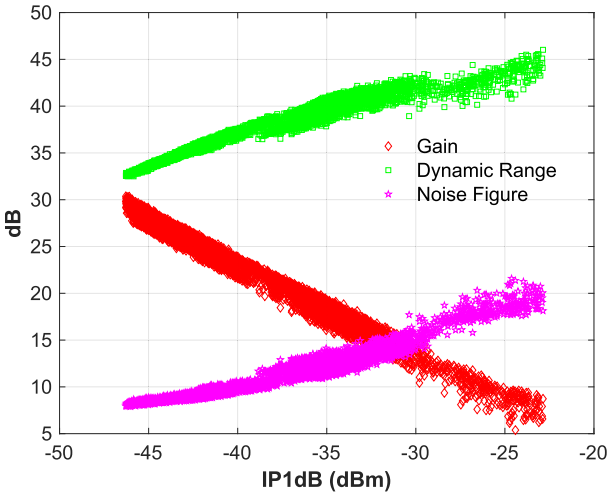


Fig. 25. Gain, NF, and estimated dynamic range of the mmWave path as a function of its input compression point. A 500-MHz signal bandwidth is used for the dynamic range calculations. Signal input is at the FE of RFIC U_1 and differential output is taken from the same RFICs mmWave C2C interface. A similar method as in Fig. 24 is used for the noise measurements.

plotted in Fig. 25. The figure shows the measured NF, RF gain, and the estimated dynamic range for a 500-MHz signal as a function of input 1-dB compression point. The dynamic range is defined as $P_{\text{out}} - P_{\text{noise}}$, with P_{out} being the output signal power as defined in (1), and P_{noise} is the output noise power as defined in (2) [46]. $P_{\text{i1 dBm}}$ refers to the input 1-dB compression point, $G_{\text{1 dB}}$ refers to the gain at 1-dB compression point, B is the bandwidth and NF is the noise figure

$$P_{\text{out}} = P_{\text{i1 dBm}} + G_{\text{1 dB}} \tag{1}$$

$$P_{\text{noise}} = -174 + 10\log B + \text{NF} + G_{\text{1 dB}}. \tag{2}$$

It can be seen from the figure that the available dynamic range varies from 33 to 48 dB as the gain decreases from 31 to 5 dB. This is because of the increase in compression point with decreasing gain and thus higher input signal power can be fed. These curves can be utilized for designing gain control for the receiver. Comparing these numbers with the simulated results in Section III-B10, it can be seen that the values do agree with in a margin of 2 dB. It has to be noted that the measured path shown here, is not directly depicted in either Figs. 17 nor 18 and has to be calculated utilizing data from both Figs. 17 and 18.

Given the relatively high power of the LO compared with other signals in a receiver along with the presence of a frequency doubler on the RFIC, LO leakage is measured at different ports of the RFIC. The different ports where LO leakage is measured are shown in Fig. 26 and the results are displayed in Fig. 27. Input LO of 9 GHz is fed from an external signal generator at a power level of 4 dBm measured at the PCB port. The strongest LO leakage is seen at the FE input port, with the 9 GHz LO being measured at a level of −47.5 dBm. No noticeable leakage is seen at the IF C2C ports and the leakage at mmWave C2C output interface is at a level of −62 dBm. Similar levels of LO leakage are also measured at the BB ports.

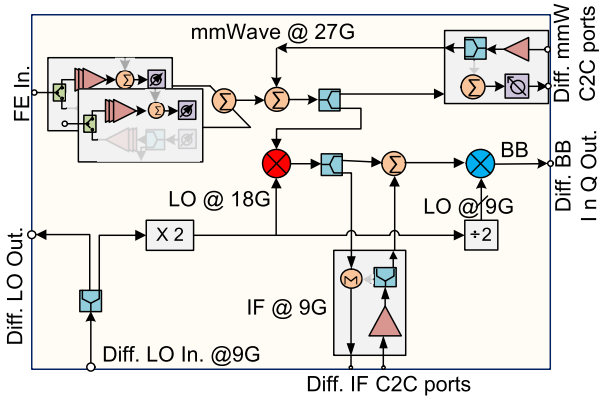


Fig. 26. Simplified block diagram depicting different ports where LO leakage is measured.

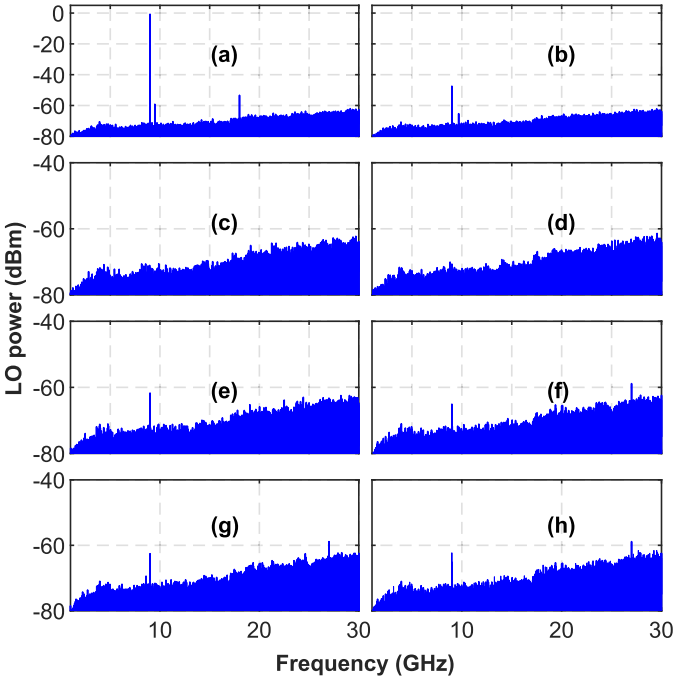


Fig. 27. Measured LO power at different ports. (a) At differential LO output port (used for daisy chaining). (b) At single-ended FE port. (c) At differential IF C2C input port. (d) At differential IF C2C output port. (e) At differential mmWave C2C input port. (f) At differential mmWave C2C output port. (g) At differential BB I port. (h) At differential BB Q port. The calibration plane is at the PCB connectors.

In order to understand the limitations of the different signal paths of the RFIC that are essential for reconfiguration requirement (shown in Fig. 28), gain and compression measurements are done. No input signal is fed to the FEs in these measurements. These results are tabulated in Table IV. Path A corresponds to the case where the RF signal from other RFICs goes through the mmWave C2C interface and is combined together with the local FE signals and is then down-converted to BB. Path B corresponds to the case of transferring the signal across the RFIC. Path C is equivalent to path B, however, operating in the IF domain via the IF C2C interface. Path D integrates one frequency conversion, from mmWave to IF. Path E corresponds to moving the signal from IF to BB. The target for the C2C interfaces is to have unity gain between

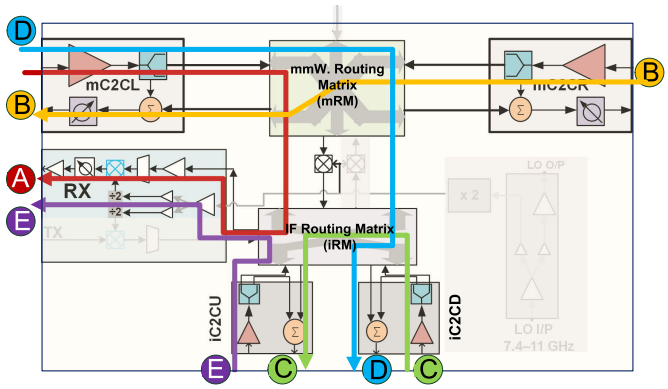


Fig. 28. Simplified block diagram depicting different signal paths required for the reconfiguration functionality.

TABLE IV
GAIN AND INPUT COMPRESSION POINT

Path	IP_{1dB} (dBm)	Gain (dB)
A	-20	20
B	-14	0
C	-7	-6
D	-18.5	-6
E	-20	17

combining nodes. The choice between active combining and passive combining at the routing matrices depends mostly on the size of the phased array panel along with the linearity of the common down-conversion and amplification path before digitization.

Conductive modulated measurements are performed using the setup shown in Fig. 29. Fig. 30 shows the EVM variation with respect to the input power for different 5G NR waveforms. Different curves correspond to different bias settings for the LNA, i.e., different gain values. It can be seen from the figure that for a 100-MHz wide signal, i.e., one component carrier (1 CC), the DUT can be configured to have an EVM of under 8% for an input power range from −60 to −25 dBm. Furthermore, for one fixed bias setting, there is a range of around 17–21 dB over which the received signal has the required fidelity. As expected, the power range decreases as the bandwidth of the modulated signal increases as seen from the traces of 400 MHz wide signal (4 CC), which has EVM less than 8% over an input power range from −55 to −27 dBm. For a 200 MHz wide 256 QAM signal, given the high dynamic range required, the available power range over which the EVM is less than 3.5% is from −47 to −32 dBm. Constellation diagrams for these different modulated signals are shown in Fig. 31. The EVM limits of 8% for 64 QAM and 3.5% for 256 QAM are obtained from the transmitter specification for the FR2 band [47]. These curves also demonstrate the optimum EVM window. It should be noted that the peak-to-average power ratio for the 5G NR waveforms is around 10.5 dB, around 5 dB higher when compared with the similar single-carrier waveforms. This along with the limited linearity of the DUT are the major reasons which limit the optimum EVM window.

In order to verify the efficacy of performing signal combination over the mmWave C2C interface, two FEs were combined using either a single RFIC or two RFICs, as shown in Fig. 32. The VSPS was configured for 27 GHz of operational frequency. Fig. 33 shows the measured results.

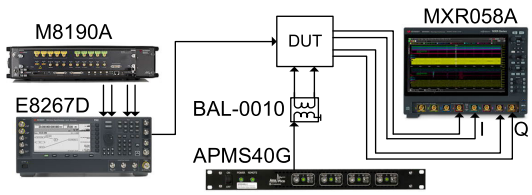


Fig. 29. Setup for the conductive modulated measurements. Various 5G NR FR2 Rel-15 waveforms are generated via M8190A, which are up-converted to 27 GHz using E8267D and fed to the mmWave input $FE_{1/1}$ of the DUT. AnaPico APMS40G-2 provides the 9 GHz LO. BB data are analyzed via the MXR058A oscilloscope, which is being controlled via PathWave Vector Signal Analysis (89 600 VSA) software.

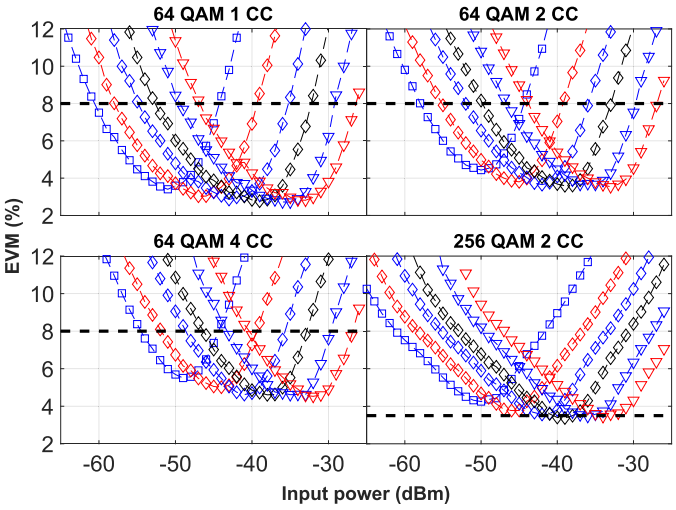


Fig. 30. EVM variation of different 5G NR FR2 waveforms as a function of the input power. The bandwidth of each component carrier (CC) is 100 MHz. Different curves correspond to different gain values of the LNA. EVM limit for different modulation schemes as defined in the 3GPP specifications [47] for the transmitter side is marked by a black dashed line.

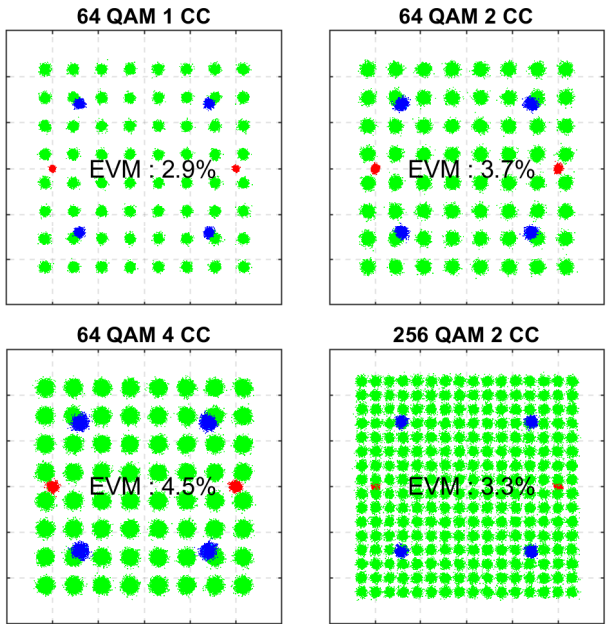


Fig. 31. Received constellation diagrams for the different NR FR2 waveforms. EVM measurements are done using the conductive modulated setup.

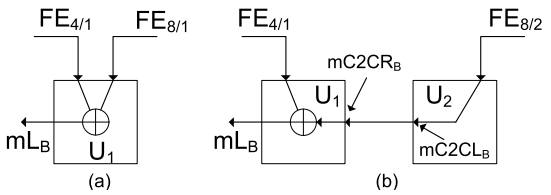


Fig. 32. Setup for combining two FEs (a) via one RFIC and (b) via two RFICs utilizing the mmWave C2C interface.

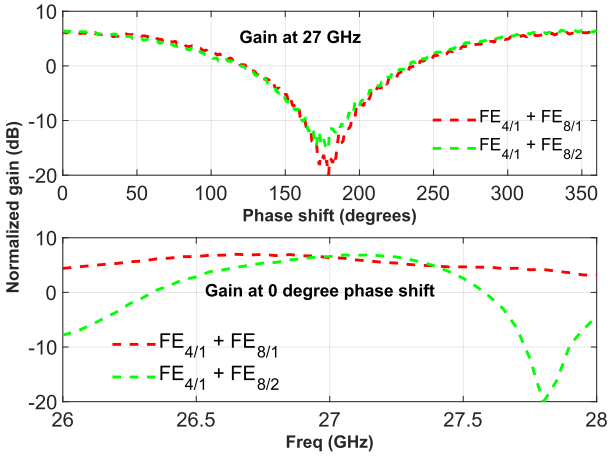


Fig. 33. Normalized amplitude response for combining two FEs via one RFIC versus two RFICs.

Normalized gain is plotted for both cases first as a function of the relative phase shift between FEs and then as a function of the frequency. In order to ease the analysis of the top half of Fig. 33, the traces are circularly shifted so that the minimum occurs at a phase shift of 180°. It can be seen from the figure, that in both cases the signal amplitude increases by 6 dB when the signals are in phase. However, looking at the frequency response from the bottom half of Fig. 33, it can be noted that for the two RFIC cases, the frequency range over which two signals are coherent is considerably smaller than the one RFIC case. One possible explanation for this behavior is the long PCB line over which signal for $FE_{8/2}$ travels.

B. Over-the-Air Measurements

The setup for performing the over-the-air (OTA) measurements is shown in Fig. 34. At the transmitter end, an external amplifier (CA2630-141) along with a horn antenna (LB-28-15) is used. The horn antenna is mounted on a fixed tripod and is placed in far-field 2.7 m away from the DUT. At the receiving end, a 64-element antenna array is used [48]. It is made up of 16 unit cells, with each unit cell containing four linearly polarized patch elements arranged in a 2 × 2 configuration. Four FEs of the DUT are connected with four unit cells of the 64-element antenna array and are mounted on a rotating platform. Measurements using both continuous wave and wide-band modulated signals are conducted. The link budget for the OTA measurements is presented in Table V.

Two different scenarios are compared in these measurements. In the first scenario, the four-unit cells of the antenna array are combined at mmWave using a single RFIC (U_1). This combined signal is either routed to PCB port mR_A via

TABLE V
LINK BUDGET FOR THE OTA MEASUREMENTS

Parameter	Value
I/P RF power	-8 dBm
Cable Loss (a)	7 dB
CA2630-141 gain	25 dB
Cable Loss (b)	2 dB
Horn gain	14 dBi
Estimated path loss (2.7 m)	70 dB
Receiver antenna gain (one sub-array)	9.6 dBi
Cable Loss (c)	1.5 dB
Estimated power at FE i/p	**-40 dBm**

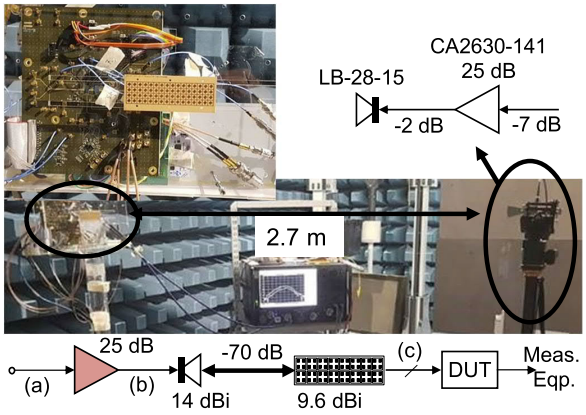


Fig. 34. Setup for doing the OTA measurements. At the receiver side, four unit cells out of 16 of a 64-element antenna array are used, providing a total antenna gain of 15.6 dBi. Details related to stand-alone antenna array can be found from [48].

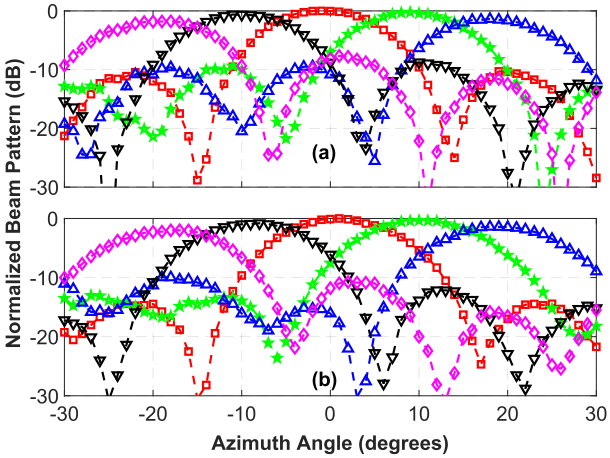


Fig. 35. Measured normalized beam pattern for a combination of four sub-arrays plotted at 27 GHz with inputs in (a) single RFIC and (b) two RFICs (3 + 1).

mmWave C2C interfaces for calibration or down-converted to BB for measurement. $FE_{1,3,5,7/1}$ are used in this scenario. In the second scenario, three FEs ($FE_{1,3,5/1}$) from RFIC (U_1) are used and one FE ($FE_{8/2}$) from RFIC (U_2) is used for combining. $FE_{8/2}$ is operated in hybrid mode and routed to RFIC U_1 via the egress port of U_2's mmWave C2C interface ($mC2CL_A$). The combination happens in RFIC U_1 and the combined signal is again either routed toward PCB port mR_A via the

TABLE VI
COMPARISON WITH STATE OF THE ART

		This Work	[20] JSSC19	[31] JSSC22	[28] JSSC21	[49] MTT20	[9] JSSC17	[21] MTT20
Technology and architecture	Technology	45 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS	0.18 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS	0.18 µm SiGe BiCMOS
	TRX	TRX[a]	TX + RX[b]	TRX	RX	TRX	TRX	TRX
	RFIC integration level	FE, Mixer, LO, BB	RX, TX, Mixer, LO	FE, Mixer, LO, BB	RX, Mixer, LO	FE	FE, Mixer, LO	FE, Mixer, LO
	Receiver type	Sliding IF	IF	Direct conversion	IF	RF	IF	IF
	Phase shifting freq.	RF	LO	LO	LO	RF	RF	RF
	Elements/RFIC	8	4	8	4	8	32	128
	No. of streams / RFIC	2	1	4	4	2	2	2
	Beamforming architecture	RF and hybrid beamforming	LO beamforming	Two-layer hybrid beamforming	Hybrid beamforming with frequency duplexed o/p	RF beamforming	Two layer RF beamforming	RF and combining at IF
	Scaling technique	Tiling via chip-to-chip interfaces	n/a	n/a	n/a	Tiling via symmetrical routing and power combining	Tiling via symmetrical routing and power combining	Reticle-to-reticle stitching with symmetrical IF distribution
	Chip-to-chip interfaces	4@RF and 2@IF	No	No	No	No	No	1@IF
	RF (GHz)	26–28	26.5–29.5	28/37	28	28–32	27–28.5	60
	IF (GHz)	8–11	2.5–5.5	-	0.37–2.63	-	2.25–3.75[c]	8
	Area / element / stream	2.7	3[c]	1.05	0.66	2.9[c]	5.2[c]	3.4[c]
Single element RX mode performance	Gain (dB)	23–50	12	44	≥ 16	2–18[c]	32	20–34
	BB BW (MHz)	≥ 800	-	680[c]	≥ 450[d]	-	-	-
	NFmin	6.2	4.1[b]	7.9	6[b]	4.8	6[f]	8–10[i]
	IP_{1dB} (dBm)	−22 to −50	-23[c]	-29	-36.9	−7 to −21	-22.5	−47 to −59
	Power / RFIC / Stream (mW)	116.5	148	98.75	28.1	163	206.2	158
mmWave PS performance	Phase resolution (°)	0.5	0.3	3–5[e]	NA	5.6	5	11.25[c]
	RMS phase error (°)	≤ 1.5	0.3	1.4[g]	NA	3.6[c]	0.8	≤ 8
	RMS gain error (dB)	0.16	0.04	0.15[g]	NA	0.6[c]	±0.7(peak)	≤ 1.1
Modulated performance	Signal Type	5G NR FR2 OFDM	SC	SC	SC	SC	SC	SC
	Max data rate / stream (Gbps)	4.3	15	1	0.4	30	5.16	12
	Constellation	64 QAM @ 800MHz[h]	64 QAM @ 2.5GS/s	16 QAM	16 QAM @ 100MS/s	64 QAM @ 5GS/s	256 QAM @ 800MHz	16 QAM @ 3Gbaud/s
	EVM (%)	6.1	5.5	9.7	4	6.9	-	9.5
	OTA distance (m)	2.7	5	1.8	-	1	1.8	1.3
	Antenna array size	4×1[h]	8×1	4×1	2×2	2×64	64	2×256

[a] Measurements are done only for RX. [b] No TRX switch. [c] Estimated from the available data in the paper. [d] Estimated from IF response. [e] Taken from [24]. [f] Taken from [50]. [g] Taken from [51]. [h] Limited by setup. [i] Simulated.

mmWave C2C interfaces of U_1 and U_2 or down-converted to RFIC U_1 BB.

The measured normalized beam patterns for both one RFIC and two RFICs with four antenna ports, i.e., 16 antenna elements are shown in Fig. 35. The different colored curves in the figure show the main lobe being pointed toward five different directions. Furthermore, in both cases, the beam patterns have roughly the same shape. Fig. 36 shows the EVM results for a 4 CC 64 QAM NR FR2 waveform. Here too, in both cases, similar EVM is achieved and the EVM is distributed spatially in roughly the same pattern. The measurements are done at a mmWave frequency of 27 GHz.

In order to visualize the beam pointing error which occurs when compensating time delay with phase shift, an 8 CC wide NR FR2 waveform is used for measuring the spatial distribution of EVM and the results are plotted in Fig. 37. It can be seen from Fig. 37(a) that in case of single RFIC combining, even with an 800 MHz wide signal, there is almost no difference in the beam pointing. That is, both the lowest and highest frequency CCs (CC 1 and CC 8) achieve their minimum EVM at roughly the same azimuth angle, which coincides with the azimuth angle at which the normalized beam pattern achieves its maximum. However, for the two RFICs case in Fig. 37(b), the individual CCs are pointing to different directions and the pointing error for CC 1 and CC 8 is

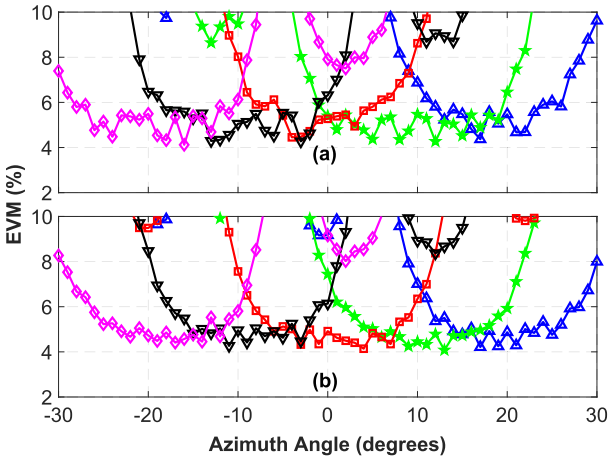


Fig. 36. Measured EVM for a combination of four sub-arrays plotted as a function of azimuth angle. A 64 QAM 4 CC NR FR2 waveform has been used as a modulated signal. The inputs are in (a) single RFIC and (b) two RFICs (3 + 1).

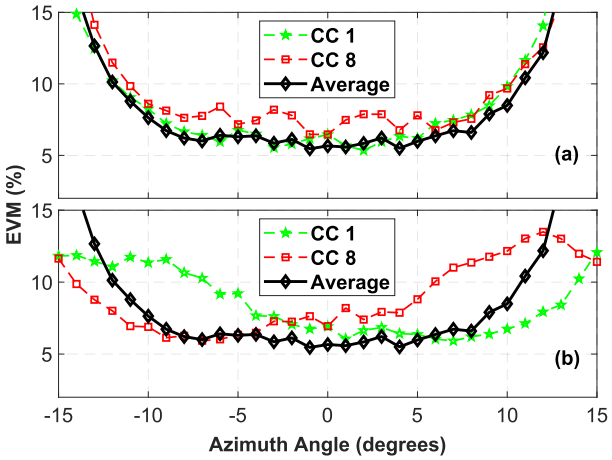


Fig. 37. Measured EVM for a 64 QAM 8 CC NR FR2 waveform showing the beam pointing error in case of a combination of four sub-arrays via inputs in (a) single RFIC and (b) two RFICs (3 + 1).

around ±5°. Yet, the azimuth pointing angle for the average EVM for all the CCs still coincides with the azimuth angle of the normalized beam pattern showing no degradation in total signal quality. One must note that the input signal path lengths are very different between the two RFICs due to the test setup limitations. This introduces a larger asymmetry than anticipated in a complete phased array.

Comparisons with other relevant recent works are shown in Table VI. It can be seen from the table that the single element performance in terms of BB bandwidth and RF gain exceeds compared with the recent works. This work provides the most versatile capabilities for reconfigurability in large-scale phased arrays at the cost of marginally larger normalized area and power compared with [28] and [31].

V. Conclusion

In this article, an architecture to enable a flexible and programmable organization of single antennas in a large antenna array was proposed. This was achieved with an RFIC with multiple C2C interfaces. The proposed transceiver architecture with the C2C interfaces enables extremely versatile mechanisms to configure large antenna array panels to support communication using multiple simultaneous beams. The RFIC was designed and fabricated using GF 45-nm PDSOI technology, and its performance was verified via both conductive and OTA measurements. The receiver performance of the mmWave RFIC was measured. Gain control was implemented by changing the bias. For beamforming, phase shifting was performed at RF using an active vector summing-based phase shifter. Furthermore, a two RFIC test PCB was constructed to validate the concept of a dynamically configurable beamformer utilizing the mmWave C2C interface. Beam pattern measurements were conducted for a combination of four sub-arrays over the mmWave C2C interface. No additional pointing error for the main lobes was found compared with similar measurements using a single RFIC.

The Achilles heel of this work seems to be the relatively low linearity that limits the power over which minimum EVM is achieved, as seen in Fig. 30. This limitation stems from the combination of excessive gain at the FE, along with the limited linearity of the mixer and downstream blocks. This is further exacerbated by the lack of independent gain control, as the bias-based gain control impacts linearity at the same time. Furthermore, it can be hypothesized that the linearity of the mRM and iRM may also become a bottleneck when combining a large number of RFICs. Having said that, the limitations are in the implementation and are not inherent to the architecture and these imitations can be overcome via revised gain partitioning, careful circuit design, and using techniques such as current bleeding and derivative superposition.

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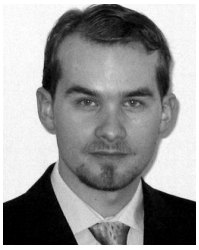

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