A 30-GHz Class-F Quadrature DCO Using Phase Shifts Between Drain–Gate–Source for Low Flicker Phase Noise and I/Q Exactness

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***Abstract*— In this article, we present a low phase noise (PN) mm-wave quadrature digitally controlled oscillator (DCO) exploiting transformers for class-F operation and harmonic extraction. A third transformer coil is added for the inter-core coupling with the source terminals of the switching transistors. We identify that the inter-core coupling in quadrature oscillators causes an asymmetric flicker noise current, thus degrading flicker PN. As a remedy, we propose a deliberate drain-to-gate phase shift of the switching transistors by means of capacitive loading to fix this asymmetry. The ±90° I/Q mode ambiguity is also resolved by introducing another phase shift in the source-coupling; it is explained by a simplified analysis with phasor diagrams. Fabricated in the TSMC 28-nm LP CMOS, the prototype achieves PN of −112 dBc/Hz and figure-of-merit (FoM) of −185 dB at 1-MHz offset of 25.7 GHz. The measured flicker PN corner is 140–250 kHz and image rejection ratio (IRR) >47 dB over the whole 18% tuning range (TR). To the best of the authors' knowledge, it is the best reported PN and IRR for a mm-wave quadrature oscillator.**

***Index Terms*— CMOS, error vector magnitude (EVM), flicker noise upconversion, I/Q imbalance, image rejection ratio (IRR), injection locking, mode ambiguity, quadrature oscillator (QOSC).**

I. Introduction

THE dramatic increase in data rates in advanced wireless communications, such as 5G NR mm-wave, poses stringent specifications on the spectral purity of the carrier signal in supporting the complex modulation schemes (e.g., 256- or 1024-QAM) [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12]. At the same time, with the signal bandwidths reaching 800 MHz in the 5G mm-wave bands, direct conversion transmitters and receivers are preferred. This requires the local oscillator (LO) to generate the quadrature frequency of ultralow phase noise (PN) and excellent in-phase/quadrature (I/Q) precision. The quality of quadrature LO is customarily quantified by an error vector magnitude (EVM) as follows:

$$\mathrm{EVM}_{\mathrm{LO,IQ}}^2 = (J_{\mathrm{rms}} \cdot 2\pi f_0)^2 + 10^{-\mathrm{IRR}/10} \tag{1}$$

where f_0 is the carrier frequency, J_{rms} is the total rms jitter, and IRR stands for an image rejection ratio (IRR) describing the I/Q imbalance, whose contribution to EVM can be estimated as shown in Table I. As an example, to support 256-QAM in the 28-/39-GHz bands, we target $\mathrm{EVM}_{\mathrm{LO,IQ}} = 1\%$ (<3.5% EVM for the total transmitter's budget [1], [12]). This requires IRR = 45 dB and J_{rms} = 50 fs with the corresponding DCO/VCO's PN of < −110 dBc/Hz at 1 MHz from 28 GHz, per analysis in [13]. Also, the $1/f^3$ PN corner should be

TABLE I
SPECIFICATIONS OF IRR AND ITS CORRESPONDING EVM

IRR (dB)	32.04	36.48	46.02
IRR-induced EVM (%)	2.5	1.5	0.5

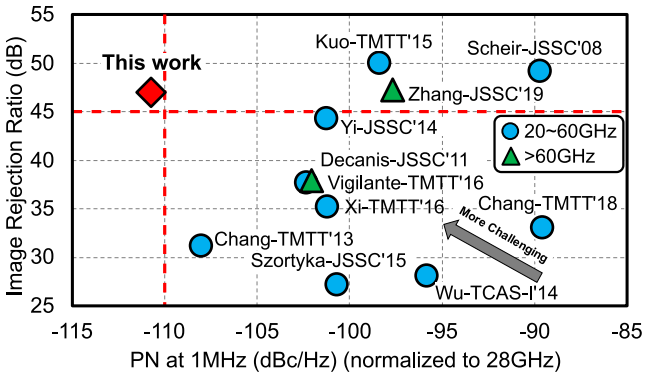

Fig. 1. Survey of key performance metrics of mm-wave QOSCs: PN at 1-MHz offset (normalized to 28 GHz) and IRR.

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smaller than 300 kHz; otherwise, it can ruin the PN at mid offsets, such as 1 MHz.

To construct an I/Q carrier signal, the designers can choose from a multi-phase oscillator (e.g., ring oscillator), a quadrature generation block (e.g., poly-phase filters (PPFs), $\div 2$ dividers), or an LC quadrature oscillator (QOSC). Poor PN and low resonating frequencies make ring oscillators unsuitable for mm-wave applications. Operating oscillators at $2\times$ frequency followed by a $\div 2$ divider is a suitable solution but only in the sub-6-GHz bands since doubling the operating frequency in mm-wave oscillators worsens the PN significantly [14], [15], [16]. Recently, a PPF seems to be a promising scheme for mm-wave I/Q generation [17], [18], [19], [20] since it would barely degrade the LO's PN. Nevertheless, a real-time I/Q calibration circuit [17] is required to maintain its I/Q accuracy against process, voltage, and temperature (PVT) variations. Furthermore, that approach tends to occupy a considerably large die area and requires power-hungry mm-wave LO isolation buffers.

As for QOSC, whether quadrature VCOs (QVCO) or DCOs (QDCO) [6], [7], [21], [22], [23], [24], [25], [26], [27], [28], [29], their I/Q accuracy [22], [30], [31], [32], [33], [34], [35], [36] is robust to the changes in PVT, requiring only one-time calibration against the local mismatches in the two cores [37]. However, their well-known $\pm 90^\circ$ I/Q mode ambiguity (i.e., low ω_L or high ω_H oscillating frequency mode), especially in "anti-phase coupling" QOSCs [22], [30], [38], [39], must be resolved before their practical integration into transceivers. This is due to the following issues: 1) the unpredictable I/Q phase ordering can confound the modulation (demodulation) in a transmitter (receiver); 2) the PN (especially, flicker PN) in one mode is typically much worse than in the other; and 3) the oscillation frequencies in the two modes may be far apart. Rofougaran et al. [21] gave an intuitive understanding that the QOSC may prefer (but not guarantee, [38]) the ω_H mode due to its higher tank impedance. On the other hand, Tonietto et al. [40] adopted an RC phase shifter in the coupling path to avoid the phase ambiguity. Later, a more rigorous analysis [39] based on complex differential equations pointed out that the ω_L mode could be completely squelched with an additional coupling delay. Interestingly, the QOSCs based on a "diode-connected MOS transistor ring" coupling [41], [42] show only one mode of oscillation due to the diode's unidirectional conduction.

On the other hand, the PN of QOSCs [31], especially the flicker PN, may suffer from a >10-dB degradation when compared with that of a single core [43]. Generally, active injection devices are commonly regarded as the main contributor to the flicker PN [30], [41]; however, QOSCs with passive coupling (e.g., transformer coupling with fundamental [44], [45], [46], [47], [48] or super-harmonics [32], [49], [50], or capacitive coupling [51], [52]) still exhibit poor $1/f^3$ PN. Recently, an introduction of additional capacitive coupling paths [53] in a series-coupled QVCO [22] demonstrated a low flicker PN in the single-gigahertz RF range with a balanced flicker noise injection from the switching devices. However, such progress has yet to be achieved for mm-wave QOSCs (see Fig. 1). As for the flicker PN theory of QOSCs, Andreani and Mazzanti provided pioneering analyses based on a time-invariant method [33] and a time-variant impulse sensitivity function (ISF) [34]. More details of the ISF-based analysis for QOSC are found in [53]. However, such analysis mainly focuses on the current-biased QOSCs in the RF range (e.g., <5 GHz) and/or a simplified flicker noise model in long-channel devices (e.g., 0.35 μm) with a sinusoidal ISF model, which may not be suitable to explain the flicker noise upconversion in the voltage-biased mm-wave QOSCs, especially in advanced CMOS. For example, the common-mode (CM) return path has been demonstrated as having a large influence on mm-wave oscillator's flicker PN [54], [55], while its relevant discussion in QOSCs is still conspicuously absent. With the supply voltage decreasing in advanced CMOS, it is inevitable that the transistors that generate the negative resistance in QOSCs will enter the triode regions for some time [56], thereby generating higher harmonic voltage content with more complex ISFs [also must consider both differential-mode (DM) and CM tank voltages]. Therefore, a mm-wave QOSC achieving low flicker PN at same level as its non-quadrature counterpart [10], [54], [57], [58] is highly desired. To ease the learning curve for the designers, we further attempt to make the new theory analysis compatible with the recent progress in the flicker PN theory of non-quadrature (i.e., single-core) oscillators [55].

In this article, we propose a mm-wave class-F quadrature DCO using phase shifts between the drain–gate–source nodes to simultaneously achieve the I/Q exactness and suppress the flicker PN. Compared with [12], [59], this article focuses on the theoretical analysis of phase shifts to resolve the mode ambiguity while reducing the flicker PN, and with further detailed discussions on the CM return path. The rest of the article is organized as follows: Section II clarifies the mode ambiguity in the conventional QOSCs and introduces a gate-source phase shift technique for the proposed class-F QDCO with a simplified phasor-based explanation. Section III discusses the flicker noise upconversion mechanism resulting from the quadrature coupling in the proposed QDCO, which is suppressed by an induced drain-to-gate phase shift. Section IV discloses the design details. The experimental setup and results are shown in Section V.

II. Resolving Mode Ambiguity in Quadrature Oscillators Using Gate-to-Source Phase Shift

A. Mode Ambiguity in Conventional QOSCs

Fig. 2(a) depicts a classic LC-tank QOSC [21]. It consists of two nominally identical oscillators coupled to each other in an "anti-phase coupling" manner [60], [61], ensuring that their phase separation will be 90°. Such "anti-phase coupling" may require four parallel injecting transistors (i.e., M_5–M_8) inter-connecting the two oscillator cores. However, it is well-known that any "anti-phase coupling" manner in QOSCs [22], [30], [44] could result in a two-mode ambiguity, e.g., V_{QN} can either *lead* or *lag* V_{IP} by 90° (see the blue and red waveforms in Fig. 2(a), respectively).

To clearly analyze the two-mode ambiguity in the conventional LC-QOSC in Fig. 2(a), we assume $V_{IP} = V_0 \cdot \sin \omega_0 t$ as a

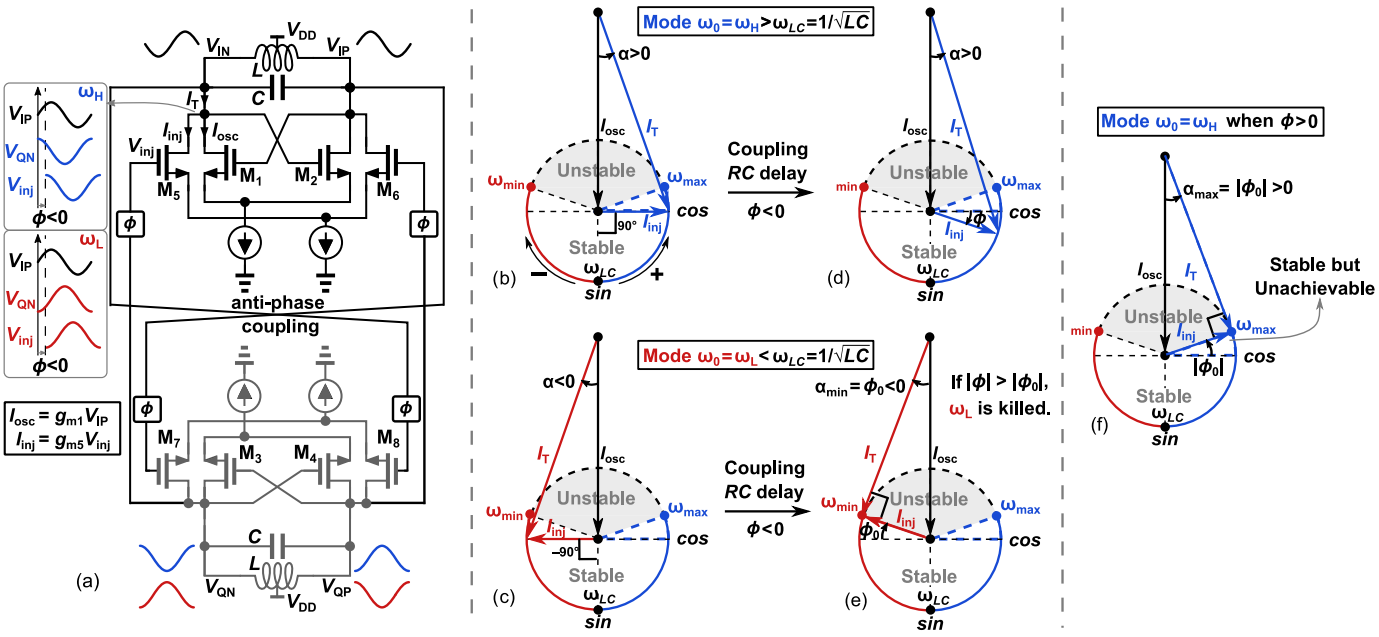

Fig. 2. (a) Schematic of a conventional LC-tank QOSC. Current phasor diagrams with ideal coupling (i.e., $\phi = 0$) in (b) $\omega_{\rm H}$ mode where $\boldsymbol{V}_{\rm QN}$ leads $\boldsymbol{V}_{\rm IP}$ by 90°, and (c) $\omega_{\rm L}$ mode where $\boldsymbol{V}_{\rm QN}$ lags $\boldsymbol{V}_{\rm IP}$ by 90°. Current phasor diagrams with $\phi < 0$ (e.g., circuit parasitic delays) in (d) $\omega_{\rm H}$ mode, (e) $\omega_{\rm L}$ mode (specifically, $\omega_{\rm L} = \omega_{\rm min}$ with $\alpha = \alpha_{\rm min}$), and (f) with $\phi > 0$ (not practical in the conventional QOSCs) in (d) $\omega_{\rm H}$ mode (specifically, $\omega_{\rm H} = \omega_{\rm max}$ with $\alpha = \alpha_{\rm max}$). Note $\angle \boldsymbol{I}_{\rm osc} = \angle \boldsymbol{V}_{\rm IP}$ and $\angle \boldsymbol{I}_{\rm inj} = \angle \boldsymbol{V}_{\rm inj} = \angle \boldsymbol{V}_{\rm QN} + \phi$ (taking $|\boldsymbol{I}_{\rm osc}| \sin \omega_0 t$ as the reference phasor).

voltage reference and no frequency mismatch between the two LC-tanks, and thus $V_{\rm QN} = V_0 \cdot \cos \omega_0 t$ (blue: $V_{\rm QN}$ *leads* $V_{\rm IP}$ by 90°) or $V_{\rm QN} = V_0 \cdot \cos(\omega_0 t + \pi)$ (red: $V_{\rm QN}$ *lags* $V_{\rm IP}$ by 90°). Then, considering initially no excess phase shift associated with the coupling (i.e., $\phi = 0$), we portray the current phasor diagrams with $\boldsymbol{I}_{\rm T} = \boldsymbol{I}_{\rm osc} + \boldsymbol{I}_{\rm inj}$[1] in these two modes in Fig. 2(b) and (c) (similarly as in the art of injection locking [62], [63]), where $\boldsymbol{I}_{\rm T}$, $\boldsymbol{I}_{\rm osc}$ (chosen as a phasor reference), and $\boldsymbol{I}_{\rm inj}$ are the phasors of tank current, intrinsic current, and injecting current, respectively. Since $\boldsymbol{I}_{\rm osc}$ and $\boldsymbol{I}_{\rm inj}$ are generated by $\boldsymbol{V}_{\rm IP}$ and $\boldsymbol{V}_{\rm inj}$ through $\rm M_1$ and $\rm M_5$ (i.e., $\boldsymbol{I}_{\rm osc} = g_{\rm m1} \cdot \boldsymbol{V}_{\rm IP}$ and $\boldsymbol{I}_{\rm inj} = g_{\rm m5} \cdot \boldsymbol{V}_{\rm inj}$ without considerations of other higher harmonics), we obtain $\angle \boldsymbol{I}_{\rm osc} = \angle \boldsymbol{V}_{\rm IP}$ and $\angle \boldsymbol{I}_{\rm inj} = \angle \boldsymbol{V}_{\rm inj} = \angle \boldsymbol{V}_{\rm QN} + \phi$. It can be further derived that $\boldsymbol{I}_{\rm osc}$ must enter the pure resistive path of the LC-tank, since it is in-phase with $\boldsymbol{V}_{\rm IP}$.

In Fig. 2(b), $\boldsymbol{I}_{\rm inj}$ leads $\boldsymbol{I}_{\rm osc}$ by 90°, suggesting $\boldsymbol{I}_{\rm inj}$ must enter the purely capacitive path of the LC-tank to generate the same tank voltage $\boldsymbol{V}_{\rm T}$ ($=\boldsymbol{V}_{\rm IP} - \boldsymbol{V}_{\rm IN}$) as $\boldsymbol{I}_{\rm osc}$ entering the resistive path. Accordingly, the phase shift between the tank current and voltage, α ($=\angle \boldsymbol{I}_{\rm T} - \angle \boldsymbol{V}_{\rm T} = \angle \boldsymbol{I}_{\rm T} - \angle \boldsymbol{I}_{\rm osc}$), is greater than 0, and so $\boldsymbol{I}_{\rm T}$ partly enters the capacitive path, implying the oscillation frequency $\omega_0 = \omega_{\rm H} > 1/\sqrt{LC}$. We define this mode as "$\omega_{\rm H}$ mode," while the other mode in Fig. 2(c) is a $\omega_{\rm L}$ ($< 1/\sqrt{LC}$) mode with $\alpha < 0$ and $\boldsymbol{I}_{\rm T}$ partly entering the inductive path.

In a practical design, $\phi < 0$ due to the RC delay of coupling wires and parasitics, which results in $\boldsymbol{I}_{\rm inj}$ rotating *clockwise* with ϕ in Fig. 2(d) and (e). This causes the total tank current $|\boldsymbol{I}_{\rm T}|$ to increase in the $\omega_{\rm H}$ mode and to decrease in the $\omega_{\rm L}$ mode.[2] In the $\omega_{\rm L}$ mode, the decreasing negative ϕ could make $\boldsymbol{I}_{\rm inj}$ perpendicular to $\boldsymbol{I}_{\rm T}$, reaching the most negative α (i.e., $\alpha_{\rm min} = \phi_0 < 0$) [see Fig. 2(e)]. Since α depends on the frequency deviation between ω_0 and $1/\sqrt{LC}$, $\alpha_{\rm min}$ represents the lowest stable $\omega_{\rm L}$ (i.e., $\omega_{\rm min}$). Any further decrease in ϕ will kill the $\omega_{\rm L}$ mode, quenching the oscillation, while the $\omega_{\rm H}$ mode with a negative ϕ in Fig. 2(d) operates even stronger with larger $\boldsymbol{I}_{\rm T}$. In other words, once

$$|\phi| > |\phi_0| = |\alpha_{\rm min}| = \sin^{-1} \frac{|\boldsymbol{I}_{\rm inj}|}{|\boldsymbol{I}_{\rm osc}|} \tag{2}$$

the QOSC will only work in the $\omega_{\rm H}$ mode. This conclusion was first derived in [39] based on complex differential equations, but we demonstrate it here in a simplified phasor circle diagram.[3]

On the other hand, we could push the QOSC to operate at the highest stable frequency $\omega_{\rm H}$, as illustrated in Fig. 2(f), where $\phi > 0$ and $\boldsymbol{I}_{\rm inj}$ is perpendicular to $\boldsymbol{I}_{\rm T}$ with the most positive α (i.e., $\alpha_{\rm max}$). In theory, the QOSC could also operate in the region between the two blue dashed lines in the $\omega_{\rm H}$ mode, but it is unachievable in the conventional QOSCs due to the $\phi < 0$ condition.

B. Resolving Mode Ambiguity in the Proposed QDCO

In a conventional mm-wave class-F oscillator [65], its drain tank (comprising $L_{\rm D}$, $C_{\rm D}$) and gate tank (comprising $L_{\rm G}$, $C_{\rm G}$)

[1] $\boldsymbol{I}$ (or $\boldsymbol{V}$) is a phasor representation of the *fundamental* component of $I(t)$ [or $V(t)$].

[2] More precisely, we could consider the change in effective $\boldsymbol{I}_{\rm osc}$ (i.e., $\boldsymbol{I}_{\rm osc}$ plus the projection of $\boldsymbol{I}_{\rm inj}$ onto the direction of $\boldsymbol{I}_{\rm osc}$), which is exactly out-of phase of $\boldsymbol{V}_{\rm IN}$, generating negative resistance for maintaining the oscillation.

[3] From the viewpoint of phasors, formula (2) could be used in both active-coupling [39] or passive-coupling [44] QVCOs to *estimate* whether $\omega_{\rm L}$ is squelched. However, this must be further verified by simulations since the effects of other higher order harmonic currents on phase shift [64] are neglected in (2).

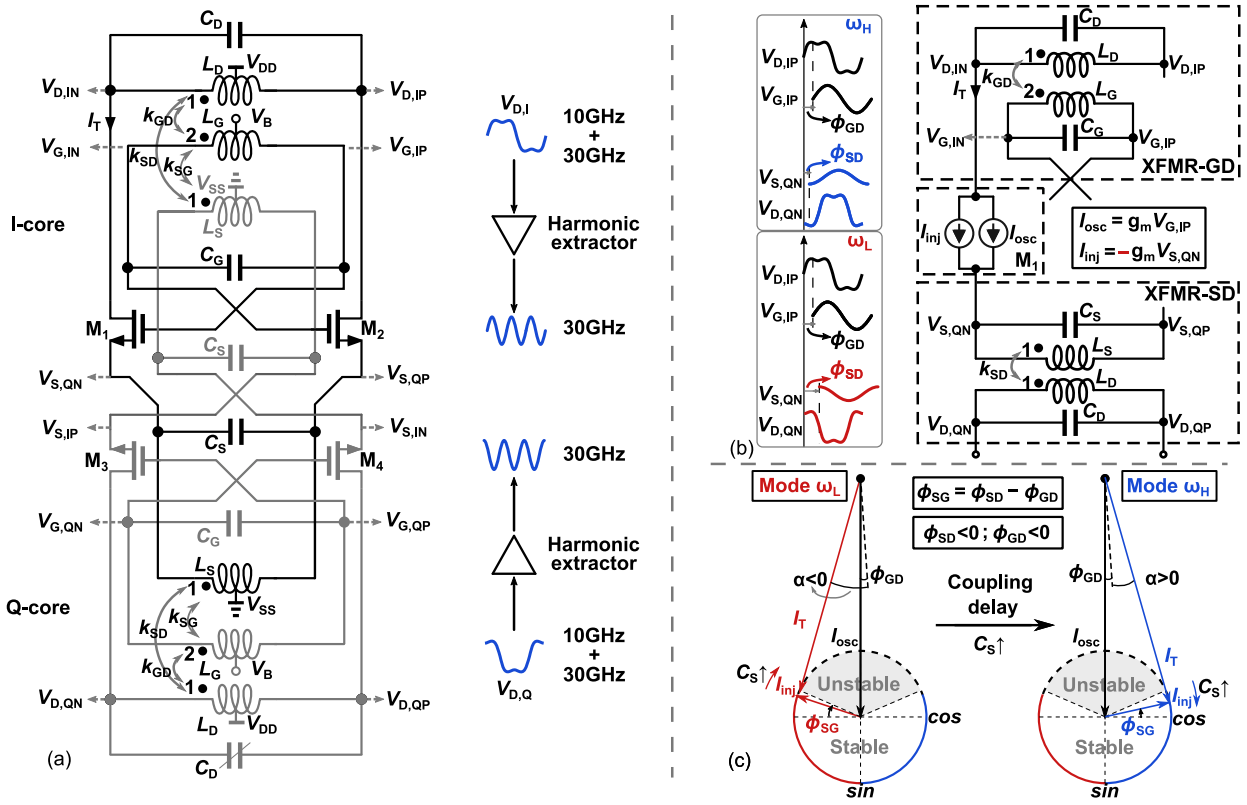

Fig. 3. Proposed quadrature class-F oscillator exploiting transformer-to-source-terminal coupling between the cores: (a) schematic and (b) its simplified model focusing on the generation of $I_{\rm osc}$ and $I_{\rm inj}$ of M_1 in $\omega_{\rm L}$ or $\omega_{\rm H}$ modes, where $\angle \boldsymbol{I}_{\rm osc} = \angle \boldsymbol{V}_{\rm G,IP}$ and $\angle \boldsymbol{I}_{\rm inj} = \angle \boldsymbol{V}_{\rm S,QN} + 180°$. (c) Current phasor cycle of M_1 showing the transformation from $\omega_{\rm L}$ mode ($\boldsymbol{V}_{\rm D,QN}$ leads $\boldsymbol{V}_{\rm D,IP}$ by 90°) to $\omega_{\rm H}$ mode ($\boldsymbol{V}_{\rm D,QN}$ lags $\boldsymbol{V}_{\rm D,IP}$ by 90°) by increasing $C_{\rm S}$ (taking $|I_{\rm osc}| \sin \omega_0 t$ as a phasor reference).

are mutually coupled (by $k_{\rm GD}$ coefficient) to boost the third-harmonic voltage (e.g., at $3\omega_0 = 3 \times 2\pi \times 10$ GHz) for an efficient mm-wave frequency generation [12], [15], [54]. This benefits from the core oscillator operating at a lower frequency (e.g., $\omega_0 = 2\pi \times 10$ GHz) to exploit the good quality (Q)-factor of switched capacitors (sw-caps).[4] In the proposed QDCO shown in Fig. 3(a), an additional source tank ($L_{\rm S}$, $C_{\rm S}$) is added [68] (thus making it a three-coil transformer [68], [69], [70]) to each of the two class-F DCOs [59] to form "anti-phase coupling" from one transistor's drain node to another transistor's (i.e., its antipodal) source node (by $k_{\rm SD}$), thereby generating quadrature phases (like source-coupling in [44]). Specifically, the transconductor ($-G_{\rm m}$) switching devices are reused as injecting devices, eliminating the significant contribution of flicker PN from the conventional injecting transistors (i.e., M_5–M_8 in Fig. 2).

The $L_{\rm D}$ coil (e.g., in the I-core) is regarded as the primary coil, generating a magnetic field that is then independently sensed by two secondary coils: $L_{\rm G}$ (in the same I-core) and $L_{\rm S}$ (in the opposite Q-core). Thus, there is no need to consider coupling from $L_{\rm G}$ to $L_{\rm S}$ by $k_{\rm SG}$ in the phase shift analysis. It is further supported by the fact that the $V_{\rm G,\{IP/IN/QP/QN\}}$ waveforms show almost perfect quadrature relationship between each other,[5] which are not affected by the $L_{\rm S}$ coupling through $k_{\rm SG}$. Thus, we could only consider two transformer-based tank models associated with M_1 (neglecting $k_{\rm SG}$) for easier understanding of the two possible modes ($\omega_{\rm L}$, $\omega_{\rm H}$) in the proposed oscillator, as shown in Fig. 3(b). As indicated within "XFRM-GD," the intrinsic current in M_1 is assumed as $\boldsymbol{I}_{\rm osc} = g_{\rm m}\boldsymbol{V}_{\rm G,IP}$. Note that there exists a small phase shift $\phi_{\rm GD} = \angle \boldsymbol{V}_{\rm G,IP} - \angle \boldsymbol{V}_{\rm D,IP}$ between the coupled gate and drain tanks. In "XFRM-SD," on the other hand, the quadrature voltage (e.g., $V_{\rm D,QN}$) is coupled by $k_{\rm SD}$ to the source node of M_1 (i.e., $V_{\rm S,QN}$) with a small phase shift of $\phi_{\rm SD} = \angle \boldsymbol{V}_{\rm S,QN} - \angle \boldsymbol{V}_{\rm D,QN}$, generating the injecting current $\boldsymbol{I}_{\rm inj} = -g_{\rm m}\boldsymbol{V}_{\rm S,QN}$. Accordingly, the total tank current is $\boldsymbol{I}_{\rm T} = \boldsymbol{I}_{\rm osc} + \boldsymbol{I}_{\rm inj}$.

To be able to remove the ±90° mode ambiguity in Fig. 3(b), we analyze the relationship between $\boldsymbol{I}_{\rm osc}$, $\boldsymbol{I}_{\rm inj}$, and $\phi_{\rm SG}$ around M_1, with the latter serving the same purpose as ϕ in Fig. 2. We can control $\phi_{\rm SG}$ through its individual components: passive phase shifts of drain-to-gate ($\phi_{\rm GD}$) and drain-to-source ($\phi_{\rm SD}$) windings of XFMR-GD and XFMR-SD transformers, respectively, as follows:

$$\phi_{\rm SG} = \phi_{\rm SD} - \phi_{\rm GD}. \tag{3}$$

[4]Another benefit is the much reduced injection pulling from the following PA that now operates at $3\omega_0$ [66]. The reduction in pulling due to the super-harmonic $3\omega_0 \rightarrow \omega_0$ coupling appears an interesting research problem [67].

[5]In simulation, we observe that only $V_{\rm S,\{IP/IN/QP/QN\}}$ waveforms include the coupling components from the other core, thus supporting our analysis. For more details on a three-winding resonator, we refer to [68].

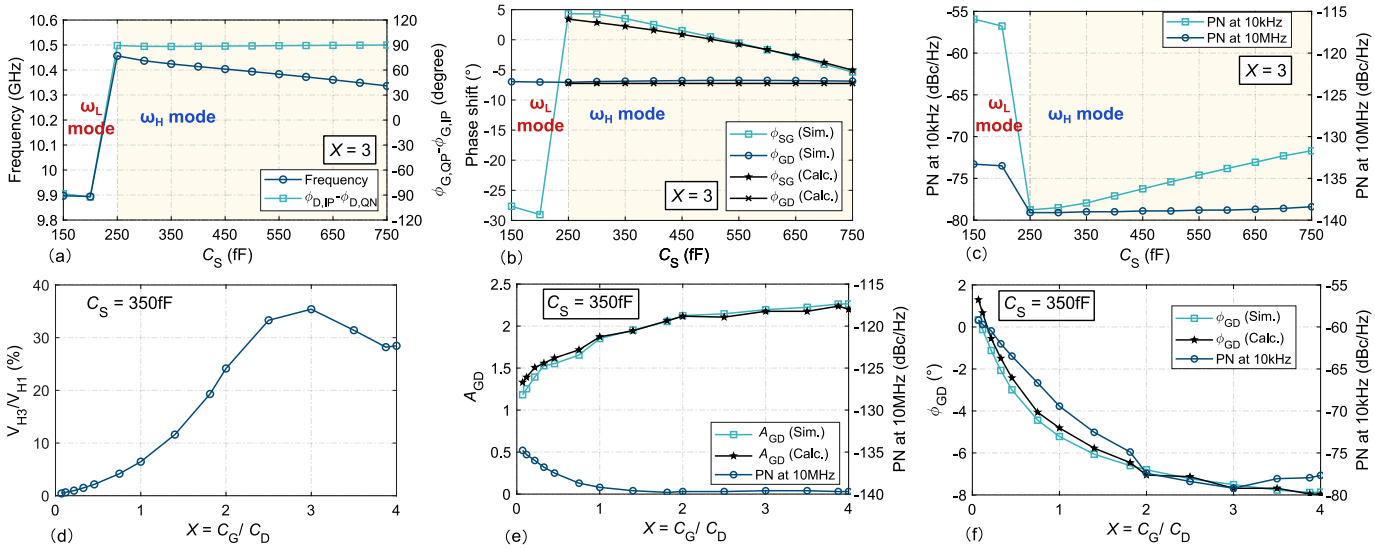

Fig. 4. Mode transformation from ω_L to ω_H by increasing C_S: (a) simulated oscillation frequency and $\phi_{D,IP}-\phi_{D,QN}$, (b) calculated and simulated ϕ_{GD}, ϕ_{SG}, and (c) PN at 10 kHz/10 MHz. Results of sweeping $X(=C_G/C_D)$: (d) simulated V_{H3}/V_{H1} ratio at the drain node, thus indicating the relative third-harmonic strength, (e) calculated and simulated A_{GD} with PN at 10 MHz, and (f) ϕ_{GD} with PN at 10 kHz.

As we demonstrate in [64], ϕ_{GD} can be controlled by the gate–drain capacitance ratio X as follows:

$$X = \frac{C_G}{C_D} \tag{4}$$

and the corresponding normalized oscillation frequency Ω_1 (with respect to the resonant frequency ω_G of the gate tank) as follows:

$$\begin{aligned}\Omega_1(X) &= \frac{\omega_0}{\omega_G} = \omega_0 \cdot \sqrt{L_G C_G} \\ &= \sqrt{\frac{1+n^2X-\sqrt{(1+n^2X)^2-4n^2X\left(1-k_{GD}^2\right)}}{2\left(1-k_{GD}^2\right)}} \\ &= \begin{cases} 0, & \text{if } X \to 0 \\ 1, & \text{if } X \to \infty \end{cases}\end{aligned} \tag{5}$$

where k_{GD} is the coupling factor between L_G and L_D coils, $n=\sqrt{L_G/L_D}$ is the effective turns ratio of the transformer in XFMR-GD, and ω_0 is the oscillation frequency that depends on C_G and C_D for a given transformer. Accordingly, $\phi_{GD}(X)$ could be derived as follows:

$$\begin{aligned}\phi_{GD}(X) &= \tan^{-1}\frac{\frac{1}{Q_D}-\frac{Q_D+Q_G}{Q_DQ_G}\Omega_1^2}{\left(\frac{1}{Q_DQ_G}+k_{GD}^2-1\right)\Omega_1^2+1} \\ &\approx \begin{cases} \tan^{-1}\dfrac{1}{Q_D} > 0, & \text{if } X \to 0 \\ 0, & \text{if } X \approx \dfrac{1}{n^2}\dfrac{1+k_{GD}^2}{2} \\ -\tan^{-1}\dfrac{1}{k_{GD}^2Q_G} < 0, & \text{if } X \to \infty \end{cases}\end{aligned} \tag{6}$$

indicating that it is a monotonically decreasing function of X. Intuitively, a large capacitance presented on the gate side of XFRM-GD would tend to delay the coupled waveform across the windings.

On the other hand, to introduce the required ϕ_{SD}, the source capacitance C_S is added. It barely affects the oscillation frequency ω_0 (unlike with C_G and C_D). Similarly, we define

$$\Omega_2(C_S) = \frac{\omega_0}{\omega_S} = \omega_0 \cdot \sqrt{L_S C_S} \approx \begin{cases} 0, & \text{if } C_S \to 0 \\ 1, & \text{if } C_S \to \dfrac{1}{\omega_0^2 L_S} \end{cases} \tag{7}$$

which mainly depends on the absolute capacitance rather than a capacitance ratio. In an analogy to (6), ϕ_{SD} is

$$\begin{aligned}\phi_{SD}(C_S) &= \tan^{-1}\frac{\frac{1}{Q_D}-\frac{Q_D+Q_S}{Q_DQ_S}\Omega_2^2}{\left(\frac{1}{Q_DQ_S}+k_{SD}^2-1\right)\Omega_2^2+1} \\ &\approx \begin{cases} \tan^{-1}\dfrac{1}{Q_D} > 0, & \text{if } C_S \to 0 \\ 0, & \text{if } C_S = \dfrac{Q_S}{Q_S+Q_D}\dfrac{1}{\omega_0^2 L_S} \\ -\tan^{-1}\dfrac{1}{k_{SD}^2Q_S} < 0, & \text{if } C_S \to \dfrac{1}{\omega_0^2 L_S} \end{cases}\end{aligned} \tag{8}$$

which is also a monotonically decreasing function of C_S (intuitively, the heavier the loading by C_S, the greater the tendency to the phase delay). Thus, considering (3), (6), and (8) for a given X (i.e., fixed ϕ_{GD}), ϕ_{SG} is also a monotonically decreasing function of C_S. In other words, $\boldsymbol{I}_{inj}$ will rotate *clockwise* with an increase in C_S to quench the ω_L mode, as shown in Fig. 3(c).

To verify this proposed technique, we sweep C_S from 150 to 750 fF in our class-F DCO with $X=3$ (e.g., $C_G=337.5$ fF, $C_D=112.5$ fF, ensuring strong V_{H3}/V_{H1} of ~40%). It can be observed in Fig. 4(a) that the QDCO first operates at ω_L ($\approx 2\pi \times 9.9$ GHz, $\boldsymbol{V}_{D,QN}$ leads $\boldsymbol{V}_{D,IP}$ by 90°) but then it switches the mode to ω_H ($\approx 2\pi \times 10.4$ GHz, $\boldsymbol{V}_{D,QN}$ lags $\boldsymbol{V}_{D,IP}$ by 90°). This validates our analysis in Fig. 3(c), which is further supported by the numerical verification of ϕ_{GD} and ϕ_{SG} in Fig. 4(b).

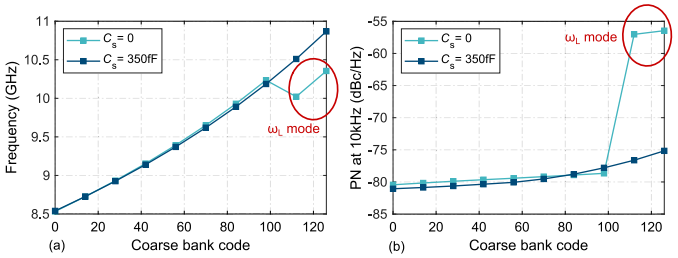

Fig. 5. (a) Oscillating frequency and (b) PN at 10 kHz under full sweep of the coarse bank with no C_S and with its optimal value from Fig. 4(a).

Interestingly, the PN of the proposed class-F QDCO, especially its flicker PN (i.e., PN at 10 kHz), improves drastically upon the switchover from ω_L to ω_H,[6] as illustrated in Fig. 4(c). At the same time, it warns against the excessively large C_S as it can ruin the close-in PN at 10 kHz. Therefore, we select $C_S = 350$ fF [with ϕ_{SG} around 2.5° at ~10 GHz; see Fig. 3(c)][7] for our design. Fig. 5 shows plots of the simulated frequency and PN at 10 kHz over the entire tuning range (TR) for two values of C_S. Fixing C_S at 350 fF completely solves the mode ambiguity problem.

III. Flicker PN in Class-F Quadrature Oscillators

In this section, we study the flicker noise upconversion mechanisms in both the modes (i.e., ω_L and ω_H) of the class-F QOSCs and propose a negative drain-to-gate phase shift technique to suppress the flicker PN.

A. Flicker Noise Upconversion in ω_L and ω_H Modes

First, let us start with analyzing the PN of the proposed class-F QDCO in the ω_H mode with $C_S = 350$ fF. By sweeping X,[8] we obtain V_{H3}/V_{H1} ratio (observed at the drain nodes), passive gain A_{GD} ($=|\boldsymbol{V}_{G,IP}|/|\boldsymbol{V}_{D,IP}|$), PN at 10 MHz (representing the thermal PN), ϕ_{GD} ($=\angle\boldsymbol{V}_{G,IP} - \angle\boldsymbol{V}_{D,IP}$), and PN at 10 kHz (representing the flicker PN), as illustrated in Fig. 4(d)–(f). Interestingly, the class-F operation by itself does not necessarily ensure a significant improvement in PN (although independently useful for the third-harmonic extraction in mm-wave frequency generation [15], [54]), since its thermal PN (i.e., PN at 10 MHz) stays almost constant from $X = 1$ (with $V_{H3}/V_{H1} \approx 6\%$) to $X = 4$ (with $V_{H3}/V_{H1} = 30\%$). This is because the thermal PN caused by the $4kT\gamma g_m$ noise is roughly reduced A_{GD} times [64], [71] (rather than by the class-F itself), while

$$A_{GD}(X) \approx \frac{n \cdot k_{GD}}{1-(1-k_{GD}^2)\Omega_1^2} = \begin{cases} n \cdot k_{GD}, & \text{if } X \to 0 \\ n, & \text{if } X = 1/n^2 \\ n/k_{GD}, & \text{if } X \to \infty \end{cases} \tag{9}$$

gets saturated when X is large enough [see Fig. 4(e)].

[6]The power consumption is almost constant at around 7.8 mW during the sweep of C_S, which allows a fair PN comparison between the two modes.

[7]In fact, it operates at the "stable but unachievable region" of the conventional QOSC's phasor circle diagram in Fig. 2(d).

[8]For a fair PN comparison, we ensure the constant ω_0 by tuning different sets of C_G and C_D, and the same power consumption by adjusting V_{DD} if necessary. It can also be done by sweeping C_G with a fixed C_D, where the PN should be normalized to a fixed frequency.

Furthermore, we observe a correlation between the reduction in flicker PN (i.e., PN at 10 kHz) and negative ϕ_{GD}. This differs from the situation in [72] and [64] where X is set to <0.4 so as to introduce *positive* ϕ_{GD} for the flicker PN suppression. To further quantitatively study the flicker PN in QOSCs, we use a periodic transfer function (PXF)-based flicker PN theory framework introduced in [54], [55], [73], and [74]. The flicker PN (caused by a single MOS transistor, e.g., M_1 in Fig. 3) is calculated as follows:

$$\mathcal{L}_{1/f^3}(\Delta\omega) = \left(\frac{1}{2}\frac{\sqrt{2}}{\Delta\omega T_0}\int_0^{T_0} h_{DS}(t)\cdot I_{1/f,\,rms}(t)\mathrm{d}t\right)^2 \tag{10}$$

where $I_{1/f,\,rms}(t)$[9] (unit: $A/\sqrt{Hz}$) is the periodically modulated rms value of the flicker noise current at a low offset frequency $\Delta\omega$ (e.g., $2\pi \times 10$ kHz), T_0 ($=2\pi/\omega_0$) is the oscillation period, and $h_{DS}(t)$ (unit: rad/C) is the non-normalized ISF [75] associated with V_{DS}, describing the phase response of V_{DS} against current impulse perturbations.[10] The intuitive understanding and simulation methods of $I_{1/f,rms}(t)$ and $h_{DS}(t)$ [based on the periodic transfer function (PXF)] were provided in [55] and [73] for numerical verification according to (10). Obviously, decreasing the *net* integral area under $h_{DS} \cdot I_{1/f,rms}$ is the *key* factor in suppressing the flicker PN [55], rather than the long-standing myth [75] of only relying on the oscillation waveform symmetry.

B. Flicker PN Reduction by Negative Phase Shift

Three representative cases are simulated and numerically verified in Fig. 6. In the ω_L mode in Fig. 6(a), $I_{1/f,rms}$ shows less exposure to the falling edge of V_{DS} than to its rising edge, leading to the positive net area of $h_{DS} \cdot I_{1/f,rms}$ [see Fig. 6(b)] and, ultimately, to the flicker upconversion. In contrast, in the ω_H mode, $I_{1/f,rms}$ is exposed less at the V_{DS}'s rising edge [see Fig. 6(c) and (e)]. However, the negative phase shift of V_{GS} against V_{DS} in Fig. 6(c) increases the $I_{1/f,rms}$ exposure to V_{DS}'s rising edge at around 70 ps [compared with that in Fig. 6(e)], ultimately *equalizing* the positive and negative areas of $h_{DS} \cdot I_{1/f,rms}$ in Fig. 6(d), thereby quenching the flicker noise upconversion. There is no such benefit in Fig. 6(e), which maintains the negative net area of $h_{DS} \cdot I_{1/f,rms}$ in Fig. 6(f), thus still suffering from the flicker noise upconversion.

To gain better insight into the above phenomenon, we should first study the terminations of second- and third-harmonic currents, which are the key factors causing the oscillator waveform asymmetries that lead to the non-zero net integral area of $h_{DS} \cdot I_{1/f,rms}$ in *non*-quadrature oscillators [55], [64]. As shown in Fig. 7(c), the CM current enters the inductive path in all the cases (in both the ω_L and ω_H modes), while the third-harmonic DM current entering the

[9]This can be roughly modeled by periodically modulated transconductance G_m and drain current I_D; hence, it mainly depends on V_{GS} around the saturation region of MOS transistor (e.g., large V_{GS} with large $I_{1/f,\,rms}$) [54].

[10]Sharper rising or falling edges in V_{DS} are more robust to noise (i.e., presenting the narrow (in time) and small (in magnitude) h_{DS} in these edges), while its less steep edges (also implying longer noise exposure time) are more vulnerable to noise (i.e., showing wide and large h_{DS}). On the other hand, V_{DS}'s peak and bottom are immune to the noise (i.e., $h_{DS} = 0$ in these time instances).

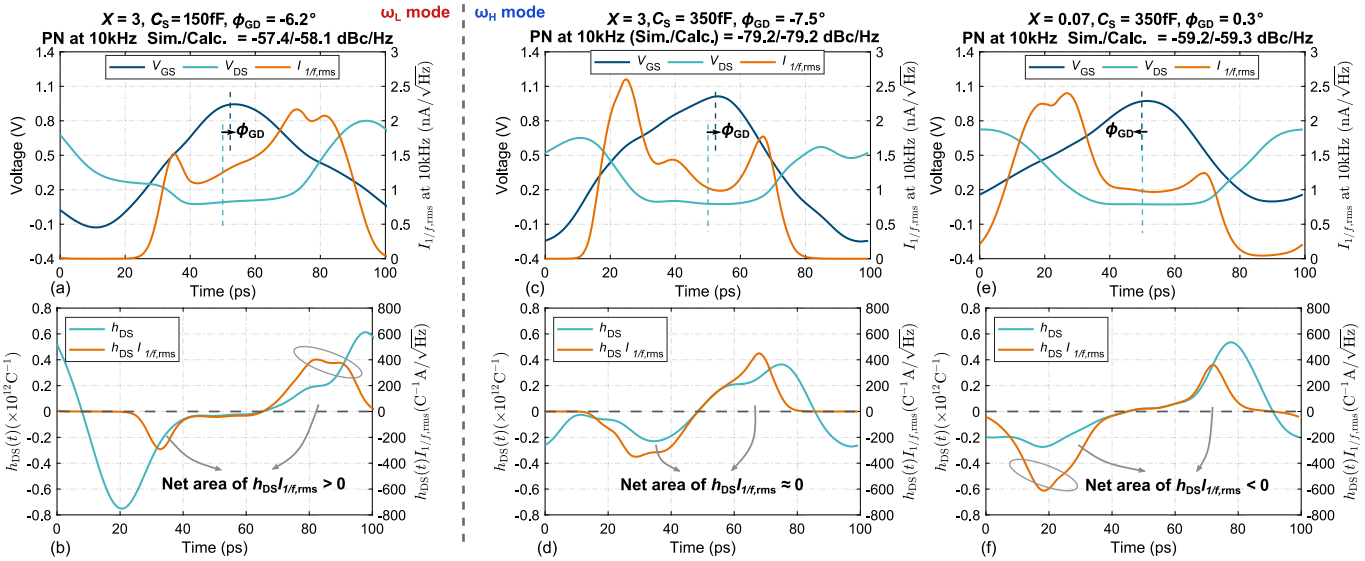

Fig. 6. Simulated waveforms of $V_{GS}(t)$ and $V_{DS}(t)$ in one period, the corresponding rms value of flicker current noise $I_{1/f,rms}(t)$ at 10 kHz, non-normalized ISF function $h_{DS}(t)$, and $h_{DS}(t) \times I_{1/f,rms}(t)$ in (a), (b) ω_L mode with $C_S = 150$ fF, $\phi_{GD} = -6.2°$ with $X = 3$; and in ω_H mode with $C_S = 350$ fF: (c), (d) $X = 3$ with $\phi_{GD} = -7.5°$, and (e), (f) $X = 0.07$ with $\phi_{GD} = 0.3°$.

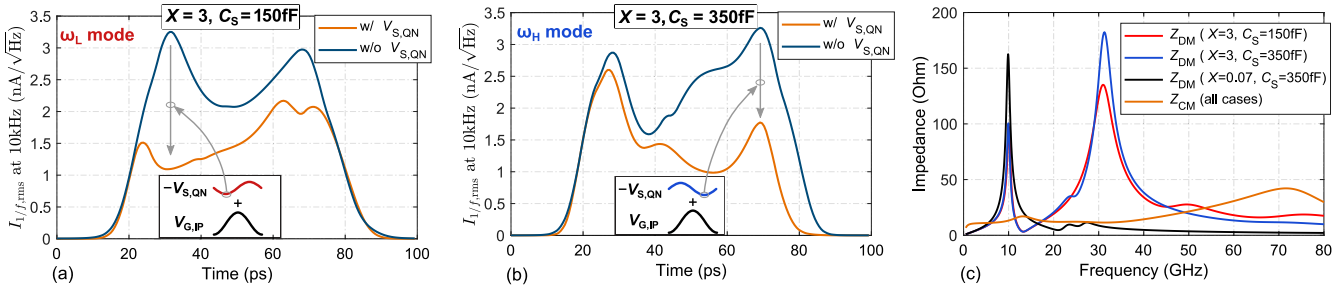

Fig. 7. Simulated $I_{1/f,rms}$ with and without the effect of the quadrature coupling voltage (i.e., $V_{S,QN}$) in (a) ω_L mode ($X = 3$, $C_S = 150$ fF) and (b) ω_H mode ($X = 3$, $C_S = 350$ fF). (c) DM and CM tank impedance in different cases.

resistive path with $X = 3$ or V_{H3} is fully suppressed by $X = 0.07$. Obviously, proper terminations of the second- and third-harmonic currents cannot explain the persistent presence of flicker noise upconversion in QOSCs.

C. Numerical Verification and Discussion

We identify that it is the quadrature coupling voltage that causes different exposure strengths of $I_{1/f,rms}$ to V_{DS}'s rising and falling edges, changing the picture of flicker PN upconversion. To verify our claim, we first simulate $I_{1/f,rms}$ (based on the simulation method in [55]) without taking into consideration the coupling source waveform $V_{S,QN}$ (i.e., setting $V_{S,QN} = 0$), which shows similar $I_{1/f,rms}$ in the two modes [see Fig. 7(a) and (b)]. Then, with $V_{S,QN}$ engaged, in the ω_L mode, the peak of $I_{1/f,rms}$ at $t \approx 30$ ps (i.e., exposure to the V_{DS}'s falling edge) gets significantly reduced, while in the ω_H mode, it decreases the peak of $I_{1/f,rms}$ at $t \approx 70$ ps (i.e., exposure to the V_{DS}'s rising edge). For easier understanding of this phenomenon, we draw the time-domain shapes of $V_{G,IP}$ and $-V_{S,QN}$ inside the boxes in Fig. 7(a) and (b) to illustrate how M_1's V_{GS} $(= V_{G,IP} + (-V_{S,QN}))$ combination affects $I_{1/f,rms}$. Obviously, in the ω_L mode, it is the bottom of the quadrature coupling waveform $-V_{S,QN}$ that reduces the rising edge of V_{GS} of M_1 and lowers the corresponding $I_{1/f,rms}$, when compared with the case without $V_{S,QN}$ coupling. On the other hand, in the ω_H mode, the bottom of $-V_{S,QN}$ lowers the falling edge of V_{GS}, resulting in the decreasing $I_{1/f,rms}$.[11]

Thanks to the controllable ϕ_{GD} in the transformer-based oscillator, we could fine-tune the $I_{1/f,rms}$ exposure in either the V_{DS}'s falling or rising edge by moving the peak of V_{GS} toward V_{DS}'s falling or rising edge to obtain the null net area of $h_{DS} \cdot I_{1/f,rms}$. All the simulated PN results are also verified with calculations based on (10), thus demonstrating the efficacy of the above analysis.

The simulated PN of the proposed class-F QDCO and the single-core class-F DCO [15] is plotted in Fig. 8, indicating that the flicker PN in the single-core case suffers from the ill-behaved second-harmonic voltage with an undefined CM

[11]This can also help explain the flicker noise upconversion in the conventional QOSCs in Fig. 2, where a lower I/Q imbalance can paradoxically lead to worse flicker PN. This is because even for symmetric V_{GS} and V_{DS} (such as with the second-harmonic resonance), $I_{1/f,rms}$ in the injecting devices [e.g., M_5 in Fig. 2(a)] mainly depends on the quadrature V_{inj}, which is always asymmetric for the V_{DS}'s rising and falling edges, thus contributing significantly to the flicker PN.

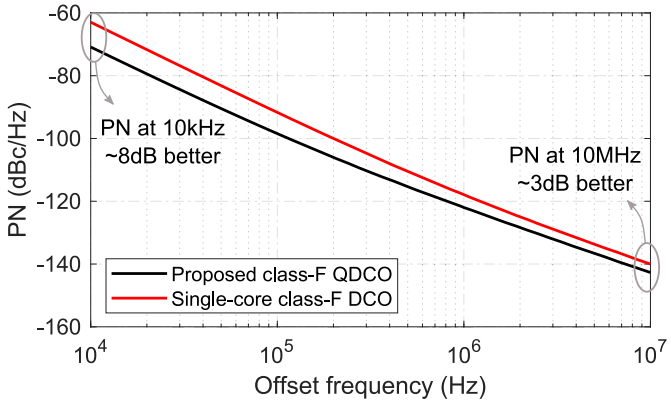

Fig. 8. Simulated PN plots of the proposed QDCO and single-core class-F DCO (without the second-harmonic resonance).

return path [54]. The proposed quadrature class-F oscillator achieves ∼3 dB better thermal PN (i.e., at 10-MHz offset) due to the two cores' coupling (the thermal noise of the equivalent parallel resistance gets reduced by half [37]) and a ∼8-dB PN improvement at 10-kHz offset, thanks to the proposed phase shifting technique.

IV. Circuit Implementation

The schematic of the implemented oscillator was shown earlier in Fig. 3(a). The QDCO core resonates at ∼10 GHz but the differential signal at the drain nodes in each of the I/Q cores is rich in the third-harmonic component and so it is fed to a harmonic extractor (HE), which is a differential amplifier operating at ∼30 GHz and is re-used from [54]. The HE is then followed by another amplifier stage to drive the 50-Ω external load of the test equipment.

A. Transformer Design Details

Fig. 9 illustrates the layout of the proposed QDCO together with the detailed transformer parameters. The coils carrying the DM currents are constructed with thick metals of AP, M9, and M8 to maintain their high-Q factors. M7–M2 are stacked for bridging the source nodes of $M_{1–4}$ to $V_{S,IP/IN/QP/QN}$. The dc current from the tap of the source coil to the outside of the transformer is carried by the stacked M7–M3, while only M2 provides V_B at the tap of L_G coil without any dc current. The two cores are connected using the "anti-phase coupling" routing, and the source coil of the I-core is placed inside the Q-core for coupling, and vice versa. L_S degrades Q_D and Q_G by 0.7 (5.5%) and 1.6 (10%), respectively, which has little influence on the oscillator's thermal PN.

As a convenient rule of thumb, the width of the coil could be set to ∼10× skin depth at the operating frequency (e.g., 10 μm at 10 GHz) as a starting point for the Q-factor optimization. The spacing between the coils is about 6 and 10 μm for, respectively, $k_{GD} = 0.63$ (boosting third-harmonic voltage for further extraction [15]) and $k_{SD} = 0.25$ (weak quadrature injection). The size of the transformer is optimized for the intended operating frequency to achieve high Q-factor but without excessive coupling to the substrate, whose self-resonant frequency (where k_{GD} vanishes) is around 5× the operating frequency. The dummy filling with the native layer ("NT_N" layer for high substrate resistivity [76] and extended in all the directions by 30 μm away from the coils) is reused from the inductor's process design kit (PDK) for easily passing the design rule check and minimizing the Q-factor loss.

B. QDCO's CM Return Path and Decoupling Scheme

A well-defined CM return path is necessary for achieving low flicker PN, especially in mm-wave oscillators [54]. Surprisingly, the CM return path in a QOSC is altogether different from that in the conventional single-core [55] or dual-core oscillators (see [77, Fig. 13]). As shown in Fig. 9, the second-harmonic currents (representing CM) generated by $M_{1,2}$ are anti-phase with those by $M_{3,4}$ (absorbing each other) since their fundamental voltage waveforms are in quadrature. This eventually results in the supply (V_{DD}) and ground (V_{SS}) nodes being in-phase for the CM currents on each side. For the purpose of completing the CM return paths and saving the I/O pads, we connect the two sets of $V_{DD}/V_{SS}/V_B$ routings of the I/Q cores by the on-chip decoupling capacitance. It should be noted that no CM currents enter these on-chip decoupling capacitors[12] (as well as the sw-cap banks), so they are merely used to stabilize the dc voltages. These shared I/Q supply lines were extracted by the EMX simulator together with the main transformers for accurate CM analysis. A "T-type" RC filter is used for V_B lines to enhance the CM stability at either high frequencies (considering the parasitic CM inductance of the transformer) or low frequencies (considering L_{bond}).

C. Switched-Capacitor Banks and I/Q Imbalance Sources

To cover the >15% TR target with sufficient resolution, the sw-cap banks are organized as shown in Fig. 10(a). The two 7-bit coarse-tuning sw-cap banks are put at both the gate and drain nodes and tuned together, ensuring $X \approx 3$ for the strong V_{H3}/V_{H1} [see Fig. 4(d)] across the TR (i.e., $C_{G,max}/C_{D,max} \approx C_{G,min}/C_{D,min} \approx \Delta C_G/\Delta C_D$, see [54]). The 8-bit IQ calibration bank and 9-bit fine-tuning bank are put only at the drain nodes for precise control of IQ mismatch and frequency, respectively, while their small capacitance ranges have little influence on X.

The coarse-tuning unit with a 13-MHz LSB uses a resistor-biased structure [78], as shown in Fig. 10(b), for enhancing the Q-factor and lowering parasitics. The resistors' bottom terminals (i.e., at the drain–source nodes of the switch) can experience a significant swing when the main switch is OFF. The disturbance can propagate to the joint upper terminal due to the layout imbalance; thus, the resistors' top terminals are connected to $\overline{CW}_{coarse}$, rather than to $\overline{CW}_{coarse}$. This arrangement could avoid any disturbance coupling back to the switch transistor's input, ultimately affecting the flicker PN due to the sw-cap banks. The 9-bit fine-tuning sw-cap bank uses a single-ended structure with biasing via transistor channel leakage for area-saving and routing ease, as depicted

[12]This includes the on-chip decoupling capacitors (∼100 pF) in series with their de-Q'ing resistors (∼10 Ω).

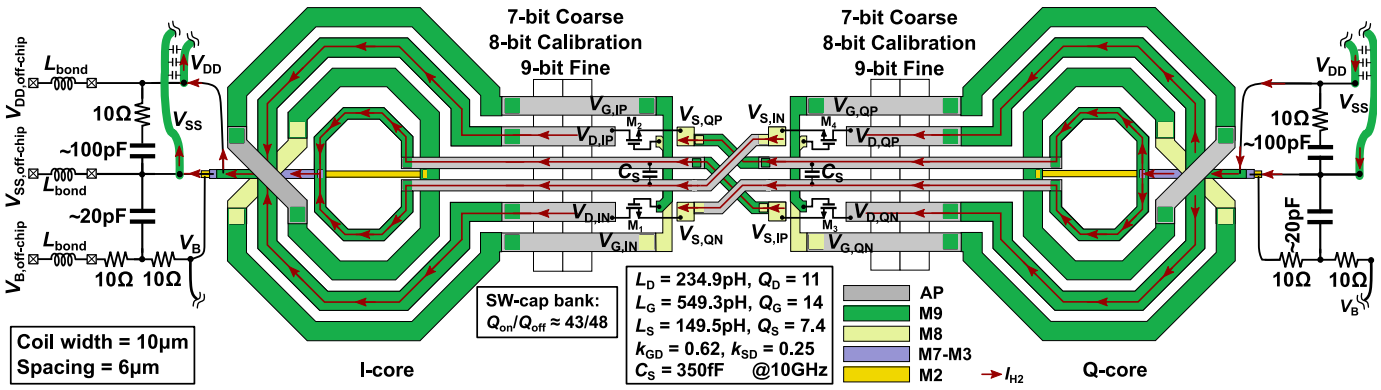

Fig. 9. Layout of the proposed class-F QDCO by source-coupling and its well-defined CM return path, where the CM currents generated by $M_{1,2}$ are anti-phase with those by $M_{3,4}$ since their fundamental voltage waveforms are in quadrature.

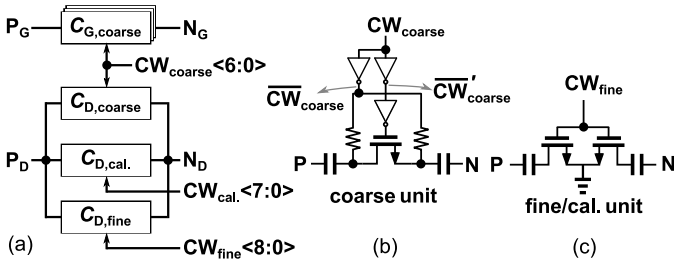

Fig. 10. (a) Configuration of sw-cap banks between the drain and gate nodes; sw-cap unit of (b) coarse bank and (c) fine bank.

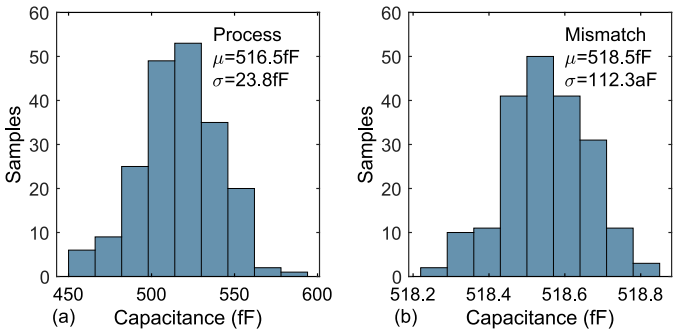

Fig. 11. Monte Carlo simulations with 200 sampling points of sw-cap banks for (a) global process variation and (b) local mismatch.

in Fig. 10(c). Thanks to the custom MoM capacitor, the unit provides $\Delta C = 50$ aF, corresponding to $\Delta f = 70$ kHz.

For the design of the I/Q calibration banks, we should consider the sources of I/Q mismatch, which mainly include: 1) local process mismatches between the two resonant tanks and 2) mismatches due to the asymmetric layout routing. The I/Q mismatch can be calibrated quite easily, without any PN degradation, by providing a small offset between the tuning codes of the two calibration banks. The Monte Carlo simulations were performed for the coarse bank (dominant capacitance), with results shown in Fig. 11: the standard deviation of capacitance $\sigma_{\text{global}} = 23.8$ fF when "global" (i.e., die-to-die) variations are applied, corresponding to a coefficient of variation (CV $= \sigma/\mu$) of 4.6%. Considering only 'local' mismatches (i.e., within a die), $\sigma_{\text{local}} = 112.3$ aF, which translates to a CV of 0.02%, thus being much less than the global mismatch. An alternative PPF-based quadrature generation [17], [18] would have to cover the global mismatches (and process corners) of both the resistance and capacitance, while the resistance can vary hugely from die to die, similar as in Fig. 11(a). However, for our QDCO, it only needs to consider the local mismatch of capacitance, while its global mismatch would not cause any I/Q mismatch. The inductance mismatch could be safely neglected, as the transformer dimensions are very large compared with the possible manufacturing error. On the other hand, based on the comparisons between different levels of EMX extraction, we identify that the routing mismatches (see Fig. 9) lead to around 0.6° of phase mismatch, while the weak magnetic coupling between the two transformers in the I- and Q-core [79] introduces a ∼1° quadrature error.

The two I/Q calibration sw-cap banks are located within the I- and Q-cores. They provide 8-bit resolution, supporting the ±12.8 fF de-tuning ($\gg 3\sigma_{\text{local}}$). The phase sensitivity of the QDCO is ∼1°/fF at the third-harmonic as per simulations. Thus, the I/Q calibration sw-cap bank can cover around ±12.8° phase mismatch. The entire sw-cap arrangement occupies a considerable area, as shown in Fig. 9. To ensure simulation accuracy, the proposed QDCO is simulated based on an EMX black-box flow, where all the transformers (I-core and Q-core) with all the routings are extracted as an S-parameter model, while the G_m and sw-cap banks are regarded as black-boxes and post-extracted by Calibre. High metal layers are only considered once in EMX, and the contact ports between the two models are carefully considered. Several iterations of tuning the sw-cap ratio may be needed to further enhance the third-harmonic voltage in the final post-layout simulation.

V. Experimental Results

The prototype of the proposed QDCO is implemented in a TSMC 28-nm LP CMOS process, occupying an area of 0.26 mm^2, as shown in Fig. 15.

A. PN Measurements

The PN measurements are performed based on an equipment combo of Keysight E5052B signal source analyzer,

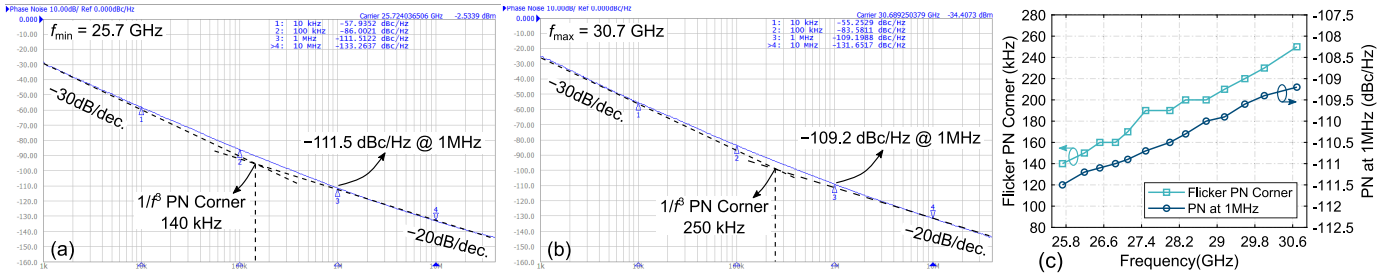

Fig. 12. Measured PN plots at (a) 25.7 GHz, (b) 30.7 GHz, and (c) PN at 1-MHz offset and flicker PN corner over TR.

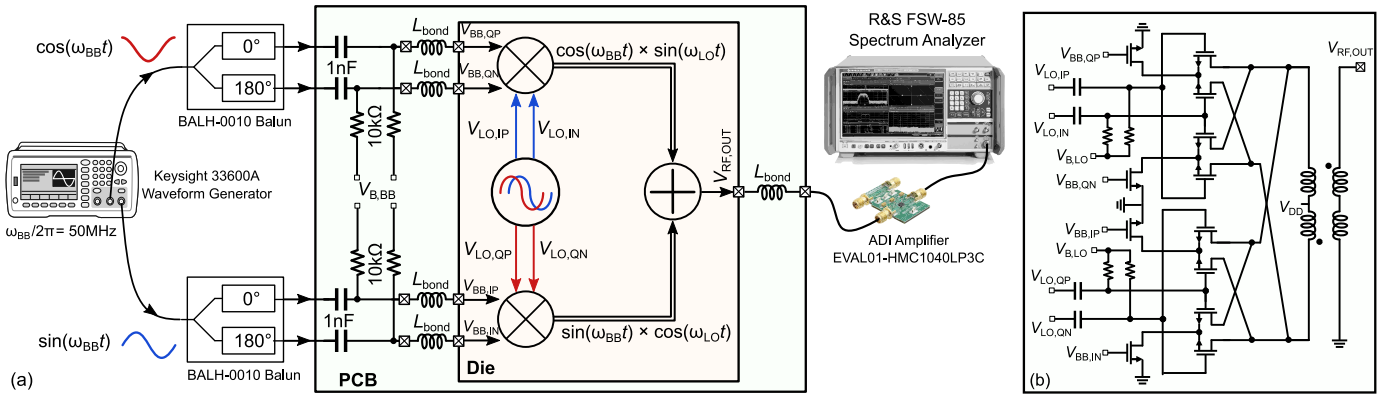

Fig. 13. (a) Measurement setup for the IRR of QDCO and (b) on-chip quadrature mixer.

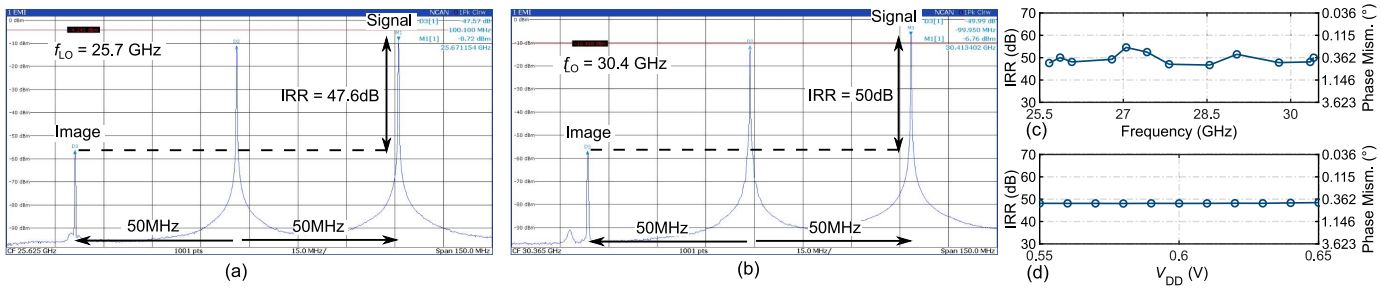

Fig. 14. Measured IRR with I/Q calibration at (a) 25.7 GHz, (b) 30.4 GHz, (c) IRR after calibration over TR and its corresponding phase mismatch (denoted as ϕ_m, assuming no gain mismatch), and (d) IRR after calibration at 30.36 GHz over QDCO VDD variations and its corresponding ϕ_m. Note: IRR(dB) $= 10\log_{10}((1-\cos\phi_m)/(1+\cos\phi_m))$.

E5053A microwave downconverter, 11970A harmonic mixer, and 11636C power divider. The output of the QDCO is down-converted by 11970A and then E5053A, and finally fed into E5052B. The three levels of capacitor banks at the drain and gate nodes cover the measured TR from 25.7 to 30.7 GHz (17.7%). When operating at 25.7 GHz [see Fig. 12(a)], the measured PN is −111.5 dBc/Hz at 1-MHz offset, with an excellent $1/f^3$ PN corner of 140 kHz. At the highest frequency of 30.7 GHz, as shown in Fig. 12(b), it achieves −109.2 dBc/Hz at 1-MHz offset, with a 250-kHz flicker PN corner. Fig. 12(c) illustrates the PN performance of the QDCO over the whole TR. The PN at 1 MHz steadily increases with frequency, whereas the flicker PN corner ranges from 140 to 250 kHz. With a power supply of merely 0.6 V, the power consumption over the TR is around 29 mW, including 10 mW consumed by two third-harmonic extractors (HE). This results in the best-in-class FoM of −185 dB and it varies only within 1 dB over the TR. The measured frequency pushing at 0.6 V is merely 24.7 MHz/V.

B. IRR Measurements

IRR measurements are based on an I/Q frequency upconversion scheme [39], [80], as shown in the setup in Fig. 13(a). A two-wire I/Q baseband signal at $\omega_{BB} = 2\pi \times 50$ MHz is generated by Keysight 33 600A, which is then converted into a four-wire differential version by two BALH-0010 baluns. The RC-bias network on the PCB sets the dc signal level before feeding it internally on-chip. In the on-chip I/Q mixer, the baseband signal $\cos\omega_{BB}$ is mixed with $\sin\omega_{LO}$ while $\sin\omega_{BB}$ is mixed with $\cos\omega_{LO}$[13]; afterward, these two components are summed. This arrangement cancels out the $\omega_{LO}-\omega_{BB}$ component while leaving only the $\omega_{LO}+\omega_{BB}$ component. Assuming

[13] ω_{LO} here denotes the signal after the HE, i.e., at 30 GHz.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

		Quadrature VCOs/DCOs							Quadrature Generation Circuits		
Reference		**This work**		Li, *TCAS-II*'21 [29]	Zhang, *JSSC*'19[50]	Bhat, *ISSCC*'19 [28]		Szortyka, *JSSC*'15 [49]	Huang, *JSSC*'20[36]	Mondal, *JSSC*'19[19]	Piri, *JSSC*'18[17]
IQ Coupling/Technique		**Drain-to-Source Transformer**		Transistor	Super-harmonic	Transistor		Super-harmonic	Transformer Network	Poly-Phase Filter	Poly-Phase Filter
Frequency (GHz)		**25.7**	**30.7**	27.57 – 33.07	41	25	38	53.8– 63.3	25 – 50	27 – 29.75, 35 – 38.75	25 – 44
Phase Noise (dBc/Hz)	100kHz	**-86**	**-83.6**	N/R	-62	-80	-70	-63 – -67	N/A	N/A	N/A
	1MHz	**-111.5**	**-109.2**	-91 – -98	-94.3	-110	-102.2	-91 – -94.5	N/A	N/A	N/A
	10MHz	**-133.3**	**-131.6**	N/R	-105	-131	-122	-117 – -119	N/A	N/A	N/A
FoM (dB)	100kHz	**-179.5**	**-178.7**	N/R	-165	-175.5	-168.3	-168– -170.7	N/A	N/A	N/A
	1MHz	**-185**	**-184.3**	-173 – -180	-177	-185.5	180.5	-175– -177.7	N/A	N/A	N/A
	10MHz	**-186.8**	**-186.7**	N/R	-168	-186.5	-180.3	-184.7	N/A	N/A	N/A
Flicker PN Corner (kHz)		**140**	**250**	>500	>1000	600		>1000	N/A	N/A	N/A
Tuning Range (%)		**18.1**		18.1	18.4	41.2		16	66.7	9.7/10.2	59.2
IRR (dB)		**> 47**		N/R	> 47[&]	N/R		-27[&]	> 32	> 35	> 40
Phase Error (degree)		**< 0.5[&]**		0.7– 1*	0.18± 0.3	N/R		± 5	± 1.8	N/R	< 0.7
Freq. Pushing (MHz/V)		**24.7**		N/R	N/R	N/R		N/R	N/A	N/A	N/A
Supply (V)		**0.6**		1.2	0.75	0.65		0.9	N/R	1	1.2
Power (mW)		**29.2 (19.2 + 10)[#]**		6– 11	8.4	17.5	21.6	14	N/R	70	39
Area (mm^2)		**0.26**		0.06	0.07	0.086		0.051	0.4^	0.22^	0.2
Technology (nm)		**28 LP**		65	28	65		40	45 SOI	65	55

*Simulation result, [#]Including 3rd Harmonic Extractor, [&]Phase only equivalent value (w/o amp. error), ^Estimated. FoM = PN- $20\log(f_0/\Delta f) + 10\log(P_{DC}/1mW)$

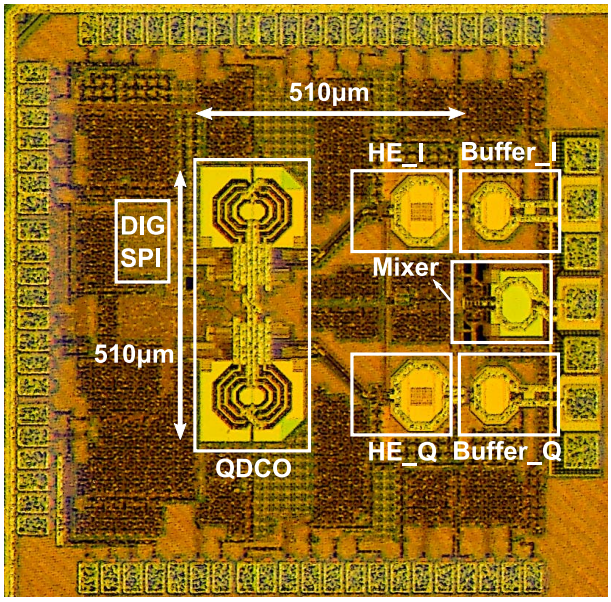

Fig. 15. Chip micrograph.

that the baseband signals are free from any mismatches, the I/Q imbalance of the LO (i.e., the QDCO under test) will cause the residue (i.e., image) signal at $\omega_{LO} - \omega_{BB}$. The power ratio of the desired signal to the image signal is defined as IRR. The single-ended I/Q mixer output is monitored by R&S FSW-85 signal analyzer. A schematic of the on-chip double-balanced current-mode mixer for the IRR testing is shown in Fig. 13(b), where the differential component outputs are combined and converted into single-ended by an on-chip transformer.

The measured IRR spectra at the two ends of TR are shown in Fig. 14(a) and (b), exhibiting IRR of 47.6 and 50 dB at $f_{LO,min}$ and $f_{LO,max}$, respectively. They maintain IRR $>$ 46 dB across the whole TR, as illustrated in Fig. 14(c). While sweeping the power supply level of the QDCO, the measured IRR maintains $>$46 dB, as plotted in Fig. 14(d) without any real-time calibration, as commonly used in PPF [17], [18]. The large LO leakage was identified to be caused by the LO signal's coupling to the power supply of the mixer, which could be normally avoided by a more careful layout and isolation.

The performance of the proposed QDCO is summarized in Table II and compared with the state-of-the-art mm-wave QVCOs/QDCOs and also mm-wave quadrature signal generation circuits in which LO is off-chip. To the best of the authors' knowledge, the QDCO achieves the lowest PN of -110 dB/Hz at 1-MHz offset from 30 GHz, the record-low flicker PN corner with a state-of-the-art FoM. In terms of I/Q imbalance, our QDCO also features the highest level of IRR.

VI. CONCLUSION

Accurate *quadrature* frequency generation with low PN in mm-wave (e.g., 28/39 GHz) bands is necessary for supporting large-bandwidth (e.g., 800 MHz) and complex modulation

schemes (e.g., 256-QAM). Compared with the poly-phase filter (PPF) approach, the conventional QOSCs are more robust to PVT variations but suffer from significant flicker noise upconversion. In this article, we propose a low flicker PN mm-wave class-F quadrature digitally controlled oscillator (DCO) with a third-harmonic extraction. We demonstrate that the quadrature coupling voltage itself causes different exposure strengths of flicker noise current to the rising and falling edges of the oscillation waveform, leading to the flicker noise upconversion, which is solved here by a negative drain-to-gate phase shift (thereby tuning the exposure strength of flicker noise current). At the same time, a deliberate phase shift is introduced in the transistor–source I/Q coupling path to avoid the $\pm 90^\circ$ mode ambiguity. This is supported by a complete analysis on the basis of a simple phasor diagram.

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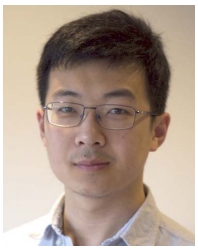
Dr. Siriburanon is currently a member of the Technical Program Committee of IEEE Radio Frequency Integrated Circuits Symposium (RFIC). He was a recipient of the Japanese Government (MEXT) Scholarship, the Young Researcher Best Presentation Award at Thailand–Japan Microwave in 2013, the ASP-DAC Best Design Award in 2014 and 2015, the IEEE SSCS Student Travel Grant Award in 2014, the IEEE SSCS Predoctoral Achievement Award in 2016, the Tejima Research Award in 2016, and the Science Foundation Ireland (SFI) Frontiers for the Future Awards in 2021. He has been a Guest Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS (2019–2020), an Associate Editor of IEEE ACCESS (since 2020), and serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS.



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During this research, he was working as a Post-Doctoral Researcher at UCD on a project with Equal1 Labs designing cryogenic CMOS high-speed data links for quantum computers. His current research interests include low-power frequency synthesizer design, low-power receiver design, grating couplers for silicon photonics, and cryogenic circuit design for quantum computer applications.

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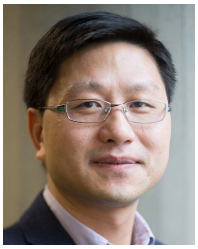
Prof. Staszewski was a TPC Chair of 2019 ESSCIRC in Kraków, Poland. He also serves on the Technical Program Committee of the VLSI Symposium on Circuits. He was a recipient of the 2012 IEEE Circuits and Systems Industrial Pioneer Award.



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