A Self-Calibration SCPA With Storage Capacitor Array Supporting 64-/256-/1024-QAM

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***Abstract*— This article presents a digital polar Doherty switched-capacitor power amplifier (SCPA) using on-chip self-calibration technique with storage capacitor array (SCA) to compensate the amplitude modulation (AM)–phase modulation (PM) distortion automatically for high data-rate signals. Such a self-calibration technique detects the AM–PM distortion at output and generates the related phase compensation in PM signals. The SCA is proposed to store control voltages of phase shifter for different amplitude code and decrease the settle time for high data-rate, which achieves fast locking of the calibration loop. Based on the proposed self-calibration with SCA, a polar Doherty SCPA is designed and fabricated in conventional 40-nm CMOS technology. This chip achieves 28.9-dBm peak output power (P_{sat}) and 43.9% peak drain efficiency (DE) at 1.8 GHz. It supports 100-MHz 64-QAM/10-MHz 1024-QAM signal with 22.6-/21.3-dBm average output power and 33.9%/32.1% average DE without digital pre-distortion (DPD).**

***Index Terms*— Amplitude modulation (AM)–phase modulation (PM) distortion, CMOS, digital power amplifier (PA), Doherty, linearization, self-calibration, storage capacitor array (SCA), switched-capacitor power amplifier (SCPA).**

I. Introduction

With the increasing demand for high data rate of wireless communication, wide modulation bandwidth and high-order modulation schemes are desired. Due to the finite frequency bandwidth, high-order complex modulation schemes are essential for radio frequency (RF) transceiver systems, such as 64-/256-/1024-QAM [1], [2], [3]. However, these spectral efficient complex modulation schemes require high amplitude modulation (AM) and phase modulation (PM) resolution of power amplifier (PA) to generate modulation signals. Meanwhile, the PA linearity affects the error vector magnitude (EVM) of signals directly, which is more important for high-order complex modulation schemes. Thus, the PAs with inherent high linearity or techniques of linearity enhancement are of great importance to high-order modulation signals.

For high linearity, analog PAs, i.e., Class-A and Class-AB PAs, have been widely used with limited efficiency [4], [5], [6]. On the contrary, digital PAs have been widely investigated in recent years for their merits of high efficiency and flexibility of operation modes [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32]. The switching unit cells contribute to the high efficiency of digital PAs. However, it causes the variation of output resistance and capacitance, which affects the linearity. Digital pre-distortion (DPD) is widely used to improve linearity for high-order modulation signals [33], [34], [35], [36], [37], [38], [39], [40], [41], [42]. DPD can be used for both AM–AM and AM–PM distortion. Nevertheless, it requires large lookup tables (LUTs), which is usually realized off-chip by algorithm, such as MATLAB on PC. For on-chip DPD, the hardware overhead depends on the size of memory to register the LUT, which is relatively large for high-resolution PAs [34], [35].

On-chip hardware calibration techniques are also reported [43], [44], [45], [46], [47], [48] instead of DPD. The AM replica feedback linearization technique is proposed to regulate the PA bias voltage with an analog feedback loop to minimize the distortion in the AM path [43]. It requires additional digital-to-analog converter (DAC) to generate the RF envelop for the linearization, which increases the area and power consumption. The built-in AM–PM distortion self-compensation technique utilizes feed-forward capacitors and digital PA biasing scheme to minimize the PA output capacitor variations over a wide range of PA output power [44]. Such a method achieves good AM–PM linearity for current-mode digital PA. An AM–PM self-compensation method is realized based on the opposite AM–PM distortion variation of current- and voltage-mode digital PAs [45]. This operation is only applicable for phase compensation of hybrid-mode digital PAs, which limits the application range. Moreover, the AM and the PM distortion are related to many parameters, such as frequency and process, voltage, and temperature (PVT). Thus, for different kinds of PAs, the adaptive linearization with low cost is still a great challenge.

In this article, a self-calibration technique with storage capacitor array (SCA) for AM–PM distortion of digital PA is presented [49]. The self-calibration technique proposed in this work reduces the AM–PM distortion by detecting phase in output and generating compensation in phase shifter. Thus, the proposed self-calibration technique can be used for

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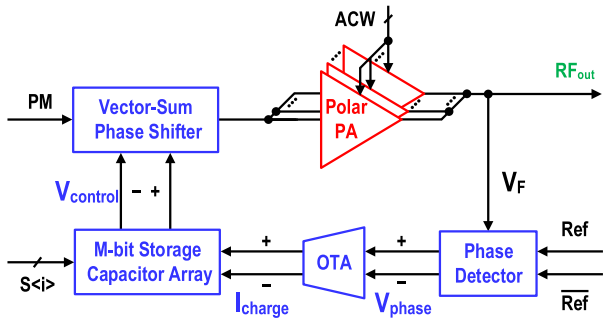

Fig. 1. Diagram of the proposed AM–PM distortion self-calibration with SCA.

both voltage- and current-mode DPAs. A switched-capacitor PA (SCPA) with the proposed self-calibration technique is designed and fabricated in 40-nm CMOS technology as a proof of concept, which shows good performance of both AM–AM and AM–PM linearity without DPD for 64-/256-/1024-QAM. This article is organized as follows. Section II introduces the theory of the self-calibration with SCA and the operation details of calibration process. Section III describes the architecture and circuits implementation of the proposed self-calibration SCPA with SCA. Section IV gives the measurement results and comparison table. Section V draws the conclusion.

II. AM–PM Distortion Self-Calibration Technique

The concept of the proposed AM–PM distortion self-calibration technique is shown in Fig. 1, which is consisted of four building blocks, i.e., phase detector, operational transconductance amplifier (OTA), M-bit SCA, and vector-sum phase shifter. The AM–PM distortion is generated by the amplitude control word (ACW) controlled digital polar PA array. The phase detector compares the phase between digital PA output signal and REF signal and converts AM–PM distortion into voltage V_{phase}. This voltage is converted to current I_{charge} by OTA to charge the SCA. The SCA is comprised of switched capacitors controlled by decoded amplitude code $S<i>$ ($i = 1, \ldots, 2^M$). One capacitor is selected by $S<i>$ to be charged by I_{charge}. Therefore, SCA generates variable voltage according to amplitude information from baseband, which controls the phase shifter. Phase shifting for input PM signal is produced by the phase shifter determined by V_{control}. Thus, the AM–PM distortion is detected and calibrated by the proposed self-calibration technique.

In the self-calibration process, the typical behaviors of each building block are shown in Fig. 2. Before the self-calibration, the typical states for building blocks are marked in red. V_{control} from SCA and phase compensation from phase shifter are both 0. During the calibration, V_{phase} and I_{charge} change toward the target states with 0 AM–PM distortion ($V_{\text{phase}} = 0$, $I_{\text{charge}} = 0$). With continuous charging of SCA by I_{charge}, V_{control} is increasing, which leads to a growing phase compensation. Once the AM–PM distortion is compensated exactly, the calibration process is ended, while AM–PM distortion, V_{phase}, and I_{charge} are all decreased to 0. Besides, $V_{\text{control}}<i>$ is stored in SCA to keep the phase compensation.

A. Analysis of Self-Calibration Building Blocks

1) Phase Detector: The proposed phase detector is used to convert phase distortion into different voltages for

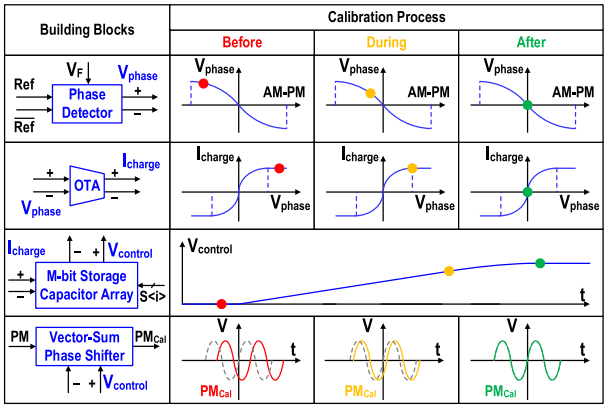

Fig. 2. Behavior of building blocks in the self-calibration process.

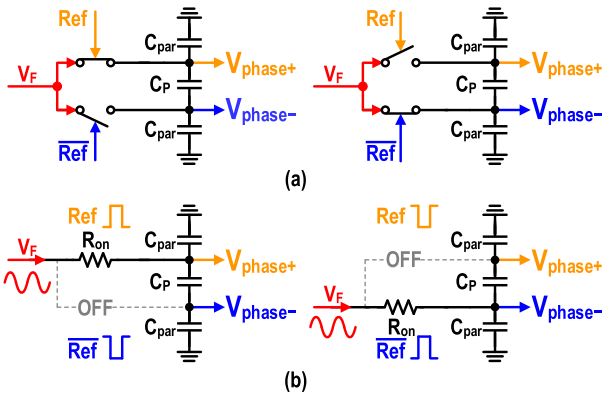

Fig. 3. Proposed phase detector with two operation states: (a) configuration and (b) equivalent model.

self-calibration. The concept of proposed phase detector is shown in Fig. 3(a), which is comprised of two switches, a parallel capacitor C_P and two parasitic capacitors C_{par}, which are the parasitic capacitors at the two output nets, i.e., $V_{\text{phase+}}$ and $V_{\text{phase–}}$. Note that V_{phase} is the difference of $V_{\text{phase+}}$ and $V_{\text{phase–}}$. Since the control signals of switches are complementary rail-to-rail reference signals, i.e., Ref and $\overline{\text{Ref}}$, the two switches turn on alternatively. Meanwhile, due to the PA output signal carrying PM information, the phase of feedback V_{F} is composed of PM and phase distortion, which increases the complexity of phase distortion detection. To avoid undesired influence of PM, the input PM signal is used to generate Ref and $\overline{\text{Ref}}$. Hence, the phase difference between reference and output signals is only related to the AM–PM distortion. Considering the ON-resistance of switches (i.e., R_{ON}), Fig. 3(b) shows the equivalent circuits of the proposed phase detector.

According to the detailed derivation in Appendix A, V_{phase} is comprised of two components (i.e., $V_{\text{phase, dc}}$ and $V_{\text{phase, non-dc}}$), which represent the desired dc component and undesired non-dc component, respectively. The non-dc component introduces swings in V_{phase} and decreases the stability of phase compensation, which should be suppressed in circuit implementation. Note that the influence of undesired $V_{\text{phase, non-dc}}$ is jumped here due to the suppression in circuit implementation. Thus, V_{phase} is replaced by the dc component $V_{\text{phase, dc}}$, which is expressed as

$$V_{\text{phase, dc}} = -(1+\gamma_C)G_C V_{\text{ac}} \sin(\theta_d) \tag{1}$$

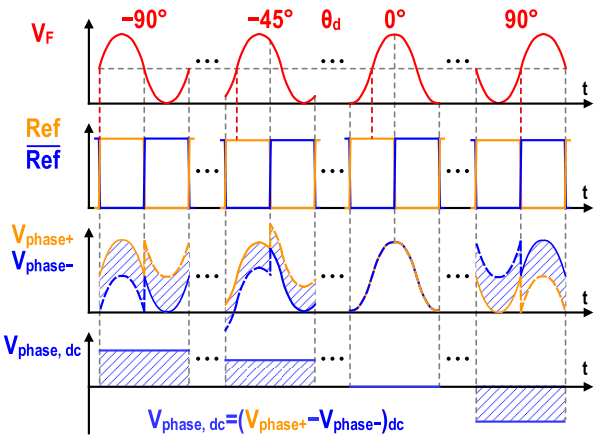

Fig. 4. Behavior of the phase detecting process of phase detector with different θ_d values.

where

$$\gamma_C = \frac{C_P}{C_{\text{par}} + C_P} \tag{2}$$

$$\theta_d = \theta_{\text{AM–PM}} - \theta_{RC}. \tag{3}$$

Equation (1) is the dc component of derivation results in Appendix, which is converted from the phase distortion θ_d. V_{ac} is the amplitude of the feedback signal V_{F}, and $\theta_{\text{AM–PM}}$ is the AM–PM distortion in V_{F}. Meanwhile, $\theta_{\text{AM–PM}}$ includes a fixed phase difference between V_{F} and differential refereneces (i.e., Ref and $\overline{\text{Ref}}$). G_C and θ_{RC} are the amplitude coefficient and phase delay caused by the RC network of phase detector, which are related to R_{ON}, C_P, and C_{par} as given in the Appendix. According to (1), the behavior descriptions for phase detection with different phase distortion are shown in Fig. 4. The waveform at nets $V_{\text{phase}\pm}$ is related to the ON/OFF of switches and phase delay of RC. Within the phase detection range of $\pm 90°$, the converted dc component $V_{\text{phase, dc}}$ varies following θ_d. When $\theta_d = 0°$, $V_{\text{phase, dc}}$ decreases to 0, which means that the phase distortion is compensated exactly. Moreover, $V_{\text{phase, dc}}$ is simultaneously affected by the amplitude (V_{ac}) and phase (θ_d) of feedback signal. The sign of $V_{\text{phase, dc}}$ is only affected by θ_d. Therefore, θ_d determines whether the OTA charges or discharges the capacitor in SCA. The magnitude of $V_{\text{phase, dc}}$ affects the charging time of calibration process. When the phase self-calibration is completed, $V_{\text{phase, dc}}$ is decreased to 0. However, the magnitude of V_{ac} is limited at small codes, which makes $V_{\text{phase, dc}}$ close to 0. Therefore, to improve the phase detection accuracy especially at small codes, the high sensitivity OTA is needed to small input voltage.

2) Operational Transconductance Amplifier: The OTA is introduced to convert phase-dependent voltage $V_{\text{phase, dc}}$ into current I_{charge}, which charges capacitors in SCA. As shown in Fig. 5, the conversion from voltage to current is achieved by differential pair with current source, which limits the saturated output current. This conversion is necessary to lock the calibration result when the self-calibration is finished, as shown in Fig. 2. After the calibration process with I_{charge} of 0, V_{control} is kept constant leading to a fixed phase shifting of the phase shifter. If $V_{\text{phase, dc}}$ directly controls vector-sum phase shifter, the required control voltage for phase compensation is conflict with $V_{\text{phase, dc}}$ after calibration. Such calibrated

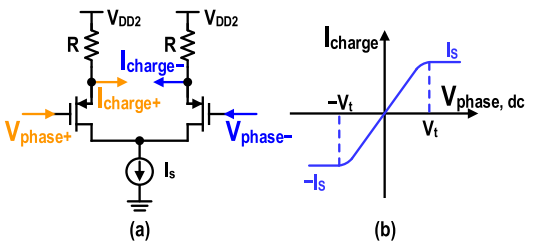

Fig. 5. (a) Circuits and (b) behavior of the differential pair in OTA.

$V_{\text{phase, dc}}$ is decreased to 0, when the AM–PM distortion is compensated. The conversion of differential pair in Fig. 5 from $V_{\text{phase, dc}}$ to I_{charge} is derived as

$$I_{\text{charge}} = \begin{cases} -I_S, & V_{\text{phase, dc}} < -V_t \\ \gamma_{\text{dp}} V_{\text{phase, dc}} \sqrt{\frac{2I_S}{\gamma_{\text{dp}}} - V_{\text{phase, dc}}^2}, & -V_t < V_{\text{phase, dc}} < V_t \\ I_S, & V_t < V_{\text{phase, dc}} \end{cases} \tag{4}$$

where I_S and V_t are the saturated output current and threshold input voltage of differential pair, respectively, and γ_{dp} is a constant coefficient related to circuit parameters of the differential pair.

3) M-Bit SCA : The circuits of M-bit SCA and charging processes with various control voltages are shown in Fig. 6. The M-bit SCA is composed of N ($\text{N} = 2^M$) identical capacitors and 2N switches. In the calibration process, $S<i>$ decoded from the baseband amplitude signal of the digital PA chooses a capacitor $C<i>$ to be charged and store V_{control} as $V<i>$. The charging process of each capacitor for the initialization of self-calibration is expressed as

$$V_{\text{control}} = \int_0^t \gamma_{\text{SCA}} I_{\text{charge}}(V_{\text{phase, dc}})dt, \quad 0 \le t \le t_{\text{init}} \tag{5}$$

where γ_{SCA} is constant coefficient related to the equivalent capacitance in the charging process, including the storage capacitor and parasitic capacitors of switches. $I_{\text{charge}}(V_{\text{phase, dc}})$ represents the varied charging current, as a function of $V_{\text{phase, dc}}$. t_{init} is the charging time.

4) Vector-Sum Phase Shifter: Fig. 7(a) shows the vector-sum phase shifter, which is introduced to generate phase compensation for AM–PM distortion. The desired phase shifting is achieved by combining the quadrature signals, i.e., $V_{\text{I+}}$ and $V_{\text{Q+}}$ ($V_{\text{I–}}$ and $V_{\text{Q–}}$), as shown in Fig. 7(b). Thus, the phase shifting is related to the amplitude of $V_{\text{I}\pm}$ and $V_{\text{Q}\pm}$, which are produced by multiplying $V_{\text{control}\pm}$ and $PM\_I \pm (PM\_Q\pm)$. Meanwhile, $PM\_I\pm$ and $PM\_Q\pm$ are converted from input PM signals to keep the PM information in $PM_{\text{Cal}\pm}$. Since the amplitudes of $V_{\text{I}\pm}$ ($V_{\text{Q}\pm}$) are assumed as $\gamma_{\text{m}} V_{\text{control+}}$ ($\gamma_{\text{m}} V_{\text{control–}}$), $\Delta\theta$ ignoring variation in γ_{m} is derived as

$$\Delta\theta = \arccos \frac{V_{\text{control+}}}{\sqrt{(V_{\text{control+}})^2 + (V_{\text{control–}})^2}}. \tag{6}$$

For the compensation of AM–PM distortion, the required $\Delta\theta$ is expressed as

$$\Delta\theta = -\theta_{\text{AM–PM}}. \tag{7}$$

By determining $\Delta\theta$, the corresponding $V_{\text{control}\pm}$ can be calculated.

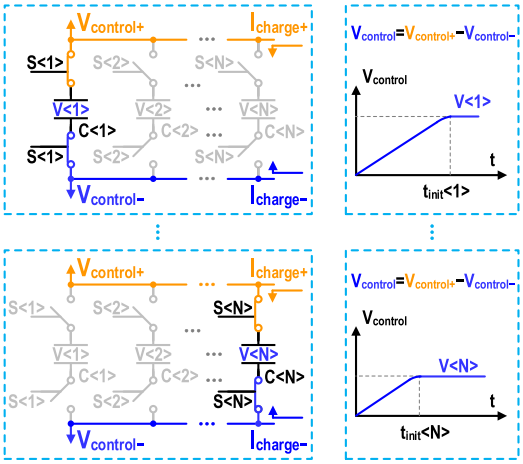

Fig. 6. Circuits of the SCA and the behavior of charging process of different $C<i>$ with various $S<i>$.

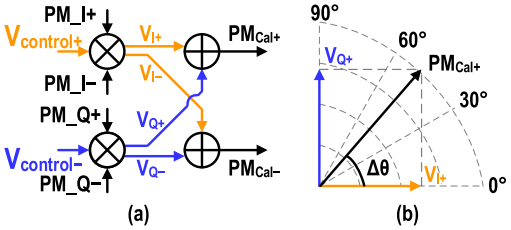

Fig. 7. Circuits and behavior of the vector-sum phase shifter.

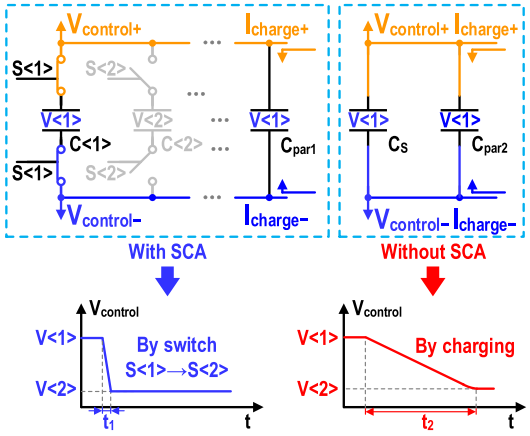

Fig. 8. Behavior of loop response time comparison with SCA or fixed capacitor.

B. Fast Locking Self-Calibration

The transmitting of high data-rate modulation signals requires fast changing amplitude codes, which demands shorter loop response time. Fig. 8 compares the loop response time with SCA or fixed capacitor. C_{par1} and C_{par2} are the parasitic capacitors for SCA and fixed capacitor C_S, respectively. Suppose that $C<i>= C_S$, and C_{par1} and C_{par2} are much smaller than $C<i>$. After $S<i>$ selects $C<i>$, $C<i>$ is charged to target $V<i>$ for AM–PM compensation. When $C<i>$ is de-selected after the initial charging, it still stores $V<i>$. Therefore, after the initial charging of all capacitors in SCA, only C_{par1} needs to be charged between different voltage levels when switching $S<1>$ to $S<2>$. For the fixed capacitor, both C_S and C_{par2} should be charged. The response time for both cases can be determined by

$$t_1 = C_{par1}\frac{\Delta V}{I_{charge}} \tag{8}$$

$$t_2 = (C_S + C_{par2})\frac{\Delta V}{I_{charge}} \tag{9}$$

It can be concluded that $t_1 \ll t_2$. Therefore, the SCA with initialization decreases the loop response time of self-calibration significantly.

III. Circuit Implementation

A. Architecture

The block diagram of the proposed self-calibrated SCPA with SCA is shown in Fig. 9(a). The proposed SCPA is designed as 2 × 10 bit to support high-order modulation schemes. Doherty operation is used to enhance the average efficiency at power back-off (PBO). SCPA is utilized for the inherently high AM linearity.

The main and auxiliary sub-PA arrays compose the Doherty architecture. Each sub-PA array consists of 6-bit MSB and 4-bit LSB, which are controlled by thermometer and binary codes, respectively. The output signals of SCPA are combined by a 4-to-1 current combining transformer. The output matching network includes the transformer and matching capacitors C_{m1} and C_{m2}. The output of the PA is feedback to the self-calibration circuits by a dc bias block, which is constructed, as shown in Fig. 9(a). The simulated transient voltage of RF_{out} and V_F at saturated power is shown in Fig. 10. The phase detector is implemented using thick-oxide transistors. When the proposed DPA delivers the output power of 29.4 dBm, V_F is limited within 0–2.6 V, which will not overstress the phase detector. The simulated drain efficiency (DE) and saturated output power with/without the self-calibration and dc bias block are compared in Fig. 11(a) and (b) respectively. It can be seen that the proposed self-calibration and dc bias block lead to maximal 0.16% degradation of DE and 0.04-dB degradation of saturated output power in the operation frequency range of 1.4–2.8 GHz.

The ACWs of PA cells are converted from the input amplitude baseband signals by deserializers and decoders. The 11-bit amplitude codes are converted to 2 × 10 bit ACW signals for main and auxiliary PAs and deserialized by four 1:5 deserializers. Then, each 10-bit ACW is converted into 6-bit thermometer codes and 4-bit binary codes by decoders, which control unit cells of sub-PA arrays. The input signal *BB_SCA* is deserialized and decoded to the control signals of SCA, i.e., $S<8:1>$. The delay generator converts differential PM signals to quadrature types ($PM\_I\pm$, $PM\_Q\pm$) for phase shifter and references (i.e., Ref and $\overline{\text{Ref}}$) for phase detector with the control of D_{IQ} and D_{Ref}. PM_{Cal} is the differential calibrated PM signal, which is produced by the vector-sum phase shifter. Meanwhile, the PM level shifter converts PM_{Cal} (0–V_{DD2}) into two signals with different amplitudes, i.e., PM_{Cal_L} with 0–V_{DD} and PM_{Cal_H} with V_{DD}–V_{DD2}.

The 3-bit SCA is adopted to achieve coarse calibration and compact circuit size. Two 10-bit SCPAs with Doherty operation are divided into eight parts corresponding to the

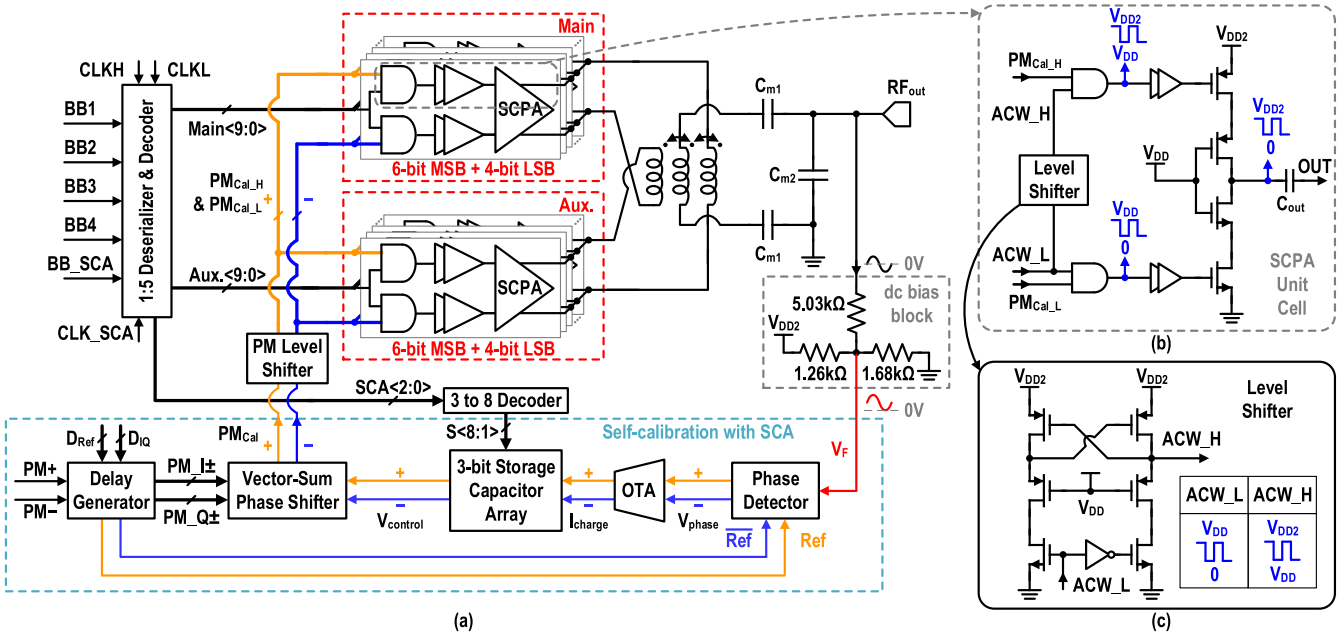

Fig. 9. (a) Block diagram of the proposed self-calibrated SCPA. Schematic of (b) SCPA unit cell and (c) level shifter.

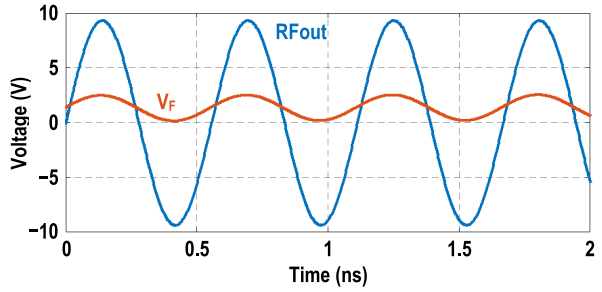

Fig. 10. Simulated transient waveforms of RF_{out} and V_F for saturated output power at 1.8 GHz.

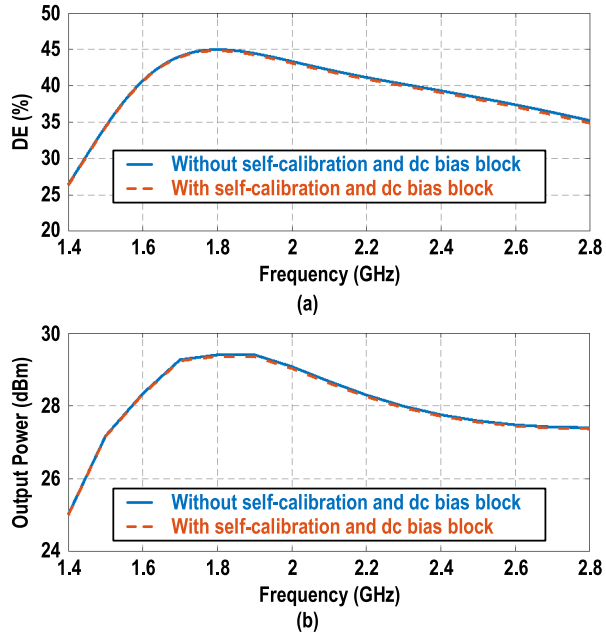

Fig. 11. Simulated (a) DE and (b) output power with/without self-calibration and dc bias block.

eight storage capacitors in SCA for coarse calibration. Such eight capacitors are controlled by the 3-bit SCA codes. The

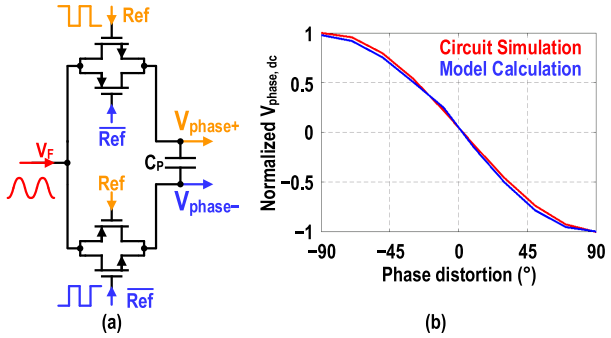

Fig. 12. (a) Circuit implementation of the phase detector. (b) Comparison of calculated and simulated results.

AM–PM distortion of the SCPA can be carefully compensated by self-calibration loop during the amplification process.

B. SCPA Unit Cell

Fig. 9(b) shows the circuits of SCPA unit cell, which consists of level shifter, AND gates, buffers, and stacked inverter. The schematic of level shifter is shown in Fig. 9(c), which shifts the voltage of the ACW from 0–V_{DD} to V_{DD}–V_{DD2}. The dimensions of NMOS and PMOS in level shifter are 0.5 μm/40 nm and 1 μm/40 nm, respectively. The AND gates combine the ACW signals (i.e., *ACW_L* and *ACW_H*) and PM signals (i.e., PM_{Cal_L} and PM_{Cal_H}), which drive the stacked inverter with buffers. The stacked inverter is used to deliver higher output power with increased supply. The dimensions of NMOS and PMOS are 32 μm/40 nm and 64 μm/40 nm, respectively. The output capacitors of the SCPA unit cell are 330 fF for 6-bit MSB and 165, 82.5, 41.2, and 20.6 fF for 4-bit LSB. However, the nonlinearity is caused by the ON-resistance mismatch of NMOS and PMOS switches [50].

C. Phase Detector

As shown in Fig. 12(a), the phase detector is comprised of two transmission gates (TGs) and a parallel capacitor C_P. TGs

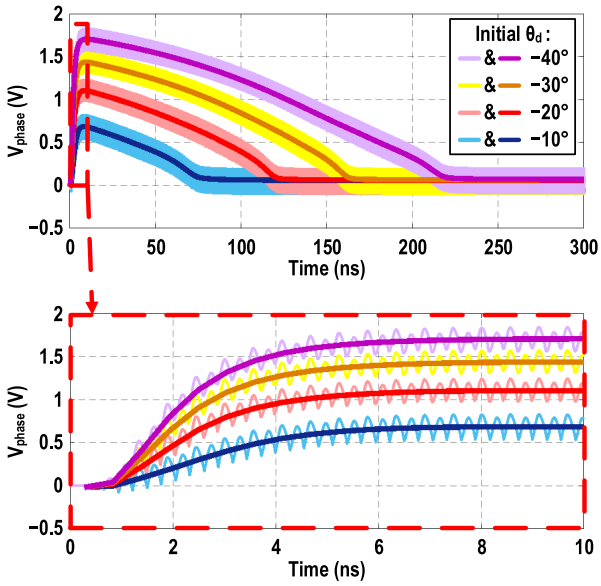

Fig. 13. Simulated transient voltage V_{phase} in different self-calibration processes with different initial θ_d.

are controlled by complementary rail-to-rail reference signals, i.e., Ref and $\overline{\text{Ref}}$, which are generated by delay generator from PM signals. The dimensions of NMOS and PMOS of TG are 0.5 μm/270 nm and 1 μm/270 nm, respectively, and C_P is 25 fF. With $R_{\text{ON}} = 2.9$ kΩ of TG and $C_{\text{par}} = 2$fF at output nets, the calculated $V_{\text{phase, dc}}$ according to (1) is normalized and compared with the simulated result, as shown in Fig. 12(b). It is seen that the calculation result matches the simulation.

Moreover, the simulated transient waveform of V_{phase} with different initial θ_d is shown in Fig. 13. The four bright lines are simulated V_{phase} with undesired non-dc component, which introduces swings in waveform. The four dark lines are set as the dc component $V_{\text{phase, dc}}$, which are calculated from V_{phase} by averaging. The simulated response time is shown in Fig. 13, which exhibits the charging and calibration process of V_{phase} with different phase distortion. Larger phase distortion leads to larger V_{phase}, which requires longer initialization time for phase compensation. When the phase distortion is compensated, $V_{\text{phase, dc}}$ is decreased to 0.06 V.

D. Operational Transconductance Amplifier

Fig. 14(a) shows the schematic of the OTA, which is composed of bias circuits, core OTA, output stage, and common-mode feedback circuit (CMFB). It uses conventional 2.5-V thick-oxide MOSFET and the dimensions of transistors are shown in the bottom of Fig. 14(a). The OTA converts V_{phase} into I_{charge}, which charges capacitors in SCA to generate V_{control} for phase compensation. The simulated I_{charge} versus V_{phase} is shown in Fig. 14(b). The OTA shows high sensitivity to small input voltage (i.e., V_{phase}) to improve the detecting accuracy at small ACW codes with limited magnitude of $V_{\text{phase, dc}}$. The improved linear range can lead to decreased calibration time. To suppress the influence of swings in I_{charge} caused by $V_{\text{phase, non-dc}}$, small output current (i.e., saturated $I_{\text{charge}} < 10$ μA) is used. As shown in Fig. 15, the open-loop gain of the OTA is simulated as 51.11 dB. The 3-dB

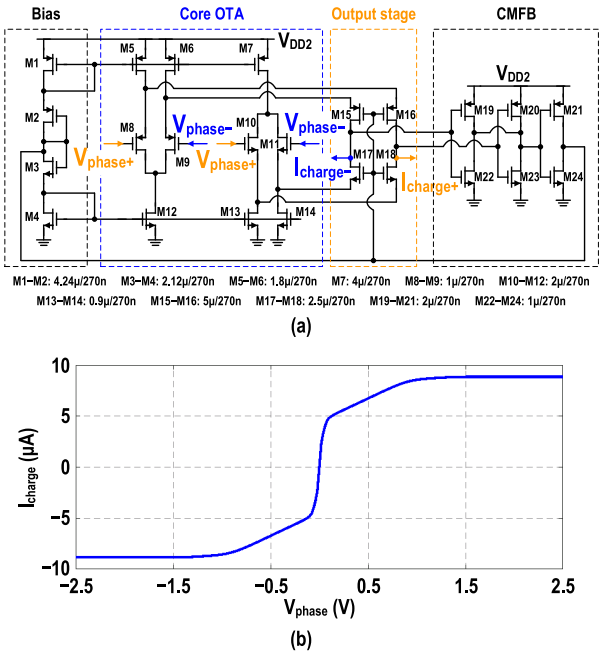

Fig. 14. (a) Schematic and (b) simulated I_{charge} of OTA.

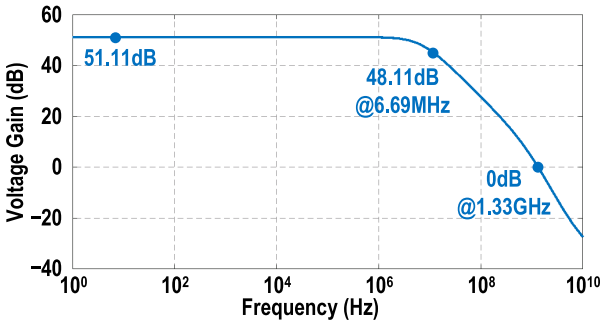

Fig. 15. Simulated open-loop gain and bandwidth of the proposed OTA.

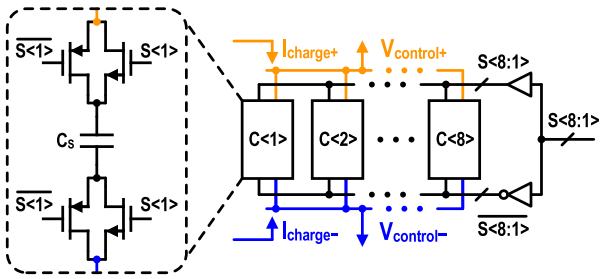

Fig. 16. Circuit implementation of 3-bit SCA.

bandwidth is 6.69 MHz, while the unit gain bandwidth is 1.33 GHz.

E. Storage Capacitor Array

The circuit of the 3-bit SCA is shown in Fig. 16, which is comprised of eight unit cells. Each unit cell is composed of a capacitor C_S and two TGs, which is controlled by a complementary switch code $S<i>$ and $\overline{S<i>}$. Here, $S<8:1>$ is generated from SCA<2:0> by a 3-to-8 decoder, which converts 3-bit binary code into 8-bit one-hot code. To decrease the impact of swings in I_{charge} caused by $V_{\text{phase, non-dc}}$, the capacitance of SCA is increased to further suppress its influence. Thus, C_S is 2 pF to get a stable V_{control} for vector-sum

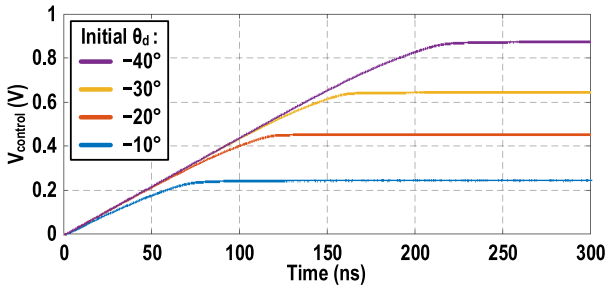

Fig. 17. Simulated V_{control} for initialization stage of the SCA.

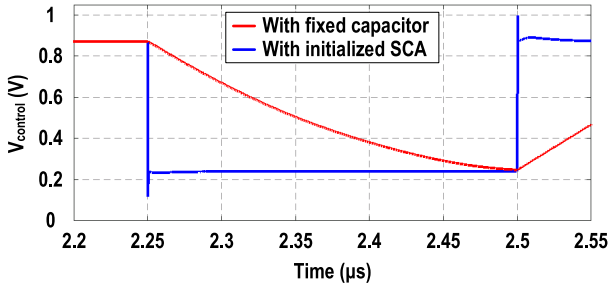

Fig. 18. Simulated response time with initialized SCA or fixed capacitor.

phase shifter. Meanwhile, the dimensions of switches are 1 μm/270 nm (NMOS) and 2 μm/270 nm (PMOS).

Fig. 17 shows V_{control} for initialization stage with different phase distortion, which shows that the influence of $V_{\text{phase, non-dc}}$ is suppressed effectively. The corresponding V_{control} values are different with various initialization time from 100 to 250 ns for initial phase distortion from $-10°$ to $-40°$. Larger phase distortion leads to higher control voltage, which increases the initialization time with limited charging current. When the phase distortion is fully compensated, I_{charge} decreases to 0 and the control voltage reaches a stable level. Fig. 18 compares the simulated response time for initialized SCA and fixed capacitor. When the phase distortion is switching between $-40°$ and $-10°$, the response time with initialized SCA is much smaller than fixed capacitor. Thus, the modulation data rate of the proposed self-calibrated SCPA with SCA can be increased.

Besides, the self-calibration loop operates in both initialization process and amplifying process. In the initialization process, the calibration loop charges the capacitors to store the calibration states. In the amplifying process, the calibration loop is used to finely tune the phase compensation and refresh the stored voltage. The stored voltage affected by leakage current is re-charged by the self-calibration loop. Thus, the self-calibration loop is continuously running to hold the charge in capacitor.

F. Vector-Sum Phase Shifter

The schematic of the vector-sum phase shifter is shown in Fig. 19, which is based on NMOS and PMOS Gilbert cells. The vector-sum phase shifter uses conventional 2.5-V thick-oxide MOSFET, while the dimensions of transistors are shown in the bottom of Fig. 19. $V_{\text{control}\pm}$ determines

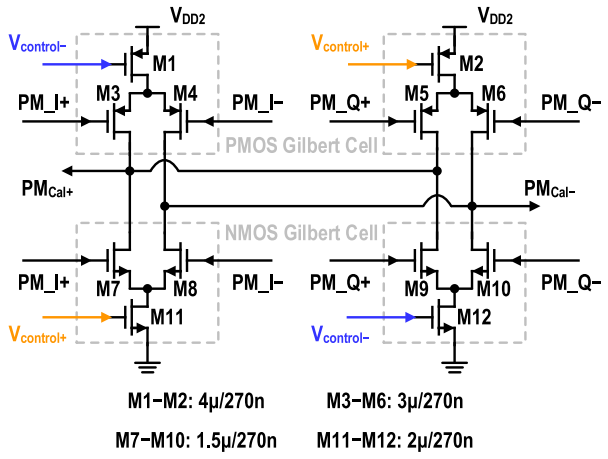

Fig. 19. Gilbert-cell-based vector-sum phase shifter.

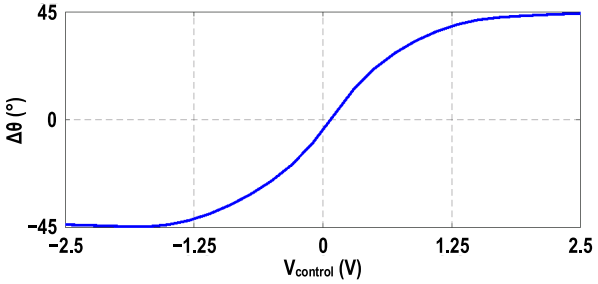

Fig. 20. Simulated phase shifting versus V_{control} for the phase shifter.

the current of Gilbert cells and multiplies with quadrature PM signals. Thus, the output signals, i.e., $\text{PM}_{\text{Cal}\pm}$, achieve phase shifting by vector sum. Since the quadrature PM signals (i.e., $PM\_\text{I}\pm$ and $PM\_\text{Q}\pm$) are generated from the input PM signals, the PM information is kept in $PM_{\text{Cal}\pm}$ after phase shifting. Fig. 20 shows the simulated phase shifting versus V_{control} for the vector-sum phase shifter, which achieves $\pm 45°$ phase shifting range. Due to the threshold voltage of transistors for conduction, the effective variation range of V_{control} for phase shifting is suppressed.

G. Delay Generator

As shown in Fig. 21(a), the structure of delay generator is comprised of buffer chain and multiplexers (MUXs), which are controlled by D_{Ref} and D_{IQ}, respectively. The input PM$\pm$ is utilized as $PM\_I\pm$ for the vector-sum phase shifter. $PM\_Q\pm$ is chosen among the delayed signals by D_{IQ}. Meanwhile, the reference signals Ref and $\overline{\text{Ref}}$ are determined by D_{Ref}. Ref and $\overline{\text{Ref}}$ constitute the phase detection range. $PM\_I\pm$ and $PM\_Q\pm$ form the phase shifting range. Note that RF_{out} only varies in the phase shifting range. Moreover, to reduce the effect of the mismatch between the AM and PM paths, the same delay chain is introduced in front of the delay generator to finely tune the delay of PM signals.

Due to the phase shifting range ($\pm 45°$) less than phase detecting range ($\pm 90°$), there are two different calibration results with uncertain phase delay in loop. Case A assumes that the phase shifting range satisfies the calibration requirement,

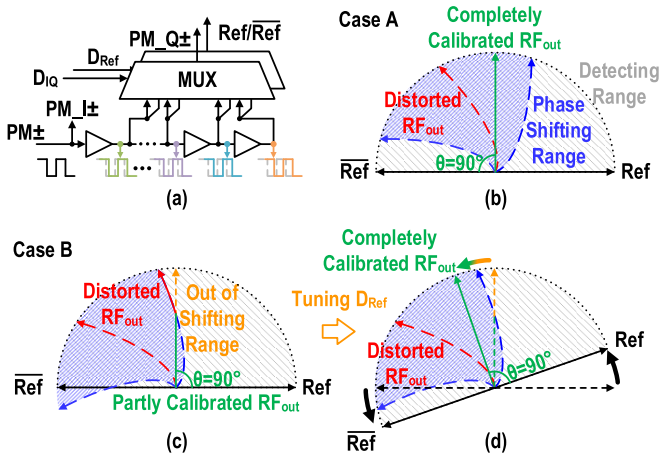

Fig. 21. (a) Structure of delay generator. (b) State of fully calibration. (c) State of partly calibration. (d) State conversion from partly calibration to fully calibration by tuning D_{Ref}.

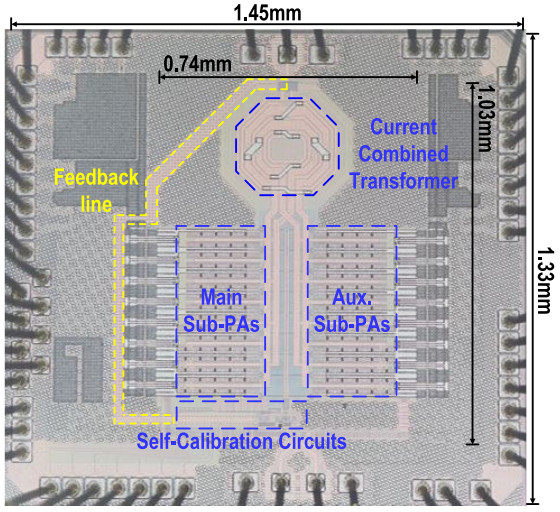

Fig. 22. Microphotograph of the proposed self-calibration SCPA chip.

i.e., the aimed calibrated RF_{out} is fully covered by the phase shifting range, as shown in Fig. 21(b). The aimed calibrated RF_{out} is the green solid line, which is orthogonal with Ref and $\overline{\text{Ref}}$. The red distorted RF_{out} can be fully compensated due to the cover. Case B is set that the phase shifting range cannot cover the aimed calibrated RF_{out}, as shown in Fig. 21(c). For the covered part of aimed RF_{out}, the phase distortion is calibrated. For the uncovered part, the AM–PM distortion exists in the shifted RF_{out}, i.e., the red solid line at the boundary of phase shifting range. To solve this problem, Ref and $\overline{\text{Ref}}$ are tunable to shift the aimed RF_{out} back to the phase shifting range. As shown in Fig. 21(d), with tuned D_{Ref}, the aimed RF_{out} is shifted back to phase shifting range, which means that the phase distortion is fully compensated.

IV. Measurement

The proposed SCPA using on-chip self-calibration technique with SCA is fabricated in conventional 40-nm CMOS technology. As shown in Fig. 22, this chip occupies 1.45×1.33 mm^2 including all I/O pads, with the core size of 0.74×1.03 mm^2.

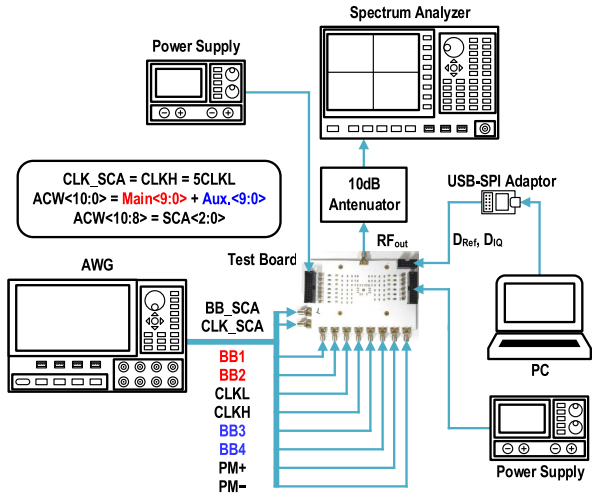

Fig. 23. Measurement setup.

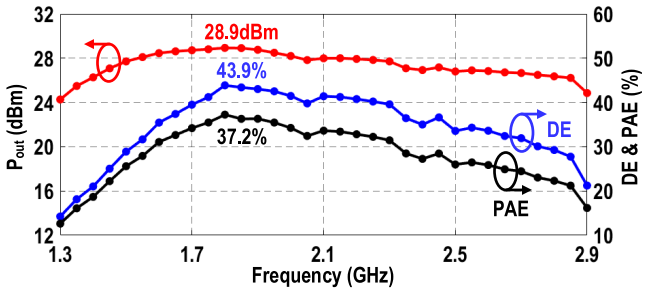

Fig. 24. Measured saturated output power, peak DE, and peak PAE.

Fig. 23 shows the measurement setup. The arbitrary waveform generator (AWG) is utilized to generate the baseband signals and the differential PM signals. The sampling rate of baseband signals is 400 MHz. The RF_{out} is attenuated by a 10-dBm attenuator and measured by a spectrum analyzer. D_{Ref} and D_{IQ} for delay generator are generated by MATLAB in PC and fed to the chip through a USB-SPI adaptor. The power supply of chip is 1.2 and 2.5 V for digital domain signals and PM/RF signals, respectively. All tests are performed without any pre-distortion.

With a continuous-wave (CW) signal, the peak output power, peak DE, and peak power added efficiency (PAE) are measured and shown in Fig. 24. The proposed digital PA achieves 28.9-dBm peak output power, 43.9% peak DE, and 37.2% peak PAE. The 3-dBm bandwidth is 1.4–2.8 GHz, i.e., 67% fractional bandwidth (FBW). The power consumption of the calibration loop is measured as 42.4 mW, which includes the self-calibration circuits and dc bias block. In Fig. 24, the reported PAE is calculated as the ratio of output power to total dc power consumption, which includes the power consumption of calibration loop.

The AM linearity and AM–PM distortion versus normalized AM codes at 1.8 GHz are shown in Fig. 25(a) and (b), respectively. The integral nonlinearity (INL) using normalized output voltage as a unit and the differential nonlinearity (DNL) using LSB as a unit of the AM–AM distortion are shown in Fig. 26(a) and (b), respectively. V_{out} is approximately

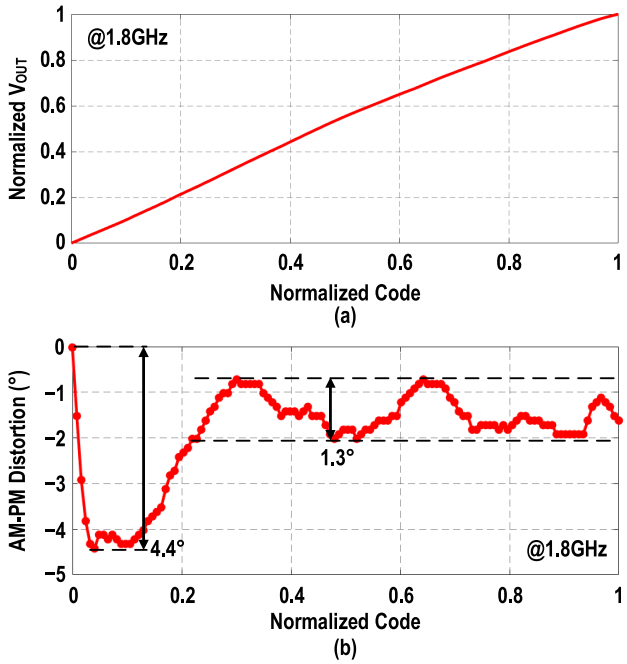

Fig. 25. Measured (a) AM–AM linearity and (b) AM–PM distortion at 1.8 GHz.

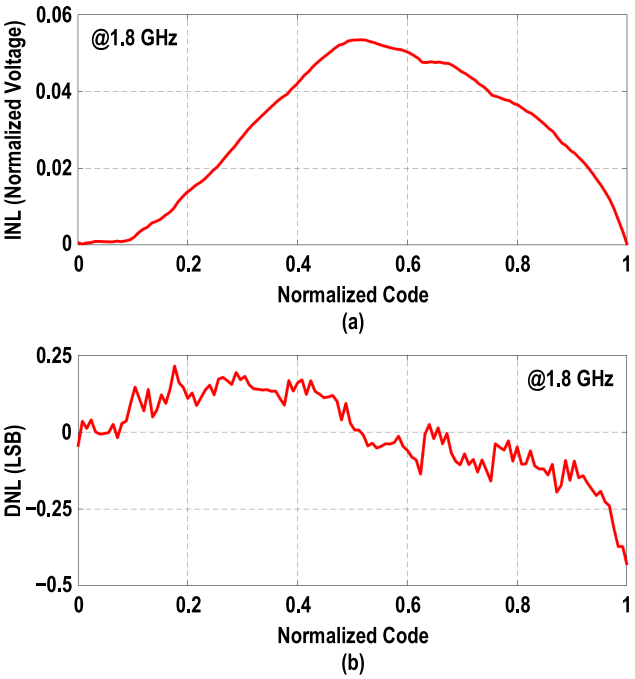

Fig. 26. Measured (a) INL and (b) DNL of the SCPA at 1.8 GHz.

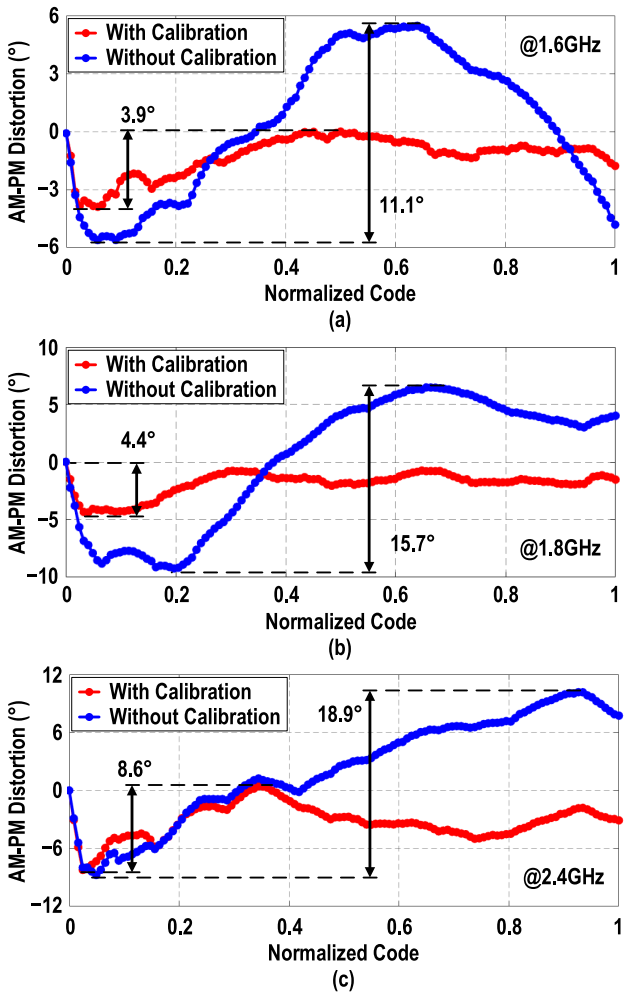

Fig. 27. Measured AM–PM distortion with/without self-calibration at (a) 1.6, (b) 1.8, and (c) 2.4 GHz.

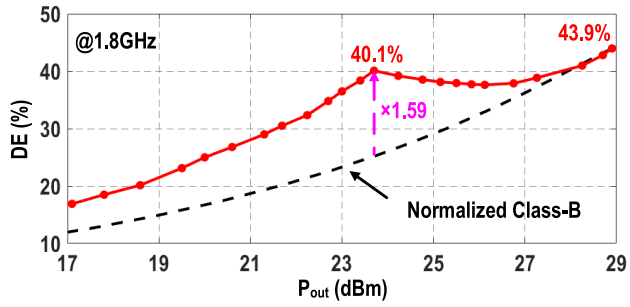

Fig. 28. Measured DE versus P_{out} at 1.8 GHz.

linear with the input code, due to the good inherent AM–AM linearity of SCPA. The maximum AM–PM distortion is about 4.4° with normalized code varying from 0 to 1. For normalized code larger than 0.22, it has $\leq$ 1.3° AM–PM distortion. Note that the initial phase is set as 0°. Fig. 27 shows the comparison of AM–PM distortion with/without proposed self-calibration at different frequencies. The proposed DPA shows maximal 11.1°, 15.7°, and 18.9° phase variations without the self-calibration at 1.6, 1.8, and 2.4 GHz, respectively. The maximal AM–PM distortions are reduced to 3.9°, 4.4°, and 8.6° with the self-calibration, which are decreased by 64%, 71%, and 54% at 1.6, 1.8, and 2.4 GHz, respectively. Note that the case without self-calibration is measured open loop. For discussion about the self-calibration effect across frequency, please refer to Appendix B.

The PBO DE of the digital PA is measured at 1.8 GHz and shown in Fig. 28. Due to the Doherty architecture adapted in the digital PA, it achieves an efficiency peak at 6-dB back-off in theory. The peak shifting from 6- to 5.2-dB PBO is caused

TABLE I
COMPARISON WITH STATE-OF-THE-ART DIGITAL POLAR PAS

Ref.	This work		JSSC'19 [42]	JSSC'19 [36]	JSSC'18 [44]	JSSC'20 [45]	JSSC'17 [46]	JSSC'20 [18]
Tech. (nm)	40		65	55	28	45 SOI	40	65
Architecture	Digital polar Doherty self-calibration SCPA		Digital polar Class-G Multi-SHS SCPA	PCT-based digital polar Doherty SCPA	Digital polar Class-D^{-1} current-mode	Digital polar hybrid Doherty PA	Digital polar Class-E/F_2 PA	Digital polar TI-Doherty single-supply Class-G SCPA
Freq. (GHz)	1.4–2.8*		1.9	0.85	2–4.3#	2.3	2	2.4
Supply (V)	1.2 / 2.5		1.2 / 2.4 / 3.6	1.2 / 2.4	1.4	1.2	0.5	2.5
Peak P_{out} (dBm)	28.9		30	28.9	24.9	22.4	14.3	30.0
Peak Efficiency (%)	43.9 (DE) / 37.2 (PAE)		45.9 (DE)	36.8 (PAE)	42.7 (DE)	38.5 (DE)	37 (DE) / 24 (PAE)	40.2 (DE)
AM-PM Distortion (°)	4.4 (1.3)$^{\$}$ @1.8GHz		25	5.9	6.8	4.7	2##	2
Linearization Techniques	Self-Calibration		AM-AM LUT +AM-PM LUT +DPD	AM-AM LUT	Feedforward Cap +Bias Scheme +AM DPD	Phase Nonlinearity Compensation +AM-AM LUT	Nonlinear Sizing +Overdrive-Voltage Tuning +Multiphase RF Clocking	Current-Reuse Class-G Switch
Modulation	100MHz 64-QAM	10MHz 1024-QAM	5MHz 16-QAM OFDM	20MHz 64-QAM WLAN	20MHz 64-QAM	40MHz 64-QAM	80MHz 64-QAM OFDM	10MHz 64-QAM OFDM
P_{avg} (dBm)	22.6	21.3	22.8	22.9	18.2	15.3	5.0	19.1
Average Effi. (%)	33.9 (DE)	32.1 (DE)	31.4 (DE)	26.1 (PAE)	23.7 (DE)	24.7 (DE)	–	30.3 (DE)
EVM (dB)	−26.3	−35.0	−24.7	−25.3	−32.1	−32.0	−26.0	−41.7
Pre-distortion	No		Yes	Yes	Yes	Yes	No	No
Chip Size (mm^2)	1.93 (0.76**)		7.2	1.11	3.24	6	0.45**	3.36

* 3 dB bandwidth. ** Core Size. # 1 dB bandwidth. ## ACW = 64–to–511. $^{\$}$ Normalized code = 0.22–to–1 in Fig. 25(b).

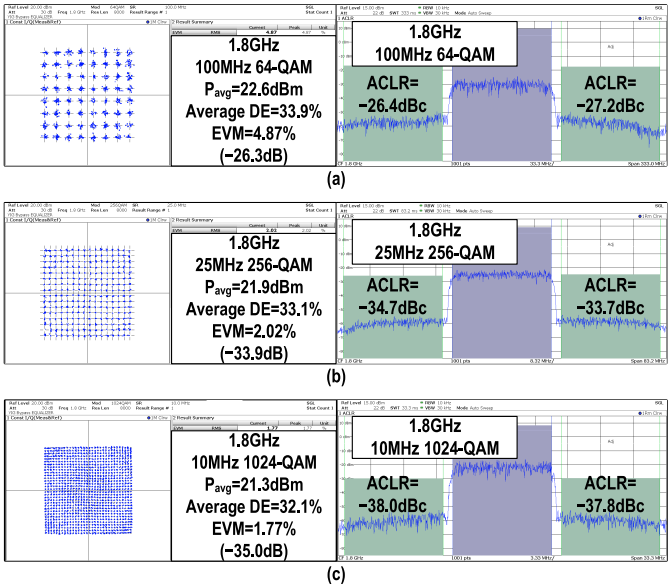

Fig. 29. Measured output spectrum and constellation of (a) 100-MHz 64-QAM, (b) 25-MHz 256-QAM, and (c) 10-MHz 1024-QAM signals.

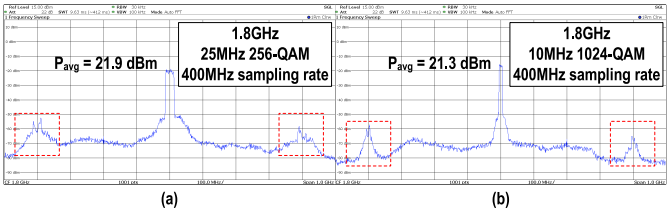

Fig. 30. Measured OOB spectrum of (a) 25-MHz 256-QAM and (b) 10-MHz 1024-QAM signals.

by the parasitic of interconnection among unit cells of sub-digital PA array. The proposed digital PA achieves the peak DE of 40.1% at 5.2-dB PBO, which shows the DE improvement of 1.59× compared with the normalized Class-B PA.

Based on the good linearity in CW measurements, the proposed self-calibration SCPA supports 100-MHz 64-QAM, 25-MHz 256-QAM, and 10-MHz 1024-QAM signals without any pre-distortion. The modulation measurements at 1.8 GHz are shown in Fig. 29, which include the average output power (P_{avg}), average DE, EVM, and adjacent channel leakage ratio (ACLR). For 100-MHz 64-QAM signal, the proposed SCPA achieves 22.6-dBm P_{avg}, 33.9% average DE, 4.87% EVM (−26.3 dB), and ACLR ≤ −26.4 dBc. The measured 25-MHz 256-QAM signal shows 21.9-dBm P_{avg}, 33.1% average DE, 2.02% EVM (−33.9 dB), and ACLR ≤ −33.7 dBc. Besides, the 10-MHz 1024-QAM signal is also supported by the proposed SCPA, which features 21.3-dBm P_{avg}, 32.1% average DE, 1.77% EVM (−35.0 dB), and ACLR ≤ −37.8 dBc. Fig. 30(a) and (b) shows the out-of-band (OOB) spectra of 25-MHz 256-QAM and 10-MHz 1024-QAM signals. Spectrum images exist due to the 400-MHz sampling rate of baseband signal [51]. Since the RF signals are generated from digital baseband signals based on zero-order hold (ZOH) interpolations, the spectral images are introduced at integer multiples of the sampling frequency, which worsen the OOB spectrum noise floor [52]. The higher sampling frequency (i.e., oversampling) can move the images to a higher offset and greatly attenuates the spectral images [34]. Besides, the first-order hold (FOH) interpolation can be adopted in DPA design to suppress spectral images [51]. The far-out spectrum of CW signal of 1.8 GHz is measured and shown in Fig. 31. The proposed DPA operating at 1.8 GHz shows −41.9-dBc suppression for the second harmonic and −28.9-dBc suppression for the third harmonics.

The measured performance of the proposed SCPA is summarized and compared with the state-of-the-art digital polar PAs in Table. I. The proposed self-calibration SCPA achieves 28.9-dBm peak P_{out}, 43.9% peak DE, 37.2% peak PAE, and 4.4° AM–PM distortion. Besides, the proposed SCPA exhibits higher average efficiency with larger data rate and more than twice modulation bandwidth compared to the counterparts. Moreover, without any pre-distortion, the SCPA supports complex modulation signals, such as 100-MHz 64-QAM, 25-MHz 256-QAM, and 10-MHz 1024-QAM sig-

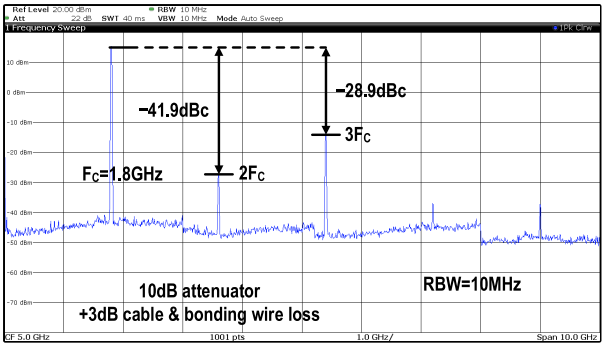

Fig. 31. Measured far-out spectrum.

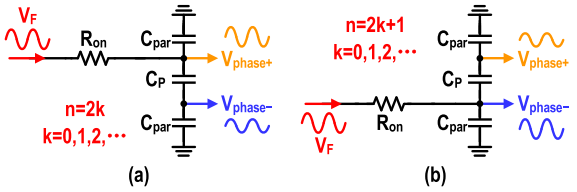

Fig. 32. Equivalent circuit of phase detector at (a) $n = 2k,\ k = 0, 1, 2, \ldots,$ and (b) $n = 2k + 1, k = 0, 1, 2, \ldots$.

nals. The non-linearity, including AM-AM and AM-PM distortions, leads to EVM degradation and limits the maximal modulation bandwidth of high QAM signals.

V. Conclusion

In this article, a prototype of self-calibration SCPA is presented with SCA for high data-rate signals. The self-calibration technique is proposed to compensate the AM–PM distortion of digital polar PAs. The SCA is introduced to decrease calibration response time to support high data-rate signals. The measurements demonstrate 28.9-dBm peak PA output power at 1.8 GHz, 43.9% peak PA DE, and 4.4° AM–PM distortion. The modulation tests with 100-MHz 64-QAM, 25-MHz 256-QAM, and 10-MHz 1024-QAM signals exhibit high linearity with the proposed self-calibration technique without any pre-distortion.

Appendix

A. Detailed Derivation of Phase Detection

The equivalent circuit of the phase detector is shown in Fig. 32, which has two states at different periods of Ref and $\overline{\text{Ref}}$. Suppose that the period time is expressed as $n\pi + \omega t$, $n = 0, 1, 2, \ldots, 0 \le \omega t \le \pi$. It is assumed that when $n = 2k, k = 0, 1, 2, \ldots,$ Ref is logic high. Oppositely, when $n = 2k + 1, k = 0, 1, 2, \ldots,$ $\overline{\text{Ref}}$ turns to logic high. Thus, the feedback signal V_{F} is fed to two-port alternatively and charges the RC circuit, which is comprised of R_{ON}, C_P, and C_{par}. Due to the voltage division of series capacitors, this charging generates a voltage difference V_{phase}, which is varying following V_{F}. Note that the variation of V_{phase} is increasing periodically because of the periodic switching. Meanwhile, the stable V_{phase} is related to the phase difference between V_{F} and switch signals of TGs.

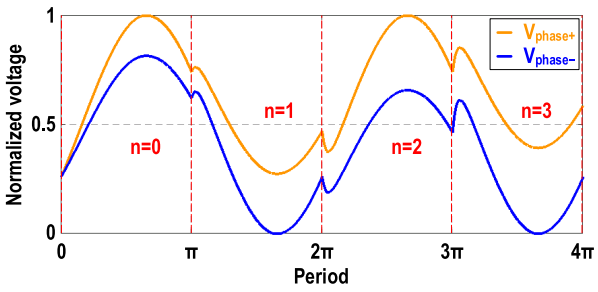

Fig. 33. Voltage variation of phase detection process.

At first, the feedback signal V_{F} is assumed as

$$V_{\text{F}}(\omega t) = V_{\text{dc}} + V_{\text{ac}} \sin(n\pi + \omega t + \theta_{\text{AM–PM}}) \tag{10}$$

where V_{dc} and V_{ac} are the component and the amplitude of ac component, respectively. $n\pi + \omega t$ varies from 0 to ∞. $\theta_{\text{AM–PM}}$ is composed of a fixed phase difference between V_{F} and control signals and the AM–PM distortion. Note that PMs are canceled because the reference signals are also phase modulated. For the two states, the circuits are both RC circuits with the same ON-resistance and effective capacitance. Thus, the voltage at output net of RC circuit is set as V_{ON} and the output net of series capacitors is set as V_{OFF}, respectively. They are calculated as

$$\begin{aligned} V_{\text{ON}} &= V_{\text{ac}} \frac{\frac{1}{j\omega C_{\text{e}}}}{R_{\text{ON}} + \frac{1}{j\omega C_{\text{e}}}} \\ &= G_{\text{C}} V_{\text{ac}} e^{-j\theta_{RC}} \end{aligned} \tag{11}$$

$$V_{\text{OFF}} = \gamma_C V_{\text{ON}} \tag{12}$$

where

$$G_C = \frac{1}{\sqrt{1 + (\omega R_{\text{ON}} C_{\text{e}})^2}} \tag{13}$$

$$\theta_{RC} = \tan^{-1}(\omega R_{\text{ON}} C_{\text{e}}) \tag{14}$$

$$C_{\text{e}} = C_{\text{par}} + \frac{C_{\text{par}} C_P}{C_{\text{par}} + C_P} \tag{15}$$

With continuous switching, $V_{\text{phase+}}$ and $V_{\text{phase–}}$ change between V_{on} and V_{off} alternatively. Based on these conditions, the phase detection process is analyzed as follows. Fig. 33 shows the variation of $V_{\text{phase+}}$ and $V_{\text{phase–}}$ when n varies from 0 to 3.

At the beginning, at $n = 0,\ \omega t = 0$, it is assumed that the voltage difference between $V_{\text{phase+}}$ and $V_{\text{phase–}}$ is 0, i.e., $V_{\text{phase+}} = V_{\text{phase–}} = V_{\text{dc}} + V_{\text{ON}} \sin(\theta_{\text{AM–PM}})$ During $n = 0$, $0<\omega t<\pi$, the voltages at net $V_{\text{phase+}}$ and $V_{\text{phase–}}$ are set as $V_{\text{phase+,0}}(\omega t)$ and $V_{\text{phase–,0}}(\omega t)$, respectively. Thus, they are calculated as

$$V_{\text{phase+,0}}(\omega t) = V_{\text{dc}} + V_{\text{ON}} \sin(\omega t + \theta_{\text{AM–PM}}) \tag{16}$$

$$\begin{aligned} V_{\text{phase–,0}}(\omega t) = {} & V_{\text{dc}} + (1 - \gamma_C) V_{\text{ON}} \sin(\theta_{\text{AM–PM}}) \\ & + \gamma_C V_{\text{ON}} \sin(\omega t + \theta_{\text{AM–PM}}) \end{aligned} \tag{17}$$

and the voltage difference is set as $\Delta V_{\text{phase},0}(\omega t)$, which is derived as

$$\begin{aligned}\Delta V_{\text{phase},0}(\omega t) =\ & V_{\text{phase+0}}(\omega t) - V_{\text{phase–0}}(\omega t) \\ =\ & -(1-\gamma_C)V_{\text{ON}}\sin(\theta_{\text{AM–PM}}) \\ & +(1-\gamma_C)V_{\text{ON}}\sin(\omega t+\theta_{\text{AM–PM}}) \end{aligned} \tag{18}$$

This voltage difference is stored in C_P, which leads to a charging process after switching TGs. When $n = 1$, the connection between $V_{\text{phase}\pm}$ and $V_{\text{ON/OFF}}$ is switched. Then, the voltages at net $V_{\text{phase+}}$ and $V_{\text{phase–}}$ are set as $V_{\text{phase+},1}(\omega t)$ and $V_{\text{phase–},1}(\omega t)$, which are derived as

$$\begin{aligned} V_{\text{phase+1}}(\omega t) =\ & V_{\text{phase+0}}(\pi) - \gamma_C V_{\text{ON}}\sin(\pi+\theta_{\text{AM–PM}}) \\ & + \gamma_C V_{\text{ON}}\sin(\pi+\omega t+\theta_{\text{AM–PM}}) \\ & + \gamma_C \Delta V_{\text{phase},0}(\pi)(1-e^{-\frac{t}{R_{\text{ON}}C_e}}) \end{aligned} \tag{19}$$

$$\begin{aligned} V_{\text{phase–1}}(\omega t) =\ & V_{\text{phase–0}}(\pi) - V_{\text{ON}}\sin(\pi+\theta_{\text{AM–PM}}) \\ & + V_{\text{ON}}\sin(\pi+\omega t+\theta_{\text{AM–PM}}) \\ & + \Delta V_{\text{phase},0}(\pi)(1-e^{-\frac{t}{R_{\text{ON}}C_e}}) \end{aligned} \tag{20}$$

and $\Delta V_{\text{phase},1}(\omega t)$ is derived as

$$\begin{aligned}\Delta V_{\text{phase},1}(\omega t) =\ & V_{\text{phase+1}}(\omega t) - V_{\text{phase–1}}(\omega t) \\ =\ & \Delta V_{\text{phase},0}(\pi) + (1-\gamma_C)V_{\text{ON}}\sin(\pi+\theta_{\text{AM–PM}}) \\ & -(1-\gamma_C)V_{\text{ON}}\sin(\pi+\omega t+\theta_{\text{AM–PM}}) \\ & -(1-\gamma_C)\Delta V_{\text{phase},0}(\pi)(1-e^{-\frac{t}{R_{\text{ON}}C_e}}) \end{aligned} \tag{21}$$

At $n = 2$, these voltages are updated as

$$\begin{aligned} V_{\text{phase+2}}(\omega t) =\ & V_{\text{phase+1}}(\pi) - V_{\text{ON}}\sin(2\pi+\theta_{\text{AM–PM}}) \\ & + V_{\text{ON}}\sin(2\pi+\omega t+\theta_{\text{AM–PM}}) \\ & - \Delta V_{\text{phase},1}(\pi)(1-e^{-\frac{t}{R_{\text{ON}}C_e}}) \end{aligned} \tag{22}$$

$$\begin{aligned} V_{\text{phase–2}}(\omega t) =\ & V_{\text{phase–1}}(\pi) - \gamma_C V_{\text{ON}}\sin(2\pi+\theta_{\text{AM–PM}}) \\ & + \gamma_C V_{\text{ON}}\sin(2\pi+\omega t+\theta_{\text{AM–PM}}) \\ & - \gamma_C \Delta V_{\text{phase},1}(\pi)(1-e^{-\frac{t}{R_{\text{ON}}C_e}}) \end{aligned} \tag{23}$$

$$\begin{aligned}\Delta V_{\text{phase},2}(\omega t) =\ & V_{\text{phase+2}}(\omega t) - V_{\text{phase–2}}(\omega t) \\ =\ & \Delta V_{\text{phase},1}(\pi) - (1-\gamma_C)V_{\text{ON}}\sin(2\pi+\theta_{\text{AM–PM}}) \\ & + (1-\gamma_C)V_{\text{ON}}\sin(2\pi+\omega t+\theta_{\text{AM–PM}}) \\ & - (1-\gamma_C)\Delta V_{\text{phase},1}(\pi)(1-e^{-\frac{t}{R_{\text{ON}}C_e}}) \end{aligned} \tag{24}$$

At $n = 3$, these voltages are updated as

$$\begin{aligned} V_{\text{phase+3}}(\omega t) =\ & V_{\text{phase+2}}(\pi) - \gamma_C V_{\text{ON}}\sin(3\pi+\gamma_C\theta_{\text{AM–PM}}) \\ & + \gamma_C V_{\text{ON}}\sin(3\pi+\omega t+\theta_{\text{AM–PM}}) \\ & + \gamma_C \Delta V_{\text{phase},2}(\pi)(1-e^{-\frac{t}{R_{\text{ON}}C_e}}) \end{aligned} \tag{25}$$

$$\begin{aligned} V_{\text{phase–3}}(\omega t) =\ & V_{\text{phase–2}}(\pi) - V_{\text{ON}}\sin(3\pi+\theta_{\text{AM–PM}}) \\ & + V_{\text{ON}}\sin(3\pi+\omega t+\theta_{\text{AM–PM}}) \\ & + \Delta V_{\text{phase},2}(\pi)(1-e^{-\frac{t}{R_{\text{ON}}C_e}}) \end{aligned} \tag{26}$$

$$\begin{aligned}\Delta V_{\text{phase},3}(\omega t) =\ & V_{\text{phase+3}}(\omega t) - V_{\text{phase–3}}(\omega t) \\ =\ & \Delta V_{\text{phase},2}(\pi) + (1-\gamma_C)V_{\text{ON}}\sin(3\pi+\theta_{\text{AM–PM}}) \\ & - (1-\gamma_C)V_{\text{ON}}\sin(3\pi+\omega t+\theta_{\text{AM–PM}}) \\ & - (1-\gamma_C)\Delta V_{\text{phase},2}(\pi)(1-e^{-\frac{t}{R_{\text{ON}}C_e}}) \end{aligned} \tag{27}$$

The formula of (25), (26), (27) is similar to (19), (20), (21), respectively. It is predictable that this similarity exists in all the following formulas. Thus, assuming these voltages are periodic, $\Delta V_{\text{phase,n}}(\omega t)$ and $\Delta V_{\text{phase,n+1}}(\omega t)$ at $n = 2k$, i.e., $k \to \infty$ are derived as

$$\begin{aligned} \Delta V_{\text{phase,n}}(\omega t) =\ & \Delta V_{\text{phase,n-1}}(\pi) \\ & - (1-\gamma_C)V_{\text{ON}}\sin(n\pi+\theta_{\text{AM–PM}}) \\ & + (1-\gamma_C)V_{\text{ON}}\sin(n\pi+\omega t+\theta_{\text{AM–PM}}) \\ & - (1-\gamma_C)\Delta V_{\text{phase,n-1}}(\pi)(1-e^{-\frac{t}{R_{\text{ON}}C_e}}) \end{aligned} \tag{28}$$

$$\begin{aligned} \Delta V_{\text{phase,n+1}}(\omega t) =\ & \Delta V_{\text{phase,n}}(\pi) \\ & + (1-\gamma_C)V_{\text{ON}}\sin[(n+1)\pi+\theta_{\text{AM–PM}}] \\ & - (1-\gamma_C)V_{\text{ON}}\sin[(n+1)\pi+\omega t+\theta_{\text{AM–PM}}] \\ & - (1-\gamma_C)\Delta V_{\text{phase,n}}(\pi)(1-e^{-\frac{t}{R_{\text{ON}}C_e}}) \end{aligned} \tag{29}$$

With the periodic condition of 2π, there is

$$\Delta V_{\text{phase,n-1}}(\pi) = \Delta V_{\text{phase,n+1}}(\pi) \tag{30}$$

Based on the difference between (28) and (29), $\Delta V_{\text{phase,n}}(\pi)$ is derived under the condition of (30), which is expressed as

$$\begin{aligned}\Delta V_{\text{phase,n}}(\pi) =\ & \Delta V_{\text{phase,n+1}}(\pi) \\ =\ & -\frac{2V_{\text{ON}}\sin(\theta_{\text{AM–PM}})}{1-e^{-\frac{\pi/\omega}{R_{\text{ON}}C_e}}} \\ \approx\ & -2V_{\text{ON}}\sin(\theta_{\text{AM–PM}}) \end{aligned} \tag{31}$$

This approximate is reliable when the product $(R_{\text{ON}}C_e)$ is small enough to finish the charging process in $0 \sim (\pi/\omega)$. Thus, $\Delta V_{\text{phase,n}}(\omega t)$ is expressed as

$$\begin{aligned}\Delta V_{\text{phase,n}}(\omega t) =\ & \Delta V_{\text{phase,n+1}}(\omega t) \\ =\ & -(1+\gamma_C)V_{\text{ON}}\sin(\theta_{\text{AM–PM}}) \\ & +(1-\gamma_C)V_{\text{ON}}\sin(\omega t+\theta_{\text{AM–PM}}) \\ & -2(1-\gamma_C)V_{\text{ON}}\sin(\theta_{\text{AM–PM}})e^{-\frac{t}{R_{\text{ON}}C_e}} \end{aligned} \tag{32}$$

Moreover, V_{ON} introduces additional phase shifting in phase detection, i.e., θ_{RC}. Therefore, the final format of $\Delta V_{\text{phase}}(\omega t)$ is derived as

$$\begin{aligned}\Delta V_{\text{phase,n}}(\omega t) =\ & -(1+\gamma_C)G_C V_{\text{ac}}\sin(\theta_{\text{AM–PM}}-\theta_{RC}) \\ & +(1-\gamma_C)G_C V_{\text{ac}}\sin(\omega t+\theta_{\text{AM–PM}}-\theta_{RC}) \\ & -2(1-\gamma_C)G_C V_{\text{ac}}\sin(\theta_{\text{AM–PM}}-\theta_{RC})e^{-\frac{t}{R_{\text{ON}}C_e}} \end{aligned} \tag{33}$$

where $-(1+\gamma_C)G_C V_{\text{ac}}\sin(\theta_{\text{AM–PM}}-\theta_{RC})$ is the converted dc component $V_{\text{phase, dc}}$. The latter two components form the $V_{\text{phase, non-dc}}$, which affects the stability of phase compensation. Due to $0<\gamma_C<1$, the swings of the latter two components in (33) are smaller than the converted dc voltage. According to (2), γ_C is influenced by C_P and C_{par}. Thus, the capacitance of C_P and dimensions of switches should be chosen carefully.

B. Analysis of Phase Detector Versus Frequency

The measured results show that the calibrated performance changes across frequency, which is caused by the phase detector. The schematic of the phase detector and driver is shown in Fig. 34(a). Here, Ref is the differential rail-to-rail

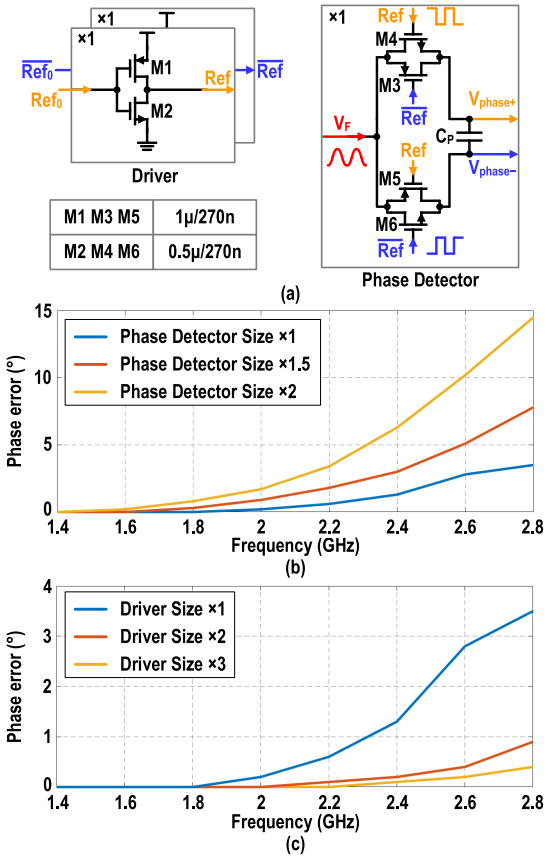

Fig. 34. (a) Schematic of the phase detector and driver. Simulated effect of transistor sizes of (b) phase detector and (c) driver on phase detection error.

square waveform signal, which controls the switches between ON- and OFF-state through the driver cells. The increasing parasitic of phased detector at higher frequency reduces the switching speed and deteriorates the phase detection accuracy. The simulated maximal phase detection error versus frequency is shown in Fig. 34(b) and (c). The phases of V_F in the range of 0°–360° are simulated with a step of 10° to obtain the maximal phase detection error. Fig. 34(b) and (c) shows the effect of transistor sizes of phase detector and driver on phase detection error, respectively. To extend the operation bandwidth (i.e., to reduce phase detection error at higher frequency), minimized transistor size of phase detector and larger driver cells are needed.

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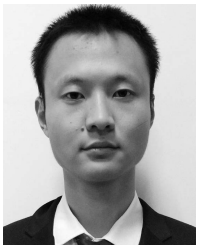

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Dr. Luo is a Technical Program Committee Member of multiple IEEE conferences, including the IEEE Custom Integrated Circuits Conference (CICC) and the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. He is also the IEEE MTT-Society Technical Committee Member of MTT-4 on Microwave Passive Components and Transmission Line Structures, MTT-5 on Filters, and MTT-23 on Wireless Communications. He was bestowed by China as the China Overseas Chinese Contribution Award in 2016 and was selected by the IEEE MTT-Society as the IEEE Outstanding Young Engineer Award in 2022. He was a recipient of the Center for ASIS of UESTC Outstanding Team for Teaching and Education Award in 2021 and the UESTC Excellent Team for Postgraduate Supervision Award in 2021. He also won the UESTC Distinguished Innovation and Teaching Award in 2018 and the UESTC Outstanding Undergraduate Teaching Promotion Award in 2016. His Research Group BEAM X-Laboratory received multiple best paper awards and design competition awards, including the IEEE RFIC Best Student Paper Award in 2021, the IEEE RFIT Best Student Paper Award in 2016 and 2019, the IEEE IWS Best Student Paper Award in 2015 and 2018, the IEEE IMS Student Design Competition Award from 2017 to 2019, the IEEE IMS Sixty-Second Presentation Competition Award in 2019, and multiple best paper award finalists from the IEEE conferences. He was the TPC Co-Chair of the IEEE IWS in 2018 and the IEEE RFIT in 2019. He is the Vice-Chair of the IEEE MTT-Society Chengdu Chapter. He serves as an Associate Editor for *IET Microwaves, Antennas and Propagation*. He was a Track Editor of IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS from 2018 to 2021.