Guest Editorial Introduction to the Special Issue on the 2022 Symposium on VLSI Circuits

This Special Issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS highlights some of the outstanding circuits papers presented at the Symposium on VLSI Technology and Circuits. The Symposium was held in person, June 13–17, 2022, in Honolulu, Hawaii, followed by virtual Q&A sessions from June 20 to 22.

After 35 years of existence as two co-located conferences, the Symposium on VLSI Technology and the Symposium on VLSI Circuits have merged into one Symposium on VLSI Technology and Circuits. The new Symposium is jointly sponsored by the IEEE Solid-State Circuits and Electron Devices Societies and the Japan Society of Applied Physics in cooperation with the Institute of Electronics, Information, and Communications Engineers. Merging of the two Symposia was a natural progression of increased overlaps in the program schedules and growing intersections between the technical areas covered by two different technical program committees. The Symposium still maintains two technical program committees that focus on technology and circuits submissions, but also jointly reviews the papers with overlapping interests.

The 2022 Symposium was the first major Solid-State Circuits Society event held in person since the start of the COVID-19 pandemic; 660 participants attended in person, and 710 joined virtually, resulting in the total registration count of 1370 being near an all-time high. While the in-person participants very much enjoyed meeting again in Hawaii after 4 years, the virtual participants were able to take part in a rich program consisting of recorded presentations, a virtual platform for interaction, and live Q&A sessions, which were held the week after the live conference. The in-person attendees had an opportunity to participate in the demonstration session, which was integrated into the reception. The live panel sessions featured spirited discussions between the panelists and the audience.

The 2022 VLSI Symposium on Technology and Circuits received 332 circuits submissions and 217 technology submissions. In addition, 31 papers were jointly reviewed by the Technology and Circuits TPCs. The program committees selected 188 papers for presentation, and 83% of the authors were able to travel to the conference and present live. Every presentation was also pre-recorded, for the benefit of both virtual and in-person audiences. The circuits sessions included processors, SoCs, machine learning accelerators, digital circuits, memories, power conversion circuits, biomedical circuits, analog amplifiers and filters, data converters, sensors and displays, wireless and wireline communications, frequency generation, and clock circuits. This issue of the journal contains 21 outstanding circuits papers selected as highlights of presentations from the 2022 Symposium. The journal articles describe the research work presented at the 2022 Symposium in greater detail than the papers provided in the Symposium digest. The papers were subject to the standard journal review process. We enjoyed working with the authors of these articles and hope that the technical details presented in these articles will be interesting and useful to the readers of the journal. The following is a summary of the contents of this Special Issue.

The first article in this issue presents a 39-GHz CMOS bi-directional Doherty phased-array beamformer for cellular 5G base stations, by Li [A1] from the Tokyo Institute of Technology. A bi-directional PA-LNA is implemented in 65nm CMOS to enhance the power back-off (PBO) efficiency with high peak-to-average power ratio in 5G signals. The digital pre-distortion is addressed through an inter-element mismatch compensation technique. In [A2], Lee et al., from the University of Michigan, present a high-voltage generation chip designed for the electrostatic actuation of micro-robots that produces a differential voltage of 103 V from the 3.6-V battery. In the next article [A3], Yang et al., from imec, present a miniature 128-channel neural recording integrated circuit for the simultaneous acquisition of local field and action potentials in neural recording interfaces. It was implemented as an ac-coupled first-order digitally intensive Δ–$\Delta\Sigma$ architecture in 22-nm FDSOI technology.

The following four articles cover the area of analog-to-digital conversion, which is often well-represented at the Symposia on VLSI. In [A4], Peng et al., from the University of Michigan, introduce a time-interleaved architecture in a third-order continuous-time $\Delta\Sigma$ modulator that relaxes the speed-resolution bottleneck of the noise-shaping successive-approximation-register (SAR) quantizer, implemented through 28-nm technology. In [A5], Li et al., from the Eindhoven University of Technology, present an innovation in a first-order continuous-time noise-shaping SAR analog-to-digital converter (ADC). This ADC utilizes a continuous-time Gm-C integrator to realize an inherent anti-aliasing function and removes the sampling switch in the SAR ADC. In [A6], Yoon et al., from Yonsei University, introduce a capacitively degenerated dynamic amplifier as the residue amplifier in the low-power pipelined SAR ADC. It is implemented in an ADC that achieves 65-dB SNDR at a sampling rate of 50 MS/s, while consuming 0.46 mW. In [A7], Whitcombe et al., from

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Intel Labs, present a hybrid time- and voltage-domain ADC that uses a single high-speed voltage-to-time converter as a high-bandwidth sampling buffer for a four-way time-interleaved SAR ADC. A prototype fabricated in 22-nm FinFET CMOS provides 13-GHz ERBW and consumes 6.0 mW with a Nyquist SNDR of 38 dB at 3.8 GS/s, for 24.4 fJ/step Walden FoM.

In [A8], Hatakeyama et al., from Toppan, demonstrate a new indirect time of flight sensor realizing long-range measurement of 30 m by a hybrid ToF (hToF) operation, which uses multiple time windows prepared by multi-tap pixels and range-shifted subframes. The VGA-resolution hToF image sensor can measure the depth up to 30 m for indoor operation and 20 m for outdoor operation under high ambient light of 100 klux.

An on-chip jitter/phase noise measurement circuit that is reference-free and self-calibrated in situ in the background is presented in [A9], by Jian and Chen, from National Yang Ming Chiao Tung University. The signal bandwidth of the $\Delta\Sigma$ time to digital converters ranges from 100 kHz to 3.125 MHz, and the measured errors are less than 1 dB by a single-tone phase modulation test across the frequency range.

Gong et al. [A10], from the Georgia Institute of Technology, present a direct 48–1 V dc–dc point-of-load converter for efficient high-voltage conversion. By combining a three-level buck converter with a hybrid Dickson converter, the proposed topology shows 10× reduced switching voltages with only five off-chip flying capacitors. The converter achieves a maximum load capacity of 12 A and a measured peak efficiency of 90.4% at 48–1 V conversion.

Zhang and Niknejad [A11], from the University of California at Berkeley, present a galvanically coupled electron paramagnetic spectrometer (GalEPR) for deep tissue oximetry and hypoxia diagnosis. A 30-MHz clock is galvanically coupled through the body to minimize attenuation and up-converted to 14 GHz by a low-power subsampling PLL. The proposed GalEPR spectrometer demonstrates 14 GHz/50 mm frequency/depth (10× better) with an in vitro hypoxia detection experiment.

Ray and Kinget [A12], from Columbia University, propose two time-mode analog signal processing circuit techniques showcased in an analog audio feature extractor chip that advances the state of the art in power- and area efficiency. Time-mode analog filter-bank interpolation uses digital XOR gates to double the number of outputs of an analog bandpass filter bank. Time-mode analog rectification uses a single digital XOR gate as an analog full-wave rectifier. The 65-nm LP CMOS chip uses only 80 nW and 0.53 mm^2 to extract from an input analog audio signal, an output digital auditory feature vector with 31 elements.

Ryu et al. [A13], from Samsung Electronics, propose practical design techniques to enhance the performance and reliability of 1024 GB/s High Bandwidth Memory-3 (HBM3). Effective data-bus design methods are applied to transfer data from a multi-bank to a data-bus. A symbol-based on-die ECC and parallelized data-bus inversion are implemented. A 16-GB HBM3 fabricated in the third generation of the 10-nm class DRAM process achieves a bandwidth of up to 1024 GB/s and provides stable operation at a high temperature while improving an error detection rate by 92.2%.

An energy-efficient high bandwidth array design using 0.0300-μm2 high-performance SRAM bitcell on Intel 4 CMOS technology is presented by Wang et al., from Intel [A20]. By employing a unique combination of design techniques such as column mux of 1, flying BL, passive write assist scheme, and energy-efficient column design, the proposed 6T SRAM array design demonstrates >80% access energy improvement over a conventional four-way interleaved 6T SRAM array design and 30% macro density improvement compared to a hierarchical bitline 8T SRAM design for high bandwidth memory applications.

Kim et al. [A14], from Intel Labs, present an SRAM-based compute-in-memory module, implemented in the Intel 22FFL process. By introducing a C-2C capacitor ladder-based charge domain computing scheme, the proposed CiM prototype chip demonstrates a maximum of 2000 multiply-accumulation (MAC) operations in one clock cycle and achieves 32.2 TOPS/W peak power efficiency with 8-bit precision.

A pair of wireline high-speed link papers follow in this Special Issue. Nishi et al. [A15], from NVIDIA, present a clock-forwarded, inverter-based short-reach simultaneous bidirectional (ISR-SBD) PHY targeted for die-to-die communication over silicon interposers to support larger systems built with chiplets. The prototype is fabricated in a 5-nm standard CMOS process and demonstrates 50.4 Gb/s/wire (25.2 Gb/s each direction) datarate over 1.2 mm on-chip channel. In the second wireline paper, Dickson et al. [A16], from IBM T. J. Watson Research Center, present a 72-GS/s, 8-bit DAC-based source-series terminated transmitter in a 4-nm process. Time-domain modulation of 216 Gb/s using PAM8 and frequency-domain modulation of 212 Gb/s OFDM are reported.

CNN-based data detection channel for hard disk drives (HDD) is implemented on an ASIC by Qin et al. [A17], from Carnegie-Mellon University. The chip demonstrates a 30.3% error rate reduction over the state-of-the-art HDD detection channel with the displaced multi-reader setting. The work incorporates a full-scale co-optimization flow between the ML algorithms and customized hardware design for achieving superior detection accuracy, high-throughput sequential detections, and improved power efficiency at the same time.

Kumar et al. [A21], from Intel Labs, present a multiplicative-masked AES-128/256 engine with measured side-channel resistance to correlation power and electromagnetic (EM) attacks implemented in Intel 4 CMOS process. Chen et al. [A18], present an experimental 8-core 64-b RISC-V processor which performs multiply-accumulate functions near the second-level cache. A test chip is implemented in Intel 4 process, operates at 1.15GHz, and has been demonstrated to accelerate machine learning workloads.

Keller et al. [A19], from NVIDIA, present a deep neural network (DNN) accelerator designed for the efficient execution of transformers. The proposed accelerator implements

per-vector scaled quantization (VSQ), which employs an independent scale factor for each 64-element vector. The 5-nm prototype achieves 95.6 TOPS/W at 0.46 V on a 4-bit benchmarking layer with VSQ. At a nominal voltage of 0.67 V, the accelerator achieves 1734 inferences/s/W (38.7TOPS/W) with only 0.7% accuracy loss on BERT-Base and 4714 inferences/s/W (38.6 TOPS/W) with 0.15% accuracy loss on ResNet-50 using quantization-aware fine-tuning to recover accuracy, demonstrating a practical accelerator design for energy-efficient DNN inference.

The 2023 Symposium on VLSI Technology and Circuits will return to Kyoto, Japan, and will be held on June 11–16. The conference format will return to in-person after four years. The Symposium will start with Sunday workshops, followed by Monday short courses and the main conference on Tuesday, Wednesday, and Thursday. The symposium will be concluded with the Friday Forum. We will certainly see the most advanced achievements in VLSI technology and circuits and we hope that you will join us as well.

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APPENDIX: RELATED ARTICLES

[A1] Z. Li, "A 39-GHz CMOS bi-directional Doherty phased-array beamformer using shared-LUT DPD with inter-element mismatch compensation technique for 5G base-station," *IEEE J. Solid-State Circuits*, early access, Jan. 4, 2023, doi: 10.1109/JSSC.2022.3232137.

[A2] S. Lee, T. Kang, S. Song, K. Kwon, and M. P. Flynn, "An 81.6 dB SNDR 15.625 MHz BW third-order CT SDM with a true time-interleaving noise-shaping quantizer," *IEEE J. Solid-State Circuits*, early access, Dec. 23, 2022, doi: 10.1109/JSSC.2022.3228760.

[A3] X. Yang et al., "An AC-coupled 1st-order Δ-$\Delta\Sigma$ readout IC for area-efficient neural signal acquisition," *IEEE J. Solid-State Circuits*, early access, Jan. 16, 2023, doi: 10.1109/JSSC.2023.3234612.

[A4] Y. Peng et al., "A high-voltage generator and multiplexer for electrostatic actuation in programmable matter," *IEEE J. Solid-State Circuits*, early access, Dec. 30, 2022, doi: 10.1109/JSSC.2022.3230927.

[A5] H. Li, Y. Shen, E. Cantatore, and P. Harpe, "A 77.3-dB SNDR 62.5-kHz bandwidth continuous-time noise-shaping SAR ADC with duty-cycled Gm-C integrator," *IEEE J. Solid-State Circuits*, early access, Dec. 16, 2022, doi: 10.1109/JSSC.2022.3227678.

[A6] H. Yoon, C. Lee, T. Kim, Y. Kwon, and Y. Chae, "A 65-dB-SNDR pipelined SAR ADC using PVT-robust capacitively degenerated dynamic amplifier," *IEEE J. Solid-State Circuits*, early access, Jan. 18, 2023, doi: 10.1109/JSSC.2023.3235521.

[A7] A. Whitcombe et al., "A VTC/TDC-assisted 4 $\times$ interleaved 3.8 GS/s 7 b 6.0 mW SAR ADC with 13 GHz ERBW," *IEEE J. Solid-State Circuits*, early access, Jan. 2, 2023, doi: 10.1109/JSSC.2022.3231783.

[A8] K. Hatakeyama et al., "A hybrid ToF image sensor for long-range 3D depth measurement under high ambient light conditions," *IEEE J. Solid-State Circuits*, early access, 2023, doi: 10.1109/JSSC.2023.3238031.

[A9] W. J. Jian and W. Z. Chen, "A reference-free phase noise measurement circuit achieving 24.2-fs periodic jitter sensitivity and 275-fs_{rms} resolution with background self-calibration," *IEEE J. Solid-State Circuits*, early access, Dec. 15, 2022, doi: 10.1109/JSSC.2022.3226167.

[A10] M. Gong, X. Zhang, and A. Raychowdhury, "A 90.4% peak efficiency 48 V/1V three-level hybrid Dickson converter with gradient descent run-time optimizer and GaN/Si hybrid conversion," *IEEE J. Solid-State Circuits*, early access, Dec. 20, 2022, doi: 10.1109/JSSC.2022.3228233.

[A11] L. Zhang and A. M. Niknejad, "GalEPR: A galvanically coupled electron paramagnetic resonance spectrometer for deep tissue hypoxia diagnosis," *IEEE J. Solid-State Circuits*, early access, Feb. 1, 2023, doi: 10.1109/JSSC.2023.3239406.

[A12] S. Ray and P. R. Kinget, "Ultra-low-power and compact-area analog audio feature extraction based on time-mode analog filterbank interpolation and time-mode analog rectification," *IEEE J. Solid-State Circuits*, early access, Dec. 22, 2022, doi: 10.1109/JSSC.2022.3227246.

[A13] Y. Ryu et al., "A 16 GB 1024 GB/s HBM3 DRAM with source-synchronized bus design and on-die error control scheme for enhanced RAS features," *IEEE J. Solid-State Circuits*, early access, Jan. 4, 2023, doi: 10.1109/JSSC.2022.3232096.

[A14] Y. Kim et al., "Energy-efficient high bandwidth 6 T SRAM design on Intel 4 CMOS technology," *IEEE J. Solid-State Circuits*, early access, Dec. 28, 2022, doi: 10.1109/JSSC.2022.3230046.

[A15] Y. Nishi et al., "A 0.297-pJ/bit 50.4-Gb/s/wire inverter-based short-reach simultaneous bi-directional transceiver for die-to-die interface in 5-nm CMOS," *IEEE J. Solid-State Circuits*, early access, Jan. 9, 2023, doi: 10.1109/JSSC.2022.3232024.

[A16] T. O. Dickson et al., "A 72-GS/s, 8-bit DAC-based wireline transmitter in 4-nm FinFET CMOS for 200 + Gb/s serial links," *IEEE J. Solid-State Circuits*, early access, Dec. 23, 2022, doi: 10.1109/JSSC.2022.3228632.

[A17] Y. Qin, R. Purdy, A. Probst, C. Y. Lin, and J. G. Zhu, "Non-linear CNN-based read channel for hard disk drive with 30% error rate reduction and sequential 200-Mbits/s throughput in 28-nm CMOS," *IEEE J. Solid-State Circuits*, early access, Feb. 10, 2023, 10.1109/JSSC.2023.3241631.

[A18] G. K. Chen, P. C. Knag, C. Tokunaga, and R. K. Krishnamurthy, "An eight-core RISC-V processor with compute near last level cache in Intel 4 CMOS," *IEEE J. Solid-State Circuits*, early access, Dec. 21, 2022, doi: 10.1109/JSSC.2022.3228765.

[A19] B. Keller et al., "A 95.6-TOPS/W deep learning inference accelerator with per-vector scaled 4-bit quantization in 5 nm," *IEEE J. Solid-State Circuits*, early access, Jan. 18, 2023, doi: 10.1109/JSSC.2023.3234893.

[A20] H. Wang, R. Liu, R. Dorrance, D. Dasalukunte, D. Lake, and B. Carlton, "A charge domain SRAM compute-in-memory macro with C-2C ladder-based 8-bit MAC unit in 22-nm FinFET process for edge inference," *IEEE J. Solid-State Circuits*, early access, Jan. 6, 2023, doi: 10.1109/JSSC.2022.3232601.

[A21] R. Kumar et al., "A 7-Gbps SCA-resistant multiplicative-masked AES engine in Intel 4 CMOS," *IEEE J. Solid-State Circuits*, early access, Dec. 28, 2022, doi: 10.1109/JSSC.2022.3230372.

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