A 39-GHz CMOS Bidirectional Doherty Phased-Array Beamformer Using Shared-LUT DPD With Inter-Element Mismatch Compensation Technique for 5G Base Station

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***Abstract*— This article demonstrates a 39-GHz CMOS phased-array beamformer aiming for power-efficient and area-efficient fifth-generation (5G) dual-polarized multiple-in–multiple-out (DP-MIMO) applications. To address the digital pre-distortion (DPD) implementation issue in the massive beamformer elements with Doherty technique integrated, an inter-element mismatch compensation technique is introduced for improving the shared-lookup table (LUT) DPD performance over the process, voltage and temperature (PVT) variations. A bidirectional Doherty power amplifier (PA)-LNA is proposed to enhance the power back-off (PBO) efficiency regarding the high peak-to-average power ratio (PAPR) 5G signals, meanwhile cost down the system by the unbalanced neutralized bidirectional operation. The proposed phased-array beamformer chip is fabricated in 65-nm CMOS technology and packaged in a wafer-level chip-scale package (WLCSP). Each element occupies only a 0.82-mm^2 chip area, including the on-chip low-dropout regulator (LDO). The measured stand-alone Doherty PA-LNA achieves 18.9-dBm saturated output power with 17.8% power-added efficiency (PAE) at 6-dB PBO in PA mode and obtains a 4.8-dB noise figure (NF) at 40 GHz in LNA mode. By utilizing the proposed mismatch compensation, the measured 64-quadrature amplitude modulation (QAM) orthogonal frequency-division multiple access (OFDMA)-mode error vector magnitude (EVM) and adjacent channel leakage ratio (ACLR) with the shared-LUT DPD are improved from −22.4 to −25.0 dB and from −28.7 to −32.1 dBc, respectively. The 64-element module achieves a 55.2-dBm saturated effective isotropic radiated power (EIRP) and supports 21-Gb/s single-carrier (SC) mode data streaming. The measured 64-element transmitter (TX) EVM is −25.2 dB at 43.2 dBm with 3.5-GSymbol/s baud rate in 64 QAM, and the corresponding 64-to-4 elements TX-to-receiver (RX) EVM is −22.5 dB. The consumed power for each element is 402 mW at saturation output point in TX mode and 87 mW in RX mode.**

***Index Terms*— 39 GHz, bidirectional, CMOS, Doherty, fifth-generation (5G) new radio (NR), inter-element mismatch compensation, phased arrays, shared-lookup table (LUT) digital pre-distortion (DPD), time-division duplex (TDD) system.**

I. Introduction

With the merit of abundant frequency resources in millimeter-wave (mm-wave) bands, the fifth-generation (5G) new radio (NR) frequency range 2 (FR2) promises high data rate and low communication latency. The 5G enhanced mobile broadband (eMBB) scenario even supports over 10-Gb/s throughput among massive wireless terminals [1]. Limited by the drastically increased free-space path loss (FSPL), the beamforming technique based on large-scale phased arrays is mandatory to reach a better signal-to-noise ratio (SNR) over long-distance communication. Widespread studies have been focused on the 5G mm-wave phased arrays in the past few years [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23]. The high-performance phased-array system should feature high effective isotropic radiated power (EIRP) for maintaining the link budget and compact system design to adapt to the narrowed antenna pitch.

Moreover, due to the high peak-to-average power ratio (PAPR) of 5G-standard orthogonal frequency-division multiple access (OFDMA)-mode modulated signals, the power

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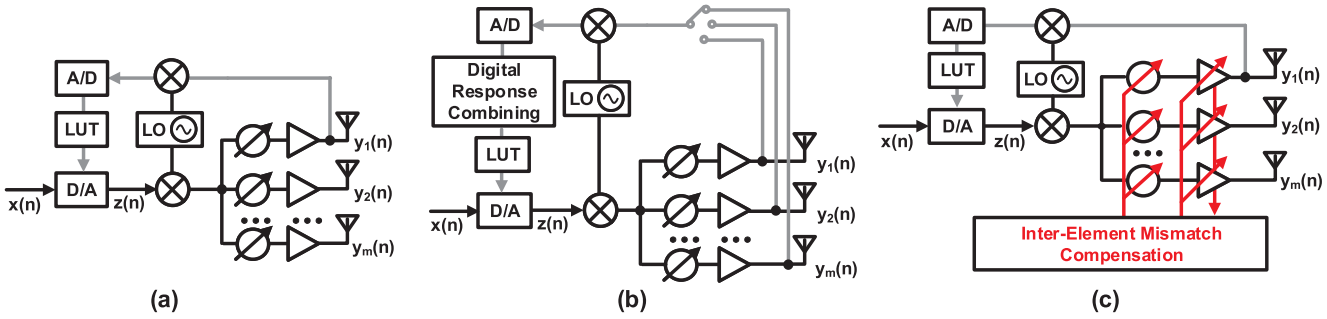


Fig. 1. DPD strategies for phased arrays. (a) Conventional single-LUT DPD. (b) Conventional combined-LUT DPD with digital response combining. (c) Proposed shared-LUT DPD with inter-element mismatch compensation.

efficiency of phased-array beamformers is easily degraded in the deep power back-off (PBO) region. The extra energy dissipation will bring in a severe thermal issue, especially in large-scale phased arrays. Thus, power-added efficiency (PAE) improvement techniques are strongly demanded. Doherty power amplifier (PA) architecture can be a promising solution, and many high-performance stand-alone Doherty PAs have been demonstrated for 5G applications so far [24], [25], [26], [27], [28], [29], [30]. However, the integration of the Doherty technique in phased arrays is still not well studied yet. The reported Doherty PAs are usually bulky and cannot fit the antenna pitch for mm-wave beamformer design.

As another cost-effective linearization solution, the digital pre-distortion (DPD) technique can also be applied to correct the distortion introduced by the PA nonlinearity in the baseband [31], [32]. Recently, there have been more and more demonstrations of the phased-array DPD strategies [33], [34], [35], [36], [37], [38], [39], [40]. Also, the most mentioned strategies, optimizing the DPD lookup table (LUT) errors during coefficient extraction, still suffer from inter-element mismatches. The cooperation with the Doherty technique will further enlarge these mismatches, thus limiting the phased-array linearity improvement.

Aiming for the power-efficient and area-efficient design, this work presents a 39-GHz bidirectional Doherty phased-array beamformer for 5G NR n259 (39.5–43.5 GHz) and n260 (37.0–40.0 GHz) bands. An inter-element mismatch compensation technique is demonstrated with shared-LUT DPD for improving the DPD performance over process, voltage and temperature (PVT) variations. A bidirectional Doherty PA-LNA is proposed to enhance the single-element beamformer efficiency and narrow the chip area occupation. The measured stand-alone Doherty PA-LNA achieves 18.9-dBm saturated output power with 17.8% PAE at 6-dB PBO in PA mode and obtains a 4.8-dB noise figure (NF) at 40 GHz in LNA mode. After utilizing the proposed mismatch compensation, both the measured 400-MHz OFDMA-mode error vector magnitude (EVM) and adjacent channel leakage ratio (ACLR) with the shared-LUT DPD achieve around 3-dB improvement in 64 quadrature amplitude modulation (QAM). The 16-IC phased-array module with 55.2-dBm saturated EIRP is also designed to support 21-Gb/s single-carrier (SC) mode data streaming. To the best of our knowledge, this is the first demonstration of combining the DPD and Doherty techniques in 5G phased-array applications.

This article is an extension of [41] and is structured as follows. The DPD strategy considerations for the 5G phased-array system are introduced in Section II. The detailed circuit implementations are demonstrated in Section III, followed by the measurement results presented in Section IV. Section V summarizes the performance and concludes at the end.

II. DPD Architecture in Phased-Array System

As mentioned previously, DPD is essential to suppress the nonlinearity and enlarge the output power for 5G mm-wave phased-array beamformers. In this section, as shown in Fig. 1, the concept of the shared-LUT DPD with inter-element mismatch compensation is discussed and contrasted with the conventional phased-array DPD strategies. The prefix "single," "combined," and "shared" are defined by the different approaches of the LUT generation and are not related to the LUT structure itself. Only one LUT is commonly applied for the phased-array system to simplify the baseband. In general, DPD captures the beamformer element output and applies inverse nonlinear operation upon the input. Based on a widely used memory polynomial model [31], the pre-distorted input signal of a uniform linear array (ULA) can be expressed as follows:

$$z_m(n) = \sum_{k=0}^{K-1} \sum_{q=0}^{Q-1} a_{kq}^m x_m(n-q)|x(n-q)|^k \tag{1}$$

where $x_m(n)$ is the mth baseband input signal, and $z_m(n)$ is the mth pre-distorted signal. The maximum nonlinear order K, maximum memory depth Q, and DPD coefficients a_{kq}^m define the memory polynomial model together. Thus, the corresponding mth element output $y_m(n)$ can be denoted as follows:

$$y_m(n) = z_m(n)e^{j\varphi_m}A_m \tag{2}$$

where $e^{j\varphi_m}$ is the mth phase shift, and A_m is the mth PA gain. This DPD strategy requires individual basebands for each phased-array element, which is impractical. In hybrid beamforming systems, the DPD LUT has to be shared among all the elements and ICs. Therefore, the linearity improvement achieved by DPD is sensitive to the path-to-path AM–AM and AM–phase modulation (PM) mismatches caused by the PVT variations. To demonstrate this issue, as a simplified strategy, the single-LUT DPD is shown in Fig. 1(a) [33]. The single-LUT DPD captures the response from a single path; assuming the DPD extracted from an arbitrary element m_0, the

output mismatch between this element and the mth element is given by

$$E_{\text{single}}(n) = z_{m_0}(n)\left(e^{j\varphi_m}A_m - e^{j\varphi_{m_0}}A_{m_0}\right) \tag{3}$$

where $z_{m_0}(n)$ is the pre-distorted signal generated by the arbitrary element m_0, which is a constant matrix. The linearity improvement is degraded by the existence of $E_{\text{single}}(n)$. Also, the error is also subject to change with the different paths, which brings in more uncertainty. While, the conventional combined-LUT DPD in Fig. 1(b) captures the responses from all paths and minimizes the errors by digital-domain response combining [34] and [35]. The digital-domain computational complexity can be relieved by the approach of far-field combining, while additional timing alignment is required to synchronize with the source signal [36], [37], [38], [39], [40]. The combined-LUT DPD output $y_{\text{opt}}(n)$ and the optimized coefficient $z_{\text{opt}}(n)$ can be represented as follows:

$$y_{\text{opt}}(n) = \frac{1}{M}\sum_{m=1}^{M} z_m(n)e^{j\varphi_m}A_m \tag{4}$$

$$z_{\text{opt}}(n) = \frac{y_{\text{opt}}(n)}{e^{j\varphi_{\text{opt}}}A_{\text{opt}}} \tag{5}$$

where $e^{j\varphi_{\text{opt}}}$ is the optimized phase shift, and A_{opt} is the optimized PA gain. The output mismatch can be expressed as follows:

$$E_{\text{combine}}(n) = z_{\text{opt}}(n)\left(e^{j\varphi_m}A_m - e^{j\varphi_{\text{opt}}}A_{\text{opt}}\right). \tag{6}$$

Thus, the achievable linearity improvement could be better than the single-LUT DPD but is still limited by the AM–AM and AM–PM mismatches among different elements.

As illustrated in Fig. 1(c), this work introduces a shared-LUT DPD with the inter-element mismatch compensation technique to further improve the DPD performance in 5G hybrid beamforming systems. Before DPD LUT extraction, the path-to-path AM–AM and AM–PM mismatches are corrected through the inter-element mismatch compensation system. In this way, the errors could be minimized after compensation, which provides a prerequisite for sharing the same DPD LUT among the entire phased array without compromising the DPD performance.

To demonstrate the performance with the conventional and proposed DPD strategies, an ACLR versus EIRP simulation of a 16-element ULA is conducted using Keysight SystemVue software in Fig. 2. The simulation condition is also shown in Fig. 2(a). An 2-dB gain offset rms error and a 10° phase offset rms error are assigned by the Monte Carlo setup. The AM–AM and AM–PM characteristics of a Doherty PA are extracted and applied to the ACLR simulation. Each PBO point is adjusted, so that the $+3\sigma$ worst case ACLR becomes less than the required -26-dBc level. By means of the proposed shared-LUT DPD with the inter-element mismatch compensation technique, the average value and the standard deviation of the simulated ACLR can be improved, as shown in Fig. 2(b). The proposed technique can realize the smallest PBO and the highest EIRP characteristics.

To evaluate the required calibration resolution, the 16-element ULA ACLR versus gain and phase rms errors are performed, as shown in Fig. 2(c) and (d), respectively. In order to minimize the calibrated ACLR degradation

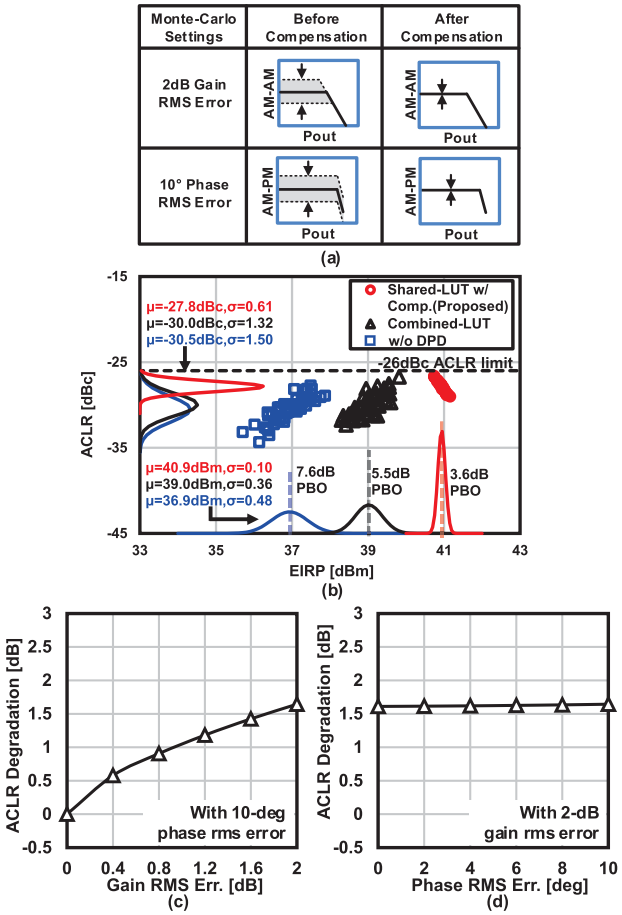


Fig. 2. Monte Carlo simulation of a 16-element ULA with different DPD strategies. (a) Offset-mismatch settings with given gain and phase rms errors. (b) Simulated ACLR versus EIRP performance. The 16-element ULA simulated (c) ACLR versus gain rms error and (d) ACLR versus phase rms error.

below 0.5 dB, the 0.4-dB gain rms error is required for the variable gain amplifier (VGA) resolution, which means a finer resolution is required for amplitude detection. The ACLR degradation will in return cost more PBO for EIRP. While the phase rms error mainly degrades the side lobes of the beampattern, the non-linearity contribution is not obvious.

The gain and phase offset calibration are applied for accurate beamforming in a phased-array system, which can mitigate AM–AM and AM–PM offset mismatches over the phased-array elements. However, the strong nonlinearity of Doherty PA cannot be compensated by the simple gain and phase offset compensation, since the class-C-biased amplifier is very sensitive to the transistor threshold voltage (V_{th}) variation. Thus, as shown in Fig. 3(b), V_{th} mismatch compensation is mandatorily required for a phased-array beamformer using Doherty PA for optimizing array EVM and ACLR characteristics. To verify the difference toward the conventional gain/phase compensation in Fig. 3(a), a Monte Carlo simulation about AM–AM and AM–PM of the single transmitter (TX) element with Doherty PA is conducted, where the same simulation samples are used for two compensation methods. The gain/phase compensation and the proposed gain/phase/V_{th} compensation results are shown in Fig. 3(c) and (d), respectively. Obviously, with the gain/phase offset compensation, the large mismatch remains in both AM–AM and AM–PM

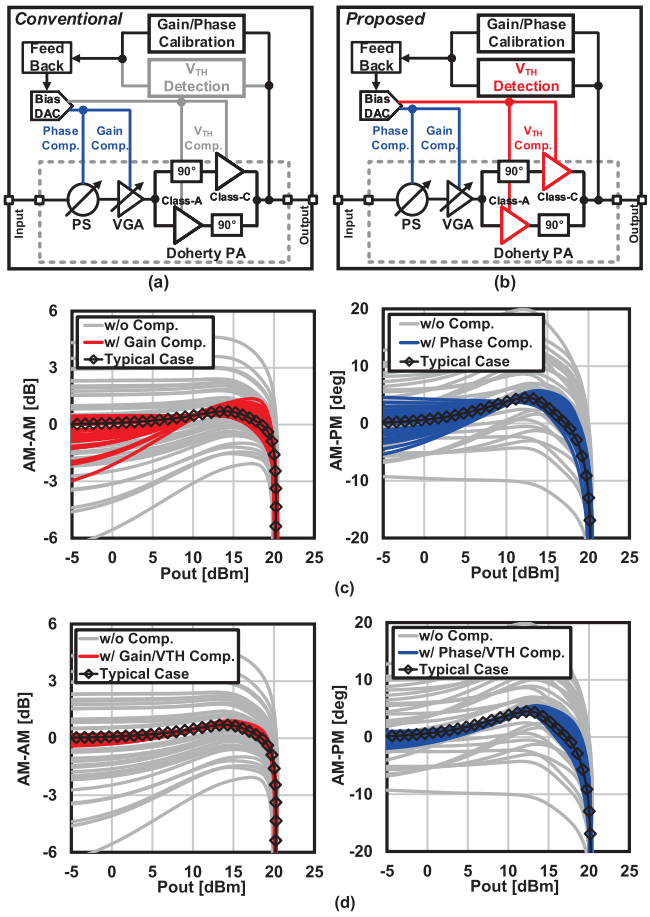


Fig. 3. (a) Concept of gain and phase compensation and (b) proposed V_{th}, gain and phase compensation. Monte Carlo simulation over process variations of (c) AM–AM and AM–PM with gain/phase compensation only and (d) AM–AM and AM–PM with gain/phase/V_{th} compensation method.

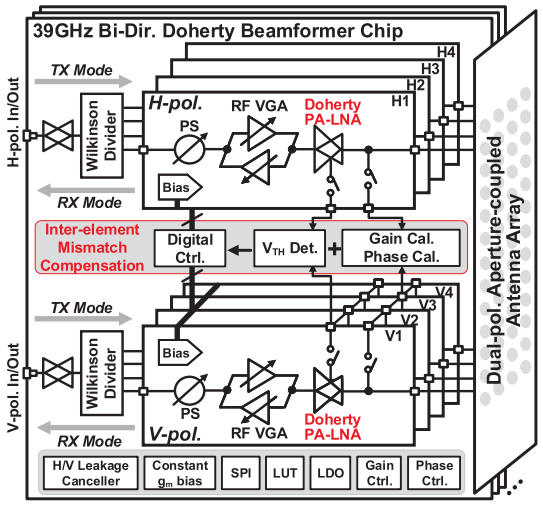


Fig. 4. Block diagram of the 39-GHz CMOS bidirectional phased-array TRX system.

characteristics. While, the AM–AM and AM–PM can be compensated from the back-off power level along to the peak power level by using the gain/phase/V_{th} method.

III. Phased-Array Beamformer Architecture

Fig. 4 illustrates the block diagram of the 39-GHz phased-array beamformer. The proposed chip consists of four horizontal-polarized and four vertical-polarized beamformer elements. Each element is composed of a bidirectional Doherty PA-LNA, a three-stage bidirectional radio frequency (RF) VGA, and an RF phase shifter (PS). The neutralized bidirectional technique is used to minimize the required chip area [2]. The cross-pol. leakage canceller is also utilized to reduce the cross-pol. leakage to support the dual-polarized multiple-in–multiple-out (DP-MIMO) better [3]. To realize an efficient shared-LUT DPD phased-array system, this work introduces a built-in inter-element mismatch compensation technique by cooperating with the V_{th} detection block and calibration block. The power supplies of beamformer elements will suffer from different onboard distribution losses without the on-chip low-dropout regulators (LDOs), which introduces additional phase and gain errors for the phased-array system. In this work, the on-chip LDOs are utilized to provide a precise 1-V power supply with high stability. The following part of this section will introduce the detailed circuit implementation of the proposed phased-array beamformer.

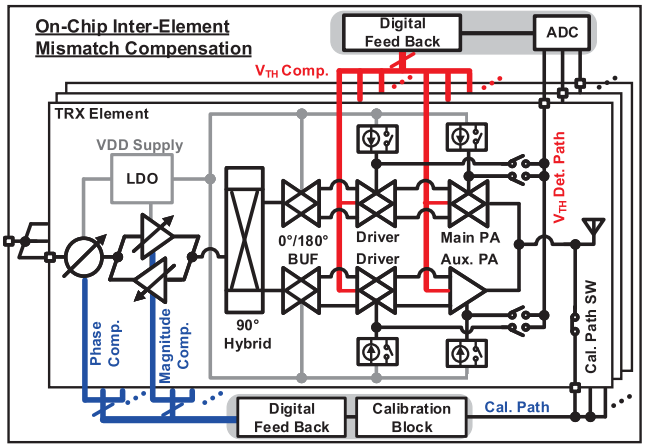


Fig. 5. System block diagram of the proposed inter-element mismatch compensation.

A. Inter-Element Mismatch Compensation

Fig. 5 shows the detailed implementation of the proposed on-chip inter-element compensation system, and the AM–AM and AM–PM mismatches are detected by embedded self-test circuitry and compensated over inter-element and inter-chip. Therefore, the nonlinearity characteristics at the TX operating points between different elements are minimized, and a shared-LUT DPD could be applied to the entire phased array. Fig. 6(a) and (b) demonstrates the V_{th} detection mode and normal TX mode, respectively. The V_{th} mismatch of the Doherty PA is detected by an on-chip threshold voltage detector and 10-bit ADC and is compensated by tuning the gate bias through the digital interface. The V_{th} detection is conducted by turning on SW_{DET}. the PA transistors are configured in diode-connection mode and operated in the subthreshold region. The drain current is controlled by the current mirror. The 10-bit ADC reads out the gate voltage of the diode-connected transistor as V_{th} [42]. The simulated V_{th} detection varies with temperature at different process corner conditions can be referred to in Fig. 6(c). When it operates in normal TX mode, SW_{DET} is turned off. Thus, the power PMOS array is turned on, and the PA transistors are placed

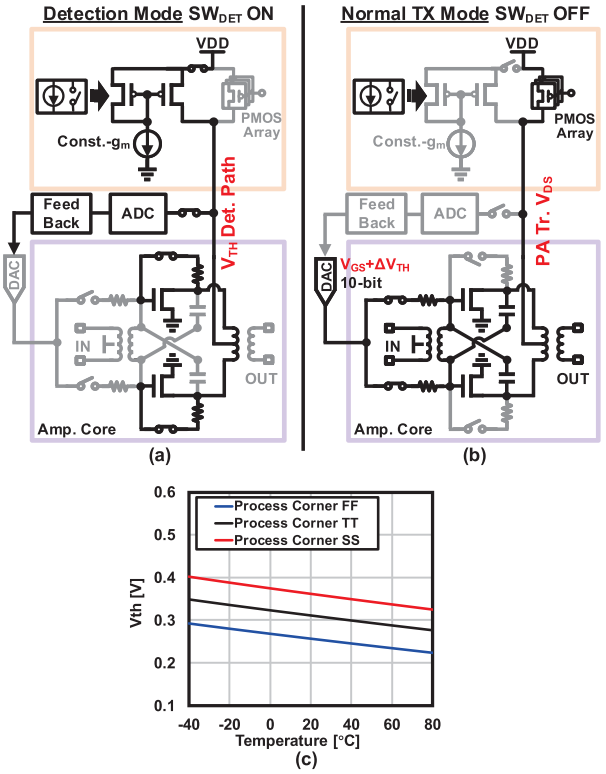


Fig. 6. Schematic of the proposed V_{th} detection circuit in (a) V_{th} detection mode and (b) normal TX operation mode. (c) Simulated V_{th} detection varies with the temperature variations at different process corner conditions.

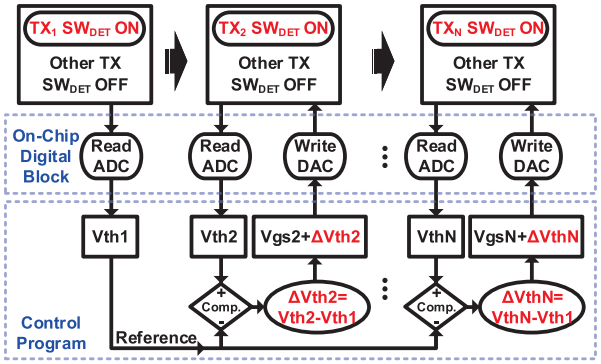


Fig. 7. Measurement flow diagram of the proposed V_{th} detection and compensation.

in the saturation region. Considering the V_{th} detection and compensation in a phased-array system, a measurement flow diagram is shown in Fig. 7. When detecting V_{th} of a specific beamformer element, only SW_{DET} of this element is turned on, while all other element switches are closed. Then, V_{th} detection is conducted element by element, and all the ADC readouts are sent to a control program with GUI. One reference element is necessary with a reference V_{th} value, e.g., $V_{th}1$ in Fig. 7. The V_{th} mismatch ΔV_{th} between the other detected V_{th} value and the reference $V_{th}1$ can be calculated by $V_{th} - V_{th}1$; then, a compensated bias of $V_{gs} + \Delta V_{th}$ is written into the DAC to perform the compensation.

The gain and phase offset mismatches are detected by an on-chip calibration block and compensated by tuning the VGA

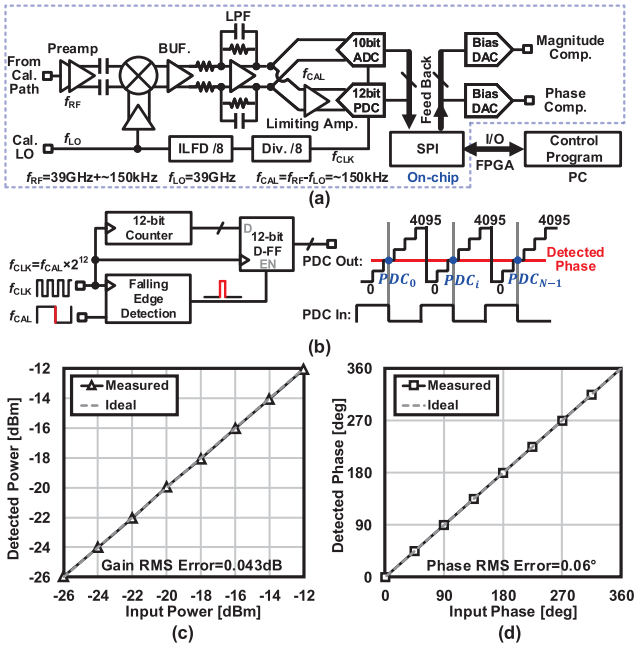


Fig. 8. (a) Block diagram of the calibration block and (b) operation of phase detection. The measured detected (c) gain rms error and (d) phase rms error.

and PS in each beamformer element. Fig. 8(a) shows the block diagram of the calibration block. To perform this calibration, e.g., at 39 GHz, the 39-GHz + ≈150-kHz output signal from each TX output is re-directed and downconverted to a ≈150-kHz calibration signal. The 39-GHz calibration local oscillator (LO) is reused and divided for digital clock generation. Then, a 10-bit ADC and a 12-bit counter-based phase-to-digital converter (PDC) are utilized for accurate magnitude and phase detection. The readouts of ADC and PDC are sent to the control program. Then, the compensated bias codes are written into the DACs of VGA and PS. Fig. 8(b) shows the operation of phase detection. The calibration signal is transformed into a square wave by the limiting amplifier as the input of PDC. The original RF signal's phase information is maintained in the transformed square wave signal. The PDC is mainly composed of a 12-bit counter, a falling edge detecter, and a 12-bit D flip-flop. The phase detection resolution is determined by the frequency ratio between the clock signal and the calibration signal, i.e., 2^{12}:1. The detected phase is evaluated by the 12-bit countered output value at each falling edge of the input signal. The measured magnitude and phase detection results are also shown in Fig. 8(c) and (d). The measured rms error for magnitude detection is 0.043 dB, while the measured rms error for phase detection is 0.06° [43].

The inter-element mismatch compensation is conducted at the beginning of the measurement. Also, repeated compensation at a certain time interval is required considering the environmental variations. The inter-element mismatch compensation time is related to the read-and-write operations through the digital interface. In this work, a 25-MHz serial peripheral interface (SPI) clock is utilized. The compensation for one chip costs around 0.2 ms. The registers for LUT storage are integrated inside the on-chip digital block. To perform the on-chip calculation for compensation, the

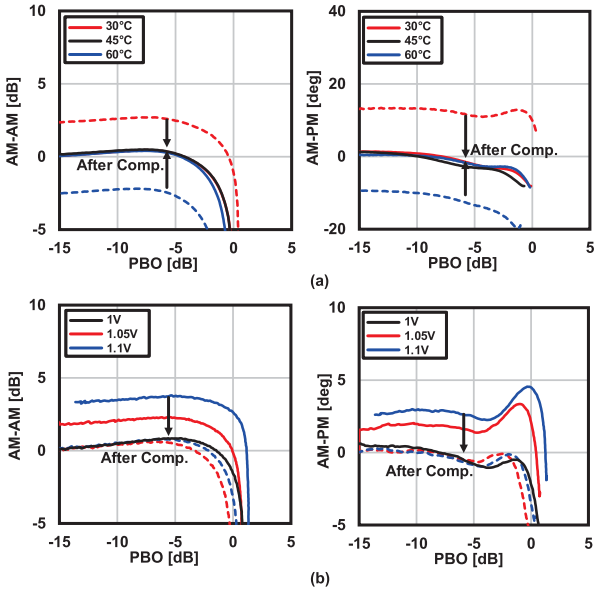


Fig. 9. Measured AM–AM and AM–PM compensation over (a) temperature variations and (b) supply voltage variations.

additional digital comparator and the supporting logic circuits are necessary.

Fig. 9 shows the measured AM–AMs and AM–PMs of the element TX before and after the proposed inter-element mismatch compensation over temperature and supply voltage variations. The mismatches caused by the temperature and supply voltage drifts can also be significantly corrected.

B. Bidirectional Doherty PA-LNA With WLCSP

In RF front-end design, the PA, LNA and antenna interface almost dominate the system performance. The low-loss antenna interface is attractive for maintaining TX output power level and reducing receiver (RX) NF. Also, the $\lambda/2$ antenna pitch is scaling down along with the increasing operation frequency, and around 4-mm antenna pitch is available at the 39-GHz band. Thus, compact packaging method is desired. In this work, a bidirectional Doherty PA-LNA is proposed and co-designed with wafer-level chip-scale package (WLCSP). The TX back-off power efficiency can be enhanced by utilizing the Doherty technique. Meanwhile, a larger TX output power is realized through the combined output, which is good for reducing the array size.

Figs. 10(a) and 11(a) show the bidirectional Doherty PA-LNA in PA mode and LNA mode, respectively. It consists of a 90° hybrid coupler, a main PA path with LNA, and an auxiliary PA path for Doherty operation. The main PA path with LNA is designed based on an unbalanced neutralized bidirectional technique [2], [3]. A minimized on-chip area could be realized by the shared inter-stage passives between PA and LNA. When the Doherty PA-LNA operates in PA mode, the main PA path is biased at class AB, while the auxiliary PA path is biased at class C to perform the Doherty load modulation. The same driver stages are applied for both the main and auxiliary PA paths to minimize the output combining mismatch. Fig. 10(b) and (c) demonstrates the simulated Doherty load modulation characteristics of the main

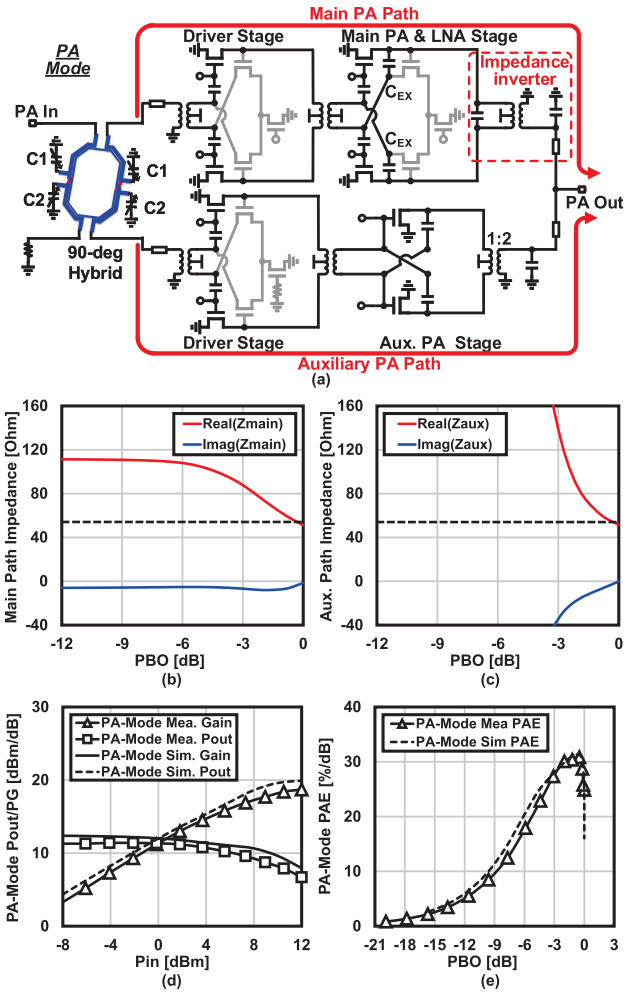


Fig. 10. (a) Proposed bidirectional Doherty PA-LNA in PA mode. Simulated PA-mode Doherty load modulation characteristics of (b) main PA path and (c) auxiliary PA path. Measured results of the stand-alone bidirectional Doherty PA-LNA test elementary group (TEG) (d) PA-mode power gain and pout and (e) PA-mode PAE versus PBO.

PA path and the auxiliary PA path, respectively. The auxiliary PA path is gradually turned on from the 6-dB PBO point, and the load impedance seen into the main PA path is slowly descending at the same time. Until the saturation region, the same load impedance is reached for both the main PA path and the auxiliary PA path. Fig. 10(d) and (e) shows the measured PA-mode results compared with its simulated results. To minimize the degradation between the measured results and the simulated results, the transistor cores are modeled with Cadence EMX Planar 3D Solver (EMX), and the passives are modeled by Ansys High-frequency Structure Simulator (HFSS) during the post-simulation. In measurement, a standalone bidirectional Doherty PA-LNA achieves an 18.9-dBm P_{sat} and a 30.4% peak PAE in PA mode with a 1-V supply voltage. The measured PAEs at 6- and 8-dB PBO are 17.8% and 12.0%, respectively.

In LNA mode, the 1:2 balun at the auxiliary PA stage is capable of providing an impedance upscaling to isolate the auxiliary path and suppress the loading effect. The simulated impedance seen from LNA input to the off-state PA auxiliary path is shown in Fig. 11(b). The extra capacitor C_{EX} is designed to be neutralized by C_{gd} of the PA-mode transistors

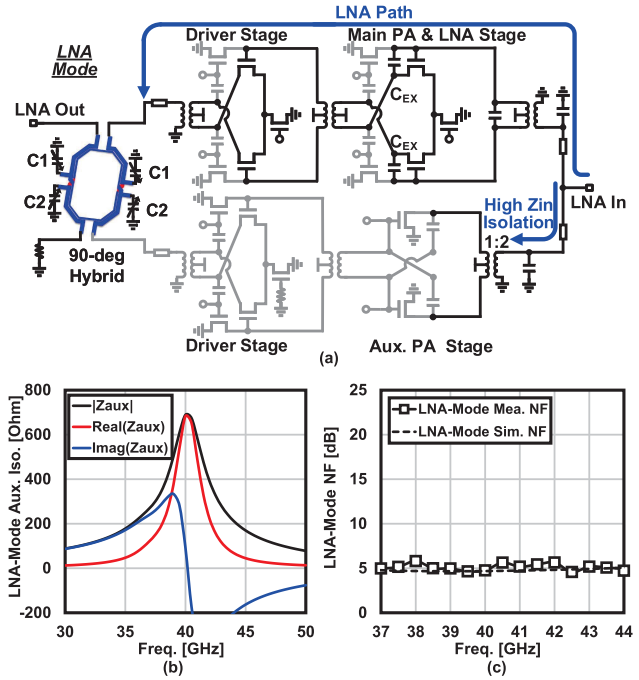


Fig. 11. (a) Proposed bidirectional Doherty PA-LNA in LNA mode. (b) Simulated LNA-mode auxiliary path isolation. (c) Measured result of the stand-alone bidirectional Doherty PA-LNA TEG LNA-mode NF.

along with C_{gd} of the LNA-mode transistors. Therefore, the Miller effect is minimized, and the LNA-mode stability is also enhanced. The NF is measured by the Keysight PNA-X N5274B network analyzer. The NF Cold Source option is selected with the Scalar Noise calibration. Fig. 11(c) presents the measured LNA-mode NF, and a 4.8-dB NF at 40 GHz and a less than 5.8-dB in-band NF are obtained in LNA mode.

Fig. 12(a) shows the WLCSP 3-D electromagnetic (EM) model for antenna and IC interconnection. In order to minimize the package capacitive loss and improve the bandwidth, the RF pad size is minimized, and the ground shield under the signal bump is removed. The additional metal-to-substrate loss of the signal bump from the P-doped substrate is smaller than the capacitive loss introduced by the ground shield [44]. A transmission lines (TLs) re-matching network is inserted between the PA-LNA and the WLCSP model, as shown in Fig. 12(b). The TL stub is shared with the calibration path to save the chip area and further reduce insertion loss. Fig. 12(c) shows the WLCSP EM simulated results with TL re-matching network, and a less than 1.2-dB insertion loss is realized from 30 to 50 GHz.

C. Bidirectional VGA and Mixed-Type Phase Shifter

A three-stage single-ended bidirectional VGA with attenuators is presented in Fig. 13(a). Two single-direction VGAs are connected end-to-end and controlled by mode-switching bias. The bidirectional operation is supported with limited power consumption. The single-ended topology is also convenient to fit the irregular layout shape. Fig. 13(b) shows the mixed-type RF PS, composed of a reflection-type PS (RTPS), a 45° switch-type PS (STPS), and a 90° STPS. A 90° directional coupler with around 25-Ω characteristic impedance is implemented in RTPS to enlarge the phase shift coverage.

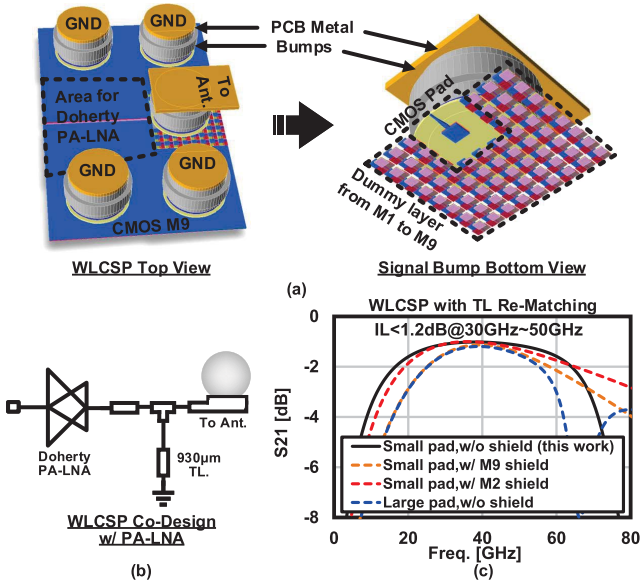


Fig. 12. (a) Optimized 3-D WLCSP EM model at the antenna port. (b) Proposed bidirectional Doherty PA-LNA with WLCSP co-design. (c) Simulated packaging insertion loss with the transmission-line rematching network.

The tunable capacitive reflection load is designed with two switching capacitors and a varactor, realizing the fine phase-tuning function. The 180° phase shift is fulfilled by swapping the outputs of the following differential stages. The measured insertion loss of the mixed-type PS is shown in Fig. 13(d). The measurement results shown in Fig. 13(c), (e), and (f) are based on the single TX-mode beamformer element. The additive phase variation introduced by the bidirectional VGA is demonstrated in Fig. 13(c) with the calculated phase rms error. Fig. 13(e) and (f) performs the measured beamformer phase coverage with the corresponding phase and gain rms error. The 360° phase coverage is achieved from 37- to 43.5-GHz band; less than 2.00° phase rms error and less than 1.03-dB gain rms error are obtained within the targeted 39-GHz band.

IV. Measurements

The proposed 39-GHz phased-array beamformer chip is fabricated in standard 65-nm CMOS technology. Its die micrograph is shown in Fig. 14 with a chip size of 4.5 × 5 mm. The area breakdown and power consumption breakdown of building blocks are available in Table I. The consumed power for each element is 402 mW at saturation point in TX mode and 87 mW in RX mode.

Fig. 15 summarizes the on-wafer measured single-element beamformer characteristics. Fig. 15(a) demonstrates the TX/RX-mode frequency responses. The single-element beamformer achieves around 28.5-dB gain in TX mode and 27.5-dB gain in RX mode, respectively. With 400-MHz channel bandwidth, the calculated SNDR of the RX-mode beamformer is shown in Fig. 15(b). A higher than 35-dB RX-mode SNDR is realized.

The 5G standard-compliant OFDMA-mode modulated signals are utilized for evaluating the TX-mode beamformer. As shown in 15(c) and (d), the proposed TX-mode beamformer achieves 10.2-dBm output power in 64 QAM with −25.1-dB EVM without DPD. The corresponding 64-QAM ACLR

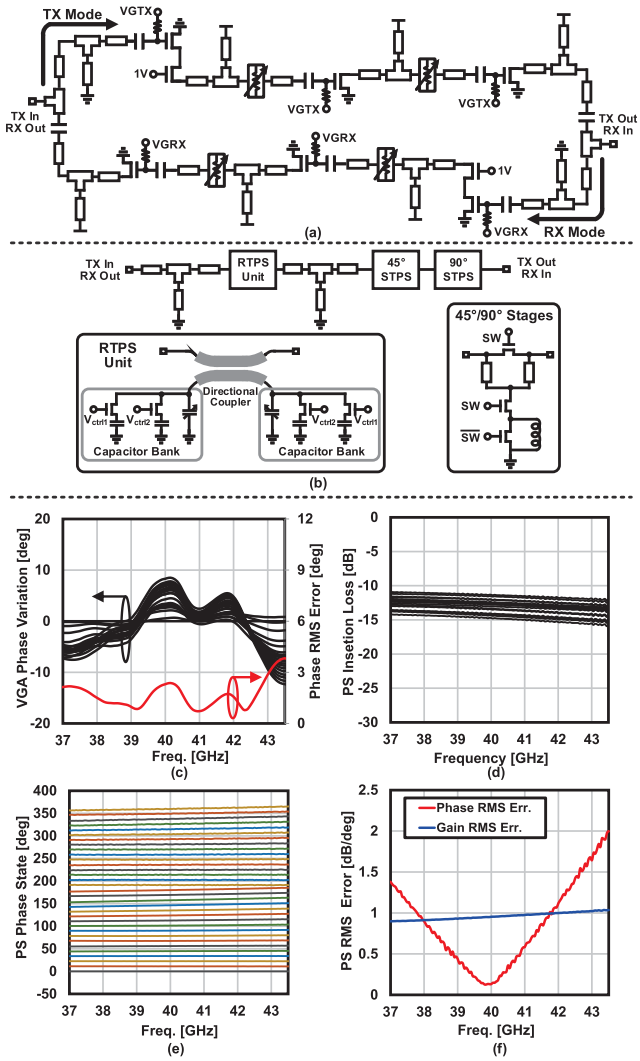


Fig. 13. (a) Circuit schematics of single-ended three-stage bidirectional RF VGA. (b) Mixed-type RF PS topology with (d) measured insertion loss. Measured results of the single TX-mode beamformer element—(c) VGA additive phase variations, and (e) phase-shifting coverage with the corresponding (f) phase and gain rms errors.

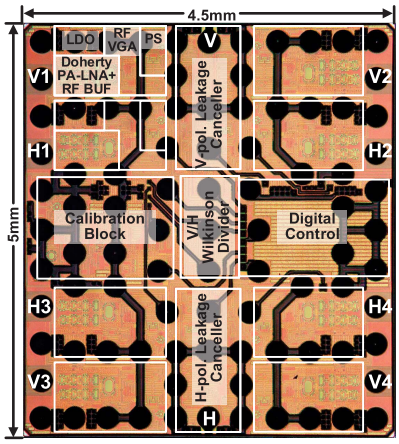


Fig. 14. Die micrograph of 39-GHz CMOS bidirectional phased-array TRX.

is −30.7 dBc. A 256-QAM EVM of −31.6 dB is also maintained with 3.9-dBm output power and −36.3-dBc ACLR.

TABLE I
CORE AREA AND POWER CONSUMPTION BREAKDOWNS

	Sub-Block	Area [mm^2]	TX-Mode PDC [mW]	RX-Mode PDC [mW]
Beamformer Element	Bi-dir. Doherty PA-LNA	0.26	207@Psat Main path:106 Aux. path:101 87@Static Main path:81 Aux. path:6	45
	RF BUF		39.5	11
	RF VGA	0.37	45.5	25
	PS	0.19	0	0
Full Chip Comb.	Canceller	1.14	15	10
	Comb. BUF		20	13
	Wilkinson Divider	0.65	0	0

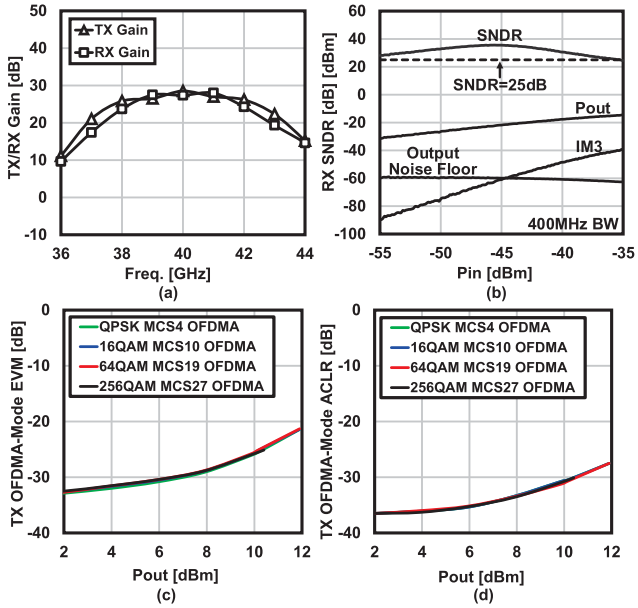


Fig. 15. Measured single-element beamformer characteristics—(a) TX/RX gain and (b) RX-mode SNDR; TX OFDMA-Mode (c) EVMs and (d) ACLRs with 400-MHz bandwidth without DPD.

To perform the over-the-air (OTA) communication with a large array size, the 16-IC phased-array dual-polarized PCB module is implemented, including 64 horizontal-pol. and 64 vertical-pol. beamformer elements. Fig. 16(a) shows the front-side photograph of the 16-IC module. The 16-IC module is controlled by Xilinx Zynq UltraScale + FPGA Kit. Fig. 16(b) shows the antenna array photograph at the back side. Each of the IC in the module is connected to a 2×2 dual-pol. antenna sub-array through the wide-band slot feedings. The PCB cross-sectional view is also demonstrated in Fig. 16(c).

The dual-pol. aperture-coupled structure is selected and optimized for the wide-band gain feature [45], [46], [47]. Its 3-D EM model is given by Fig. 17(a) in Γ-type slot configuration. As shown in Fig. 17(b), a higher than 5-dB single-element wide-band antenna gain with larger than 25-dB isolation at 40 GHz is realized according to the antenna simulated results.

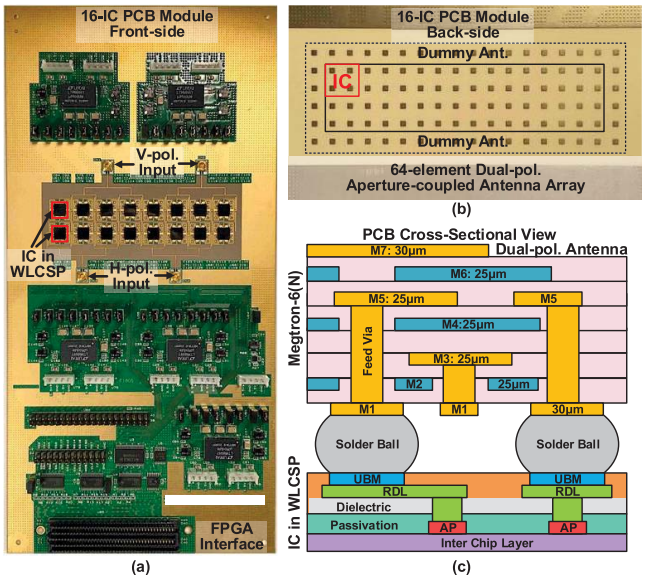


Fig. 16. (a) Front-side photograph of proposed 16-IC phased-array module. (b) 64-element dual-polarized aperture-coupled antenna array at the back side. (c) Seven-layer PCB cross-sectional view.

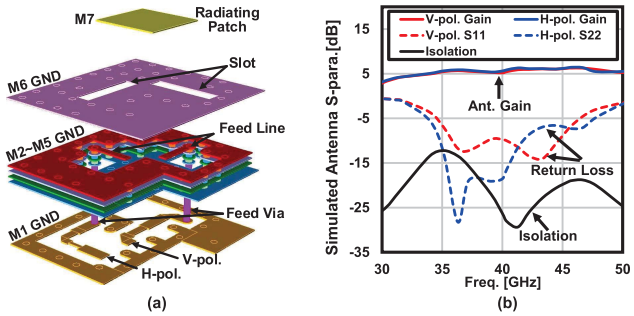


Fig. 17. (a) 3-D EM model of the dual-polarized aperture-coupled antenna with offset slots in Γ-type configuration and (b) simulated antenna performance.

Fig. 18(a) shows the measured saturated EIRPs at the broadside against the number of activated beamformers. The proposed mismatch compensation technique is conducted to realize a better EIRP result. The measured single-element saturated EIRP is 20.1 dBm, calculated by the saturated TX output power of 18.9 dBm and $G_{\mathrm{ANT\_SE}} - \mathrm{IL}_{\mathrm{WLCSP}}$. The single-element antenna gain $G_{\mathrm{ANT\_SE}}$ with the WLCSP insertion loss $\mathrm{IL}_{\mathrm{WLCSP}}$ equals 1.2 dB. The measured saturated EIRP at room temperature reaches 55.2 dBm for the 64-element phased-array module. The 64-element saturated EIRP can be estimated by 18.9 dBm $+20\log_{10}64 + G_{\mathrm{ANT\_ARR}} - \mathrm{IL}_{\mathrm{WLCSP}}$, resulting in a 0.2-dB $G_{\mathrm{ANT\_ARR}} - \mathrm{IL}_{\mathrm{WLCSP}}$. In this case, the antenna pattern gain $G_{\mathrm{ANT\_ARR}}$ is around 1-dB smaller than the single-element antenna gain $G_{\mathrm{ANT\_SE}}$ due to the additional coupling among the antenna array. Additional thermal solutions, such as heatsinks with high thermal conductivity and thermal area, are mandatory to maintain the high EIRP performance. Fig. 18(b) shows the measured 16 × 2 elements beam patterns in the azimuth plane. The phased-array module is able to cover ±45° scanning angle with less than −10-dB sidelobe level. No tapering window is appended during the measurement.

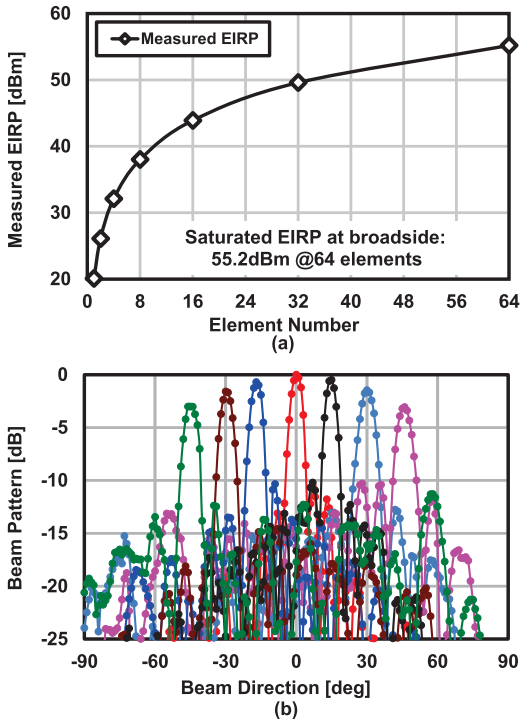
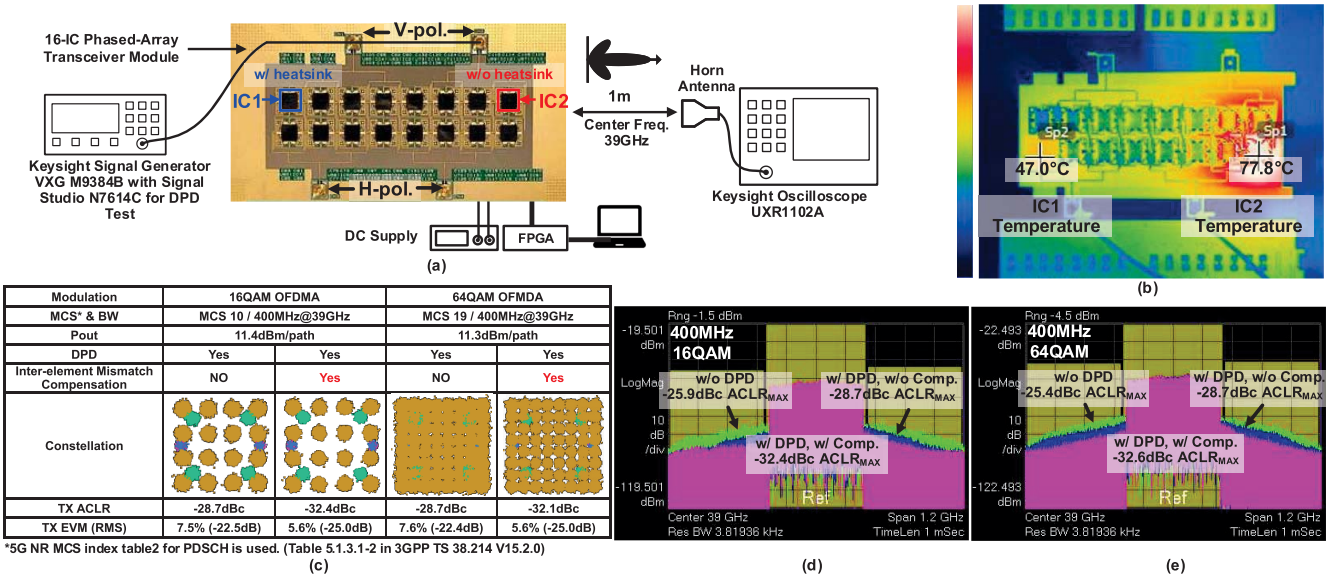


Fig. 18. Measured TX-mode phased-array module continuous-wave features. (a) Saturated EIRPs at broadside against the number of beamformers and (b) measured 16 × 2 elements beam pattern in azimuth plane.

To validate the proposed shared-LUT DPD with the inter-element mismatch compensation, an OTA measurement with the proposed phased-array module is performed. Fig. 19(a) shows the equipment setup for this measurement. The Keysight signal generator VXG M9384B is used to generate the 5G-standard OFDMA-mode modulated signals. The Keysight real-time oscilloscope UXR1102A is used to analyze the far-field signal caught by the horn antenna. To better extract the nonlinear behavior with the memory effect, the close-loop memory polynomial model is utilized. The DPD loop is controlled by Keysight signal studio N7614C for DPD Test, and the functions of crest factor reduction (CFR) and envelope tracking (ET) are disabled during the measurement. Several types of PVT variation are considered in phased array. Because the measured beamformer chips are manufactured in the same lot, the process influence is not obvious during the measurement. The simulated performance with process variations is given in Fig. 3. Considering the feasibility of the experiment, the temperature variation is performed to demonstrate the inter-element mismatch compensation. Two of the ICs, eight beamformer elements, located at relative distal positions are activated for EVM and ACLR measurements. The proposed compensation technique can be extended to full phased-array systems. Additional temperature difference is introduced between IC1 and IC2 by adding heat sink only to IC1. As demonstrated in Fig. 19(c), the measured temperatures with a thermal camera are 47.0°C and 77.8°C for IC1 and IC2, respectively. The DPD LUT is then extracted from IC1 and applied to both IC1 and IC2. The measurements are conducted in the condition with the proposed compensation technique or by turning off both the V_{th} compensation and



Modulation	16QAM OFDMA		64QAM OFMDA	
MCS* & BW	MCS 10 / 400MHz@39GHz		MCS 19 / 400MHz@39GHz	
Pout	11.4dBm/path		11.3dBm/path	
DPD	Yes	Yes	Yes	Yes
Inter-element Mismatch Compensation	NO	Yes	NO	Yes
Constellation				
TX ACLR	-28.7dBc	-32.4dBc	-28.7dBc	-32.1dBc
TX EVM (RMS)	7.5% (-22.5dB)	5.6% (-25.0dB)	7.6% (-22.4dB)	5.6% (-25.0dB)

*5G NR MCS index table2 for PDSCH is used. (Table 5.1.3.1-2 in 3GPP TS 38.214 V15.2.0)

Fig. 19. (a) Equipment setup for 2-IC 5G OFDMA-mode OTA measurement with shared-LUT DPD. (b) Thermal imaging photograph of the PCB module with temperature difference between IC1 and IC2. (c) Measured constellations, EVMs and ALCRs in both 16-QAM and 64-QAM OFDMA mode with and without proposed inter-element mismatch compensation, (d) measured 400-MHz 16-QAM OFDMA-mode ACLRs, and (e) measured 400-MHz 64-QAM OFDMA-mode ACLRs.

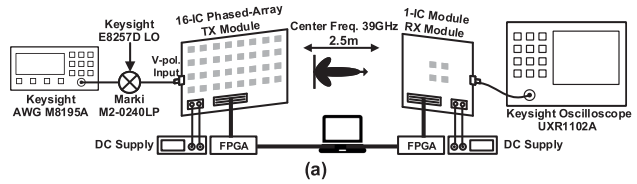
TABLE II

COMPARISON WITH STATE-OF-THE-ART 39-GHz BEAMFORMERS

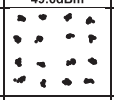
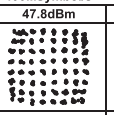
		This work			[21] CMU JSSC2020	[4] Tokyo Tech JSSC2019	[17] Samsung ISSCC2020		[18] UCSD TMTT2020
Process		65nm CMOS			65nm CMOS	65nm CMOS	28nm CMOS		0.18μm SiGe BiCMOS
Freq. Band		39GHz			39GHz	39GHz	39GHz		39GHz
Beamformer Integration		Bi-directional Doherty PA-LNA, PS			Dual-band PA,LNA	Class-AB PA, LNA,PS	Stacked PA, LNA,PS		PA,LNA,PS
TX Psat#		18.9dBm			16.7dBm	15.5dBm	>16.5dBm		12.0dBm
TX EIRPsat in CW		55.2dBm 64 elements			N/A	53.0dBm 64 elements	N/A		51.0dBm 64 elements
PA Peak PAE		30.4%			22.2%	25.5%	N/A		N/A
PA PAE @6dB PBO		17.8%			<10%*	9.5%*	N/A		N/A
TX Peak Efficiency		19.3%			N/A	9.5%*	N/A		5%†
PDC/path		TX:402mW@18.9dBm 181mW@Static RX:87mW			TX:116.2mW @Static RX:37.6mW	TX:375mW RX:125mW	TX:105mW @6dBm RX:39mW		TX:250mW @11dBm RX:150mW
Area/path		0.82mm^2**			0.48mm^2	1.78mm^2*	0.77mm^2*		N/A
SC Mode	**Modulation Scheme**	64QAM			64QAM	N/A	N/A		64QAM
	Data Rate	21Gb/s			1.5Gb/s	N/A	N/A		30Gb/s
	EIRP in SC	43.2dBm 64 elements			6.5dBm***	N/A	N/A		34.0dBm 64 elements
5G OFDMA-Mode	**Modulation Scheme**	64QAM+			N/A	64QAM	64QAM		N/A
	Inter-Element Mismatch Comp.	No	No w/ DPD	Yes w/ DPD	N/A	No	No		N/A
	TX Pout/path [dBm]	11.3	11.3	11.3	N/A	3.6	6	8.8	N/A
	TX EVM [dB]	N/A	−22.4	−25	N/A	−24.6	−34	−27	N/A
	TX ACLR [dBc]	−25.4	−28.7	−32.1	N/A	N/A	−36.5	N/A	N/A

* Estimated from paper. # Probe measurement without packaging. + 2-IC measurement results. † Refer to OP1dB point.
** On-chip LDO and WLCSP included. *** Only single-element data is available.

gain/phase calibration. To minimize the input difference introduced by different DPD LUTs, the measurements are based on the same shared LUT and referred to a fixed Pout per path. The 2-IC subarray achieves 30.3-dBm EIRP and 6% TX efficiency with an 11.3-dBm Pout per path. The measured 5G standard-compliant OFDMA-mode EVMs with shared-LUT



(a)

64-to-4 elements TX-to-RX Single Carrier OTA	Modulation Scheme	16QAM	64QAM	256QAM	64QAM
	Baud Rate	400MSymbol/s			3.5GSymbol/s
	TX EIRP (64 elements)	49.6dBm	47.8dBm	45.1dBm	43.2dBm
	TX Constellation				
	TX EVM (RMS)	9.1% (-20.8dB)	5.6% (-25.0dB)	2.6% (-31.6dB)	5.5% (-25.2dB)
	TX-to-RX EVM (RMS)	11.8% (-18.6dB)	7.6% (-22.4dB)	3.4% (-29.4dB)	7.6% (-22.5dB)

(b)

Fig. 20. (a) Equipment setup for TX-to-RX OTA SC-mode measurement in SISO scenario and (b) measured SC-mode constellations and EVMs.

DPD are improved from −22.5 to −25.0 dB in 16 QAM and −22.4 to −25.0 dB in 64 QAM. The corresponding ACLRs are suppressed from −28.7 to −32.4 dBc in 16 QAM and −28.7 to −32.1 dBc in 64 QAM. Fig. 19(d) and (e) shows the spectra measured in 400-MHz 16 QAM and 400-MHz 64 QAM, respectively. More than 6.5-dB ACLR enhancement is achieved by the proposed inter-element mismatch compensation with shared-LUT DPD. Significant improvement in linearity and power efficiency can be realized by utilizing the inter-element mismatch compensation in 5G NR applications.

The SC-mode OTA measurement is also performed, as shown in Fig. 20(a). The SC-mode root-raised-cosine filtered signals are generated by Keysight arbitrary waveform generator M8195A. The corresponding roll-off factor is 0.35. The 64-element TX-mode beamformers and four-element RX-mode beamformers are placed 2.5 m apart in the measurement. The measurements are conducted after calibration without DPD, and the broadside beam direction is selected during the measurement. Due to the different EVM requirements for different modulation schemes, this measurement is aiming for the highest EIRP on the base station side with the EVM requirement fulfilled. As summarized in Fig. 20(b), under 400-MSymbol/s baud rate, the 64-element module can realize −20.8-dB EVM with 49.6-dBm EIRP in 16 QAM, −25.0-dB EVM with 47.8-dBm EIRP in 64 QAM, and −31.6-dB EVM with 45.1-dBm EIRP in 256 QAM. The corresponding 64-to-4 elements TX-to-RX EVMs are −18.6, −22.4, and −29.4 dB, respectively. The 64-element module can also support 21-Gb/s SC-mode data streaming. The measured 64-element TX EVM is −25.2 dB with 43.2-dBm EIRP in 3.5-GSymbol/s 64-QAM modulation. The corresponding 64-to-4 elements TX-to-RX EVM is −22.5 dB. The 64-element TX module cannot support 256 QAM with 3.5-GSymbol/s baud rate due to the high EVM requirement of 256-QAM modulation.

V. Conclusion

Table II compares this work with the state-of-the-art 39-GHz phased-array beamformers. The proposed bidirectional Doherty beamformer achieves excellent transceiver continuous-wave characteristics. A bidirectional Doherty PA-LNA is proposed and co-designed with WLCSP. The PA mode realizes 18.9-dBm saturated output power and 17.8% PAE at 6-dB PBO due to the Doherty technique. Because of the proposed inter-element mismatch compensation technique, the AM–AM and AM–PM characteristics are minimized between different elements over PVT variations, which enhances EVM and ACLR characteristics. The measured EVM and ACLR in 64 QAM are improved from −22.4 to −25.0 dB and from −28.7 to −32.1 dBc, respectively, with a shared-LUT DPD. In 64-to-4-element TX-to-RX communication, the 64-element module achieves a 55.2-dBm saturated EIRP and also supports 21-Gb/s SC-mode data streaming at 43.2 dBm.

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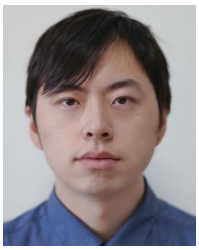

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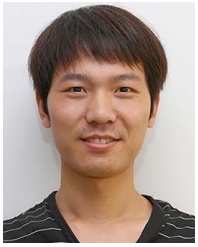

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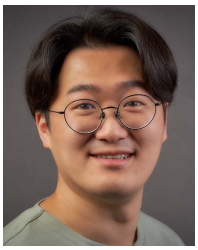

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