A 20-μs Turn-On Time, 24-kHz Resolution, 1.5–100-MHz Digitally Programmable Temperature-Compensated Clock Generator

Yongxin Li, *Graduate Student Member, IEEE*, Nilanjan Pal, *Member, IEEE*, Tianyu Wang, *Student Member, IEEE*, Mostafa Gamal Ahmed, *Member, IEEE*, Ahmed Abdelrahman, *Graduate Student Member, IEEE*, Mohamed Badr Younis, *Student Member, IEEE*, Kyu-Sang Park, *Graduate Student Member, IEEE*, Ruhao Xia, *Student Member, IEEE*, and Pavan Kumar Hanumolu, *Fellow, IEEE*

***Abstract*— A clock generator using a fast-locking frequency-locked loop (FLL)-based *RC* oscillator and delta-sigma fractional dividers (FDIVs) to generate programmable temperature-insensitive output frequencies is presented. Successive approximation register (SAR) logic is used to speed up the locking of the FLL, and truncation error cancellation (TEC) is performed in FDIVs to reduce delta-sigma-induced jitter. A prototype clock generator fabricated in a 65-nm CMOS process generates output clocks in the range of 1.5–100 MHz with a resolution of 24-kHz, 140-ps peak-to-peak period jitter, 6.8-ppm/°C inaccuracy, and can be turned on within 20 μs.**

***Index Terms*— Delta-sigma modulator, fractional divider (FDIV), frequency-locked loop (FLL), phase-locked loop (PLL), *RC* oscillator, ring voltage-controlled oscillator (VCO), temperature compensation.**

I. Introduction

THE demand for portable electronic devices with a small form factor and extended battery life is ever-increasing. Timing circuits impose several critical impediments in meeting this demand. For example, low-power microcontroller units that are vital components in portable devices use multiple crystal oscillators (XOs) and several on-chip fractional-N phase-locked loops (PLLs) to generate the desired clocks, which significantly increase board space, power consumption, and cost. Furthermore, XOs and PLLs cannot be turned on and off rapidly, severely limiting the ability to employ system-level power-reduction strategies such as power cycling.

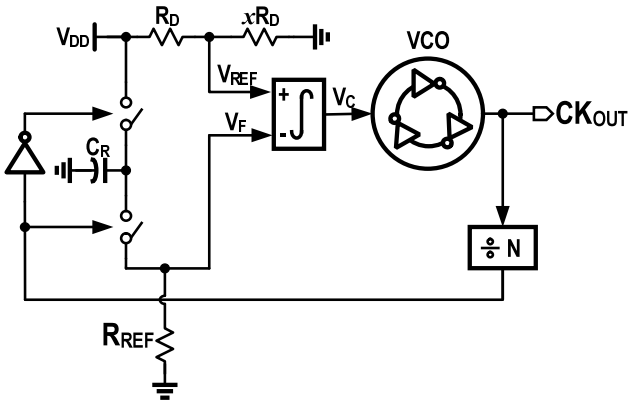

Fig. 1. Conventional FLL-based *RC* oscillator.

On-chip *RC*-based oscillators have recently garnered significant interest as attractive alternatives to traditional XO-based timing circuits [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18]. Among them relaxation oscillators are the simplest, occupy a small area, and can be turned ON/OFF instantaneously [1], [2], [3], [4], [5], [6], [7], but their frequency accuracy degrades significantly with temperature variations. Addressing this major drawback requires a temperature-compensated resistor and a comparator whose delay is a tiny fraction of the output clock period [4]. The need for such a high-speed comparator operating under severe power constraints significantly limits the output frequency below a couple of mega-Hertz.

Closed-loop frequency-locked loop (FLL)-based oscillators achieve excellent accuracy at high output frequencies by eliminating the need for a high-speed comparator [19]. The schematic of a conventional FLL-based oscillator is shown in Fig. 1. It uses the time constant ($R_{\text{REF}}C_R$) associated with the resistor, R_{REF}, and capacitor, C_R, as the reference time base and locks the period of a voltage-controlled oscillator (VCO) to a fraction of $R_{\text{REF}}C_R$. As a result, the output frequency temperature coefficient (TC) is dictated by the TC of the reference time constant. Recognizing the resistor TC

Manuscript received 10 July 2022; revised 23 October 2022; accepted 23 November 2022. Date of publication 19 December 2022; date of current version 24 February 2023. This article was approved by Associate Editor Yan Lu. This work was supported in part by the Semiconductor Research Corporation (SRC) under GRC Task 2810.036 and in part by Silicon Laboratories. *(Corresponding author: Yongxin Li.)*

Yongxin Li, Tianyu Wang, Ahmed Abdelrahman, Mohamed Badr Younis, Kyu-Sang Park, Ruhao Xia, Pavan Kumar Hanumolu are with the Department of Electrical and Computer Engineering (ECE), University of Illinois at Urbana–Champaign, Urbana, IL 61801 USA (e-mail: li204@illinois.edu).

Nilanjan Pal was with the Department of Electrical and Computer Engineering (ECE), University of Illinois at Urbana–Champaign, Urbana, IL 61801 USA. He is now with Texas Instruments, Dallas, TX 75243 USA.

Mostafa Gamal Ahmed was with the Department of Electrical and Computer Engineering (ECE), University of Illinois at Urbana–Champaign, Urbana, IL 61801 USA. He is now with Ain Shams University, Cairo 11566, Egypt, and also with Analog Devices Inc., Cairo, Egypt.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2022.3227139.

Digital Object Identifier 10.1109/JSSC.2022.3227139

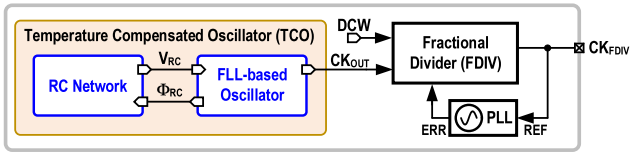

Fig. 2. Simplified block diagram of the proposed clock generator.

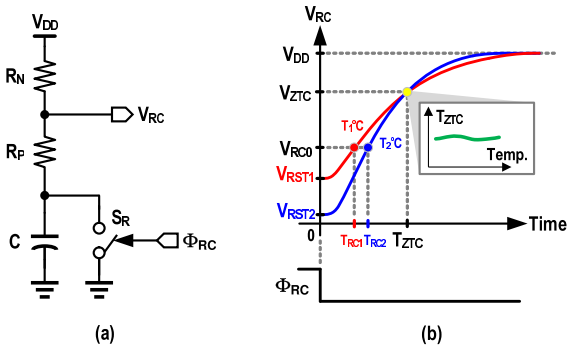

Fig. 3. RC-network. (a) Schematic. (b) Step response at two different temperatures.

dominates, many compensation schemes for implementing a temperature-insensitive resistor have been proposed, and excellent frequency accuracies are achieved using them [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18]. However, the FLL-based architecture suffers from two drawbacks not previously addressed. First, the bandwidth of the feedback loop is typically very low, in the order of a kHz, resulting in a long settling time that severely limits the efficacy of duty-cycled operation used in low-power devices. Second, these oscillators can only provide a single fixed frequency output, and replicating it to generate multiple outputs at digitally-programmable frequencies incurs a hefty area penalty.

This article presents a fast startup, a temperature-stable digital FLL-based oscillator, and low-jitter open-loop fractional dividers (FDIVs) that can provide programmable clock outputs. Fabricated in a 65-nm CMOS process, the prototype timing device can generate clocks from about 1.5–100 MHz with a frequency inaccuracy and resolution of 6.8 ppm/°C and 24 kHz, respectively.

The rest of the article is organized as follows. Section II presents the proposed architecture. Section III shows the details of the FDIV. Circuit implementation of key building blocks is described in Section IV. Experimental results from the prototype chips are presented in Section V. Key contributions of this article are summarized in Section VI.

II. Proposed Architecture

The simplified block diagram of the proposed clock generator is shown in Fig. 2 [20]. It comprises a digital FLL-based fast startup temperature-compensated oscillator (TCO), a low-jitter FDIV, and a digital PLL used for calibrating the FDIV. We first describe the TCO followed by FDIV in Section III.

TCO employs the RC network, depicted in Fig. 3(a), consisting of resistors R_N and R_P and a capacitor C, connected between the supply rails, $V_{\rm DD}$, and ground. To understand

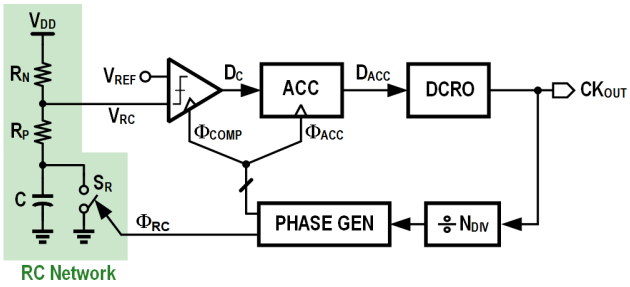

Fig. 4. Digital FLL used to lock DCRO's period to $T_{\rm ZTC}$.

how this RC network can be used to build an oscillator with excellent intrinsic temperature stability, consider the RC network's step responses at two temperatures, T_1 °C and T_2 °C, illustrated in Fig. 3(b). When the input Φ_{RC} is high ($\Phi_{RC} = 1$), switch S_R is closed, resetting the capacitor to ground and the output to $V_{RC} = V_{\rm RST} = V_{\rm DD} \cdot R_P/(R_P + R_N)$. Due to the temperature dependence of resistors, the output voltage is reset to $V_{\rm RST1}$ and $V_{\rm RST2}$, respectively. When a negative step is applied ($\Phi_{RC} = 1 \rightarrow 0$), S_R opens, causing the RC-network's output voltage, V_{RC}, to approach $V_{\rm DD}$ exponentially from $V_{\rm RST}$. The time taken by the output voltage to reach a voltage of V_{RC0}, denoted by T_{RC}, can be calculated using

$$T_{RC}(T) = -C(R_N(T) + R_P(T)) \times \ln\left[\left(1 - \frac{V_{RC0}}{V_{\rm DD}}\right)\frac{R_N(T) + R_P(T)}{R_N(T)}\right]. \quad (1)$$

Note that the temperature dependence of the resistors makes T_{RC} also a function of temperature, resulting in, in general, two different charging times T_{RC1} and T_{RC2}, at T_1 °C and T_2 °C, as shown in Fig. 3(b). We assume that the TC of the capacitor is negligible, a reasonable assumption in practice, and treat the capacitor as a constant in the above equation. Interestingly, by appropriately choosing the resistors and the capacitor in the RC network, V_{RC} can be made to reach $V_{\rm ZTC}$ after $T_{\rm ZTC}$ seconds, independent of temperature [1]. In other words,

$$T_{RC}(T_1) \approx T_{RC}(T_2) \approx T_{\rm ZTC} \text{ at } V_{RC} = V_{\rm ZTC}. \quad (2)$$

This is illustrated in Fig. 3(b), where the step responses at two temperatures, T_1 °C and T_2 °C, intersect at coordinates ($T_{\rm ZTC}$, $V_{\rm ZTC}$). ZTC stands for zero-TC to capture this temperature-independent behavior (at least to the first order). In our 65-nm CMOS processes, choosing $C = 9$ pF, R_P (unsalicided P+ diffusion resistor) = 80 kΩ, and R_N (unsalicided N+ poly resistor) = 55 kΩ resulted in a $T_{\rm ZTC} = 1.06$ μs. Having identified a stable time base in the form of $T_{\rm ZTC}$, we now describe how to build a temperature-insensitive frequency reference using it.

The schematic of digital FLL that generates a stable frequency reference by locking the period of a ring oscillator to $T_{\rm ZTC}$ is shown in Fig. 4. It consists of the RC network, a clocked comparator, a digital accumulator, a digitally controlled ring oscillator (DCRO), a frequency divider, and a phase generator. The frequency of DCRO's output, $CK_{\rm OUT}$, is divided by $N_{\rm DIV}$, and three clock phases, Φ_{RC}, $\Phi_{\rm COMP}$, and $\Phi_{\rm ACC}$, are generated from it, such that $\Phi_{\rm COMP}$'s positive edge is separated from the negative edge of Φ_{RC} by $N_{\rm DIV}/2$ output

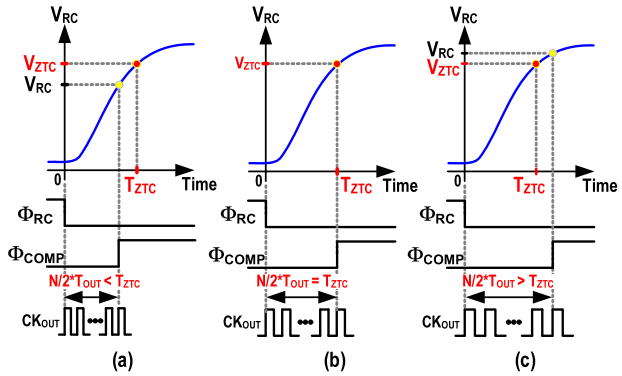

Fig. 5. Frequency error detection. (a) $F_{OUT} > F_{DES}$. (b) $F_{OUT} = F_{DES}$. (c) $F_{OUT} < F_{DES}$.

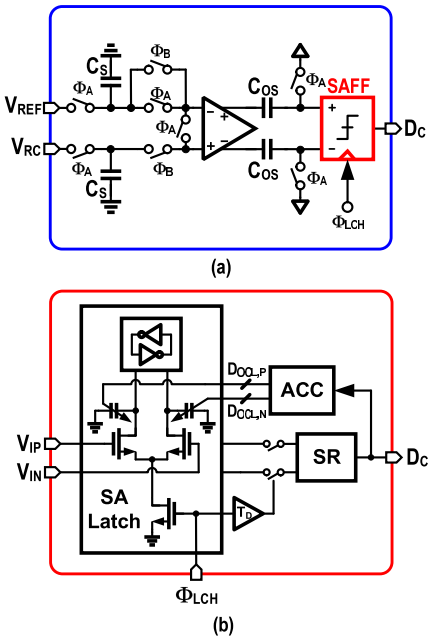

Fig. 6. (a) Offset-compensated comparator. (b) SAFF.

clock periods ($T_{OUT} \cdot N_{DIV}/2$). The factor of 2 in the expression appears because only half the divided clock period is allocated for RC charging.

As described earlier, when Φ_{RC} transitions from high to low, RC-network's output voltage, V_{RC}, starts settling toward V_{DD}. The clocked comparator samples V_{RC} on the rising edge of Φ_{COMP} and compares it with a reference voltage V_{REF} that is set to be equal to V_{ZTC}. If the sampled voltage is less than V_{ZTC}, the comparator outputs a logic one indicating Φ_{COMP} arrived early, as depicted in Fig. 5. In other words, it shows that the DCRO's period (T_{OUT}) is smaller than the target period, indicating DCRO is running faster. Similarly, if the comparator outputs a logic-low signal, it means that DCRO is running slow. The comparator output is integrated by a digital accumulator and used to tune DCRO's frequency. In the steady state, the average of the comparator output is zero, and the input voltage sampled by the comparator is V_{ZTC}, leading to an output period (T_{OUT}) and frequency (F_{OUT}) equal to

$$T_{OUT} = \frac{2T_{ZTC}}{N_{DIV}} \Longrightarrow F_{OUT} = \frac{N_{DIV}}{2T_{ZTC}}. \tag{3}$$

Thus, by making T_{ZTC} independent of temperature as described earlier, F_{OUT} becomes insensitive to temperature variations. However, in practice, the comparator's offset voltage severely degrades the TCO's stability. Denoting the input-referred offset voltage of the comparator by V_{OS}, T_{ZTC} and its temperature sensitivity can be expressed as a function of V_{OS} as follows:

$$T_{ZTC,OS}(T) = -C(R_N(T) + R_P(T)) \times \ln\left[\left(1 - \frac{V_{ZTC} + V_{OS}(T)}{V_{DD}}\right)\frac{R_N(T) + R_P(T)}{R_N(T)}\right] \tag{4}$$

$$\frac{\partial T_{ZTC,OS}}{\partial T} \approx \frac{\partial T_{ZTC,OS}}{\partial V_{OS}}\frac{\partial V_{OS}}{\partial T}. \tag{5}$$

Because V_{OS} has strong temperature dependence, T_{ZTC} and consequently F_{OUT} also becomes highly sensitive to temperature. We address this drawback by compensating the comparator's offset.

A. Offset-Compensated Comparator

The schematic of the offset-compensated comparator is shown in Fig. 6. It is composed of a preamplifier, a strong-arm latch-based flip-flop (SAFF), and a pair of offset-storage capacitors (C_{OS}) connected to the output of the preamplifier. The SR latch is disconnected from the SA latch during the SA latch's amplification and regeneration phases to prevent kickback. The SAFF's offset is suppressed by a coarse offset cancellation scheme in which its inputs (V_{IP}, V_{IN}) are shorted together, the circuit is clocked, and the decisions are accumulated in a register and used to control the amount of capacitance connected to drains of the input NMOS pair [21]. The unequal amount of capacitance added at the drain nodes compensates for the SAFF offset. Thirty-one thermometer-coded unit capacitors (1.4 fF) were added on each side to achieve an offset cancellation range and resolution of ± 40 and 1.3 mV, respectively. The preamplifier's gain (A_{PRE}) further attenuates the SAFF's offset, but the preamplifier itself introduces offset, which becomes the dominant source of the comparator offset. So, an output offset cancellation scheme depicted in Fig. 6(a) is used to mitigate it [22]. The operation of OCC is controlled by two nonoverlapping clock phases Φ_A and Φ_B. When Φ_A is high, and Φ_B is low, input voltages V_{REF} and V_{RC} are tracked onto capacitors (C_S), preamplifier inputs are shorted to V_{REF}, and the amplified offset ($A_{PRE}V_{OS}$) is stored on C_{OS}. When Φ_A and Φ_B are both low, C_S holds the sampled V_{RC}, and C_{OS} has the amplified offset voltage of the preamplifier. As soon as Φ_B goes high, the preamplifier amplifies the difference between the sampled voltages. At the rising edge of Φ_{LCH}, the comparator produces an output based on the amplified input voltage difference minus the stored preamplifier's offset voltage [$\approx A_{PRE}(V_{REF} - V_{RC})$]. The timing diagram can be found in Fig. 13. The simulated preamplifier gain is 45 V/V, and the sampling and offset-storage capacitors were chosen to be 990 and 588 fF, respectively. Monte-Carlo simulations (200 iterations) were performed to quantify the impact of the

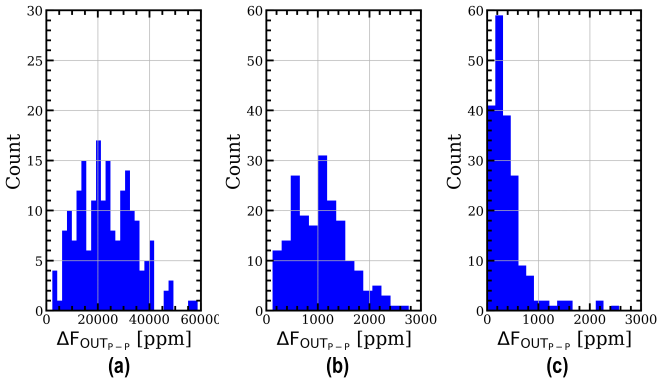

Fig. 7. Histograms of output frequency variation (a) without any compensation, (b) with the preamplifier's offset compensation, and (c) with both the preamplifier and SAFF offset compensation.

comparator offset on frequency error and the effectiveness of the offset-cancellation scheme in mitigating it. The results depicted in Fig. 7 show that without offset compensation, the mean and standard deviation of the peak-to-peak frequency variation ($\Delta F_{\mathrm{OUT_{P-P}}}$) over a temperature range of -40 °C to 80 °C is 23 518 and 10 910 ppm, respectively. The preamplifier's offset compensation reduces the mean variation by 20 times to 1222 ppm, and the standard deviation improves to 1044 ppm. The coarse cancellation of SAFF's offset further reduces the mean and standard deviations to 510 and 760 ppm, respectively.

B. Settling Time Improvement

The proposed TCO suffers from a long settling time like the conventional TCOs. The main reason for this drawback is the combination of the low update rate and small update step size. As depicted in Fig. 8, the output frequency starts from DCRO's free-running frequency F_{FR} and slews toward the desired output frequency F_{DES} in steps of DCRO's LSB (8.6 kHz in the prototype), resulting in a very long settling time. The locking process can be sped up by increasing the update step size, but this increases the dithering jitter because the comparator's nonlinearity causes the TCO's steady state to be a bounded limit cycle. To overcome this issue, we employ the successive approximation register (SAR) algorithm [23] and quickly bring the output frequency to the desired frequency (see Fig. 8). After the initial warm-up phase, the MSB of the K-bit SAR register is set to 1, causing the DCRO frequency to be in the middle of its tuning range. In the next update cycle, the second-most significant bit is set to 1, and the MSB is set based on the result of the first comparison. This binary search process continues until all the K bits in the SAR are tested, which takes only K updates to complete compared to at most 2^K updates in the conventional case. At the end of the SAR search, the control is handed back to the accumulator mode of operation.

III. Fractional Divider

The FDIV schematic is shown in Fig. 9. It comprises an edge combiner (EC), a multimodulus divider (MMD) controlled by a $\Delta\Sigma$ modulator, a digital-to-time converter (DTC), and a digital PLL for calibrating the DTC. A 17-bit digital

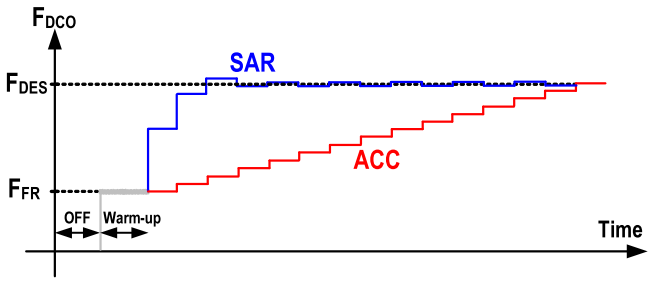

Fig. 8. DCRO's control code settling behavior.

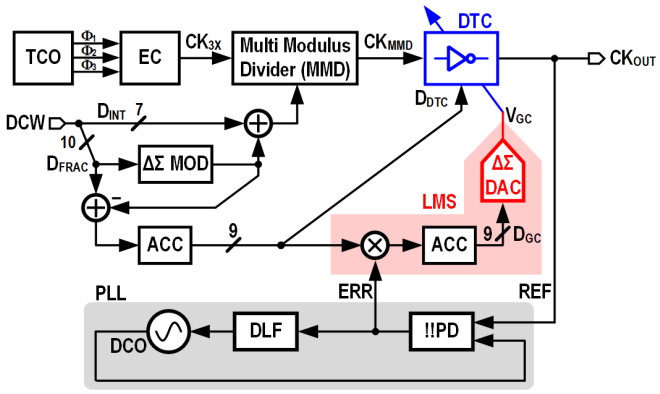

Fig. 9. FDIV with quantization error cancellation.

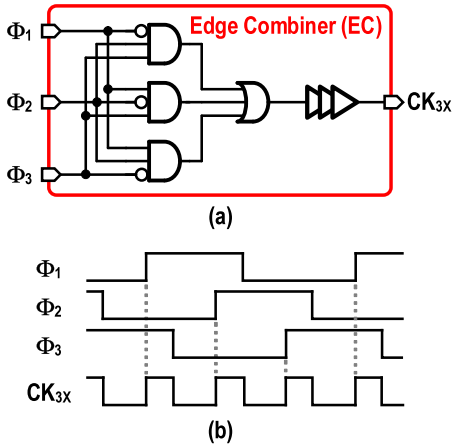

Fig. 10. (a) EC schematic and (b) its waveforms.

control word (DCW) controls the FDIV's output frequency. Of the 17-bits, 7-bits (D_{INT}) are used to set the integer division ratio, and the remaining 10-bits (D_{FRAC}) are used to set the fractional division ratio. D_{FRAC} is truncated to 1-bit using a first-order $\Delta\Sigma$ modulator, and the resulting output is added to D_{INT} and used to control the MMD [24]. The shaped truncation error of the $\Delta\Sigma$ modulator appears as a jitter in the FDIV's output clock. Note that in a typical fractional-N PLL where the $\Delta\Sigma$ FDIV is commonly used, the loop filter suppresses the truncation error and significantly reduces its impact on the PLL's output jitter. However, in the absence of such filtering, as in an open-loop FDIV, the truncation-error-induced jitter is prohibitively large (about one input CLK period, T_{IN}), severely limiting FDIV's usability.

We employ two mitigation techniques to reduce the jitter. First, FDIV's input clock frequency is increased by three

times, thereby reducing the $\Delta\Sigma$ modulator-induced jitter by a factor of 3 to about $T_{\rm IN}/3$. To this end, the outputs of three inverters in the DCRO ($\Phi_{1/2/3}$) are edge-combined to generate a clock, $\rm CK_{3X}$, at three times the DCRO output frequency as shown in Fig. 10. This frequency multiplication technique is susceptible to mismatches between the three inverters as phase spacing errors caused by them directly appear as jitter at the FDIV output. The jitter performance can be improved by upsizing the logic gates for edge combining and minimizing the routing mismatches in the layout. Note that the $\Delta\Sigma$ modulator is clocked at FDIV's output frequency, so the proposed frequency multiplication only incurs a minor power penalty in the first couple of stages in the MMD due to increased input frequency.

The EC reduces the aforementioned $\Delta\Sigma$ modulator-induced output jitter to $T_{\rm IN}/3$, but it is still prohibitively large in most applications. So, a second technique, truncation error cancellation (TEC), is employed to reduce the jitter further [25] (see Fig. 9). The TEC uses a DTC at the output of the MMD to add the right amount of delay and cancel the jitter caused by the $\Delta\Sigma$ modulator's truncation error. To this end, the truncation error is extracted by taking the difference between the $\Delta\Sigma$ modulator's input and output, accumulated to account for implicit integration due to frequency-to-phase conversion in the MMD before using it to control the DTC [25]. For this approach to be practical, the DTC gain must be tuned precisely such that the range of DTC is equal to one input clock period, a requirement difficult to guarantee in practice due to DTC's sensitivity to process, voltage, and temperature (PVT) variations. Therefore, the DTC gain is calibrated using a least-mean-square (LMS) algorithm running in the background [25]. However, unlike in [25], an error signal (ERR) needed for LMS adaptation is unavailable in the open-loop FDIV scenario. So, a separate digital PLL, implemented using a bang-bang phase detector (PD), a digital loop filter (DLF), and a digitally controlled oscillator (DCO), is used to generate the ERR, as depicted in Fig. 9. The LMS loop correlates the accumulated truncation error ($D_{\rm DTC}$) with the ERR signal and generates the DTC gain calibration code, $D_{\rm GC}$.

The DTC's schematic and gain-controlling circuitry are shown in Fig. 11. The DTC is implemented using a current-starved inverter. Its gain is tuned by starving the inverter of charging current using voltage $V_{\rm GC}$, generated from $D_{\rm GC}$ using a $\Delta\Sigma$ digital to analog converter (DAC). DTC delay is tuned by controlling the inverter's load capacitance with $D_{\rm DTC}$. The digital PLL was designed to occupy a small area and to turn on rapidly.

IV. Circuit Implementation

The detailed schematic of the proposed clock generator is shown in Fig. 12. As described earlier, a digital FLL locks DCRO's period to a temperature-insensitive time base provided by the RC network and SAR logic reduces the settling time significantly. The nominal steady-state DCRO frequency is about 133 MHz, and the feedback frequency division ratio ($N_{\rm DIV}$) is 282, which results in a loop update rate of 0.47 MHz. The timing diagram illustrating loop operation in more detail

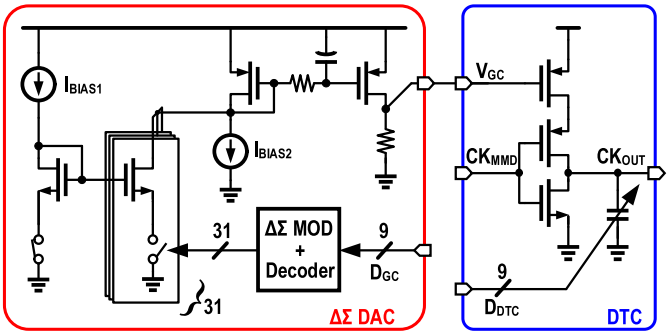

Fig. 11. DTC schematic along with its gain control circuitry.

is shown in Fig. 13. The phase generator produces all the clocks shown in the figure from the divided feedback clock. On the falling edge of Φ_{RC}, the RC network's output voltage V_{RC} starts charging exponentially toward $V_{\rm DD}$ and the voltage across the sampling capacitor C_S tracks V_{RC} until the falling edge of Φ_A. During this phase, the preamplifier's offset voltage is stored on capacitors $C_{\rm OS}$. The offset cancellation of the SAFF is also carried out during this period. On the rising edge of Φ_B, the voltage held on C_S is amplified by the preamplifier and sampled at the subsequent rising edge of $\Phi_{\rm LCH}$. The SAR logic and accumulator use the comparator's decision to update the DCRO control word $D_{\rm SAR}$. The frequency of DCRO needs to settle before the next RC charging starts; a requirement easily met in practice.

The circuit implementation of some critical blocks in the loop is described in Sections IV-A–IV-C.

A. RC Network

In the prototype manufactured in 65-nm CMOS processes, the RC network is implemented using $C = 9$ pF, R_P (unsalicided P+ diffusion resistor) = 80 kΩ, and R_N (unsalicided N+ poly resistor) = 55 kΩ. We provide the design considerations for choosing R_P, R_N, and C as follows. From the expression of the reference time constant shown in (1), and the temperature dependence of the resistors described by the following expressions:

$$R_N = R_{N,0}\left(1 + \Delta T \cdot tc_{1,N} + \Delta T^2 \cdot tc_{2,N}\right) \quad (6)$$

$$R_P = R_{P,0}\left(1 + \Delta T \cdot tc_{1,P} + \Delta T^2 \cdot tc_{2,P}\right) \quad (7)$$

it is easy to show that scaling the nominal resistance $R_{N,0}$ and $R_{P,0}$ by factor K results in scaling of T_{RC} by the same factor. Therefore, the normalized spread of T_{RC} across temperatures is independent of the scaling of the nominal resistance. In other words, when an oscillator is locked to the time constant T_{RC}, the temperature stability of its frequency is only determined by the TCs, and the ratio between $R_{N,0}$ and $R_{P,0}$. The design procedure used to size the RC network is described next. For a given set of TCs, the ratio between $R_{N,0}$ and $R_{P,0}$ is swept, and the temperature stability of T_{RC} is calculated. At each setting, the reference voltage V_{RC0} is set to $V_{\rm ZTC}$, which is found by sweeping V_{RC0} and finding the value that gives $T_{RC}(-40\ ^\circ\text{C}) = T_{RC}(85\ ^\circ\text{C})$. After fixing the ratio of resistors that achieve a T_{RC} with minimum temperature dependence, the

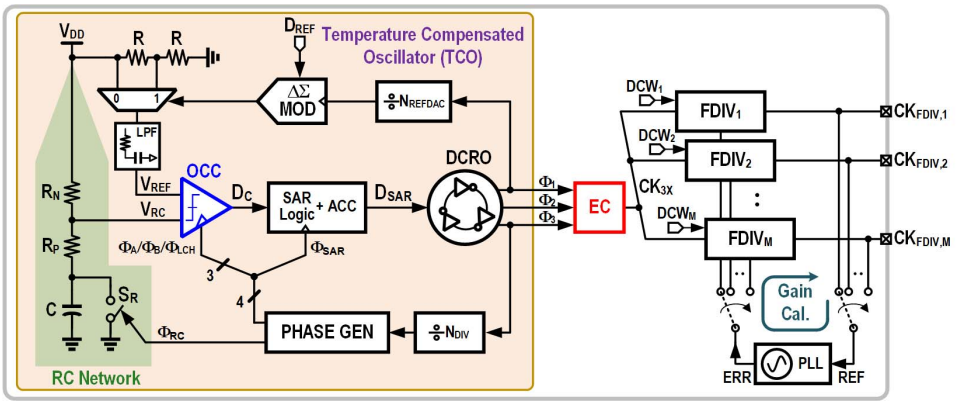

Fig. 12. Detailed block diagram of the proposed clock generator.

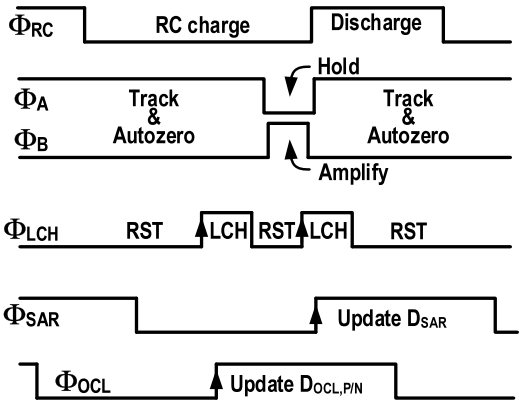

Fig. 13. Timing diagram of the FLL.

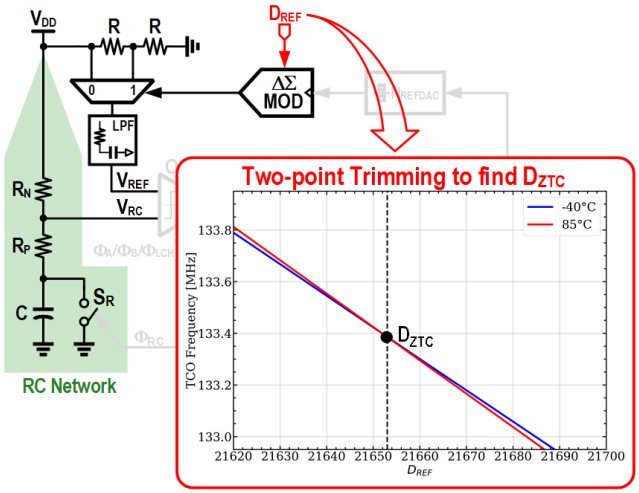

Fig. 14. Two-point trimming method.

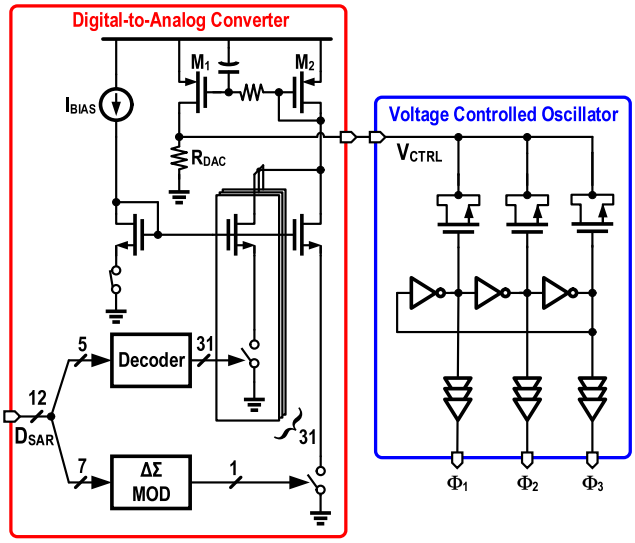

Fig. 15. Schematic of DCRO.

capacitance and absolute resistance are chosen. Note that T_{RC} scales linearly with the capacitance as well, so the capacitor does not affect the frequency stability. However, its value should be chosen to be much larger than the sampling capacitor connected to the output of the RC network so that the first-order settling response assumption is valid. To satisfy this condition, a 9-pF capacitor was selected. The resistance is then chosen to achieve a T_{RC} value of around 1 μs to provide ample time for operations such as voltage amplification, SA latch decision, DCRO control word generation, and DCRO settling. Global resistor variation across corners does not affect the temperature stability because it does not change the resistance ratio. Local resistor variation changes the ratio and therefore degrades the temperature stability. However, according to simulation, even with a 20% skew in resistance, the peak-to-peak inaccuracy of the reference time constant across the temperature is limited to 200 ppm.

B. Reference Voltage Generation

The reference voltage to the comparator, V_{REF}, is generated using a 15-bit second-order $\Delta\Sigma$ DAC. The $\Delta\Sigma$ modulator truncates the 15-bit digital input D_{REF} to one bit, which is converted to voltage using a simple 1-bit resistor DAC and filtered using a second-order RC low-pass filter. A two-point trimming method is used to determine V_{ZTC} in the form of the DCW D_{ZTC}. D_{REF} was swept at -40 °C and 85 °C, the corresponding output frequencies were recorded, and D_{ZTC} was found at the intersection point of the two frequency datasets, as shown in Fig. 14.

C. Digitally Controlled Ring Oscillator

The DCRO schematic is shown in Fig. 15. It consists of a DAC and a three-stage CMOS inverter-based

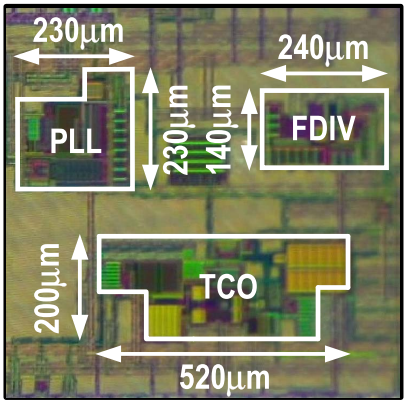

Fig. 16. Die micrograph.

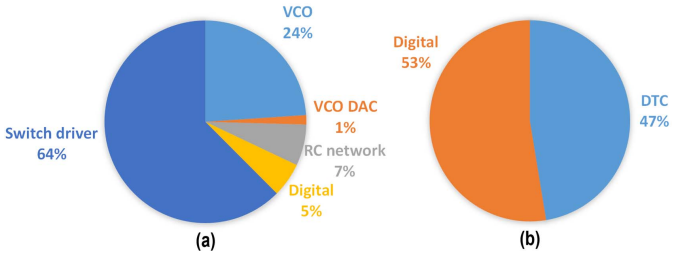

Fig. 17. Pie chart of power consumption. (a) TCO. (b) FDIV.

voltage-controlled ring oscillator (VCRO). The five most significant bits of the 12-bit input (D_{SAR}) are thermometer-coded and used to control 31 unit-cell current sources. The rest of the seven least significant bits are truncated to 1 bit using a $\Delta\Sigma$ modulator, and the resulting output controls one unit cell. The current from the 32 unit cells is summed and filtered using a first-order RC filter in the current mirror formed by devices M_1 and M_2. The filtered current is converted to control voltage, V_{CTRL}, using resistor R_{DAC}. The RO frequency is tuned with V_{CTRL} by varying the inverter's load capacitance, implemented using an MOS varactor. The simulated DCRO's tuning range and gain are 37 MHz and 8.6 kHz/LSB, respectively.

V. Measurement Results

A prototype clock generator was fabricated in a 65-nm CMOS process and packaged in a plastic QFN package. The die micrograph is shown in Fig. 16. The active area is 0.15 mm^2. The total power consumption of the TCO is 547 μW, and its breakdown is shown in Fig. 17(a). 64% of the power is consumed by the clock drivers, which are implemented using inverters operating at 1.8 V to drive the high-voltage (low-leakage) switches used in the RC branch and the OCC. The driver power can be significantly reduced by better transistor sizing in the driver. Transistor-level simulations indicate that 99% of the power of the clock drivers is consumed by the dc current in the first few stages of the inverter chain, which operates in the 1.8-V domain and with an input clock in the 1-V domain. Halving the size of the first inverter reduces the power by half at the expense of about a 30 ps increase in the driver output's delay. Since the drivers are used for the sampling switches in both the RC branch and the OCC, the extra 30 ps delay is common to Φ_{RC}, Φ_A, and Φ_B, resulting in a negligible change in the output frequency and its temperature stability. The power consumption of FDIV, shown in Fig. 17(b), is 464 μW at 100-MHz output frequency, of which the DTC consumes 244 μW, and the digital blocks (MMD, $\Delta\Sigma$ modulators, TEC logic) consume the remaining power. The power of FDIV reported in [20] is inaccurate as it included the power consumed by test circuitry used for monitoring purposes. The PLL consumes 1.2 mW, but the duty-cycling ratio will reduce its contribution to the total power consumption in the mission mode.

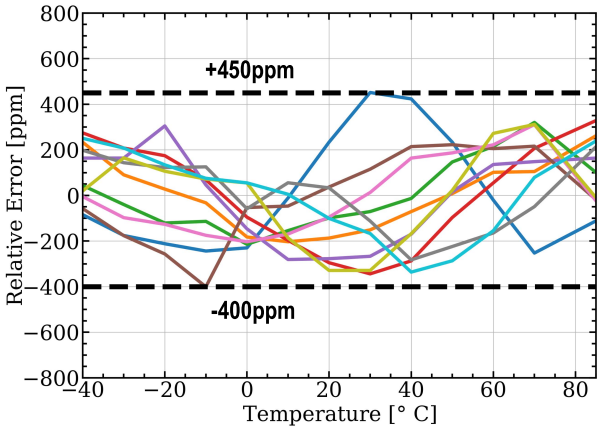

Fig. 18. Measured temperature stability.

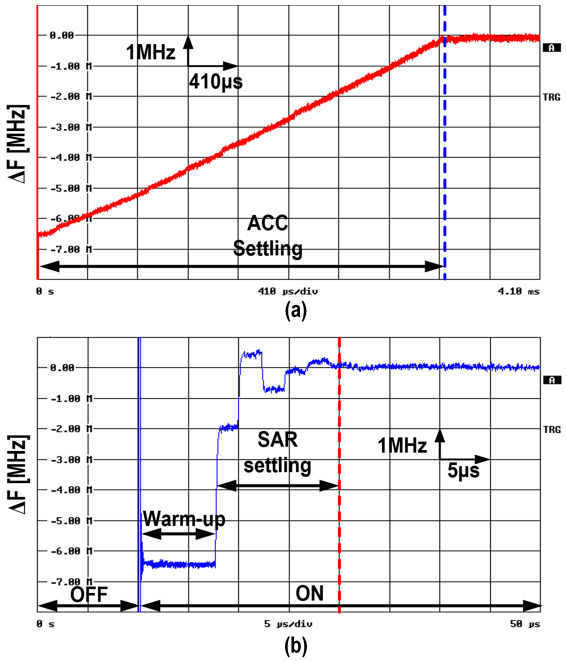

Fig. 19. FLL settling. (a) Accumulator mode. (b) SAR mode.

Fig. 18 shows the measured temperature stability of ten TCO samples. Each sample is trimmed at two temperatures (−40 °C and 85 °C), and the digital code D_{REF} to generate the optimal V_{ZTC} is written onto an on-chip register. The worst-case inaccuracy is 6.8 ppm/°C, illustrating the effectiveness of the proposed techniques in mitigating temperature sensitivities. The output frequency settling behavior during a power-on event shows the output frequency settles in less than

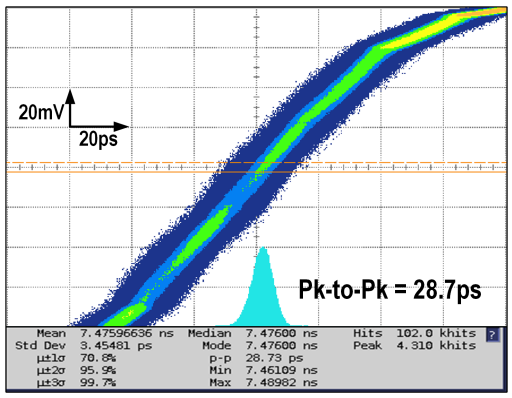

Fig. 20. Measured TCO period jitter.

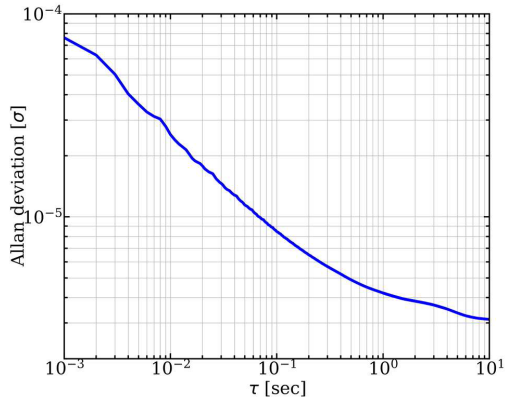

Fig. 21. Measured Allan deviation of the TCO.

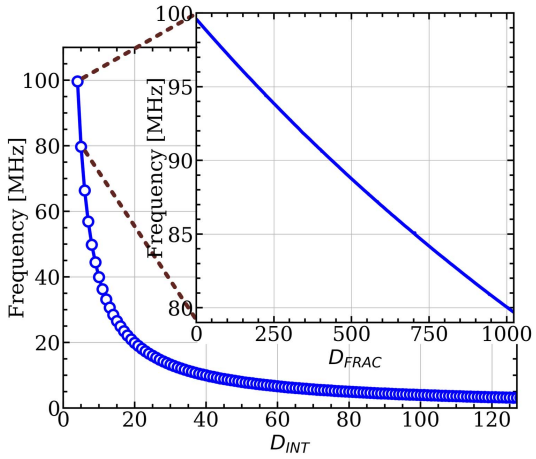

Fig. 22. Measured FDIV output frequency range.

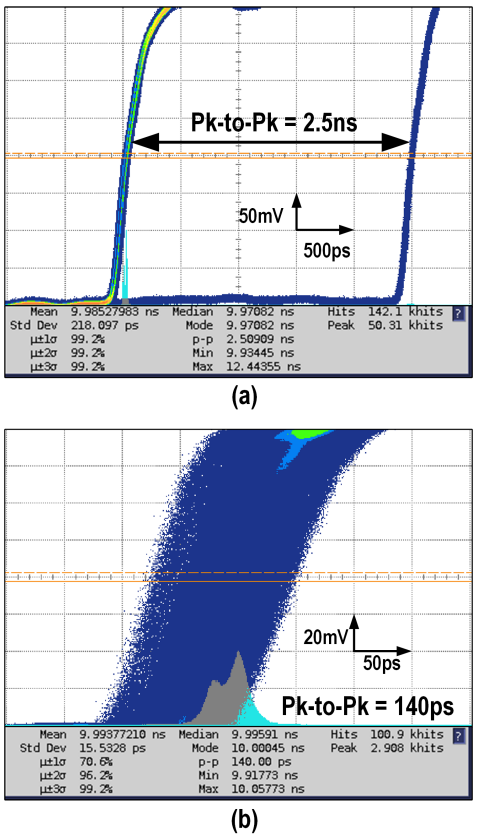

Fig. 23. FDIV output jitter (a) without TEC and (b) with TEC.

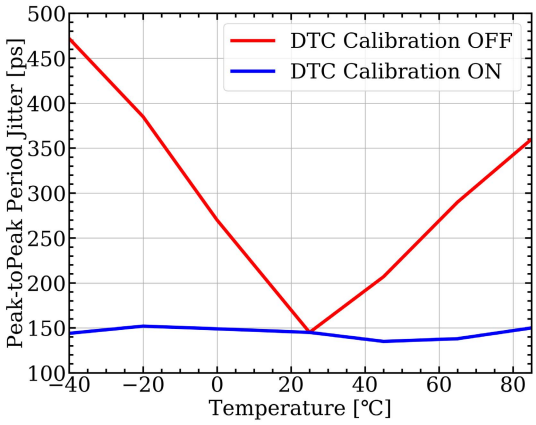

Fig. 24. Measured period jitter of FDIV versus temperature.

20 μs, compared to 3000 μs when the SAR-logic is disabled, as shown in Fig. 19. The initial 7.5 μs is allocated for the DCRO and other circuits to warm up, and the SAR logic takes 12.5 μs.

The TCO's peak-to-peak and rms period jitter at 133-MHz output frequency are 28 and 3.5 ps, respectively (see Fig. 20). Fig. 21 shows the measured Allan deviation in a 1-s stride is 4 ppm. The performance of the FDIV is presented next.

The measured FDIV output frequency versus the integer division control word (D_{INT}) shown in Fig. 22 indicates an output frequency range of 1.5–100 MHz is achieved. A sweep of the fractional division control word (D_{FRAC}) shows that the worst-case resolution is 24 kHz (see the inset of Fig. 22). The peak-to-peak period jitter when $D_{\mathrm{INT}} = 4$ and $D_{\mathrm{FRAC}} = 10$ ($F_{\mathrm{OUT}} \approx 100$ MHz) is 2500 ps when TEC is disabled. This large jitter is expected and equals one period of the 400-MHz FDIV input clock, as shown in Fig. 23. When the TEC is turned on, the peak-to-peak period jitter reduces to 140 ps across the entire temperature range.

When the DTC calibration code is fixed at its value at room temperature, the jitter degrades to 470 ps at -40 °C, indicating the necessity to perform background calibration (see Fig. 24). The period jitter along the signal path is illustrated in Fig. 25. The peak-to-peak period jitter is increased from 28.7 ps at the TCO output to 140 ps at the FDIV output.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART FLL-BASED *RC* OSCILLATORS

	This Work		Park [10] CICC21	Jiang [12] ISSCC21	Cristiano [15] VLSI20	Khashaba [9] JSSC21	Gurleyuk [14] JSSC22	Choi [13] JSSC21
Process	65nm		65nm	180nm	180nm	65nm	180nm	65nm
TC [ppm/°C]	6.8		2.1	5.2	8.7	8.4	1.4	2.56
Temperature range [°C]	−40 to 85		−40 to 95	−45 to 85	−15 to 85	−40 to 85	−45 to 85	−40 to 85
Trim points	2		3	1+batch		2	2+batch	
# of samples	10		20	18	10	6	20	16
Voltage sensitivity [ppm/V]	1000		83****	2000	3800	80****	1200	2900
Voltage range [V]	0.9 to 1.1 / 1.8*		1.1 to 2.5	1.6 to 2.0	1.8 to 2.0	1.1 to 2.3	1.6 to 2.0	0.85 to 1.05
Start-up time [μs]	20		1kHz*****	-		1kHz*****	50Hz*****	-
	TCO	FDIV						
Frequency [Hz]	133M/400M	1.5M to 100M	100M	16M	116k	32M	16M	28M
Frequency resolution[Hz]	-	24k	-					
RMS period jitter [ps]	3.5@133MHz	15.5@100MHz	13.4	10.2	-	24.4	39.9	7
Power [W]	547μ	464μ**	101μ	158μ	694n	34μ	220μ	142μ
Power efficiency [μW/MHz]	1.4@400MHz	4.6**@100MHz	1	9.9	5.98	1.06	13.8	5
Area [mm^2]	0.072	0.033+0.046***	0.19****	0.14	1.2	0.18****	0.3	0.06
ADEV floor [ppm]	3		1.3	0.35	4	2.5	0.32	2

* 1.8V is used for S_R in RC network and the sampling switches in OCC. Its supply sensitivity is negligible.
** The power consumption is smaller than the numbers reported in [20] because auxiliary output buffers were not excluded in [20].
*** The area overhead of the calibration PLL, 0.046mm^2, is amortized in the multi-output scenarios, where multiple FDIVs share one PLL.
**** With on-chip LDO.
***** No start-up time measurement. Loop bandwidth is shown instead as an indication of start-up time.

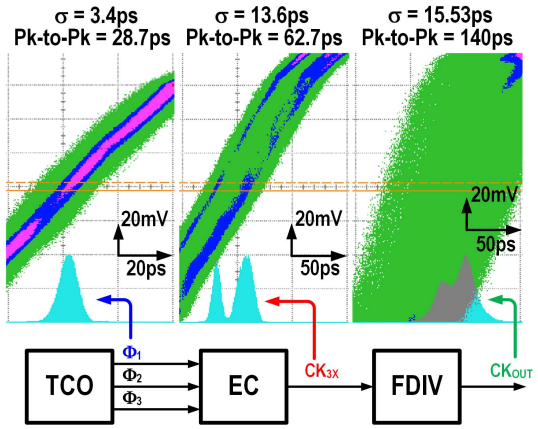

Fig. 25. Measured period jitter of TCO (133 MHz), EC (400 MHz), and FDIV (100 MHz) outputs.

The degradation is caused by both the deterministic jitter and random jitter introduced along the path. The deterministic jitter is mainly caused by the systematic and random mismatch between the three phases in the ring oscillator and the EC. In the prototype, the three inverter stages are placed sequentially, like the placement shown in Fig. 15. Therefore, the three inverter stages have different surroundings, and the routings between the three stages are unequal, thus causing a systematic mismatch. The mismatch caused by the random variation of the device parameters can be significant as well. Minimum-sized gates in the EC of the prototype can suffer from substantial mismatches, which can be reduced by upsizing the transistors. Apart from the deterministic jitter, the random jitter introduced by the DTC's thermal noise is another big source of jitter degradation, which can be significantly reduced by increasing the charging current and proportionally upsizing the capacitor.

The performance of the TCO is summarized and compared to state-of-the-art *RC* oscillators in Table I. The proposed TCO's temperature stability is comparable to the state-of-the-art. Still, it also achieves fast startup and provides output with digitally programmable output frequencies, two attributes not present in any of the reported *RC*-oscillator-based clock generators.

VI. CONCLUSION

A new clock generator capable of providing multiple temperature-compensated outputs with digitally programmable frequencies is presented. It locks the period of a ring oscillator to the temperature-insensitive time constant of the *RC* network and generates a temperature-stable output. The settling time of this locking loop is significantly reduced without sacrificing the jitter performance by using a binary search algorithm implemented using digital SAR logic. Multiple low-jitter outputs are generated using FDIVs in which the delta-sigma-induced jitter is reduced by canceling $\Delta\Sigma$ modulator's truncation error with a calibrated DTC placed at the output of the divider. A prototype clock generator fabricated in a 65-nm CMOS process generates output clocks in the range of 1.5–100 MHz with a resolution of 24-kHz, 140-ps peak-to-peak period jitter, 6.8-ppm/°C inaccuracy, and can be turned on within 20 μs, making it an attractive alternative for clock generators in low-power microcontrollers.

REFERENCES

[1] K.-K. Huang and D. D. Wentzloff, "A 1.2-MHz 5.8-μW temperature-compensated relaxation oscillator in 130-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 5, pp. 334–338, May 2014.
[2] Y. Tokunaga, S. Sakiyama, A. Matsumoto, and S. Dosho, "An on-chip CMOS relaxation oscillator with voltage averaging feedback," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1150–1158, Jun. 2010.
[3] K.-J. Hsiao, "A 32.4 ppm/°C 3.2–1.6V self-chopped relaxation oscillator with adaptive supply generation," in *Proc. Symp. VLSI Circuits*, Jun. 2012, pp. 14–15.

[4] A. Paidimarri, D. Griffith, A. Wang, A. P. Chandrakasan, and G. Burra, "A 120 nW 18.5 kHz RC oscillator with comparator offset cancellation for ±0.25% temperature stability," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 184–185.

[5] D. Griffith, P. T. Roine, J. Murdock, and R. Smith, "A 190 nW 33 kHz RC oscillator with ±0.21% temperature stability and 4ppm long-term stability," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 300–301.

[6] A. Savanth, J. Myers, A. Weddell, D. Flynn, and B. Al-Hashimi, "A 0.68 nW/kHz supply-independent relaxation oscillator with ±0.49%/V and 96ppm/°C stability," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 96–97.

[7] T. Wang et al., "A 6 μW 50 ppm/°C 1500 ppm/V 1.5 MHz RC oscillator using self-regulation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 8, pp. 1297–1301, Aug. 2019.

[8] M. Choi, S. Bang, T.-K. Jang, D. Blaauw, and D. Sylvester, "A 99 nW 70.4 kHz resistive frequency locking on-chip oscillator with 27.4ppm/°C temperature stability," in *Proc. Symp. VLSI Circuits*, Jun. 2015, pp. 238–239.

[9] A. Khashaba, J. Zhu, N. Pal, M. G. Ahmed, and P. K. Hanumolu, "A 32-MHz, 34-μW temperature-compensated RC oscillator using pulse density modulated resistors," *IEEE J. Solid-State Circuits*, vol. 57, no. 5, pp. 1470–1479, May 2022.

[10] K.-S. Park et al., "A second-order temperature compensated 1 μW/MHz 100 MHz RC oscillator with ±140ppm inaccuracy from −40°C to 95°C," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2021, pp. 1–2.

[11] C. Gurleyuk, L. Pedala, S. Pan, F. Sebastiano, and K. A. A. Makinwa, "A CMOS dual-RC frequency reference with ±200-ppm inaccuracy from −45°C to 85°C," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3386–3395, Dec. 2018.

[12] H. Jiang, S. Pan, C. Gurleyuk, and K. A. A. Makinwa, "A 0.14 mm^2 16 MHz CMOS RC frequency reference with a 1-point trimmed inaccuracy of ±400ppm from −45°C to 85°C," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 436–438.

[13] W. Choi, J. Angevare, I. Park, K. A. A. Makinwa, and Y. Chae, "A 0.9-V 28-MHz highly digital CMOS dual-RC frequency reference with ±200 ppm inaccuracy from −40°C to 85°C," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2418–2428, Aug. 2022.

[14] C. Gurleyuk, S. Pan, and K. A. A. Makinwa, "A 16 MHz CMOS RC frequency reference with ±90 ppm inaccuracy from −45°C to 85°C," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2429–2437, Aug. 2022.

[15] G. Cristiano, J. Liao, A. Novello, G. Atzeni, and T. Jang, "A 8.7ppm/°C, 694 nW, one-point calibrated RC oscillator using a nonlinearity-aware dual phase-locked loop and DSM-controlled frequency-locked loops," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2020, pp. 1–2.

[16] T. Jang, M. Choi, S. Jeong, S. Bang, D. Sylvester, and D. Blaauw, "A 4.7 nW 13.8ppm/°C self-biased wakeup timer using a switched-resistor scheme," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 102–103.

[17] G. Zhang, K. Yayama, A. Katsushima, and T. Miki, "A 3.2 ppm/°C second-order temperature compensated CMOS on-chip oscillator using voltage ratio adjusting technique," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1184–1191, Apr. 2018.

[18] P. Chen, D. Li, Z. Yu, Q. Jin, and K. Yang, "A 0.84 pJ/cycle wheatstone bridge based CMOS RC oscillator with reconfigurable frequencies," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2019, pp. 1–4.

[19] A. A. Abidi, "Linearization of voltage-controlled oscillators using switched capacitor feedback," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 3, pp. 494–496, Jun. 1987.

[20] Y. Li et al., "A 20 μs turn-on time, 24 kHz resolution, 1.5–100 MHz digitally programmable temperature-compensated clock generator with 7.5ppm/°C inaccuracy," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2022, pp. 1–2.

[21] P. Nuzzo, F. De Bernardinis, P. Terreni, and G. Van Der Plas, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.

[22] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

[23] A. E. AbdelRahman and S. A. Ibrahim, "A fast-locking all-digital clock and data recovery circuit using successive approximation," in *Proc. IEEE 59th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Oct. 2016, pp. 1–4.

[24] T. A. D. Riley, M. A. Copeland, and T. A. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 553–559, May 1993.

[25] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 2.9–4.0-GHz fractional-N digital PLL with bang-bang phase detector and 560-fs$_{rms}$ integrated jitter at 4.5-mW power," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2745–2758, Dec. 2011.

Yongxin Li (Graduate Student Member, IEEE) received the B.S. and M.S. degrees in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Urbana, IL, USA, in 2017 and 2020, respectively, where he is currently pursuing the Ph.D. degree.

He was an Intern with the Silicon Photonics Link Group, Cisco, Allentown, PA, USA, in 2019 and 2020, and was with the FPD Link Group, Texas Instruments, Santa Clara, CA, USA, in 2021. His research interests include clocking circuits and high-speed links.

Nilanjan Pal (Member, IEEE) received the B.Tech. and M.Tech. degrees in electronics and electrical communications engineering from IIT Kharagpur, Kharagpur, India, in 2015, and the Ph.D. degree from the Department of Electrical and Computer Engineering, University of Illinois at Urbana–Champaign, Urbana, IL, USA, in 2021.

From 2015 to 2017, he was an Analog Design Engineer with Analog Devices, Inc., Cairo, Egypt, where he was involved in designing low dropout regulators (LDOs), temperature-compensated ring oscillators, and very low-current measurement modules. He is currently with Texas Instruments, Dallas, TX, USA, where he works on high-efficiency dc–dc converters.

Tianyu Wang (Student Member, IEEE) received the B.S. and M.S. degrees from the University of Illinois at Urbana–Champaign, Urbana, IL, USA, in 2015 and 2018, respectively, where he is currently pursuing the Ph.D. degree.

His research interests are power-efficient wireline SerDes systems.

Mostafa Gamal Ahmed (Member, IEEE) received the B.Sc. (Hons.) and M.Sc. degrees in electrical engineering from Ain Shams University, Cairo, Egypt, in 2011 and 2015, respectively, and the Ph.D. degree from the University of Illinois at Urbana–Champaign, Urbana, IL, USA, in 2021.

From 2011 to 2015, he was with Si-Ware Systems, Cairo, designing high-performance clocking circuits and LC-based reference oscillators. From June 2016 to August 2017, he was with Elenion, New York, NY, USA, developing limiting/linear TIAs and optical modulator drivers for direct detection and coherent optical links. In 2021, he was a Post-Doctoral Research Associate with the University of Illinois at Urbana–Champaign. He is currently an Assistant Professor with the Faculty of Engineering, Ain Shams University. He is also with Analog Devices Inc., Egypt. His current research interests include high-speed optical communication links, clocking circuits, and RF/millimeter-wave circuits.

Ahmed Abdelrahman (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from Ain Shams University, Cairo, Egypt, in 2011 and 2017, respectively. He is currently pursuing the Ph.D. degree in electrical engineering with the University of Illinois at Urbana–Champaign, Champaign, IL, USA.

From 2011 to 2019, he was a Staff Analog/RF Design Engineer with Si-Ware Systems, Cairo, designing high-performance LC reference oscillators and RF power delivery transceivers. His current research interests are high-speed coherent electrical/optical communication links and clocking circuits.

Mr. Abdelrahman is a two-year recipient of the Andrew T. Yang Research and Entrepreneurship Award from the University of Illinois at Urbana–Champaign for the period 2020–2022.

Mohamed Badr Younis (Student Member, IEEE) received the B.Sc. degree in communications and computer engineering and the M.Sc. degree in electronics and communications engineering from Cairo University, Giza, Egypt, in 2016 and 2019, respectively. He is currently pursuing the Ph.D. degree in electrical and computer engineering with the University of Illinois at Urbana–Champaign, Champaign, IL, USA.

Since graduating in 2016, he has been working as a Teaching Assistant with the Department of Electronics and Electrical Communications Engineering, Cairo University. Alongside being a Teaching Assistant, he has worked as a part-time Analog/Mixed-Signal Design Engineer with Si-Ware Systems (currently Goodix), Cairo, Egypt, from 2016 to 2019. With Si-Ware Systems, he has participated in research, design, verification, and testing activities for their timing and low-speed RF products and IPs.

Kyu-Sang Park (Graduate Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 2008 and 2010, respectively. He is currently pursuing the Ph.D. degree with the University of Illinois at Urbana–Champaign, Champaign, IL, USA.

In 2018, he joined the University of Illinois at Urbana–Champaign. From 2010 to 2018, he was a Senior Engineer with GCT Semiconductor and Anapass, Seoul, South Korea, where he worked on CMOS RF transceivers for cellular products and high-speed links for mobile display interface systems. He completed internships with Intel, Hillsboro, OR, USA, and Analog Devices, Wilmington, MA, USA. During these internship periods, he performed research on low-jitter clock generation and distribution for ultra-high-speed wireline transceivers and high-speed data converters. His current research interests include temperature-compensated oscillators and high-speed links.

Mr. Park is a recipient of the Analog Devices Outstanding Student Designer Award in 2022.

Ruhao Xia (Student Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Illinois at Urbana–Champaign, Urbana, IL, USA, in 2019, where he is currently pursuing the Ph.D. degree.

His current research interests include temperature-compensated on-chip oscillators and optical transmitters.

Pavan Kumar Hanumolu (Fellow, IEEE) received the Ph.D. degree from the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR, USA, in 2006.

He subsequently served as a Faculty Member with Oregon State University till 2013. He is currently a Professor with the Department of Electrical and Computer Engineering, University of Illinois at Urbana–Champaign, Urbana, IL, USA. His research interests include energy-efficient integrated circuit implementation of wireline communication systems, analog and digital signal processing, sensor interfaces, and power conversion.

Dr. Hanumolu was the Editor-in-Chief of the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2019 to 2022.