A Highly Integrated Hybrid DC–DC Converter With nH-Scale IPD Inductors

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***Abstract*— This article presents a new integrated step-down dc–dc hybrid converter that uses only nano-Henry scale inductors at 2–5-MHz switching frequency. Since it is derived from a Dickson-star switched capacitor (SC) converter, the proposed converter inherits the benefit of low voltage stress on switches while enjoying an efficient fine regulation by phase shift, similar to a dual active bridge (DAB) converter. The converter is optimized, designed, and fabricated in 1.7 × 1.9 mm area of a 130-nm bipolar-CMOS-DMOS (BCD) process. The active die is flip-chipped on a 6.5 × 6.5 mm package substrate together with power capacitors and two 10-nH integrated passive device (IPD) inductors for demonstration, illustrating the feasibility of passive components' integration, resulting in a peak efficiency of 91.2% and a peak power density of 1.36 W/mm^3 from 9.6–12-V input to 2.15–3.3-V output. Another demonstration is constructed on the same package substrate but with discrete air-core inductors. It achieves a peak efficiency of 92.4% and a peak power density of 0.62 W/mm^3, while delivering a max power of 7.5 W. To achieve the performance, a detailed loss analysis and a unique optimization methodology for the converter, together with the design of key sub-blocks, including gate drivers (GDs), phase shift modulator (PSM), and ramp generator (RG), are provided in this article.**

***Index Terms*— DC–DC conversion, hybrid converter, inductors integration, phase shift modulation, power management integrated circuits, switching converters.**

I. Introduction

WHEN reviewing the history of electronic devices, there is a noticeable trend of dimension shrinking. A computer, for example, changes from a gigantic machine when it was first invented, to a portable device that is used in everyday life. However, to satisfy boosting computation capability and enriching of available features, the power density that these electronic devices require has been continuously increasing [1], [2], making the power delivery design more and more challenging. Even though active devices benefit from semiconductor technology scaling, passive devices, particularly the magnetics, do not keep up with the rate of scaling and miniaturization [3]. As a consequence, inductors dominate the size of modern power converter implementations. In other words, to diminish the board dimension and increase the power density, it is important to reduce the required inductance and the inductor size.

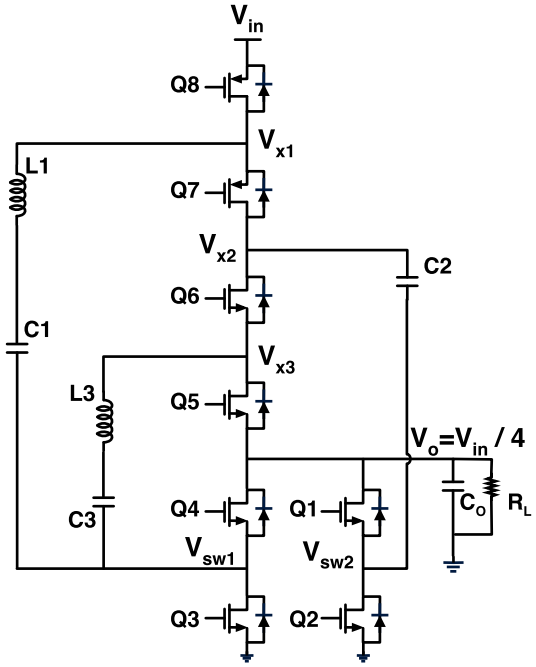

Fig. 1. Schematic of the proposed ITSAB converter.

In addition to improving the quality of inductors, significant efforts have been invested in coming up with new converter topologies and different operating principles to reduce the required inductance [4], [5], [6], [7], [8]. Switched capacitor (SC) converters, which require no inductors, are good candidates for realization of fully integrated power converters [9], [10], [11]. However, drawbacks of an SC converter include significantly degraded efficiency when operating away from the nominal conversion ratio, and large output noise with variable frequency that could cause EMI issues in the system. Apart from the SC converters, the most straightforward approach to minimize inductance is operating a power converter at very high frequency (VHF) [12], [13]. However, the benefit of reduced inductance comes with increased switching losses leading to reduced efficiency. In an another effort to use less inductance, resonant or quasi-resonant converters are employed. Unfortunately, output regulation is often challenging for converters with a resonant tank while satisfying high

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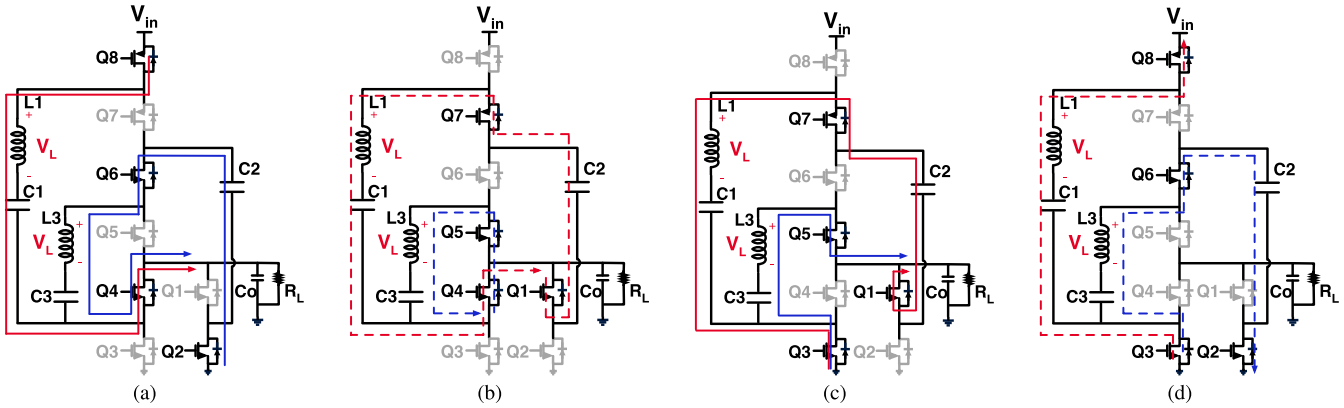


Fig. 2. Power stage operation of the ITSAB converter. (a) State 1. (b) State 2. (c) State 3. (d) State 4.

efficiency and small size requirements. The quasi-resonant converter demonstrated in [5] was a successful demonstration of this type of converter, capable of regulation at relatively low switching frequency. However, its efficiency is relatively low, and more importantly, the 36 nH inductor used is still large, which makes it difficult for ON-chip realization. Further increasing the switching frequency to achieve a smaller inductor would face significant challenge in maintaining high efficiency [3]. Therefore, new topologies that efficiently utilize inductors are emerging, such as hybrid converters [4], [6], [7], [8], [14], [15]. With the help of capacitors that block high dc voltage, the inductors are magnetized with much lower voltage such that smaller inductors can be used. Nonetheless, most of the previously proposed hybrid converters are based on discrete-circuit realizations, still requiring inductances in the range of 100 nH or larger.

Starting from the preliminary discrete-circuit implementation in [16] and [17], the ITSAB converter in this work strives to achieve superior power density based on a combination of novel operation and topology requiring inductors in the nH range, while operating at modest switching frequency in the MHz range. The small inductance enables the use of integrated passive devices (IPDs) combined with an advanced packaging effort to further improve the overall power density [18]. Operation of the ITSAB power stage and its dc characteristics are described in Section II. A detailed loss analysis is presented in Section III. Optimization of the ITSAB power stage is addressed in Section IV. Section V introduces the design of the key sub-blocks and the control loop for a 12-V ITSAB converter prototype realized in a 130-nm bipolar-CMOS-DMOS (BCD) process, with the active die flip-chipped on a package substrate together with power stage capacitors and two 10-nH inductors. The experimental results are provided in Section VI. Finally, this article is concluded in Section VII.

II. Power Stage Topology and Operation

Fig. 1 shows the power stage of the proposed ITSAB converter. It consists of two p-type power switches $Q7$ and $Q8$, six n-type power switches $Q1$–$Q6$, three flying capacitors $C1$–$C3$, and two nH-scale inductors $L1$ and $L3$. The proposed converter can be viewed as adding inductors to the flying capacitors of a Dickson-star SC converter. The presence of these inductors helps with soft-charging the flying capacitors to achieve high efficiency. Although the circuit topology resembles the prior works that rely on resonant operation [5], [19], [20], [21], the ITSAB converter has completely different operation that enables the use of nH-scale inductors at moderate switching frequency. A detailed comparison between these topologies has been presented in [16].

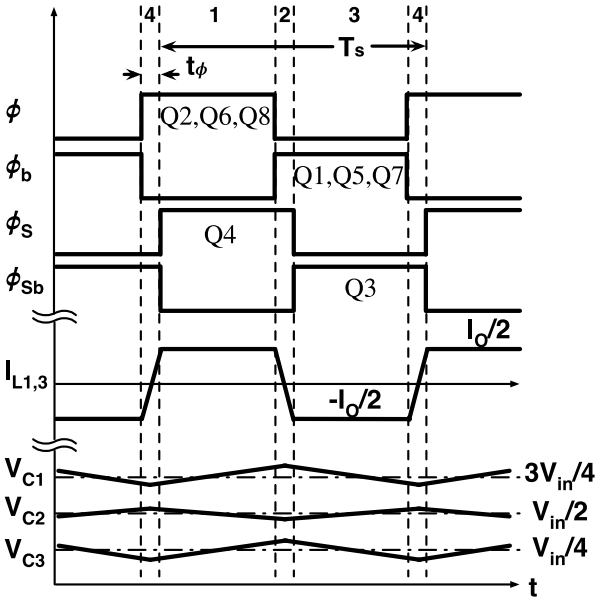


Fig. 3. Operating waveforms in the ITSAB converter.

The operation of the ITSAB converter can be divided into four different states as shown in Fig. 2. Two phases of gate control signals, ϕ–ϕ_b and ϕ_S–ϕ_{Sb}, are illustrated in Fig. 3 together with the waveforms of the inductor currents and flying capacitor voltages. Phase ϕ_S–ϕ_{Sb} is shifted by t_ϕ from ϕ–ϕ_b forming the two phase shift states 2 and 4. The operation of the capacitor charge transfer in the ITSAB converter resembles that of a Dickson-star SC converter. The key difference is that the charge transfer between flying capacitors and to the output in the Dickson-star SC converter is hard-charging, while it is soft-charging in the ITSAB using the two inductors $L1$ and $L3$. As a result, the steady-state voltages across $C1$, $C2$, and $C3$ is (3 $V_{\text{in}}/4$), ($V_{\text{in}}/2$), and ($V_{\text{in}}/4$), respectively. Unlike the resonant switched-capacitor (ReSC) converters in [22] and [5],

the passive components values are selected to ensure $L1$ ($L3$) and $C1$ and $C2$ ($C3$ and $C2$) tank resonant frequency is well below the switching frequency f_s.

State 1: Unique in this converter, both the inductors carry near-constant $I_o/2$ currents to the output as a result of near-zero voltage across each of the inductors during this time interval. Subsequently, both the flying capacitors $C1$ and $C3$ are softly charged, while $C2$ is softly discharged, all by the same amount of current.

State 2: This phase shift time interval starts when all the switches toggle except for $Q3$ and $Q4$. As a consequence, both the inductors have $V_L = -V_{\text{in}}/4$ across them, which is the voltage of $C3$ for $L3$ and the voltage difference across $C1$ and $C2$ for $L1$. As the result, both the inductor currents ramp down to zero and then continue ramping up in the opposite direction. All the flying capacitors shift their charging/discharging status during this time interval when the inductor currents are zero. This state ends when $Q3$ and $Q4$ change their ON/OFF status as the inductor current reaches approximately $-I_o/2$.

State 3: This state is the same as State 1, except the inductor currents are flipped. The capacitors' charging status is also altered.

State 4: Inductor currents are flipped compared with State 2. The voltages across the inductors are $V_L = V_{\text{in}}/4$.

During the two phase shift States 2 and 4, the inductor currents ramp up and down at the same rate of

$$\frac{di_L}{dt} = \frac{V_{\text{in}}}{4L}. \tag{1}$$

From charge balance, the output current I_o can be found as [16]

$$I_o = \frac{V_{\text{in}}}{8Lf_s}\phi(1-\phi) \tag{2}$$

where $\phi = (2t_\phi/Ts)$ is the phase shift ratio. Therefore, by modulating t_ϕ, I_o and thus the output voltage V_o can be regulated.

The length of t_ϕ depends on the inductance, the load current, and the input voltage. Practically, it is in nano-second range when using nano-Henry inductors, considering 1-A output current and 12-V input voltage. The trapezoidal shape with ripple-free maximum values of currents I_{L1} and I_{L3} not only leads to small rms value and thus small conduction loss but also results in small output voltage ripple. This eventually reduces the required output capacitance, which further contributes to high power density.

As an additional benefit of flipping the inductor current flowing direction, at the end of States 2 and 4, the switching node V_{sw1} is fully soft-discharged and soft-charged by the inductor currents during the deadtime of ϕ_S and ϕ_{Sb}, as illustrated in Fig. 4. Consequently, $Q3$ and $Q4$ are fully soft-switched. On the contrary, I_{L3} and I_{L1} keep forward biasing the body diodes of $Q2$ and $Q1$ during the deadtime between States 1 and 2, and the one between States 3 and 4, respectively. In other words, $Q1$ and $Q2$ are hard-switched. Meanwhile, the switches $Q5$–$Q8$ are partially soft-switched, because the switching nodes V_{x1-3} are partially charged/discharged by I_{L1} and I_{L3} while being impacted by

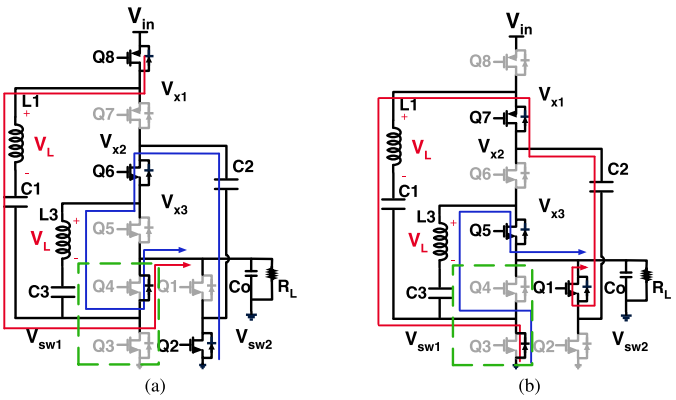


Fig. 4. ZVS of Q3 and Q4 between (a) States 4 and 1 and (b) States 2 and 3.

hard-switching node V_{sw2}. As an example, V_{x1}, also the source of $Q7$, is soft-charged to V_{in} by I_{L1} once $Q7$ is turned off at the end of state 3. When $Q1$ and $Q2$ hard-switch in State 4, V_{x2} jumps from 3 $V_{\text{in}}/4$ to $V_{\text{in}}/2$ causing drain-to-source capacitor C_{ds} of $Q7$ being hard-charged. Even though $Q1$ and $Q2$ are hard-switched, they are half the size of the switches $Q3$ and $Q4$ because they carry half the current and thus cause lower additional switching loss. Because of the zero-voltage-switching (ZVS) operation, the ITSAB power stage can operate efficiently at switching frequency in the MHz range.

III. Loss Analysis

The power loss of the ITSAB converter can be categorized into two major parts: conduction loss and switching loss. To accurately calculate the conduction loss, the rms value of the inductor currents is needed. In this section, the detailed loss analysis with rms current value calculation is given.

A. Conduction Loss

The conduction loss can be written as

$$\begin{aligned} P_{\text{cond}} = &\sum_{i=7}^{8} R_{\text{ON}_i} I_{L1,\text{rms}}^2 + \sum_{i=5}^{6} R_{\text{ON}_i} I_{L3,\text{rms}}^2 \\ &+ \sum_{i=3}^{4} R_{\text{ON}_i} I_{L1+L3,\text{rms}}^2 \\ &+ R_{\text{ON}_2} I_{L3,\text{rms}}^2 + R_{\text{ON}_1} I_{L1,\text{rms}}^2 \end{aligned} \tag{3}$$

where R_{ON_i} is the ON-resistance of each power switch, and $I_{L1,\text{rms}}$ and $I_{L3,\text{rms}}$ are the rms current of $L1$ and $L3$, respectively. While the inductor currents are displayed in Fig. 3 as having an ideally trapezoidal shape with $(I_o/2)$ value at the top, they slightly curve in practice owing to the response of the LC tank network with parasitic series resistances. To improve the conduction loss model accuracy, it is necessary to include these effects in calculation of the current rms values.

The approach described in [23] can be extended to the 4-to-1 ITSAB circuit. In each switch state shown in Fig. 2, the state-space equation can be written as

$$\dot{x} = A_i x + b_i V_{\text{in}}, \quad i = 1, 2, 3, 4 \tag{4}$$

where $x = [i_{L1}, i_{L3}, v_{C1}, v_{C3}, v_{C2}, v_O]^T$ and

$$A_1 = \begin{vmatrix} -\frac{Rs}{L1} & 0 & -\frac{1}{L1} & 0 & 0 & -\frac{1}{L1} \\ 0 & -\frac{Rs}{L3} & 0 & -\frac{1}{L3} & \frac{1}{L3} & -\frac{1}{L3} \\ \frac{1}{C1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C3} & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C2} & 0 & 0 & 0 & 0 \\ \frac{1}{Co} & \frac{1}{Co} & 0 & 0 & 0 & -\frac{1}{R_L Co} \end{vmatrix}$$

$$b_1 = \begin{vmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{vmatrix}$$

$$A_2 = \begin{vmatrix} -\frac{Rs}{L1} & 0 & -\frac{1}{L1} & 0 & \frac{1}{L1} & 0 \\ 0 & -\frac{Rs}{L3} & 0 & -\frac{1}{L3} & 0 & 0 \\ \frac{1}{C1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C3} & 0 & 0 & 0 & 0 \\ -\frac{1}{C2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{R_L Co} \end{vmatrix}, \quad b_2 = \begin{vmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{vmatrix}$$

$$A_3 = \begin{vmatrix} -\frac{Rs}{L1} & 0 & -\frac{1}{L1} & 0 & \frac{1}{L1} & \frac{1}{L1} \\ 0 & -\frac{Rs}{L3} & 0 & -\frac{1}{L3} & 0 & \frac{1}{L3} \\ \frac{1}{C1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C3} & 0 & 0 & 0 & 0 \\ -\frac{1}{C2} & 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{Co} & -\frac{1}{Co} & 0 & 0 & 0 & -\frac{1}{R_L Co} \end{vmatrix}, \quad b_3 = \begin{vmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{vmatrix}$$

$$A_4 = \begin{vmatrix} -\frac{Rs}{L1} & 0 & -\frac{1}{L1} & 0 & 0 & 0 \\ 0 & -\frac{Rs}{L3} & 0 & -\frac{1}{L3} & \frac{1}{L3} & 0 \\ \frac{1}{C1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C3} & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{R_L Co} \end{vmatrix}$$

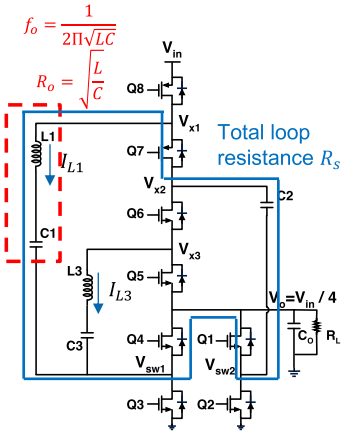


Fig. 5. Definitions of parameters f_o, R_o, and R_s.

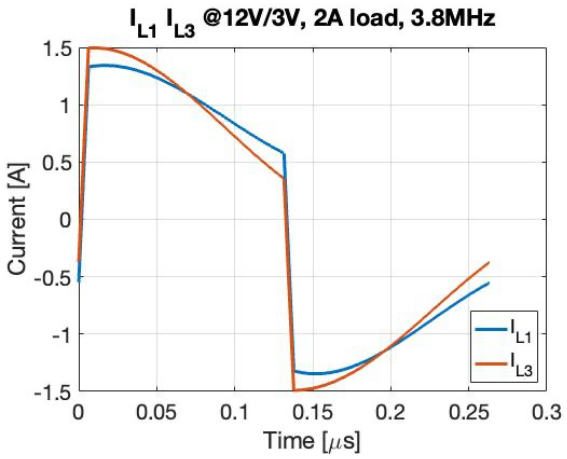


Fig. 6. Calculated I_{L1}, I_{L3} waveforms for 12–3-V conversion, 2-A load, $f_s = 3.8$ MHz, with $R_s = 55$ mΩ.

$$b_4 = \begin{vmatrix} \frac{1}{L1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{vmatrix} \tag{5}$$

where R_s is the total loop resistance as drawn in Fig. 5.

To numerically compute the inductor currents at various time, the augmented state-space approach [24] is used in this work. It provides a viable way to accurately calculate the exact solution of the aforementioned state-space equations, especially when the system matrix A_i is singular. Examples of the computed I_{L1} and I_{L3} are plotted in Fig. 6, assuming $R_s = 55$ mΩ. When the load current is 2 A, and each inductor delivers 1 A on average, with ∼1 A ripple during States 1 and 3. One may note how the exact rms values of these currents are higher than ideal $I_o/2$, which yields a more accurate conduction loss evaluated from (3).

B. Switching Loss

Switching loss is primarily related to power switches' gate capacitances C_{gg} and the parasitic capacitors of the switching nodes, namely, C_{X1}, C_{X2}, C_{X3}, C_{SW1}, and C_{SW2}. The gate

capacitors switching loss can be written as

$$P_{\text{gate}} = \sum_{i=1}^{8} C_{\text{ggi}} V_{\text{DD}}^2 f_s \tag{6}$$

where V_{DD} is the V_{GS} driving voltage for the power switches. As mentioned in Section II, $Q5$–$Q8$ are partially soft-switched, $Q3$ and $Q4$ are fully soft-switched, while $Q1$ and $Q2$ are completely hard-switched. Therefore, the total switching loss of the switching nodes' parasitic capacitors can be approximated by

$$P_{\text{coss}} = \left(\sum_{i=1}^{3} \frac{1}{2} C_{Xi} + C_{\text{SW2}}\right) V_{\text{ds}}^2 f_s \tag{7}$$

where $V_{\text{ds}} = V_{\text{in}}/4$. The last part of switching loss is caused by V–I overlap [25] during the hard-switching transitions of $Q1$ and $Q2$ and partial hard-switching transitions of $Q5$–$Q8$, which can be expressed by

$$P_{\text{tr}} = P_{\text{tr,ON}} + P_{\text{tr,OFF}} = 8 \times \frac{1}{2} V_{\text{ds}} I_{L1,3} t_{\text{tr}} f_s \tag{8}$$

where the transition time t_{tr} indicates V–I overlap time. Practically in this design, the P_{tr} is small compared with other losses and therefore can be ignored. This is because: 1) the nature of Dickson-star SC that blocks most of V_{in} so that $Q1$ and $Q2$ are only stressed by $(V_{\text{in}}/4)$ and 2) t_{tr} is short as for small power switches. However, this type of loss cannot be ignored when the ITSAB converter is designed for heavier loads that the power switches are large enough to have significant reverse recovery charge and long t_{tr}.

C. Inductor Loss

Considering an air-core inductor realization, no core loss needs to be accounted for. As a consequence, only DC resistance (DCR) and AC resistance (ACR) losses of the inductor are considered. The DCR loss is given by

$$P_{\text{ind,DCR}} = \left(I_{L1,\text{rms}}^2 + I_{L3,\text{rms}}^2\right) R_{\text{dc}} \tag{9}$$

where the rms value of the inductor currents can be computed by the same approach as described in Section III. The ac loss of the specific inductor can be calculated using the model provided by the manufacturer. For simplicity, the inductor loss is approximated as the DCR loss, $P_{\text{ind}} \approx P_{\text{ind,DCR}}$.

The loss model is verified by comparing the calculated efficiency to the computer aided design (CAD) simulated results, as shown in Fig. 7, which shows a good match. Two pie charts of the loss breakdown computed at 12/3 V, $f_s = 3.8$ MHz, and 0.5 and 2 A loads are given in Fig. 7(b) and (c), respectively. In the calculation, switching loss P_{sw} includes P_{coss} and P_{tr}. It can be seen that the frequency-related losses, mostly P_{sw} and P_{gate}, dominate the total loss at light load as a result of less conduction loss and insufficient I_o for completely soft-switching $Q3$ and $Q4$ [16]. At heavy load, however, the conduction loss dominates and it is therefore crucial to properly design and operate the converter so that the minimum rms value of the inductor currents is achieved. In Section IV, the optimization methodology is discussed in more detail.

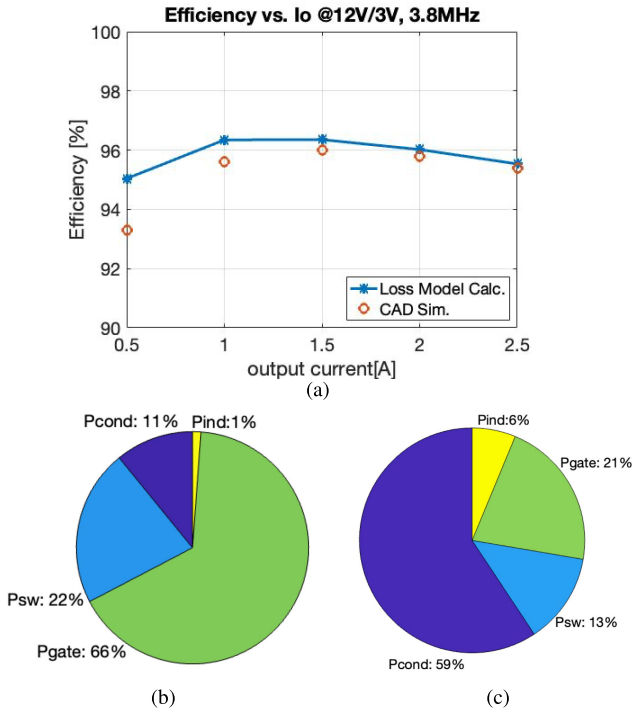


Fig. 7. Loss model verification: (a) efficiency comparison. Loss breakdown at (b) 0.5-A load and (c) 2 A load.

IV. Optimization Methodology

As discussed in Section III, two major loss mechanisms in the ITSAB converter are conduction loss P_{cond} and switching loss $P_{\text{sw}} + P_{\text{gate}}$. To minimize the power loss at a desired operating point, one can sweep the converter parameters, including power switch area, switching frequency, and so on. However, as shown in Fig. 6 and the analysis in Section III, the shape of the inductor currents is sensitive to the system parameters. In other words, even though a minimum power loss can be found by sweeping the parameters, the inductor currents could potentially be distorted and peaking above the saturation current of the inductors, potentially resulting in malfunction of the circuit. In this section, a novel optimization methodology is proposed so that the inductor current distortion can be prevented while the minimum power loss is found.

A. Minimum RMS Current

As marked in Fig. 5, the resonant frequency and the characteristic impedance of each resonant tank are

$$f_o = \frac{1}{2\pi\sqrt{LC}}, \quad \text{and} \quad R_o = \sqrt{\frac{L}{C}} \tag{10}$$

where L is the inductance of $L1$ and $L3$, and C is the capacitance of $C1$ and $C3$. Two variables are used in this optimization process; k is defined as

$$k = \frac{f_s}{f_o} \tag{11}$$

and the quality factor Q as

$$Q = \frac{R_o}{R_s} \tag{12}$$

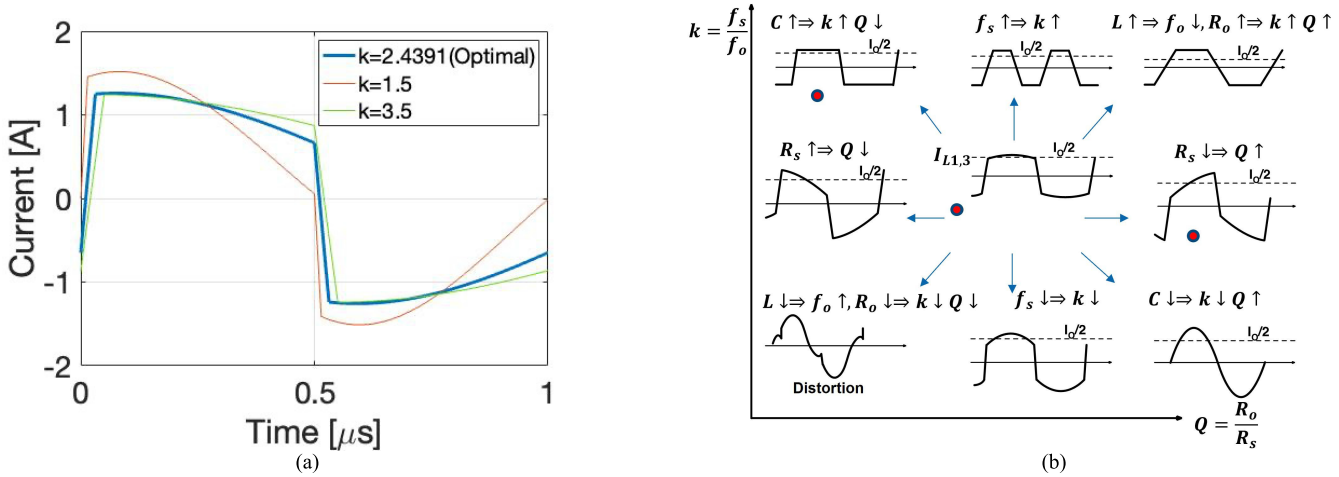


Fig. 8. Illustration of how inductor rms current is minimized using $k = f_s/f_o$ and $Q = R_o/R_s$ as optimization parameters. (a) Inductor current wave shape for $Q = 2.6$ and three different values of $k = f_s/f_o$. The minimum $I_{L1,\text{rms}}$ is obtained for $k = 2.4391$. (b) Summary of inductor current wave shapes in the k versus Q plane. The minimum rms cases are highlighted (red dots).

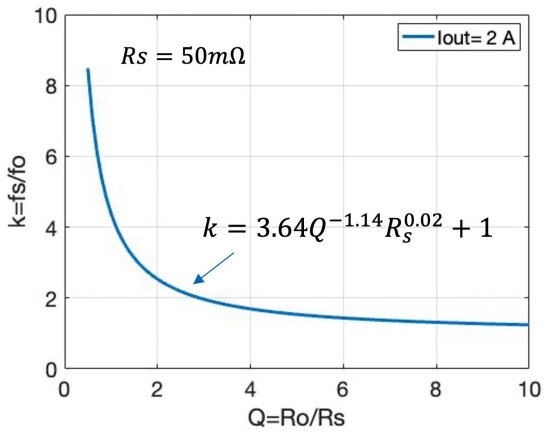


Fig. 9. Optimum k as a function of Q for $R_s = 50$ mΩ and $I_o = 2$ A.

where R_s is the total loop resistance as indicated in Fig. 5, which comprises power switches ON-resistance and equivalent series resistance (ESR) of L and C. Given the above equations, the inductance and the capacitance of each resonant tank can be expressed in terms of k and Q

$$L = \frac{kQR_s}{2\pi f_s}, \quad C = \frac{k}{2QR_s\pi f_s} \tag{13}$$

where f_s is the switching frequency. To find the parameters that make the inductor current achieve minimum rms value, a relationship between k, Q, and R_s must be carried out. The augmented state-space approach [24] is used to obtain the inductor current waveforms for various sets of parameters and operating conditions. For instance, when Q is picked as 2.6 and R_s equals 50 mΩ, current I_{L1} can be depicted in Fig. 8(a) for different k at 12 V-to-3 V, 2 A conversion at $f_s = 1$ MHz. The highlighted curve, which is for $k = 2.4391$, has minimum rms value. When k is smaller, indicating a smaller L and the resonant frequency becomes closer to the switching frequency, the curve has higher ripple. On the other hand, an increased k means larger L and slower current ramping speed during States 2 and 4, leading to shorter times for States 1 and 3, and thus higher peak current to deliver

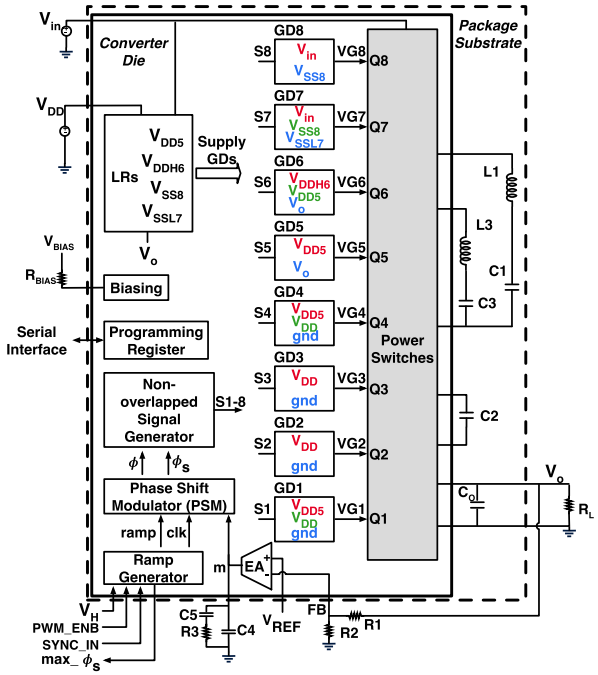


Fig. 10. Block diagram of the prototype ITSAB converter realized on a 130-nm BCD die flip-chipped on a package substrate together with power capacitors and two 10-nH inductors.

the same load current. Neither of the above two cases can achieve smaller rms value than the optimal point. A brief summary of how k and Q values change along with the circuit parameters L, C, and R_s and the resulted inductor current shapes is listed in Fig. 8(b). The dots on each column indicate the corresponding minimum rms value point. Once a range of Q is evaluated in the same manner, the targeted parameters' relationship can be depicted using a curve-fitting method as shown in Fig. 9. It sets the boundary of distortion region which is the area below the curve. This curve-fit relationship is

$$k = 3.64Q^{-1.14}R_s^{0.02} + 1. \tag{14}$$

From this equation, it can be seen that the optimum k approaches 1 when Q approaches infinity, which represents

TABLE I
OPTIMIZATION RESULTS

Parameters	Details
L	10 nH
C1, C3	1.05 μF
C2	4 μF
f_s	3.35 MHz
Q1, Q2 area	0.1139 mm^2
Q3, Q4 area	0.2007 mm^2
Q5, Q6 area	0.1194 mm^2
Q7, Q8 area	0.1373 mm^2

operation at resonance. For a practical, finite Q, the optimum is for above-resonance $k > 1$ operation.

B. Optimization Process

The semiconductor parameters are scaled with the device area A_s

$$R_{\text{ON}} = \frac{R_{\text{ON,sp}}}{A_s} \tag{15}$$

$$Q_{\text{tot}} = (Q_{\text{gg,sp}} + Q_{\text{dd,sp}} + Q_{\text{ss,sp}})A_s \tag{16}$$

where $R_{\text{ON,sp}}$, $Q_{\text{gg,sp}}$, $Q_{\text{dd,sp}}$, and $Q_{\text{ss,sp}}$ are the density of ON-resistance, gate charge, drain charge, and source charge per unit area, respectively. After plugging these scaling equations (7) and (15), the loss modeling expressions (3), (6), and (7) can then be formulated as

$$P_{\text{cond}} = \frac{P_{\text{cond,sp}}}{A_s} \tag{17}$$

$$P_{\text{gate}} = P_{\text{gate,sp}}A_s \tag{18}$$

$$P_{\text{sw}} = P_{\text{sw,sp}}A_s \tag{19}$$

where $P_{\text{cond,sp}}$, $P_{\text{gate,sp}}$, and $P_{\text{sw,sp}}$ represent the specific power loss per unit area. As a result, the total power loss can be turned into the following form:

$$P_{\text{tot}} = \sum_{i=1}^{8}\left(\frac{P_{\text{cond,sp}_i}}{A_{s_i}} + (P_{\text{gate,sp}_i} + P_{\text{sw,sp}_i})A_{s_i}\right) + P_{\text{ind}}. \tag{20}$$

The optimization process of the proposed circuit can be expressed in the following form:

$$\begin{aligned} &\min\ P_{\text{tot}}(X) \\ &\text{s.t.}\ \sum_{i=1}^{8} A_{s_i} \le A_{\text{tot,max}} \\ &\quad A_c \le A_{c,\text{max}} \\ &\quad L \le L_{\text{max}} \end{aligned} \tag{21}$$

where the vector $X = [f_s, A_s, R_o]^T$ denotes the variables in this converter design, and $A_{\text{tot,max}}$, $A_{c,\text{max}}$, and L_{max} set the limit of the chip area, capacitor footprint area, and inductor value, respectively. Mathematically, minimizing P_{tot} in (20) is a geometric programming (GP) problem [26], which can be efficiently solved using tools such as CVX [27]. The optimization results, including selected passive component, switching frequency, and areas of the power switches, are summarized in Table I.

TABLE II
SOURCE AND GATE VOLTAGES OF EACH SWITCH DURING ON AND OFF INTERVALS, WHEN THE ITSAB PROTOTYPE IS GENERATING $V_o = 2.4$ V FROM $V_{\text{in}} = 9.6$ V

Switch	Source Voltage		Gate Voltage	
	ON	OFF	Low Swing	High Swing
Q8	V_{in} (9.6V)	V_{in} (9.6V)	V_{SS8} (6V)	V_{in} (9.6V)
Q7	$3V_{\text{in}}/4$ (7.2V)	V_{in} (9.6V)	V_{SSL7} (3.6V)	V_{in} (9.6V)
Q6	$V_{\text{in}}/2$ (4.8V)	$V_{\text{in}}/4$ (2.4V)	V_{o} (2.4V)	V_{DDH6} (8.4V)
Q5	$V_{\text{in}}/4$ (2.4V)	$V_{\text{in}}/4$ (2.4V)	V_{o} (2.4V)	V_{DD5} (6V)
Q1,4	$V_{\text{in}}/4$ (2.4V)	gnd (0V)	gnd (0V)	V_{DD5} (6V)
Q2,3	gnd (0V)	gnd (0V)	gnd (0V)	V_{DD} (3.6V)

V. IMPLEMENTATION DETAILS

The system block diagram including all the key blocks and the power stage is shown in Fig. 10. The blocks within the solid rectangle are implemented ON-chip, while the passive components between the solid line and the dashed line are on the package substrate. The key ON-chip blocks include gate drivers (GDs) (GD1–GD8) and their voltage supply linear regulators (LRs); ramp generator (RG) for synchronization and generating ramp signal at the required frequency; phase shift modulator (PSM) for closed-loop regulation; non-overlapped signal generator for deadtime control; serial programming register for setting up frequency and deadtime; Biasing circuit for creating bias currents for other sub-blocks throughout the chip; operational transconductance amplifier (OTA)-based error amplifier (EA) to form the closed-loop controller. In the following parts of this section, the control signal generation, GDs and LRs, control loop design, and synchronization are addressed separately.

A. Control Signal Generation

As derived in (2), the output voltage of the implemented ITSAB converter is fully regulated by the phase shift between ϕ and ϕ_S. These control signals are generated from the PSM and the RG, as illustrated in Fig. 11 along with the timing diagram of the corresponding signals. Particularly, ϕ_S is periodically toggled by the rising edge of cmp_out [Fig. 11(b)] which is the output of comparing the error voltage m with the ramp signal from RG [Fig. 11(a)]. Meanwhile, ϕ is triggered by the rising edge of the clk signal after a short delay as indicated in Fig. 11(c). Practical delay mismatches on signal paths from this control circuit to the final power gates would

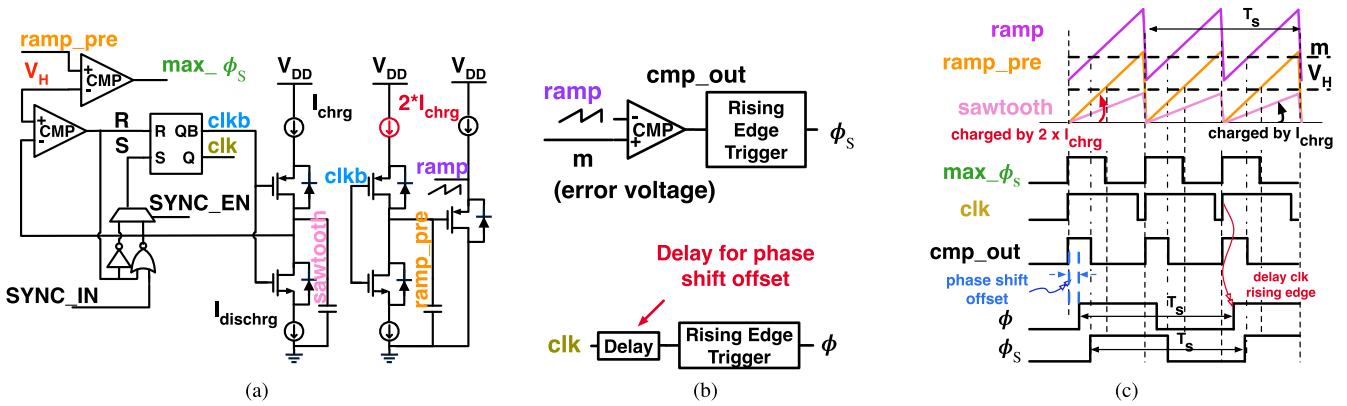


Fig. 11. Phase-shifted control signal generation, including block diagrams of (a) RG and (b) PSM; (c) timing diagram: generation of ϕ and ϕ_S.

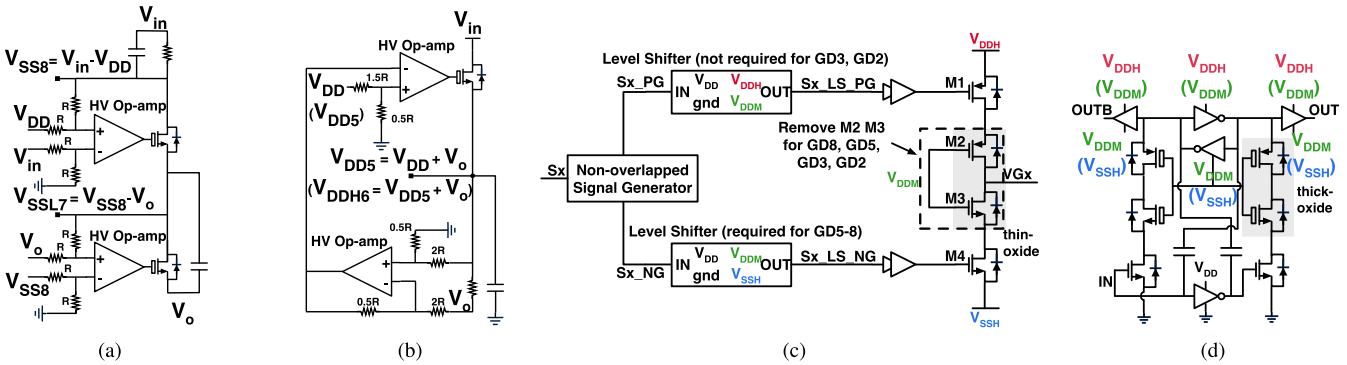


Fig. 12. Block diagrams of (a) subtraction LR to generate V_{SS8} and V_{SSL7}, (b) summation LR to generate $V_{DD5}(V_{DDH6})$, (c) GD for Q6, and (d) level shifter.

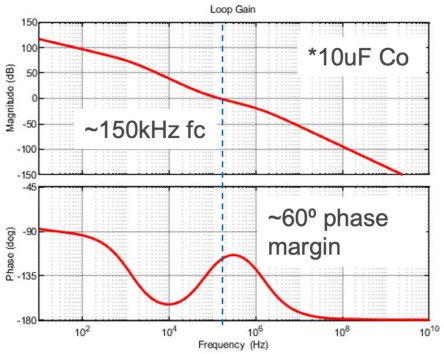


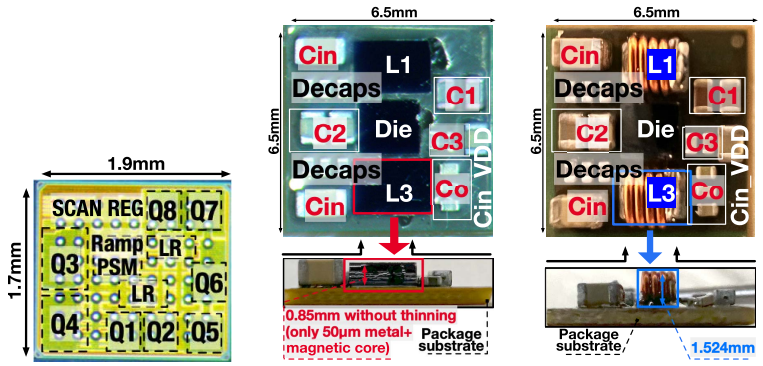
Fig. 13. Magnitude and phase responses of the loop gain obtained under the following conditions: $V_{\text{in}} = 9.6$ V and $V_o = 2.38$ V, with ~74 nH parasitic inductors of the wire loops used to measure inductor currents, as shown in Fig. 15.

TABLE III
COMPONENTS FOR THE PI (TYPE-II) COMPENSATOR

Component	Details
C4	2.7 pF
C5	56 pF
R3	43.2 kΩ
R1,2	80 kΩ

potentially result in delay mismatch on ϕ and ϕ_S at the converter power stage, which could lead to a minimum phase shift that is larger than zero even if the control circuit sets the phase shift to zero. A non-zero minimum phase shift would limit the minimum load current that the converter can support, following (2). To ensure that the converter can support an output current at light load current down to open-circuited load, it is desirable to generate a negative phase shift value of t_ϕ at this control circuit to compensate for any possible timing mismatch in the signal paths. Therefore, a short delay of ~15 ns is added after clk to give ϕ the phase shift offset for this purpose, as shown in Fig. 11(c).

The sawtooth waveform is generated by charging an MiM capacitor with I_{chrg} between ground and V_H. In this design, $V_H = 1.5$–2.5 V depending on the target frequency, while V_{DD} can vary from 3 to 5 V to optimize the switching loss and conduction loss of power switches. From (2), it can be seen that the maximum output current is achieved when the phase shift time $t_\phi = (Ts/4)$. $t_\phi > (Ts/4)$ will lead to smaller average output current, because there is not sufficient time left after the phase shift to allow inductor currents to flow to the output. Therefore, the comparison to generate ϕ_S for phase shift control need only be in the lower half of the sawtooth waveform. Exploiting this characteristic to get better noise immunity in generating the phase shift control signal, ramp_pre is generated by a second branch with two times larger charge current. Finally, ramp_pre is slightly shifted up using a source–follower stage to make the ramp signal that fits in the input common-mode range of the comparator inside PSM and the output range of error amplifier, m. To prevent the regulation loop from falling into a positive feedback when $t_\phi > (Ts/4)$, the phase shift must be limited using the



(a) (b) (c)

Fig. 14. Top and side views of the ITSAB converter prototype, including (a) 1.7 × 1.9 mm die in a 130-nm BCD process, 6.5 × 6.5 mm package substrate with flip-chipped die, power capacitors, and 2 × 10 nH, (b) IPD inductors, or (c) discrete (Coilcraft 0807SQ-10N) inductors.

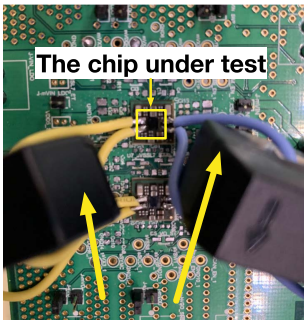


Fig. 15. Current measurement test setup with wire loops having ~74 nHparasitic inductances serving as the power stage inductors.

signal max_ϕ_S, which is a byproduct of ramp generation, by comparing the intermediate signal ramp_pre with the peak voltage V_H of the sawtooth signal.

Another feature of this design is to allow multiple converter chips to be synchronized, possibly in an interleaved manner, to improve the output current capability. This synchronization mode, therefore, is added and enabled by turning SYNC_EN of the RG to 1. With this setting, the current chip frequency can be triggered and synchronized by an OFF-chip clock signal to SYNC_IN. The synchronization is proven to work well when two chips are synchronized to the same frequency with 180° out-of-phase operations, as shown in the experiments in Section VI.

B. Gate Drivers and Supply Voltage Generation

The GD design is more challenging for a multilevel converter, because of flying source voltages and a larger number of power switches. The source voltages and the required gate voltages during ON- and OFF-states of all the power switches are listed in Table II. There are four additional voltage levels defined as follows:

$$\begin{aligned} V_{\mathrm{SS8}} &= V_{\mathrm{in}} - V_{\mathrm{DD}} \\ V_{\mathrm{SSL7}} &= V_{\mathrm{SS8}} - V_o \\ V_{\mathrm{DD5}} &= V_{\mathrm{DD}} + V_o \\ V_{\mathrm{DDH6}} &= V_{\mathrm{DD5}} + V_o. \end{aligned} \tag{22}$$

A bootstrap driver containing a large capacitor and a diode is the most common way of driving high-side switches. However, the large bootstrap capacitor and diode would require to be OFF-chip and take significant area and volume. Furthermore, the diode voltage drop may reduce the available gate-drive swing resulting in weak driving, especially in the context of a multilevel power converter with multiple high-side switches. To overcome these obstacles, and to guarantee the same voltage (V_{DD}) over V_{gs} during ON time, regardless of the value of V_{in} and V_{DD}, fixed-level GD structures with the driver supply voltages generated by LRs are designed and presented in Fig. 12.

The subtraction LR, implemented using two high-voltage op-amps as shown in Fig. 12(a), is used to generate V_{SS8} and V_{SSL7}. The stacked structure is used to reduce power loss as the efficiency of a linear regulator depends on the voltage difference between its input and output voltages. Another type of LR is for summation function as shown in Fig. 12(b). Two circuits of this type are used for supplying V_{DD5} and V_{DDH6}, respectively. Two high-voltage op-amps are connected so that the reference voltages are summed at the output. Both the subtraction LR and summation LR recycle the residual charge to V_o to further save power.

As an example, the GD for $Q6$ is given in Fig. 12(c). To minimize the shoot-through current at the last stage of the GD, PMOS $M1$ and NMOS $M4$ are driven separately with deadtime created by the non-overlapped signal generator at the front of this block. Stacking of $M2$ and $M3$ reduces the voltage stress on $M1$ and $M4$ so that when driving the switches with flying source voltages, such as $Q1$, $Q4$, $Q6$, and $Q7$, it is still safe to use only thin-oxide devices. $M2$ and $M3$ are not present in GD2, GD3, GD5, and GD8 gate drivers.

Level shifters are also required for non-gnd referenced signals. The level shifter circuit is shown in Fig. 12(d), with MiM capacitors used for coupling signals between different voltage domains with minimal latency while keeping small area. The cross-coupled inverters at the high-voltage domain use weak NMOS transistors to ensure rail-to-rail operation [6].

C. Control Loop Design

To achieve a large dc gain and adequate phase margin as well as fast closed-loop transient response, a proportional–integral (PI, or Type-II) compensator is used in this implementation, as indicated in Fig. 10. An ON-chip OTA together

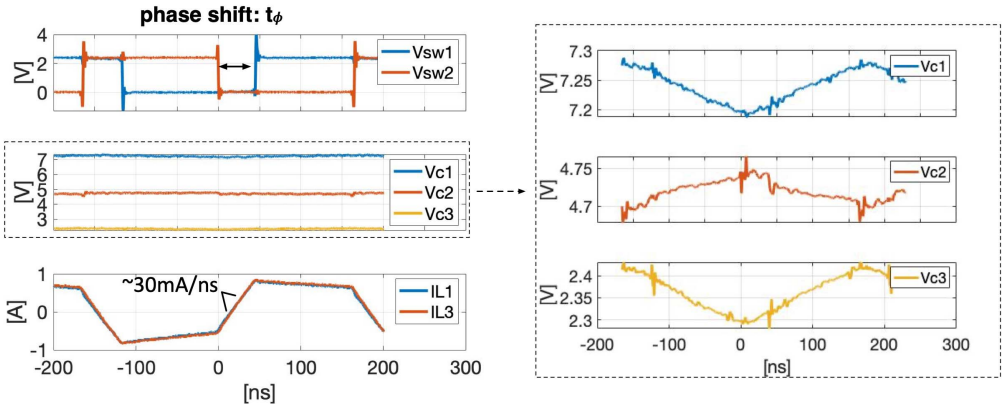


Fig. 16. Measured steady-state converter waveforms, with 74-nH inductors due to the current measurement setup shown in Fig. 15, $V_{\text{in}} = 9.6$ V, $V_o = 2.38$ V, and $I_o = 1$ A.

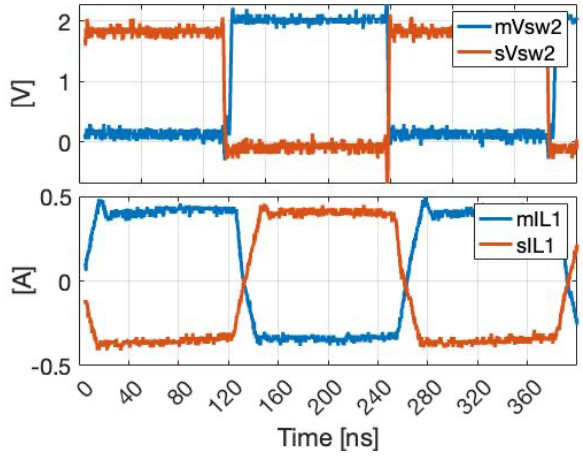


Fig. 17. V_{sw2} and I_{L1} of two converters (m and s) with 180° phase shift at 8.2/2 V, 3.8 MHz, 1 A, (0.5 A each), open-loop.

TABLE IV
COMPONENTS ON THE PACKAGE SUBSTRATE

Component	Details
C1	2 x 2.2 µF, 16 V 0402 (0.92 µF)
C2	2 x 10 µF, 10 V 0402 (4 µF)
C3	1 x 2.2 µF, 6.3 V 0201 (0.87 µF)
Cin(V_{in})	2 x 10 µF, 25 V 0603 (3.2 µF)
Cin(V_{DD})	1 x 10 µF, 10 V 0402 (2 µF)
Co	3 x 2.2 µF, 6.3 V 0201 (2.6 µF)
Decap(V_{DDH6})	2 x 1 µF, 16 V 0201 (304 nF)
Decap(V_{DD5})	1 x 1 µF, 16 V 0201 (244 nF)
Decap(V_{SS8})	2 x 1 µF, 16 V 0201 (408 nF)
Decap(V_{SSL7})	1 x 1 µF, 16 V 0201 (353 nF)
L1,3	10 nH, Ferric IPD or 0807SQ-Coilcraft

with PSM enables the design of a fast analog control loop. The control-to-output transfer function can be expressed as [23]

$$\hat{I}_o = \frac{V_{\text{in}}}{8Lf_s}\hat{\phi} = K_\phi\hat{\phi}$$
$$G(s) = \frac{\hat{V}_o}{\hat{\phi}} = K_\phi\frac{1}{1+s/\omega_p} \tag{23}$$

where $\omega_p = 1/R_L Co$. The transfer function of the compensator is

$$G_c(s) = G_0\frac{1+\omega_z/s}{1+s/\omega_p} \tag{24}$$

where $G_0 = (R2/(R1+R2))((g_m R3C5)/(C4+C5))$, $\omega_p = ((C4+C5)/(R3C4C5))$, and $\omega_z = (1/(R3C5))$. The position and connection of the passive components $R1$–$R3$, $C4$, and $C5$ are shown in Fig. 10. As part of the control loop, the ramp signal has the gain of $(1/2V_H)$, because its peak voltage is about $2V_H$. Consequently, the loop gain can be written as

$$T(s) = \frac{R_2}{R_1+R_2}G_c(s)G(s)\frac{1}{2V_H}. \tag{25}$$

The system is designed to work at a switching frequency f_s of around 3 MHz. The crossover frequency f_c is selected to be around $f_s/10$. As (23) suggests, the system dynamic performance is highly related to the circuit parameters L, f_s, output capacitor Co, and load current. Based on the values of passive components in the converter, the Type-II compensator is designed for 3-MHz switching frequency and 0.2-A load is listed in Table III. The Bode plot of the computed loop gain is shown in Fig. 13. The designed 150-kHz crossover frequency and 60° phase margin ensure the fast response and stable operation.

VI. EXPERIMENTAL VERIFICATION

The demonstration chip was fabricated in TSMC 130-nm BCD technology with a dimension of 1.9 × 1.7 mm as indicated in Fig. 14(a). Aiming for a high power density performance, the chip die was flip-chipped on a 6.5 × 6.5 mm six-layer organic package substrate together with flying capacitors, decoupling capacitors, input–output capacitors, and two 10-nH IPD inductors supplied by Ferric Semiconductor. Note that the IPD inductors promise much higher power density because they achieve a thickness of 50 μm (plus 800 μm unused silicon carrier as shown in Fig. 14(b), which could be thinned substantially down to 10 sμm), while discrete inductors are 1.524–mm thick. While the flip-chip die has 180–μm bump pitch, the organic substrate has a ball grid array (BGA) with 0.8–mm ball pitch to reduce the cost of

TABLE V
PERFORMANCE COMPARISON: DISCRETE VERSUS IPD INDUCTORS

Inductor		V_{in}/V_o	$I_{o,max}$ [A]	Peak Eff. @I_o	Pout,max [W]	Peak power density [W/mm^3]*
10 nH	Discrete	9.6 V/2.33 V	2.5	92.4% @1 A	7.5	0.62
	IPD	9.6 V/2.33 V	1.5	91.2% @0.6 A	4.4	1.36

*Space counts active die, flying capacitors and effective inductors volume only.

TABLE VI
COMPARISON WITH PRIOR WORKS

	This Work	[4]	[5]	[6]	[7]	[8]
Topology	**ITSAB**	Tri-State DSD	3:1 ReSC	Hybrid SC	Hybrid Dickson	Cascade Hybrid
Technology	**130 nm**	180 nm	180 nm	130 nm	65 nm	180 nm
Inductor	**2x10 nH**	2x560 nH	36 nH	1 µH	180 nH	240 nH
Inductor switching frequency	**2-5 MHz**	200 k-2 MHz	1.7 MHz	2.3 MHz	400 k-10 MHz	1.5 MHz*
Input voltage [V]	$V_{in} \geq 9V$				$V_{in}<9V$	
	9.6-12	12/24	12	9	3-4.5	4-6
Output voltage [V]	**2.15-3.3**	1	3.5-3.8	3-4.2	0.3-1	0.4-1.2
Peak output current [A]	**2.5**	3	1.24*	3.4	1.53	1
Peak power density [W/mm^3] ***	**1.36 @ 4.1****	0.06 @ 12*	1.12 @ 3.4*	0.41 @ 2.7*	0.14 @ 5.2*	0.18 @ 4.5*
Efficiency [%] @ CR	**92.4 @ 4.12**	91.2 @ 12	82 @ 3.4	94.3 @ 2.5	88.3 @ 5.2	96.9 @ 4.2
Regulation Method	**Phase shift modulation**	Duty cycle	Deadtime control	Duty cycle	Duty cycle	Ripple injection
Package	**Flip-chip**	Wire-bonding	Flip-chip	Flip-chip	Flip-chip	Wire-bonding

*Estimation from reported measurement results, **Assuming Ferric IPD inductor being used

***Area counts active die, flying capacitors and inductors only. Calculated at given conversion ratio (CR)=V_{in}/V_o

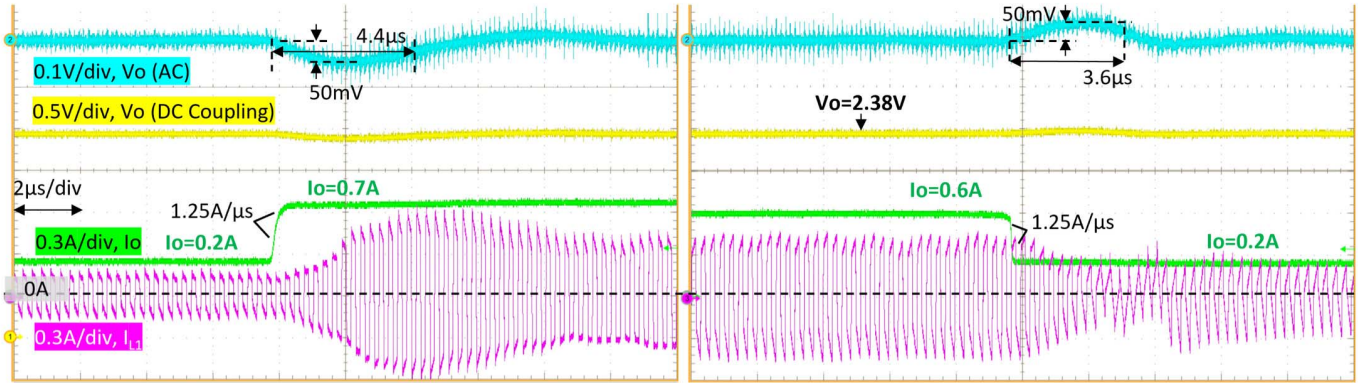


Fig. 18. Step-load transient responses of the experimental prototype operating at $f_s = 3$ MHz with wire loops as inductors. The output is closed-loop regulated at $V_o = 2.38$ V from $V_{in} = 9.6$ V.

the printed circuit board (PCB). The details of each passive component are listed in Table IV. The selection of the flying capacitors guarantees that the actual capacitance of $C1$ and $C3$ is equal and much less than the one of $C2$ so that R_o and f_o are relatively the same for both LC tanks. Since the design uses small inductors of 10 nH, any additional wires with reasonable length added in series with the inductors to allow measuring their currents with current probes would add significant inductance beyond the inductors themselves. Therefore, to measure operational waveforms, the inductors are removed and replaced by two short wire loops, as shown in Fig. 15. Note that even when the two wires are sized just long enough to clip the small current probes, their effective parasitic inductances are approximately 74 nH, which is about 7× more than the inductors used on the package. The significantly larger wire-loop inductances limit the maximum load current

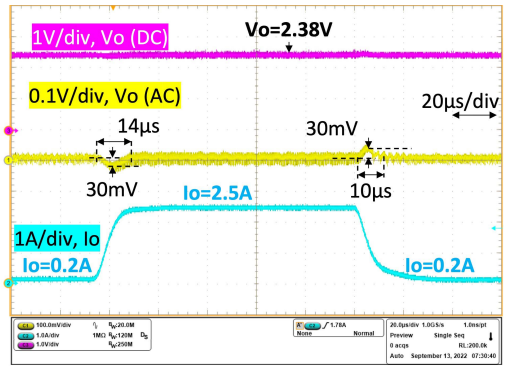


Fig. 19. Step-load transient responses of the experimental prototype with 10-nH discrete inductors operating at $f_s = 3.8$ MHz. The output is closed-loop regulated at $V_o = 2.38$ V from $V_{\text{in}} = 9.6$ V.

according to (2), but the measurement setup still provides verification of operating waveforms at light to medium loads.

Fig. 16 shows the measured steady-state waveforms of switching node voltages V_{sw1} and V_{sw2}, flying capacitor voltages, and inductor currents. The noticeable time difference between V_{sw1} and V_{sw2} is the phase shift time t_ϕ, during which the inductors are magnetized or demagnetized with a slope of ~30 mA/ns, implying ~74 nH parasitic inductance of the wires. The top of I_{L1} and I_{L3} is not as flat as in the theoretical waveforms in Fig. 3 due to the additional path resistances. The flying capacitor voltages are measured by a differential probe, verifying the soft-charging behavior as discussed in Section II.

The synchronization feature is verified by running two ITSAB converters at the same time. The phases are set up by two 180° phase-shifted synchronization control signals generated by an FPGA, which also allows any other amount of phase shift if more converters are connected in parallel for a larger load. The measured switching node V_{sw2} voltages and the inductor current I_{L1} for both the converters are shown in Fig. 17.

Fast closed-loop load-step transient performance is measured at a 9.6–2.38-V conversion and $f_s = 3$ MHz, with 0.5- and 0.4-A load steps. The waveforms of ac-coupled and dc-coupled output voltage V_o, output current I_o, and inductor current I_{L1} are shown in Fig. 18. Corresponding to the two load steps, the output voltage takes 4.4 and 3.6 μs to settle within 1%, and the undershoot and overshoot during the step-load transients are within 2% of its dc value. In addition, the full-load step response is performed on the prototype with 10-nH discrete inductors as in Fig. 14(c). V_o settles in 14 and 10 μs with undershoot and overshoot of 30 mV when responding to 2.3-A step load as shown in Fig. 19.

A line transient of $1.4 - V$ step at V_{in} is performed on the experimental prototype that has two 10-nH discrete inductors and operates at 1-A load. As shown in Fig. 20, V_o is well-regulated to 2.5 V with no significant fluctuation.

On Fig. 21, the efficiency is measured with two types of inductors, discrete and IPD, at various input–output voltages and different switching frequencies. The peak efficiency measured at 9.6/2.33-V, 3.1-MHz, 1-A load is 92.4% with 0807SQ discrete inductors, compared with 91.2% with Ferric IPD inductors at 0.6 A. The efficiency difference between the prototypes with two types of inductors is largely caused by the large difference in the inductor series resistance, which is consistent with the differences in size. Fig. 21(a) also illustrates the matched efficiency between analytical calculation and simulation in addition to the drop in measurement results. This is largely due to the paths and connection resistances and capacitances in both the silicon layout and the PCB prototype. The additional resistances not only directly affect the conduction loss but also result in larger inductor current ripple, which further increases the total conduction loss across all the load conditions. An additional efficiency calculation considering 50% more ON-resistance due to paths and vias on silicon layout, 30% more parasitic resistance from PCB routing and connection, and 40% more parasitic capacitance from dense layout routing is plotted in Fig. 21(a), which shows an excellent match with the measurement results. The converter prototype is also tested for its output regulation range. As shown in Fig. 22, the output voltage ranges from 2.15 to 2.65 V and 2.7 to 3.3 V with an input voltage of 9.6 and 12 V, respectively. The lower boundary of V_o is set once there is zero phase shift, meaning the inductors couple and resonate directly with $C1, 3$ and deliver charge to the output during States 1 and 3, without the charging States 2 and 4. The peak values of I_{L1} and I_{L3} are determined by f_o and f_s as well as the desired load current. On the other hand, the upper boundary is limited by the maximum phase shift ratio which is one quarter of T_s as calculated from (2) and Section V-A. Hence, the upper boundary of V_o can be larger than the measured values. However, as the inductors are charged longer time during States 2 and 4, the peak current can be significantly larger than the saturation current of small and integrated inductors. The large rms currents in steady-state can also be detrimental to other parts of the circuits, including the power switches and capacitors. To keep the prototype in a safe and reliable operating region, a range of $\pm 10\%$ of nominal V_o is chosen for the demonstration. In this output voltage range, the efficiency remains greater than 75%.

The power density of the prototype with IPD inductors is about two times larger compared with the power density of the prototype with the discrete inductors, counting the volume of the active die, the flying capacitors, and the effective inductors volume. The comparison is summarized in Table V. One may note that the package substrate is not fully optimized for power density. As indicated by the thermal image in Fig. 23, which is measured at 12/2.93-V, 3.8-MHz, 1.-A load, the temperature rise is only 10 °C from the room temperature. This suggests that a finer pitch package design can be used to further increase the overall power density.

The connection of inductors and capacitors in ITSAB converter form resonant tanks similar to well-known resonant converters. In contrast, however, the ITSAB converter requires less inductance and much lower switching frequency because of phase shift modulation, although both these types of converters achieve best efficiency at nominal conversion ratio, i.e., 4. Moreover, as (23) suggests, the ITSAB converter is a first-order system, which allows for faster closed-loop design and transient responses.

The proposed ITSAB converter uses only two 10-nH inductors, at least 1.8× smaller values compared with the

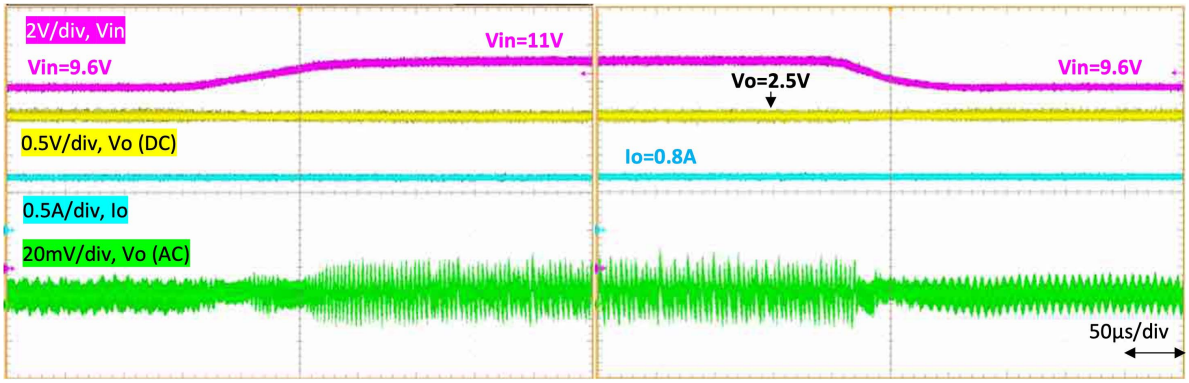
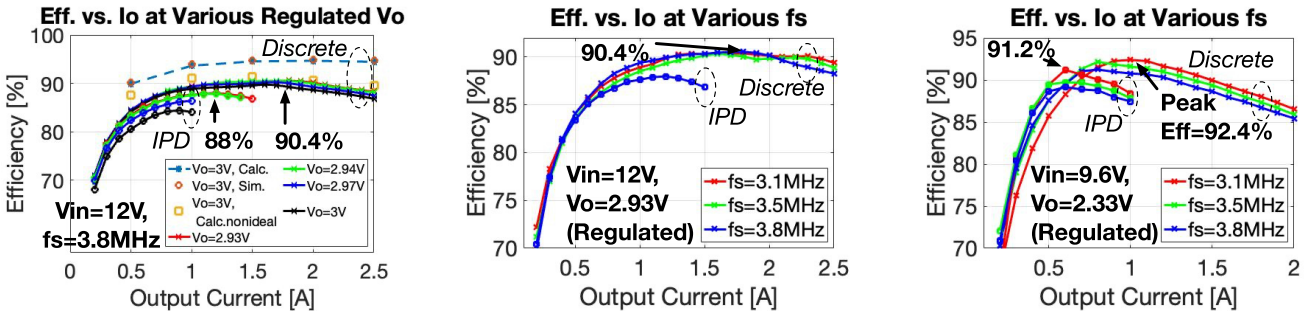


Fig. 20. Line transient responses of the experimental prototype operating at $f_s = 3.8$ MHz with 10-nH discrete inductors. The output is closed-loop regulated at $V_o = 2.5$ V.



(a) (b) (c)

Fig. 21. Efficiency versus load current I_o measured at (a) $V_{\text{in}} = 12$ V, $f_s = 3.8$ MHz, various V_o, (b) $V_{\text{in}} = 12$ V, $V_o = 2.93$ V, various f_s, and (c) $V_{\text{in}} = 9.6$ V, $V_o = 2.33$ V, various f_s.

TABLE VII
COMPARISON BETWEEN CONVERTER TOPOLOGIES

Converter	Inductor	Regulation	Efficiency
Resonant	tens to hundreds of nH	Limited in most cases	Good
Switched-capacitor (SC)	N/A	Limited	Poor trade-off with regulation
Conventional hybrid	hundreds of nH to µH	Yes	Good
ITSAB converter (this work)	**up to tens of nH**	**Yes**	**Good**

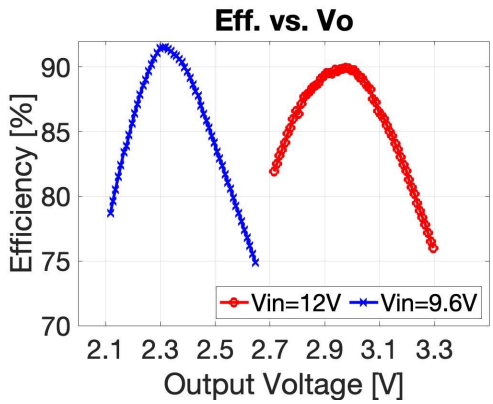


Fig. 22. Efficiency versus V_o at 1-A load, 3.8-MHz f_s.

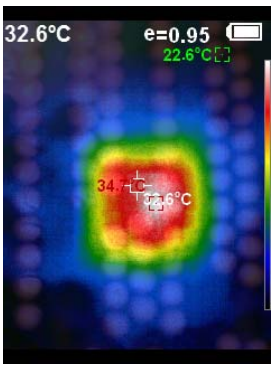


Fig. 23. Thermal image of the prototype with IPD inductors taken at full load (1.5 A).

state-of-the-art designs with otherwise similar specifications, as shown in the comparison Table VI. Because of the small inductors, the prototype converter has an outstanding power density of 1.36 W/mm^3. Furthermore, it is capable of operating over a wide input and output range with similar peak efficiency of 92.4%. As summarized in Table VII, the ITSAB converter in this article exhibits an effort to overcome challenges in other types of converter that require much larger inductors (con-

ventional hybrid converter), have no regulation or difficulty in achieving regulation together with high efficiency and compact size (resonant converter), or suffer from lower efficiency for fine regulation (SC converter).

VII. Conclusion

The evolution of electronic devices clearly indicates the trend of dimension shrinking. While the power management system has been playing a more important role, inductors used in power converters are difficult to scale with semiconductors to support the miniaturization needs. In response to this need, this article presents a new hybrid converter, named integrated transformerless stacked active bridge (ITSAB) converter, which requires only 10-nH inductors, while operating at a modest switching frequency in the MHz range. A voltage regulation approach is provided as well as a detailed loss analysis for the ITSAB converter. In addition, an augmented state-space method is used to accurately calculate the inductor current wave shapes and rms values. A novel optimization methodology is described, which is used to determine passive components, switching frequency, and areas of the power devices so as to minimize the total loss. Moreover, circuit design details are provided for the key sub-blocks, including an adaptive GD design and phase-shifted control signal generation. The article also includes an analysis of open-loop control-to-output frequency responses, based on which a voltage control loop with a PI (Type-II) compensator is designed.

To validate operation and design of the proposed ITSAB converter, the power stage and the controller are implemented and fabricated on a 1.7 $\times$ 1.9 mm die in a 130-nm BCD process. Two prototypes are constructed: one with Ferric IPD inductors and another one with discrete air-core inductors, both using an organic substrate and BGA package to house the flip-chip die, power capacitors, and inductors. Steady-state operation and load transients are verified by replacing the discrete inductors with two wire loops to facilitate capturing of inductor currents. Peak efficiencies of 91.2% and 92.4%, which are comparable to prior works, are measured for the two prototypes operating from 9.6–12 V input to 2.15–3.3 V output, respectively. Thanks to the low inductance requirements, and the usage of IPD inductors, the ITSAB converter prototype reaches a superior maximum power density of 1.36 W/mm^3.

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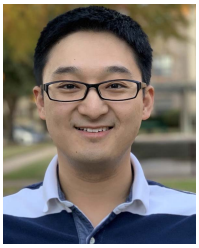

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