Millimeter-Wave Quadrature Mixed-Mode Transmitter With Distributed Parasitic Canceling and LO Leakage Self-Suppression

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***Abstract*— In this article, a 2 × 9-bit millimeter-wave quadrature mixed-mode transmitter (TX) with distributed parasitic canceling and LO leakage self-suppression is proposed. The mixed-mode architecture uses both digital switched capacitor power amplifier (SCPA) and analog amplifier to achieve high output power and enhanced peak/average efficiency at millimeter-wave. In addition, the distributed parasitic canceling with 3-D shielded horizontal capacitor (3-D SHCAP) is adopted to decrease the passive loss for improved efficiency. Besides, the LO leakage self-suppression is introduced, which benefits to linearity and dynamic range. The proposed quadrature mixed-mode TX is implemented and fabricated in the 40-nm CMOS technology. With 1.1/2.2-V supply, it achieves saturated output power of 24.03 dBm with peak system efficiency (SE) of 31.5% at 24 GHz. It also exhibits 23.6% SE for 6-dB PBO at 24 GHz due to Doherty operation. It supports 400-MHz 64QAM signal with an average output power (i.e., P_{avg}) of 16.37 dBm, an EVM of −29.6 dB, and an ACLR $\leqslant$ −29.98 dBc. For 200-MHz 256QAM, it exhibits 15.21 dBm P_{avg} with an EVM of −30.9 dB and an ACLR $\leqslant$ −31.71 dBc at 24 GHz.**

***Index Terms*— CMOS, LO leakage, millimeter-wave, mixed-mode, parasitic canceling, switched capacitor power amplifier (SCPA), transmitter (TX).**

I. Introduction

TO MEET the demands of multi-Gb/s data rate wireless transmission such as 5G new radio, there is growing requirement of millimeter-wave transmitters (TXs) with high output power, high efficiency, and large data rate [1], [2], [3], [4]. The outphasing TX uses two high-efficiency power amplifiers (PAs) with constant envelop to achieve high system efficiency (SE), which is attractive for millimeter-wave wireless [5], [6], [7], [8], [9]. Nevertheless, the high-resolution phase control of each sub-PA is challenging in the out-phasing architecture to support the complex modulation signal and higher data rate. The analog PAs are usually adopted in millimeter-wave TXs [10], [11], [12], [13], [14], [15], [16]. However, the digital-to-analog-converter (DAC) is required for the analog PA-based TX, which is power-hungry for large data rate operation and deteriorates TX efficiency.

The digital PA (DPA) achieves directly digital modulation according to the baseband (BB) control signals, which leads to the simplified architecture without mixer and DAC circuits. The DPA operating at the switching mode features high efficiency. The high-efficiency DPAs are usually developed for sub-6 GHz in recent year [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39]. The current-mode DPAs based on Class-E [24], [25] and inverse Class-D [26], [27] are reported with high efficiency. However, current-mode DPA introduces significant AM–AM and AM–PM distortions, which requires the digital pre-distortion (DPD) for linearity enhancement. The voltage-mode switched capacitor PA (SCPA) is introduced with high linearity by controlling the ratio of switched-on capacitance and total capacitance of all unit cells [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39].

With the above-mentioned merits, DPAs also exhibit good potential for millimeter-wave TXs. Some millimeter-wave digital TXs are reported with relatively low effective number of bits (ENoBs) [40], [41], [42]. The high-order QAM signals, such as 256QAM, cannot be supported by these digital TXs. The millimeter-wave digital TXs with improved ENoBs are reported in [43], [42], and [45], which shows relatively low P_{out} and efficiency. The increasing parasitic of transistors at millimeter-wave frequency limits the switching speed of power DAC, which leads to efficiency degradation of digital TX. Meanwhile, the routing parasitics also deteriorate P_{out} and efficiency. Recently, the millimeter-wave digital TXs are proposed with improved P_{out} and efficiency [46], [47], [48]. The current-mode millimeter-wave quadrature digital TX using synthesized impedance variation compensation is proposed for 5G wireless and backhaul communication [46]. The parasitic of routing is compensated by the notched-matching network with improved efficiency. A millimeter-wave quadrature switched capacitor RFDAC is proposed with good linearity [47].

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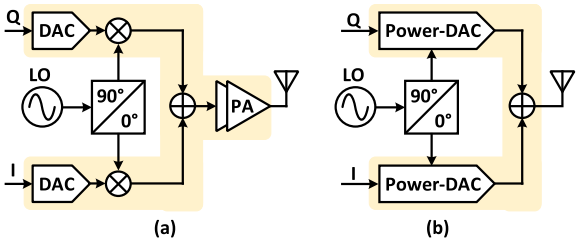

Fig. 1. Simplified architectures of (a) quadrature analog TX and (b) quadrature digital TX.

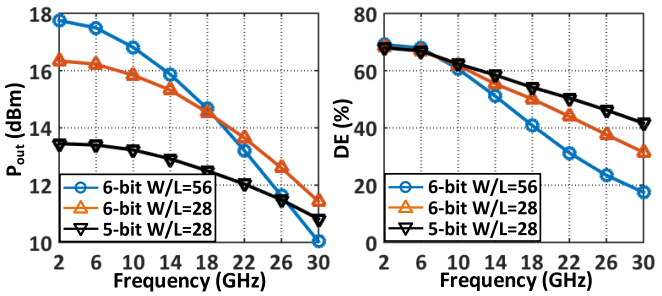

Fig. 2. Simulated P_{out} and DE of the conventional SCPA with various sizes of MSB unit cells versus operation frequency.

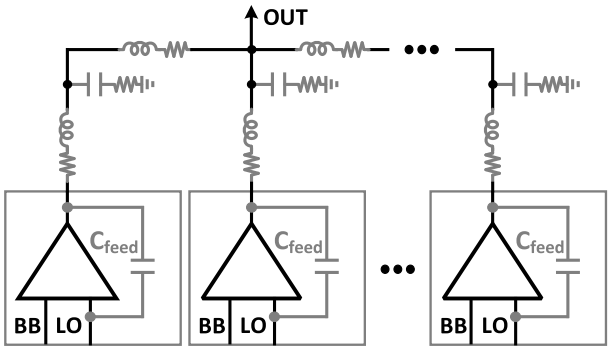

Fig. 3. Simplified configuration of power DAC with interconnections.

The edge-combining technique is introduced to allow the switching transistors to operate properly at millimeter-wave with high efficiency. Besides, a four-way series Doherty digital polar TX is introduced [48]. The current-mode unit cell consisting of a differential pair and a switchable tail transistor is adopted to implement the power DAC with high efficiency. These reported millimeter-wave digital TXs support high date rate transmission with improved performance. However, they still suffer from relatively low P_{out} and SE. Besides, the LO leakage at millimeter-wave significantly limits the dynamic range [49] and deteriorates the linearity of DPA. Therefore, there are still great challenges in millimeter-wave digital TX design with high performance including P_{out}, efficiency, linearity, LO leakage, and dynamic range.

In this article, a 2 × 9-bit millimeter-wave quadrature mixed-mode TX with distributed parasitic canceling and LO leakage self-suppression is proposed [50]. Both the digital and analog PA techniques are introduced in the mixed-mode TX to achieve high P_{out} and efficiency at millimeter-wave. The distributed parasitic canceling sub-PA array is adopted to decrease the passive loss and increase the SE. The LO leakage self-suppression technique is introduced to improve the linearity and dynamic range. Besides, a Doherty PA is used to improve the power back-off (PBO) efficiency. This article is organized as follows. Section II discusses the architecture and principle of the proposed mixed-mode TX with distributed parasitic canceling and LO leakage self-suppression. Section III introduces the circuit implementation of the proposed mixed-mode TX. Section IV shows the measurement results and comparisons with the state-of-the-arts. Finally, conclusion is given in Section V.

II. Millimeter-Wave Mixed-Mode TX With Distributed Parasitic Canceling and LO Leakage Self-Suppression

A. Mixed-Mode TX

The quadrature architecture is chosen due to its larger modulation bandwidth compared with the polar architecture. The simplified architecture of the quadrature analog TX is shown in Fig. 1(a). The multistage analog PA is usually used in the final stage for higher output power (P_{out}) and gain. The separate modules of DAC and mixer are required for the analog architecture, which introduces extra power consumption and limits SE. The simplified architecture of the quadrature digital TX is shown in Fig. 1(b). The modules of DAC, mixer, and PA are replaced by power DAC, which leads to compact architecture with improved SE. However, the increased parasitics of transistors limit the performances of digital TXs, especially at millimeter-wave. The simulated P_{out} and drain efficiency (DE) of the conventional SCPA with various sizes of MSB unit cells versus operation frequency are shown in Fig. 2. P_{out} and DE of SCPA are decreasing with increased operation frequency. Higher P_{out} can be achieved using larger transistor size and bit number as shown in Fig. 2. However, the parasitics increase with larger transistor size and bit number, which deteriorate the efficiency at higher frequency. Besides, as shown in Fig. 3, a key problem of millimeter-wave digital TXs is the parasitic of interconnections. Digital TXs with larger bit number require more complex interconnections, which further decrease the efficiency. Besides, the parasitic capacitor C_{feed} between the input and the output of each unit cell leads to LO leakage, which decreases the dynamic range and linearity. Therefore, it is a great challenge to design large dynamic range and linear digital TX featuring both high P_{out} and high efficiency at millimeter-wave frequency.

To achieve high P_{out}/efficiency and LO leakage suppression at millimeter-wave, the mixed-mode TX with distributed parasitic canceling and LO leakage self-suppression is proposed as shown in Fig. 4, which is composed of a quadrature SCPA and a Doherty analog PA. The quadrature SCPA achieves signal modulation according to BB signals without DAC and mixer circuits, which simplifies the TX architecture. The SCPA shows high linearity, which benefits to high-order modulation with wide modulation bandwidth. Meanwhile, the small-size transistors are adopted in SCPA, which introduce

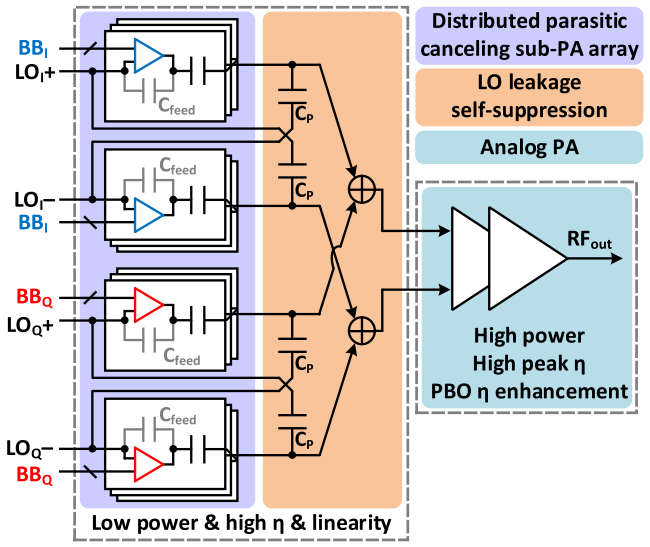

Fig. 4. Proposed mixed-mode TX with distributed parasitic canceling and LO leakage self-suppression.

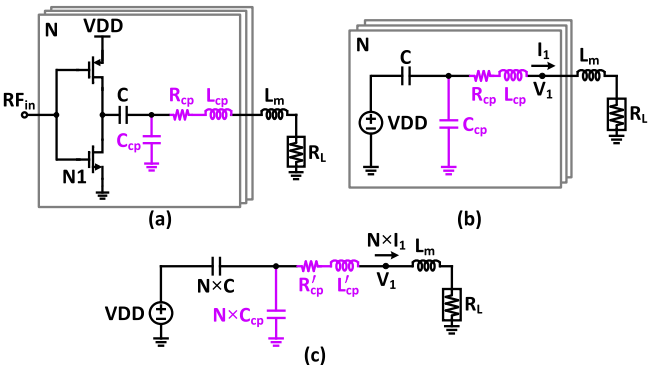

Fig. 5. (a) Schematic of SCPA considering parasitics. (b) Circuit model of SCPA. (c) Equivalent circuit of SCPA.

lower parasitic for enhanced efficiency. In addition, the distributed parasitic canceling is proposed in SCPA to further decrease the parasitic caused by interconnection for high passive efficiency. Besides, to improve the dynamic range and linearity, the LO leakage self-suppression using compensation capacitors C_p is proposed. To achieve enough P_{out} for wireless communication, the high-efficiency analog PA is adopted after the quadrature SCPA. The Doherty technique is introduced for PBO efficiency enhancement.

B. Distributed Parasitic Canceling

To analyze the effect of parasitic on P_{out} and DE of SCPA, the schematic and circuit model of the conventional SCPA are shown in Fig. 5(a) and (b), respectively. Suppose the SCPA consists of N identical unit cells. Each unit cell is composed of an inverter and unit capacitor C. The inductor L_m is used as the output matching network. C_{cp} represents the parallel parasitic capacitor from interconnection. R_{cp} and L_{cp} are the equivalent parasitic resistance and inductance of interconnection, respectively. Under saturated P_{out}, all the unit cells are switched on with supply voltage of VDD. The output current of each unit cell is I_1. The equivalent circuit of the SCPA with peak output power is shown in Fig. 5(c). $R'_{\text{cp}} = R_{\text{cp}}/N$ and $L'_{\text{cp}} = L_{\text{cp}}/N$. The maximal output voltage of the SCPA can be calculated by

$$V_{\text{out}} = \frac{2}{\pi}\left(\frac{C}{C + C_{\text{cp}}}\right)\text{VDD}. \tag{1}$$

P_{out} of the SCPA is expressed by

$$P_{\text{out}} = \frac{2}{\pi^2}\left(\frac{C}{C + C_{\text{cp}}}\right)^2 \frac{\text{VDD}^2}{R_L + R'_{\text{cp}}}. \tag{2}$$

The effective output power delivered on the load R_L is represented by the following equation:

$$P_{\text{out},e} = P_{\text{out}} \times \frac{R_L}{R_L + R'_{\text{cp}}}. \tag{3}$$

The dynamic power dissipation, which is caused by parasitic capacitor C_{cp}, can be evaluated by

$$P_{\text{SC}} = \frac{C \times C_{\text{cp}}}{C + C_{\text{cp}}} N \times \text{VDD}^2 \times f_c \tag{4}$$

where f_c is the carrier frequency. Then, the peak DE of SCPA can be calculated by

$$\text{DE}_{\text{peak}} = \frac{P_{\text{out},e}}{P_{\text{out}} + P_{\text{SC}}} = \frac{4Q_{\text{loaded}} \times \frac{R_L}{R_L + R'_{\text{cp}}}}{4Q_{\text{loaded}} + \frac{\pi N C_{\text{cp}}(C + C_{\text{cp}})}{C^2}} \tag{5}$$

where Q_{loaded} is the loaded quality factor of the network. It can be seen that P_{out} and DE of SCPA are affected by the ratio of C_{cp}/C. By defining r as

$$r = \frac{C_{\text{cp}}}{C}. \tag{6}$$

Equations (3) and (5) can be further expressed by

$$P_{\text{out},e} = \frac{2}{\pi^2}\left(\frac{1}{1 + r}\right)^2 \times \frac{\text{VDD}^2}{\left(R_L + R'_{\text{cp}}\right)^2} R_L \tag{7}$$

$$\text{DE}_{\text{peak}} = \frac{4Q_{\text{loaded}}}{4Q_{\text{loaded}} + \pi N r(1 + r)} \times \frac{R_L}{R_L + R'_{\text{cp}}}. \tag{8}$$

For output impedance matching, the inductance of L_m is determined by

$$L_m = \frac{1}{4\pi^2 f_c^2 N \times (C + C_{\text{cp}})} - L'_{\text{cp}}. \tag{9}$$

Note that C_{cp} is absorbed into the matching network as shown in Fig. 5(c). The maximal P_{out} is deteriorated by r and resistance of R'_{cp}. To improve the effective P_{out}, the parasitic C_{cp} and R'_{cp} should be limited when C and R_L are determined in the circuit design. Based on (8), the peak DE of SCPA is affected by r, R'_{cp}.

The EM-simulated C_{cp} introduced by the typical interconnection with the MOM capacitor is shown in Fig. 6. The typical size of the routing is 6 × 10 um, which is implemented using single top thick metal layer. It introduces C_{cp} of about 5.2 fF from 20 to 40 GHz. When operating at low frequencies (e.g., sub-6 GHz), C in SCPA is usually larger than 100 fF. Therefore, the ratio r of C_{cp}/C is 0.052, which introduces little effect on P_{out} and DE. However, at millimeter-wave frequency,

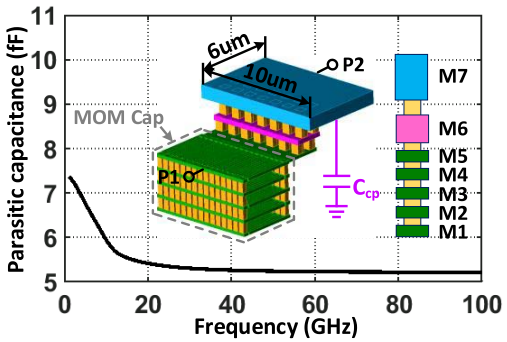

Fig. 6. EM-simulated C_{cp} introduced by interconnection.

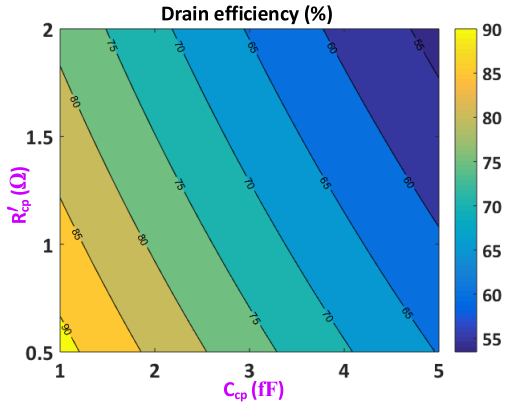

Fig. 7. Calculated DE of 6-bit SCPA at 28 GHz (C = 20 fF, R_L = 10 Ω).

C should be lower, which leads to higher r. Therefore, P_{out} and DE are degraded at mm-wave.

The DE of a 6-bit (i.e., $N = 63$) SCPA with $C = 20$ fF and $R_L = 10\ \Omega$ is calculated at 28 GHz according to (8), as shown in Fig. 7. The calculated DE is decreased rapidly from 90% to about 65% when C_{cp} increases from 1 to 5 fF, which implies the significant effect of C_{cp} for millimeter-wave SCPA. Therefore, C_{cp} and R_{cp} caused by interconnection should be reduced for enhanced performances of millimeter-wave SCPA.

To reduce C_{cp} and R_{cp}, the distributed parasitic canceling is introduced to implement the sub-PA array in this work. Fig. 8(a) shows three types routing configurations (i.e., Types I, II, and III) for sub-PA array. For conventional solution (i.e., Type I), the MOM capacitor C is located besides the routing. The electric field of the routing reaching the lossy substrate introduces high passive loss, which leads to increased R_{cp} with lower SCPA efficiency. Meanwhile, the quality factor (Q) of the conventional MOM capacitor is limited by the diverging electric field reaching the lossy substrate. In addition, the parasitic capacitor caused by both the unit capacitor and routing contributes to C_{cp}, which leads to lower efficiency. The EM-simulated C_{cp} of the single unit cell for Type I is shown in Fig. 8(b). C_{cp} is about 5.2 fF from 20 to 40 GHz. For Type II, the conventional MOM capacitors are placed under the routing to shield the electric field. C_{cp} is decreased compared with Type I, which is about 4 fF from 20 to 40 GHz as shown in Fig. 8(b). However, the electric field of routings is partially absorbed by

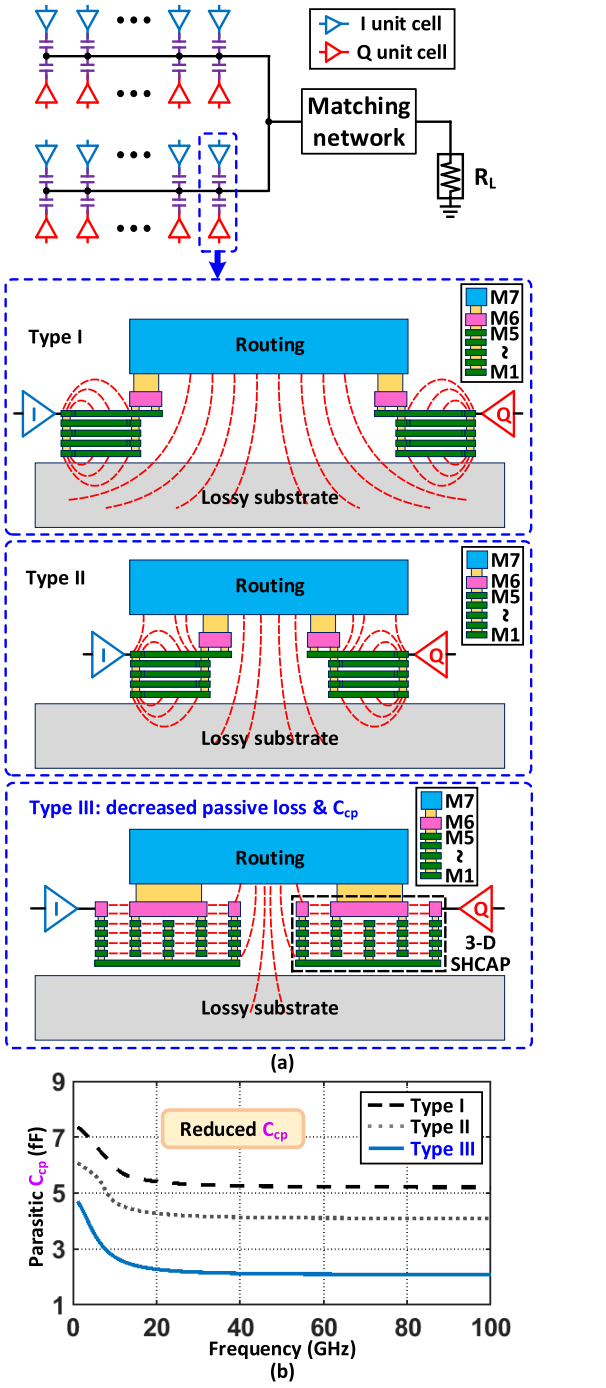

Fig. 8. (a) Three types of routings for sub-PA array. (b) EM-simulated C_{cp} of Types I, II, and III.

the conventional MOM capacitor, which decreases the model accuracy of MOM capacitor.

To decrease the parasitics, the 3-D shielded horizontal capacitor (3-D SHCAP) with intrinsic high Q is introduced as shown in Fig. 8(a), i.e., Type III. The detailed characteristics' discussion about 3-D SHCAP is shown in the Appendix. The 3-D SHCAPs are located under the routings dispersedly. Most of the routing electric field is absorbed by the 3-D SHCAP, which leads to reduced substrate loss and C_{cp}. In addition, the 3-D SHCAP features higher Q compared

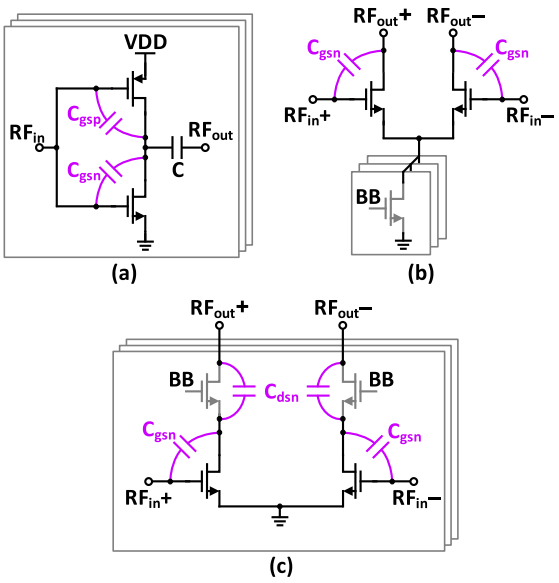

Fig. 9. Analysis of the feed-through capacitor of (a) conventional SCPA, (b) unit cell using a differential pair and switchable tail transistors, and (c) unit cell based on the cascode structure.

with the conventional MOM capacitor, which further decreases the passive loss. Besides, the parasitic inductance from the routing between two SCPA unit cells is smaller for Type III, which is partially absorbed into the embedded 3-D SHCAP. The EM-simulated C_{cp} for Type III is shown in Fig. 8(b), which is much lower than Type I and Type II (about 2 fF from 20 to 40 GHz). The 3-D SHCAP also shows high Q for lower passive loss. Therefore, the efficiency of SCPA can be improved by the proposed distributed parasitic canceling technique, which features lower R_{cp} and C_{cp}.

C. LO Leakage Self-Suppression

The parasitic capacitor C_{feed} between the input and the output of the unit cell introduces LO leakage, especially at millimeter-wave. Fig. 9 shows three types of unit cells, which are usually used in millimeter-wave DPA design. C_{feed} of the SCPA unit cell can be expressed by the following equation:

$$C_{feed,a} = C_{gsp} + C_{gsn}. \tag{10}$$

C_{feed} of the unit cell using differential pair with switchable tail transistors is

$$C_{feed,b} = C_{gsn}. \tag{11}$$

C_{feed} of the unit cell based on the cascode structure is expressed by

$$C_{feed,c} = \frac{C_{dsn}C_{gsn}}{C_{dsn} + C_{gsn}}. \tag{12}$$

For the SCPA unit cell, both the parasitic gate–source capacitor of NMOS and PMOS (i.e., C_{gsn} and C_{gsp}) contribute to C_{feed}. $C_{feed,a}$ is larger than $C_{feed,b}$ or $C_{feed,c}$. Therefore, SCPA shows larger LO leakage than other types of unit cells. In addition, in the CMOS technology, the carrier mobility of NMOS and PMOS is different. To obtain better AM–AM and AM–PM

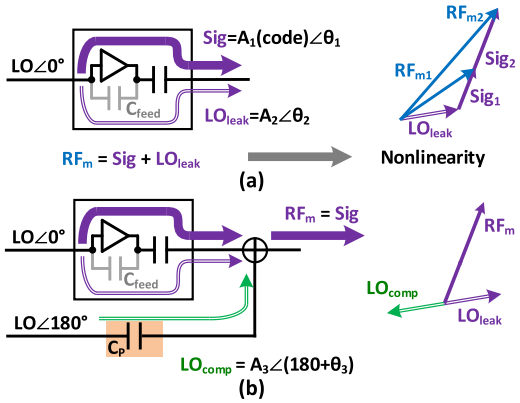

Fig. 10. (a) Simplified circuit model considering LO leakage. (b) Concept of the proposed LO leakage self-suppression.

linearity, the on-resistances of NMOS and PMOS for the SCPA unit cell should be the same [29]. The width of the transistor with lower carrier mobility should be increased for the same on-resistance. Thus, the parasitic C_{gsp} further increases and introduces growing LO leakage.

A simplified ideal circuit model of SCPA is adopted to evaluate the effect of LO leakage, as shown in Fig. 10(a). Ideally, the amplitude A_1 of the amplified SCPA output signal (i.e., Sig) is supposed to be linearly increasing with control code, while the phase of Sig should maintain θ_1 in ideal condition for SCPA. However, C_{feed} leads to LO leakage LO_{leak} at SCPA output. Here, for simple analysis, the LO leakage is assumed to be unchanged (i.e., $\mathrm{LO}_{leak} = A_2\angle\theta_2$) versus control code. Then, the output signal RF_m of SCPA (i.e., vector sum of Sig and LO_{leak}) can be expressed by

$$\mathrm{RF}_m = \mathrm{Sig} + \mathrm{LO}_{leak} = A_1(\mathrm{code})\angle\theta_1 + A_2\angle\theta_2. \tag{13}$$

The LO leakage leads to reduced dynamic range and linearity. To address these issues, the LO leakage self-suppression is introduced in this work, as shown in Fig. 10(b). A LO signal path with opposite phase is used to decrease LO leakage. The compensation capacitor C_p should be equal to the total C_{feed} and C. Then, the LO with 180° phase difference introduces the compensation signal LO_{comp} at SCPA output. LO_{comp} can be represented as

$$\mathrm{LO}_{comp} = A_3\angle(\theta_3 + 180°). \tag{14}$$

When $A_3 = A_2$ and $\theta_3 = \theta_2$, LO_{comp} and LO_{leak} featuring opposite phase are canceled by each other. Then, the output signal of SCPA is

$$\begin{aligned}\mathrm{RF}_m &= \mathrm{Sig} + \mathrm{LO}_{leak} + \mathrm{LO}_{comp}\\ &= A_1(\mathrm{code})\angle\theta_1 + A_2\angle(\theta_2) + A_3\angle(\theta_3 + 180°)\\ &= A_1(\mathrm{code})\angle\theta_1.\end{aligned} \tag{15}$$

The simplified circuit of differential SCPA with LO leakage self-suppression is shown in Fig. 11. Two compensation capacitor C_p are introduced to suppress the LO leakage. The calculated normalized output voltage (V_{out}) and output phase versus normalized control code with/without LO leakage self-suppression at the output node of SCPA are compared

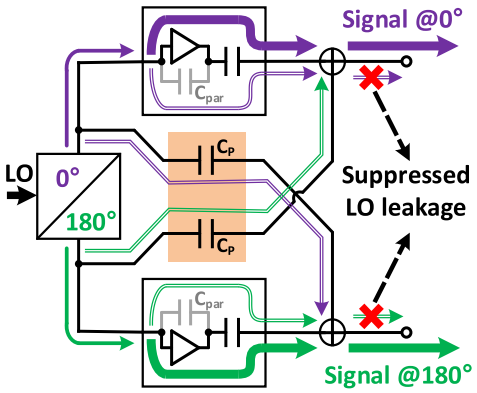

Fig. 11. Implementation of differential SCPA with LO leakage self-suppression.

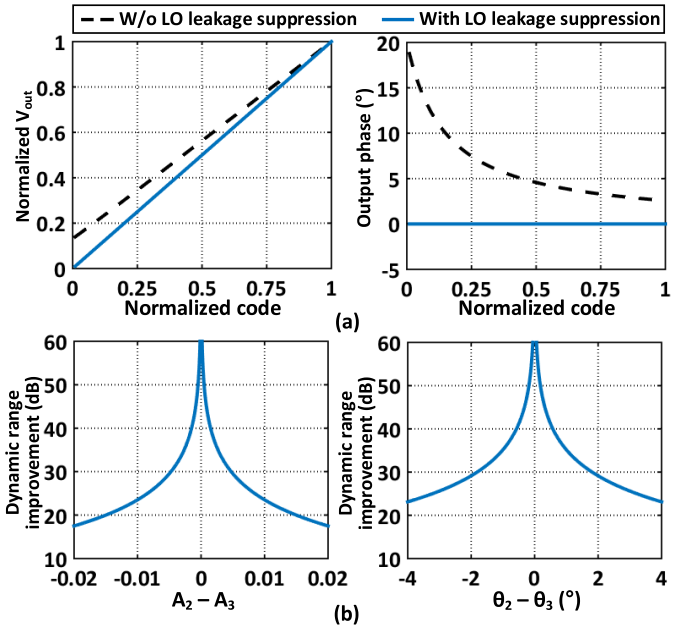

Fig. 12. (a) Calculated AM–AM and AM–PM distortions with and without LO leakage self-suppression of an ideal circuit model for SCPA. (b) Calculated effects of amplitude and phase differences between LO_{leak} and LO_{comp} on dynamic range improvement (A_1 is linear to code. $A_2 = 0.15$, $\theta_1 = 0°$, $\theta_2 = 20°$).

according to (13)–(15), as shown in Fig. 12(a). A_1 is learnt with the input code and $A_2 = A_3 = 0.15$. θ_1 is 0° and $\theta_2 = \theta_3 = 20°$. The AM–PM/AM–AM distortions can be eliminated by introducing the LO leakage self-suppression. The LO leakage self-suppression avoids the dynamic range degradation. Ideally, the LO leakage can be eliminated to 0. However, the amplitude and phase differences between LO_{leak} and LO_{comp} deteriorate LO leakage suppression level and dynamic range. The calculated effects of amplitude and phase differences between LO_{leak} and LO_{comp} on dynamic range improvement are shown in Fig. 12(b).

III. Circuit Implementation

A. Architecture

The block diagram of the proposed 2 × 9-bit quadrature mixed-mode TX with distributed parasitic canceling and LO leakage self-suppression is shown in Fig. 13. The 2 × 9-bit BB IQ signals I⟨8:0⟩ and Q⟨8:0⟩ are generated by the deserializers. The quadrature LO generator and sign-map circuit consist of the coupler A and two BPSK modulators. The sign bits I⟨8⟩ and Q⟨8⟩ determine the quadrant of the output signal. The quadrature SCPA is composed of the 5-bit MSB and 3-bit LSB unit cells, which are controlled by thermometer codes (i.e., BBQ⟨33:3⟩ and BBI⟨33:3⟩) and binary codes (i.e., BBQ⟨2:0⟩ and BBI⟨2:0⟩) converted from parallel BB signals I⟨7:0⟩ and Q⟨7:0⟩ by decoders, respectively. To increase the data rate, six 1:3 deserializers are used in this work, which convert the serial BB signals into parallel BB signals.

Four compensation capacitors C_p are introduced for LO leakage suppression. The value of C_p is determined by C_{feed}. Considering the practical interconnection metal routings in the canceling path, C_p is optimized to compensate the unexpected effects caused by parasitics. The simulated LO leakage and dynamic range with various values of C_p are shown in Fig. 14(a) and (b), respectively. C_p can be finely adjusted for the case of wideband operation covering 22–30 GHz with similar LO leakage suppression level around −30 dBm. Besides, C_p can be tuned to improve the LO leakage suppress level for high dynamic range. Here, C_p is optimized as 70 fF considering the tradeoff between wideband operation and LO leakage suppression level.

The simulated results of normalized V_{out} and output phase for the proposed mixed-mode TX versus normalized control code at 28 GHz when I = Q with/without LO leakage self-suppression are compared in Fig. 15. The comparison verifies that LO leakage of the proposed mixed-mode TX is decreased over 10% compared with the one without LO leakage self-suppression. The AM–PM distortion is also reduced about 12.8°. The schematic of the quadrature SCPA unit cell is shown in Fig. 13. The sizes of the NMOS transistors are 5 um/40 nm, while the sizes of PMOS transistors are 4 um/40 nm. The 3-D SHCAP with high Q is introduced to decrease the passive loss. The 3-D SHCAP is 32 fF for the 5-bit MSB unit cell. The unit capacitors for the 3-bit LSB unit cell capacitors are 16, 8, and 4 fF, which can be finely achieved in the CMOS technology [51]. The output signal RFm of quadrature SCPA is further amplified by a two-stage Doherty PA, which achieves high output power and improves the efficiency at 0- and 6-dB PBOs.

B. Distributed Parasitic Canceling Sub-PA Array

The floor plan of the distributed parasitic canceling sub-PA array is shown in Fig. 16, which includes the 2 × 31 MSB quadrature unit cells (including differential pair), 2 × 3 LSB quadrature unit cells (including differential pair), decoders, and interconnections. The routings connected to the positive and negative output ports (i.e., OUT+ and OUT−) are colored by green and blue, respectively. The decoders converts the 5-bit binary codes I⟨7:3⟩ and Q⟨7:3⟩ into thermometer codes, which control the 5-bit I and Q unit cells, respectively. The I and Q LSB unit cells are controlled by the I⟨2:0⟩ and Q⟨2:0⟩,

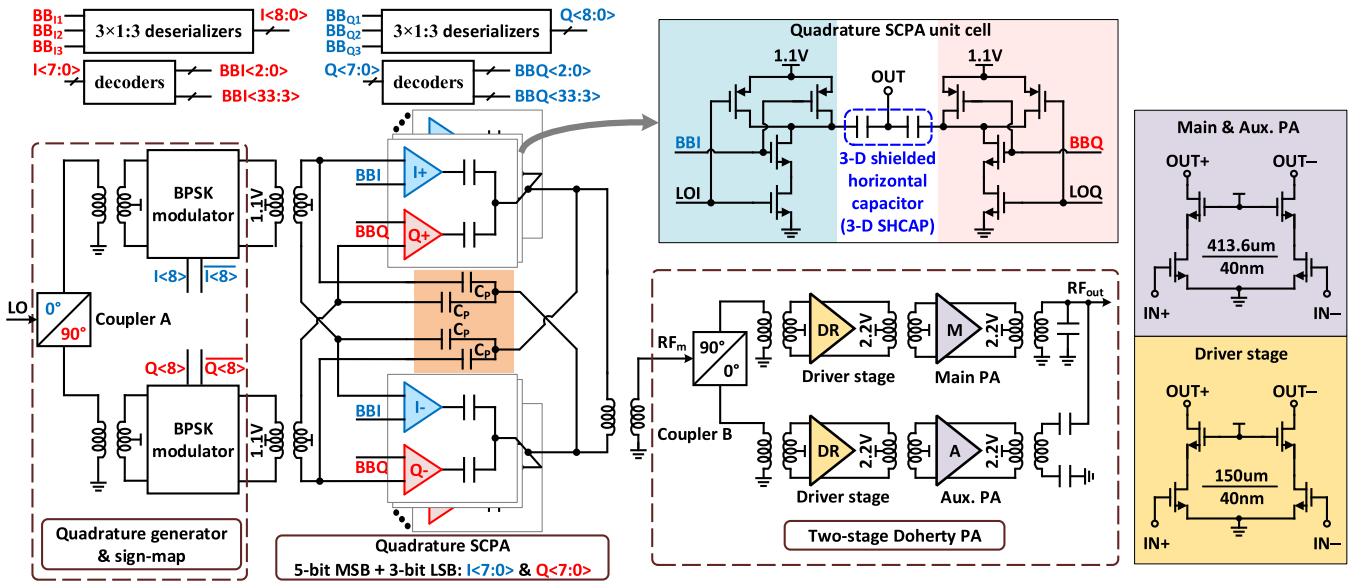

Fig. 13. Block diagram of the proposed quadrature mixed-mode TX.

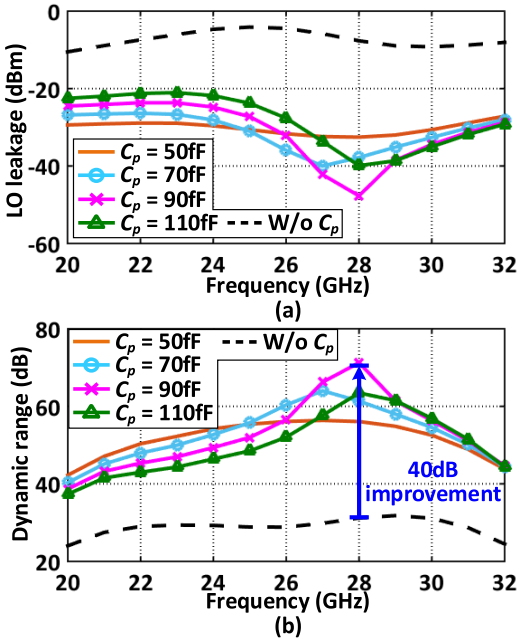

Fig. 14. Simulated effect of C_p on (a) LO leakage and (b) dynamic range in operation frequency from 22 to 30 GHz.

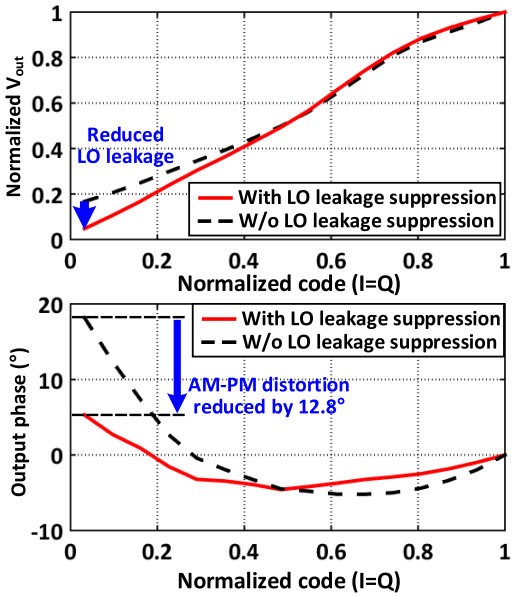

Fig. 15. Simulated typical AM–AM and AM–PM distortions at 28 GHz.

respectively. The BB control codes for differential unit cells are identical.

The passive loss including the substrate loss can be decreased using the proposed distributed parasitic canceling. Fig. 17(a) shows the simulated passive efficiency of the conventional Type I and proposed Type III using distributed parasitic canceling. It achieves 16%–32% improvement of passive efficiency in 20–32 GHz compared with conventional Type I. The simulated DEs of the conventional Type I and proposed Type III are compared in Fig. 17(b). The DE of the proposed quadrature SCPA is increased in 20–32 GHz, while the peak DE is improved by 9% at 25 GHz.

C. Two-Stage Doherty PA

The proposed two-stage Doherty PA is shown in Fig. 13, which consists of a coupler B, driver stages, Main PA, and Aux. PA. Coupler B generates the RF signals with 90° and 0° phase. The Main PA is operating at Class-AB, and the Aux. PA operates at Class-B. The cascode common-source (CS) structure is introduced to implement the drivers, Main PA, and Aux. PA. The transistor sizes of drivers are 150 um/40 nm, while the transistor sizes of Main and Aux. PAs are 413.6 um/40 nm, respectively. An output matching network with 90° phase shifting is adopted for load modulation. The simulated linearity of the two-stage Doherty PA is shown in Fig. 18(a). It shows a saturated P_{out} of 25 dBm at 24 GHz.

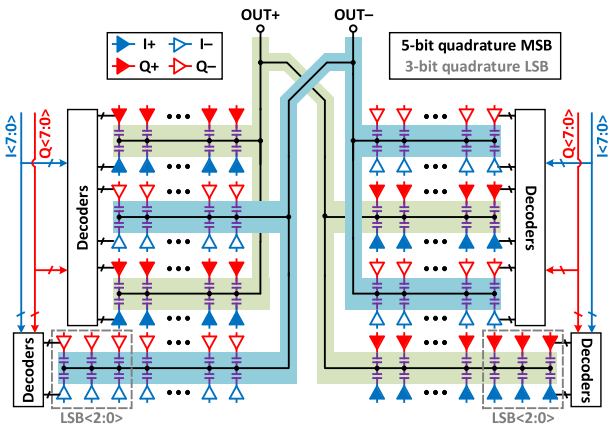

Fig. 16. Floor plan of the distributed parasitic canceling sub-PA array with the 5-bit MSB and 3-bit LSB quadrature unit cells.

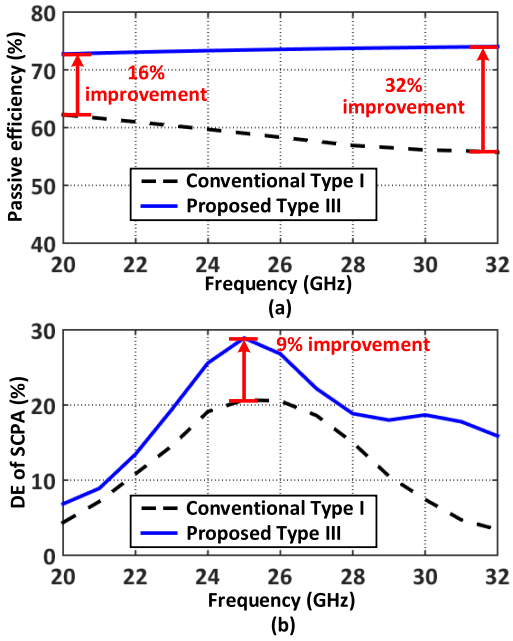

Fig. 17. (a) Simulated passive efficiency of interconnections. (b) Simulated DE of SCPA.

Fig. 18(b) exhibits the simulated small-signal gain and power-added efficiency (PAE) at saturated P_{out}. It features a power gain of about 20 dB from 22 to 30 GHz. The peak power gain and peak PAE are 20.7 dB and 35% at 24 GHz, respectively.

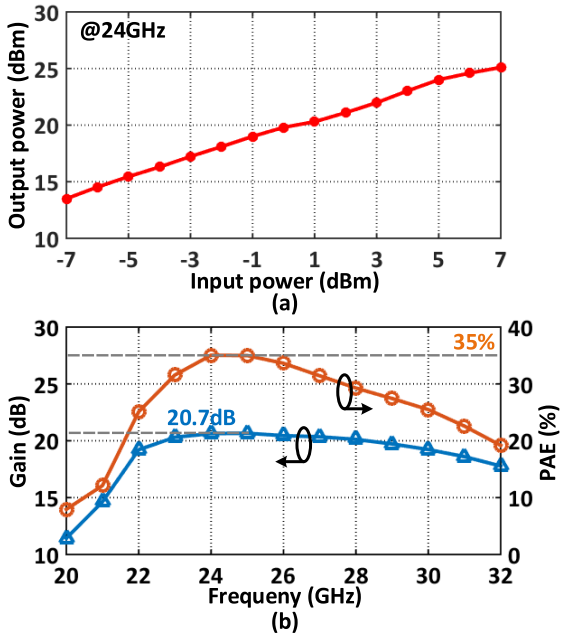

Fig. 18. (a) Simulated linearity of the two-stage Doherty PA. (b) Simulated small-signal gain and PAE of the PA at saturated P_{out}.

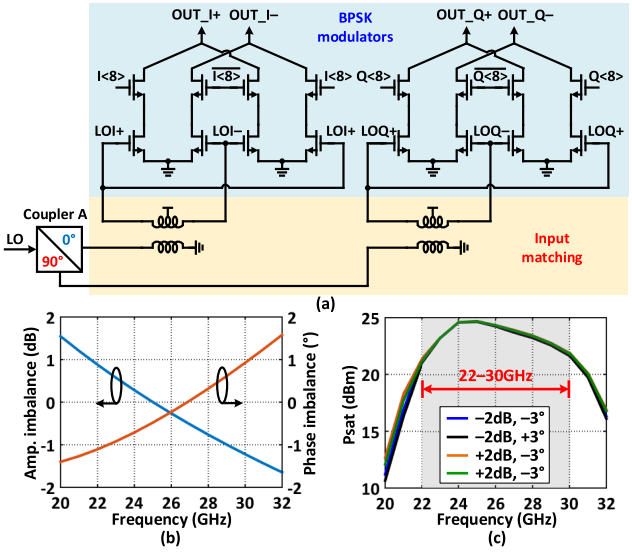

Fig. 19. (a) Schematic of the sign-map circuit. (b) Simulated amplitude and phase imbalances of coupler A. (c) Simulated effect of amplitude and phase imbalance on saturated output power of the proposed mixed-mode TX.

D. Sign-Map Circuit

The schematic of sign-map is shown in Fig. 19(a), which is composed of a coupler A, two input matching networks based on the transformer, and two BPSK modulators. The LOs with the in-phase and quad-phase (i.e., I and Q signals) are generated by coupler A. The two BPSK modulators switch the I and Q signals between in-phase and out-of-phase according to sign bits I⟨8⟩ and Q⟨8⟩, respectively. The simulated amplitude and phase imbalances of coupler A is shown in Fig. 19(b). It exhibits amplitude/phase imbalances of ±1.65 dB/±1.58° in the operation frequency range. The simulated effects of amplitude and phase imbalances on the saturated output power of the proposed mixed-mode TX are shown in Fig. 19(c). The four conditions (i.e., amplitude/phase imbalances of −2 dB/−3°, −2 dB/+3°, +2 dB/−3°, and +2 dB/+3°) are compared, which leads to maximal 0.38 dBm variation on TX P_{out} in the operation frequency from 22 to 30 GHz.

IV. Fabrication and Measurement

The proposed millimeter-wave quadrature mixed-mode TX is fabricated in a 40-nm CMOS technology, which occupies 1.2 × 1.7 mm including all I/O pads with 1.1/2.2-V supply,

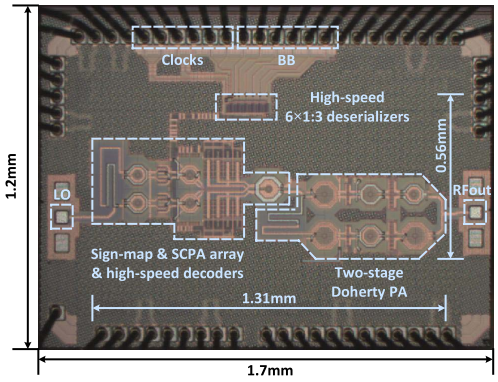

Fig. 20. Die micrograph.

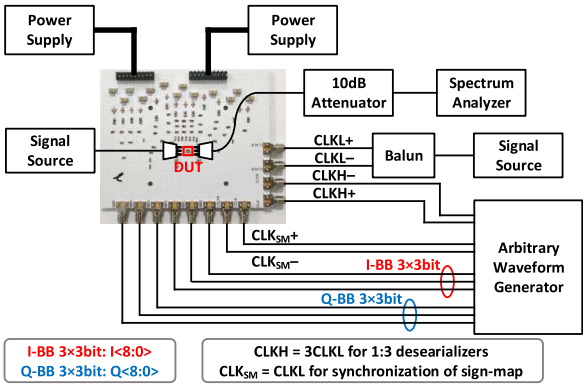

Fig. 21. Measurement setup.

as shown in Fig. 20. The chip core size is 0.56 × 1.31 mm. The measurement setup is shown in Fig. 21. A signal generator is used to generate the LO signal. The 3 × 3 bit I/Q BB signals are generated by the arbitrary waveform generator (AWG). The two differential sampling clocks (i.e., the CLKL and CLKH with CLKH = 3CLKL) for the deserializers are generated by the signal generator with balun and AWG, respectively. The synchronization clock CLK_{SM} for the sign-map circuit is generated by the AWG. The output signal of the proposed mixed-mode TX is attenuated by a 10-dB attenuator and measured by the spectrum analyzer.

As shown in Fig. 22(a), the proposed mixed-mode TX features peak P_{sat} of 24.03 dBm with 31.5% SE at 24 GHz. The 3-dB bandwidth is about 22–30 GHz. The power consumption of the sign-map circuit, deserializers, digital circuits, all the unit cells of digital SCPA, and the two-stage Doherty PA are considered in SE calculation. The measured LO leakage and dynamic range of the proposed mixed-mode TX are depicted in Fig. 22(b). It shows a minimal LO leakage of −31.2 dBm and a maximal dynamic range of 53.9 dB.

The measured typical normalized V_{out} and output phase versus IQ code (I = Q) for the proposed mixed-mode TX at 24 and 28 GHz are shown in Fig. 23(a) and (b), respectively. It shows about 10.45° and 11.86° AM–PM distortion at 24 and 28 GHz with I = Q, which is mainly caused by LO leakage. The gain compression of the two-stage Doherty PA deteriorates the AM–AM linearity of the TX. The measured

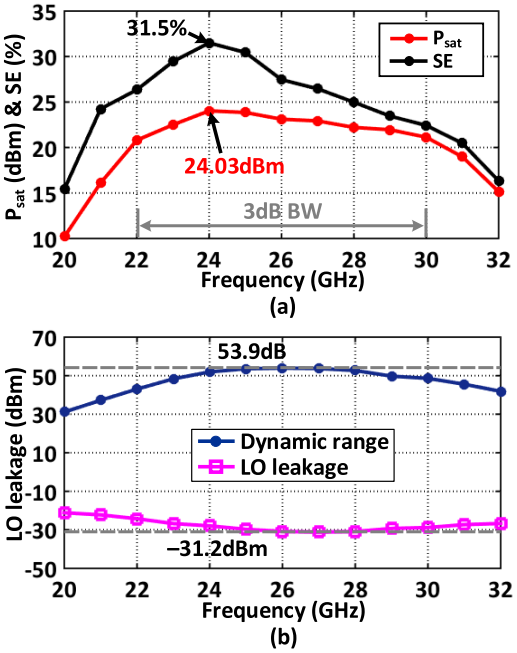

Fig. 22. (a) Measured saturated output power and SE. (b) Measured LO leakage and dynamic range.

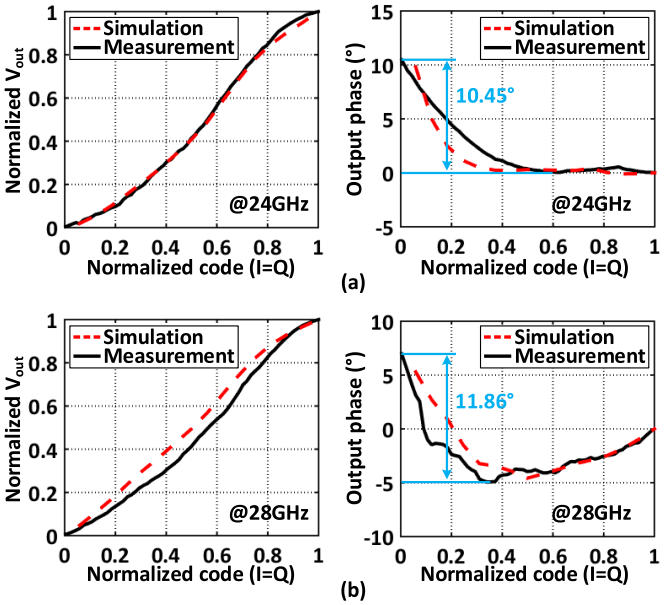

Fig. 23. Measured typical AM–AM and AM–PM distortions of the proposed mixed-mode TX at (a) 24 and (b) 28 GHz (I input code = Q input code).

SE at PBOs is shown in Fig. 24. Due to the Doherty operation, the proposed mixed-mode TX achieves 23.6% SE for 6-dB PBO at 24 GHz, which is 1.4 times of normalized Class-B.

The 2-D DPD is adopted in modulation measurement, which further minimizes the AM–AM and AM–PM distortions. The measured output spectrum and constellation of the single-carrier 400-MHz 64QAM and 200-MHz 256QAM modulation signals at 24 GHz are shown in Fig. 25(a). The measured 400-MHz 64QAM signal shows average output power (P_{avg}) of 16.37 dBm with an average SE of 17.3%, an EVM of

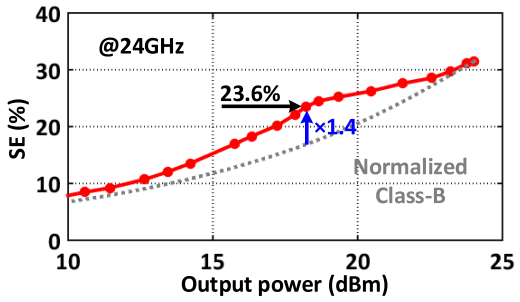

Fig. 24. Measured SE of the mixed-mode TX at PBO levels for 24 GHz.

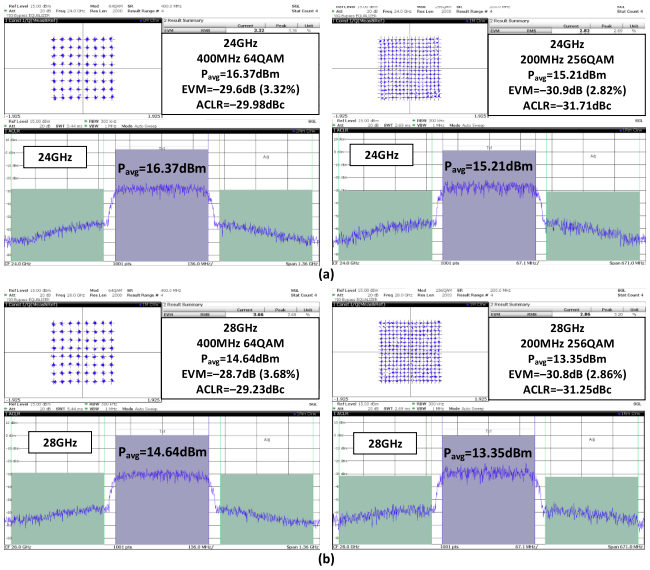

Fig. 25. Measured output spectrum and constellation of the single-carrier 400-MHz 64QAM and 200-MHZ 256QAM signals at (a) 24 and (b) 28 GHz.

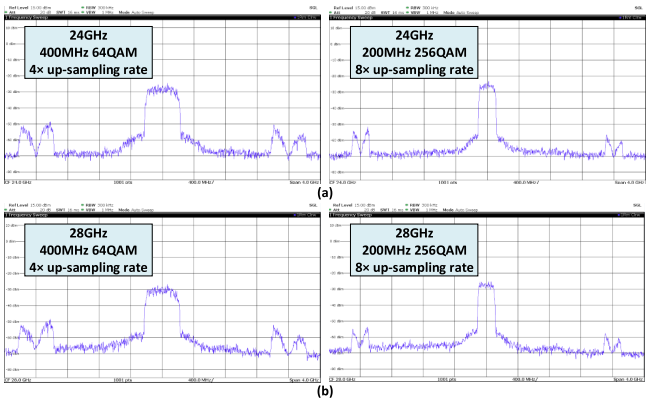

Fig. 26. Measured out-of-band spectrum of the single-carrier 200-MHz 256QAM and 400-MHz 64QAM signals at (a) 24 and (b) 28 GHz.

−29.6 dB, and an ACLR $\leqslant$ −29.98 dBc at 24 GHz. The measured 200-MHz 256QAM signal shows P_{avg} of 15.21 dBm with an average SE of 14.8%, an EVM of −30.9 dB, and an ACLR $\leqslant$ −31.71 dBc at 24 GHz. The measured output spectrum and constellation of the single-carrier 400-MHz 64QAM and 200-MHz 256QAM modulation signals at 28 GHz are shown in Fig. 25(b). The measured 400-MHz 64QAM signal

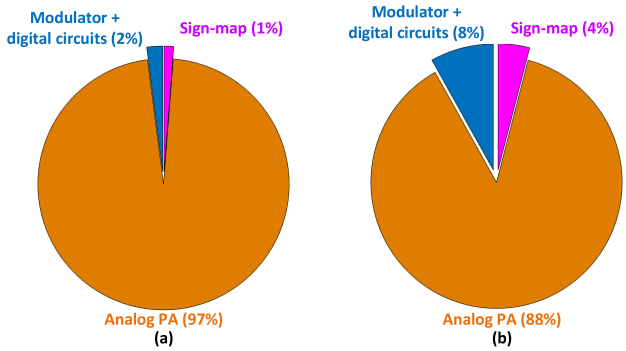

Fig. 27. Power break-down of the proposed mixed-mode TX at 24 GHz for (a) saturated P_{out} under CW measurement and (b) single-carrier 400-MHz 64QAM modulation measurement.

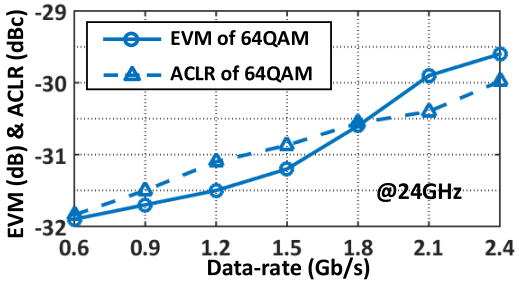

Fig. 28. Measured EVM and ACLR of the single-carrier 64QAM signals versus data rate.

TABLE I
COMPARISON OF TX ARCHITECTURES

	Proposed quadrature mixed-mode TX	Quadrature analog TX
Architecture	Quadrature modulator +analog PA	DAC + proposed analog PA
P_{sat}	24.03dBm	24.03dBm
P_{dc} of analog PA	773mW	773mW
P_{dc} of modulator & sign-map	26.2mW	N/A
P_{dc} of DAC	N/A	380mW
SE	31.5%	21.9%

exhibits P_{avg} of 14.64 dBm with an EVM of −28.7 dB and an ACLR $\leqslant$ −29.23 dBc at 28 GHz. The measured 200-MHz 256QAM signal shows P_{avg} of 13.35 dBm with an EVM of −30.8 dB and an ACLR $\leqslant$ −31.25 dBc at 28 GHz. The sampling frequency for the 200- and 400-MHz modulation signals of this work is 1.6 GHz, which is limited by the deserializers in this work. The measured out-of-band spectra of the single-carrier 200-MHz 256QAM and 400-MHz 64QAM at 24 and 28 GHz are shown in Fig. 26.

The measured power breakdown for saturated P_{out} at 24 GHz is shown in Fig. 27(a). The two-stage Doherty PA introduces the large power consumption for the TX, which is 773 mW for saturated P_{out} at 24 GHz. The quadrature modulator based on SCPA features a high efficiency, which leads to a lower power dissipation. With decreased efficiency caused by parasitic C_p, the DC power dissipation of the modulator

TABLE II
COMPARISON WITH THE STATE-OF-THE-ART MM-WAVE TXS/PAS

	Mixed-mode TX		Digital TX		Analog PA		Quadrature Analog TX	Outphasing	
	This work		Mortazavi, JSSC'22 [48]	Qian, JSSC'20 [46]	Garay, ISSCC'21 [15]	Qunaj, ISSCC'21 [16]	Pashaeifar, JSSC'21 [1]	Li, JSSC'21 [9]	Ning, JSSC'20 [8]
Technology	40nm CMOS		40nm CMOS	28nm CMOS	45nm SOI CMOS	28nm CMOS	40nm CMOS	45nm SOI CMOS	45nm SOI CMOS
Architecture	Quadrature mixed-mode TX with LO leakage suppression & distributed parasitic-canceling		Four-way series Doherty	2×10-bit IQ power-DAC	Dual-drive analog PA	Doherty-like load-modulated balanced amplifier	Double-quadrature direct upconverter with series-Doherty balanced PA	Inverse outphasing TX	Outphasing PA with current-mode combiner
Digital TX/PA/TX	Mixed-mode IQ TX		Digital polar	Digital IQ	Analog PA	Analog PA	Analog IQ	Outphasing TX front-end	Outphasing PA
Frequency (GHz)	24		29.5	20–32	28	36	27	29	30
Supply (V)	1.1/2.2		1	1	1.9	1	1	1.0/2.0	1.2
Psat (dBm)	24.03		18.7	19.02	20.1	22.6	20 (P_{1dB})	22.7	17
Peak SE (%)	31.5		24	22.1	N/A	N/A	28.5	N/A	N/A
Peak PAE (%)	N/A		N/A	N/A	48.3	32	31 (DE)	42.6 (DE)	50.5 (DE)
η@6dB PBO (%)	23.6 (SE)		15 (SE)	N/A	N/A	24.2 (PAE)	26 (DE)	30 (DE)	40 (DE)
Modulation	400MHz 64QAM	200MHz 256QAM	300MHz 64QAM	125MHz 256QAM	1.5GHz 64QAM	3GHz 64QAM	800MHz 64QAM	2.5GHz 64QAM	500MHz 64QAM
Data-rate (Gb/s)	2.4	1.6	1.8	1.0	9.0	18.0	4.8	15.0	3.0
P_{avg} (dBm)	16.37	15.21	12	10.58	14.07	15.5	11.36	15.6	10.2
Average η (%)	17.3 (SE)	14.8 (SE)	11.9 (SE)	N/A	25.13 (PAE)	20 (PAE)	17.6 (DE)	22.5 (DE)	31.2 (DE)
EVM (dB)	−29.6	−30.9	−29.39	−31.2	−25.04	−25.1	−24.6	−22.5	−28
ACLR (dBc)	−29.98	−31.71	−28	−32.4	N/A	N/A	−31.45	−29.2	−26.4
Chip size (mm^2)	2.04, 0.73 (core)		1.1 (core)	1.6	1.56	1.44	3.66	7.5	1.65

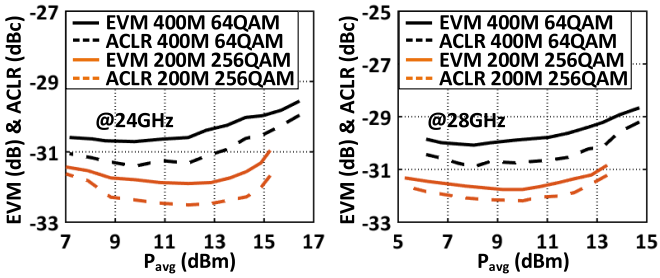

Fig. 29. Measured EVM and ACLR of the single-carrier 400-MHz 64QAM and 200-MHz 256QAM signals versus P_{avg} at 24 and 28 GHz.

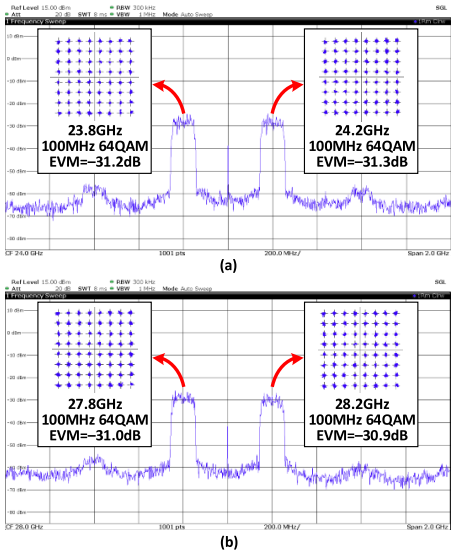

Fig. 30. Measured output spectrum and constellation of the two-carrier 100-MHz 64QAM at (a) 23.8/24.2 and (b) 27.8/28.2 GHz.

increases, which introduces growing effect on TX efficiency. Fig. 27(b) exhibits the power breakdown for the single-carrier 400-MHz 64QAM modulation measurement at 24 GHz.

The measured EVM and ACLR of the single-carrier 64QAM signals versus data rate at 24 GHz are shown in Fig. 28. The EVM and ACLR increase with higher data rate, which means a lower up-sampling rate. The 64QAM signal with 0.6 Gb/s data rate shows the EVM of −31.9 dB and ACLR of −31.8 dBc. A 2.4-Gb/s data rate is supported by the proposed millimeter-wave quadrature mixed-mode TX. The measured maximal modulation bandwidth in this work is limited by the sampling frequency of 1.6 GHz. The measured EVM and ACLR of the single-carrier 64QAM and 256QAM signals versus P_{avg} at 24 and 28 GHz are shown in Fig. 29. The proposed mixed-mode TX can support carrier aggregation (CA) operation. The measured output spectrum and constellation of two carriers at 23.8/24.2 and 27.8/28.2 GHz with the 100-MHz 64QAM modulation signals are shown in Fig. 30(a) and (b), respectively. The EVM of the 100-MHz 64QAM at 23.8 and 24.2 GHz is −31.2 and −31.3 dB, respectively. The EVM of the 100-MHz 64QAM at 27.8 and 28.2 GHz is −31.0 and −30.9 dB, respectively.

The comparison between the proposed mixed-mode TX and the convention analog TX is depicted in Table I. For example, a high-speed DAC AD9734 of ADI with 10-bit resolution and 1.2G sampling rate are adopted in the conventional analog TX system, which shows the DC power consumption of 380 mW. For a fair comparison, the analog PA in this work is used to evaluate the efficiency of the conventional analog TX. Meanwhile, the proposed 2 × 9-bit modulator with 1.6G sampling frequency shows the power dissipation of 26.2 mW and leads to higher SE, which is 9.6% higher than the conventional analog TX. The comparison with the state-of-the-arts millimeter-wave TXs and PAs is shown in Table II. The digital TXs, analog PAs, outphasing TXs, and analog TXs are compared. The proposed quadrature mixed-mode TX achieves both high P_{out} and SE at millimeter-wave frequency. In addition, it supports high-order QAM signals (i.e., 64QAM and 256QAM) with high data rates. Besides, the

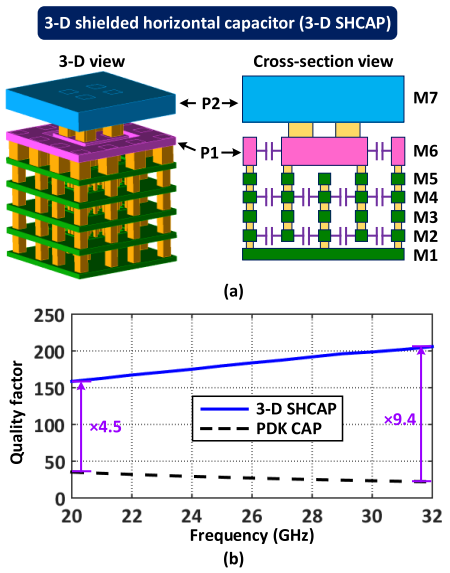

Fig. 31. (a) Configuration of the 3-D SHCAP. (b) Simulated quality factors of 3-D SHCAP and PDK capacitor with the same capacitance of 32 fF.

SE at 6-dB PBO is enhanced for higher average efficiency. With the competitive performances, the proposed quadrature mixed-mode TX is attractive for millimeter-wave wireless transmission.

V. Conclusion

In this article, a 2 × 9-bit millimeter-wave quadrature mixed-mode TX with distributed parasitic canceling and LO leakage self-suppression is proposed. It obtains enhanced peak/average efficiency and P_{out} using both digital modulator based on SCPA and Doherty analog PA. The distributed parasitic canceling sub-PA array is adopted to further decrease the passive loss and increase the efficiency. The LO leakage self-suppression decreases the LO leakage, which benefits to linearity and dynamic range. The proposed millimeter-wave mixed-mode TX fabricated in the 40-nm CMOS technology shows the merits of high output power, SE, and data rate, which are attractive for wireless applications.

Appendix

The 3-D view and cross-sectional view of the proposed 3-D SHCAP are shown in Fig. 31(a). Such 3-D SHCAP is mainly composed of two parts with stacked metals. Port P1 is tapped on the metal layer M6 of the outer stacked part. Port P2 is located on the top thick metal layer M7 of the inner stacked part. The stacked metal ring connected with P2 is nested with the stacked metal connected with P1. Therefore, the capacitance of the proposed 3-D SHCAP is mainly composed of the horizontal capacitive coupling between P1 and P2. Then, the vertical capacitive coupling through the high loss substrate is avoided, which results in enhanced Q [51]. The simulated quality factors of the conventional MOM PDK capacitor and proposed 3-D SHCAP with the same capacitance of 32 fF are compared in Fig. 31(b). The typical 32-fF 3-D SHCAP in this work shows the capacitance density of 0.7 fF/nm^2, while the capacitance density of a typical MOM PDK capacitor with identical capacitance is 1.2 fF/nm^2. Meanwhile, the proposed 3-D SHCAP avoids the vertical capacitive coupling through the lossy substrate introducing an extra passive loss, which leads to higher quality factor Q. The proposed 3-D SHCAP shows about 4.5–9.4 times Q of the conventional MOM PDK capacitor, as shown in Fig. 31(b).

References

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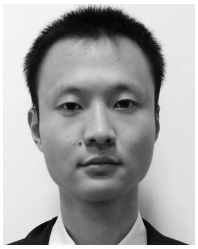

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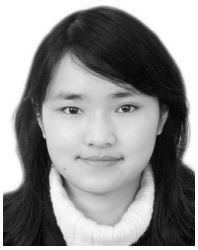

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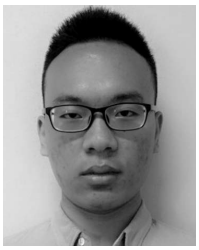

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