A CMOS Wideband Watt-Level 4096-QAM Digital Power Amplifier Using Reconfigurable Power-Combining Transformer

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***Abstract*— In this article, a wideband watt-level digital power amplifier (DPA) with high efficiency and large dynamic range is presented in CMOS technology for wireless applications. To achieve high output power with enhanced operation bandwidth (BW), the wideband matching network based on a reconfigurable power-combining transformer is used. Meanwhile, the *L–C* circuit is used to suppress the harmonics, which further improves the output power of the fundamental signal. In addition, the LO leakage is suppressed by the 12-bit power digital-to-analog converter (power DAC), which leads to high dynamic range of the proposed DPA. To verify the mechanism, a 1.2–3.6-GHz watt-level 12-bit polar DPA is implemented and fabricated using a conventional 40-nm CMOS technology. With 1.1-/2.5-V supply, the fabricated DPA exhibits peak output power (P_{out}) of 32.67 dBm, peak drain efficiency (DE) of 45.1%, and peak power-added efficiency (PAE) of 35.5% at 2 GHz. It supports 50-MSyms/s 256-QAM with average output power (P_{avg}) of 22.76 dBm, error vector magnitude (EVM) of −31.46 dB, and adjacent channel leakage ratio (ACLR) of −30.67 dBc, 10-MSyms/s 1024-QAM with P_{avg} of 25.54 dBm, EVM of −38.2 dB, and ACLR of −38.71 dBc, and 5-MSym/s 4096-QAM with P_{avg} of 22.97 dBm, EVM of −43.0 dB, and ACLR of −46.32 dBc, respectively.**

***Index Terms*— 4096-QAM, CMOS, digital power amplifier (DPA), dynamic range, harmonic suppression, reconfigurable transformer, tunable inductor, watt-level, wideband.**

I. Introduction

THE modern wireless communication systems often require watt-level power amplifier (PA) for higher signal-to-noise ratio and large communication coverage. Meanwhile, wideband PAs are developed to meet limits of multi-standards simultaneously. Besides, the increasing demands on high speed access require PAs with high linearity and large dynamic range to support high-order modulation signals, such as 1024-QAM and 4096-QAM. Moreover, mobile, wearable access, and mini-station demand a miniaturized and low-cost solution. In general, III–V or SiGe linear PAs are used to achieve watt-level output power and high linearity with the merit of high power density [1]–[4]. However, high supply voltage and high cost limit the applications of these PAs. To lower the cost, watt-level CMOS analog PAs were developed in the past decades. The cascode and stacked PAs are introduced to overcome the limitation from low breakdown voltage of CMOS transistors [5]–[11]. Such implementations allow the operation at higher supply voltage while keeping reliability. However, the operating points have to be carefully selected so that the devices operate optimally [12]. Moreover, these PAs still need high supply voltage and show relatively low efficiency. CMOS digital PAs (DPAs) are developed with significant merits of high efficiency and high integration level [13]–[25]. The polar architecture [26] and IQ cell sharing [27] are attractive for high-power applications. Besides, to achieve watt-level output power with limited supply voltage, the on-chip power-combining technique is developed. Recently, the watt-level CMOS DPAs are developed with competitive efficiency and relatively low supply voltage [28]–[35]. However, the matching networks of these DPAs are normally fixed, which limit the operation bandwidth (BW).

The reconfigurable matching network is introduced for extended operation BW and enhanced efficiency in PA design. The impedance of such a matching network can be adjusted to meet the design requirements of optimized load impedance (Z_{opt}) for PA implementation in a wide frequency range. The switched capacitor [36] and dynamic matching network [37] are proposed to improve the output power and efficiency for enhanced operation BW. The dynamic load trajectory manipulation with switch-controlled capacitors is reported in [38] to optimize the PA load impedance during power back-off. Besides, a programmable capacitor array is introduced in switched capacitor PA (SCPA) for frequency tuning [39]. The reconfigurable matching network and programmable network used in these works can effectively enhance the operation BW and improve PA efficiency. However, the saturated output power of these works is lower than 25 dBm. For higher power applications, the circuit reliability and extra loss of switches are key challenges to design reconfigurable matching network. Once the 2-W power is delivered into a 50-Ω load, a nearly 28.3-V peak-to-peak voltage swing is generated, which is much higher than the supply voltage of advanced-scaling CMOS transistor. It is not easy to implement high quality factor CMOS switch under such high voltage swing with

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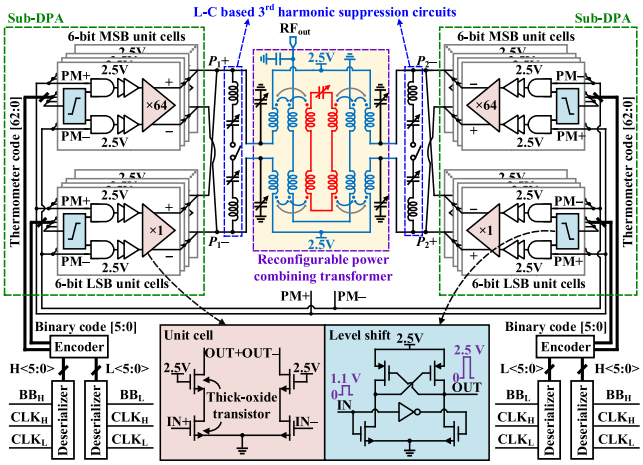

Fig. 1. Architecture of the proposed watt-level wideband DPA.

good reliability. Furthermore, large dynamic range and low LO leakage are demanded in DPA design to support high-order modulation signals [40]. Therefore, it is still challenging to achieve watt-level DPA with wideband operation, high efficiency, and low LO leakage using CMOS technology.

To address these challenges, this article presents a wideband watt-level 12-bit polar DPA with large dynamic range using a reconfigurable power-combining transformer [41]. First, the tunable inductor is proposed with enhanced reliability. The theory of tunable inductor is analyzed. Based on the tunable inductor, the reconfigurable power-combining transformer is proposed in the watt-level DPA to extend the operation BW with improved reliability. Meanwhile, the harmonics are suppressed by L–C circuits, which further improve the output power of the fundamental signal. In addition, the 12-bit power digital-to-analog (power DAC) with isolation enhancement is used to achieve high-resolution amplitude control and LO leakage suppression. Then, large dynamic range can be achieved to support high-order modulation, such as 1024-QAM and 4096-QAM.

This article is organized as follows. Section II introduces the architecture of the proposed wideband watt-level CMOS DPA. Section III discusses the matching network of the proposed DPA with a reconfigurable power-combining transformer, where the theory and implementation are clearly analyzed and explained. The implementation of sub-DPA with harmonic suppression is presented in Section IV. Section V shows the measurement results and comparisons with state-of-the-arts. Finally, the conclusion is given in Section VI.

II. Architecture of Watt-Level DPA

The architecture of the proposed wideband watt-level DPA is shown in Fig. 1. Such DPA consists of the output matching network with a reconfigurable power-combining transformer, harmonic suppression circuit, and two identical differential sub-DPAs. The Class-E switching PA is chosen for the unit cell of sub-DPA. Two differential sub-DPAs are power-combined to improve the output power, while a reconfigurable power-combining transformer is used to extend the operation BW. Each differential sub-DPA is constituted of the 6-bit MSB unit cells controlled by thermometer code and 6-bit

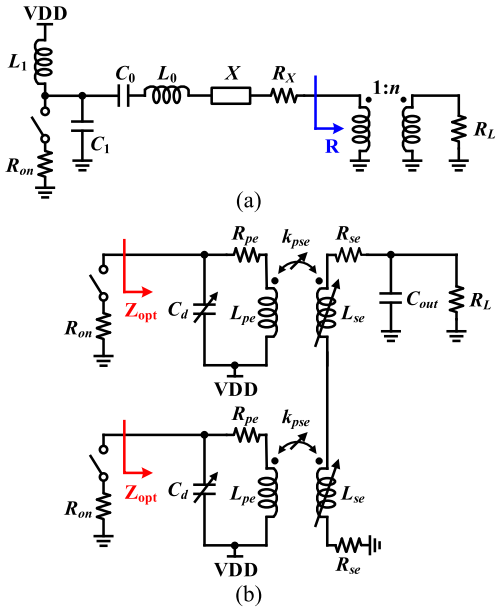

Fig. 2. (a) Model of the single-ended Class-E PA with finite dc-feed inductance L_1 and switch ON-resistance R_{ON}. (b) Model of the single-ended Class-E PA with a reconfigurable power-combining matching network.

LSB unit cells controlled by the binary code. The 12-bit unit cells lead to a high-resolution amplitude control for high-order modulation. To obtain higher output voltage swing, the 2.5-V thick-oxide transistors are used to implement both the MSB and LSB unit cells. The LO leakage is also suppressed by the 2.5-V thick-oxide transistors. Therefore, a large dynamic range can be achieved. Meanwhile, considering the reliability, the cascode topology is introduced in unit cell design. The L–C based circuits are introduced to suppress the harmonics, which could further improve the output power of the fundamental signal. The 2.5-V digital AND gates with buffers combine the phase-modulated (PM) signal and thermometer/binary codes, which drive the MSB and LSB unit cells. Two parallel 1:6 deserializers are introduced in each sub-DPA to convert the serial input baseband signals BB_H and BB_L into parallel signals $H<5:0>$ and $L<5:0>$, respectively. Two sampling clocks CLK_H and CLK_L ($\mathrm{CLK}_H = 6\mathrm{CLK}_L$) are required in each deserializer. The encoders transform the $H<5:0>$ and $L<5:0>$ signals to thermometer and binary control codes. The level shift circuits convert 1.1-V rail-to-rail output signals of encoders into 2.5-V signals, which drive the digital AND gates. Note that the baseband signals and sampling clocks are shared for each sub-DPA.

III. Reconfigurable Power-Combining Matching Network

To discuss the matching network design of watt-level DPA, the model of the single-ended Class-E PA with finite dc-feed inductance L_1 and switch ON-resistance R_{ON} is shown in Fig. 2(a). R_X is the parasitic resistor. Considering the ideal impedance transform network with a turn ratio of 1:n, the output power on the effective load R can be calculated by

$$P_{\text{out}} = \frac{\text{VDD}^2\, p(q,m)^2}{2K_{L_1}(q,m)^2} \times \frac{1}{\frac{R_X^2}{R} + R + 2R_X}. \tag{1}$$

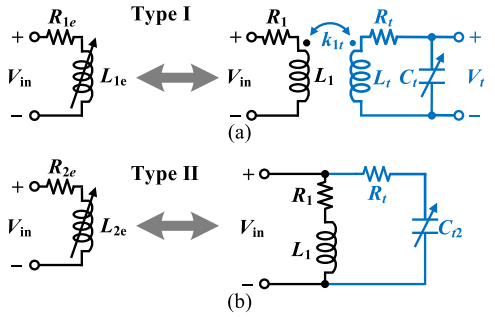

Fig. 3. Equivalent circuit and schematic of (a) proposed tunable inductor and (b) conventional directly connected tuning network using tunable capacitor.

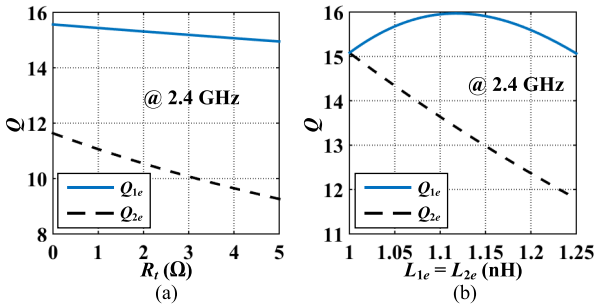

Fig. 4. (a) Calculated Q_{1e} and Q_{2e} when only R_t is changed ($L_1 = 1$ nH, $R_1 = 1\ \Omega$, $L_t = 500$ pH, $k_{1t} = 0.5$, and $C_t = C_{t2} = 1$ pF). (b) Calculated Q_{1e} and Q_{2e} when $L_{1e} = L_{2e}$ ($L_1 = 1$ nH, $R_1 = 1\ \Omega$, $L_t = 500$ pH, $k_{1t} = 0.5$, and $R_t = 0.5\ \Omega$).

The drain efficiency (DE) can be evaluated by

$$\eta = \frac{R}{R_X + R}\left(1 - \frac{\int_0^{\frac{\pi}{\omega}} \left(V_{\mathrm{Con}}(t)^2\right) dt}{\mathrm{VDD}\int_0^{\frac{\pi}{\omega}} V_{\mathrm{Con}}(t) dt}\right). \tag{2}$$

where $V_{C_{\mathrm{ON}}}$ is the transient voltage across capacitor C_1 in the time interval $0 \le t \le \omega/\pi$. The design parameters (i.e., K_{L_1} and p) of the model can be expressed by the free design variables $q = 1/(\omega\sqrt{L_1 C_1})$ and $m = \omega R_{\mathrm{ON}} C_1$ [42]. The parasitic resistance R_X should be much smaller than $R = R_L/n^2$ for higher DE. With limited supply voltage VDD in the conventional CMOS technology, a smaller impedance $R = R_L/n^2$ should be adopted to achieve watt-level output power. Therefore, the transformation network with larger turn ratio n is needed to convert the smaller impedance R into R_L. However, the loss of the transformation network usually increases with larger turn ratio n, which would further decrease the PA efficiency. Besides, to obtain wideband operation, the matching network should be finely designed to meet the design requirement of R in a wide frequency range.

In this work, the matching network with a reconfigurable power-combining transformer is introduced, as shown in Fig. 2(b). The tunable inductor with enhanced reliability under high voltage swing and high quality factor is introduced in reconfigurable transformer design. The matching network with reconfigurable transformer can be reconfigured to meet the design requirement of Z_{opt} in a wide frequency range. Moreover, the voltage-mode power-combining technique, which needs lower impedance turn ratio compared with the current-mode combining technique [43], [44], is used to further improve the output power of the proposed DPA.

A. Reconfigurable Transformer

The equivalent circuit of the tunable inductor is shown in Fig. 3(a) (i.e., Type I). R_1 is the parasitic resistor of the inductor L_1. The extra inductor L_t connected to the tunable capacitor C_t is coupled to L_1 with a coupling factor of k_{1t}. R_t is the parasitic resistance of the tuning network. L_{1e} and Q_{1e} are the equivalent inductance and qualify factor of the tunable inductor, respectively. The conventional directly connected tuning network using tunable capacitor C_{t2} is shown in Fig. 3(b) (i.e., Type II). The tunable capacitor C_{t2} with the parasitic resistor R_t is connected to the inductor L_1. L_{2e} and Q_{2e} are the equivalent inductance and qualify factor of Type II, respectively. L_{1e}, L_{2e}, Q_{1e}, and Q_{2e} can be calculated and compared. The corresponding equations and derivations in detail are shown in Appendix A. The calculated Q_{1e} and Q_{2e} across R_t are shown in Fig. 4(a). The proposed tunable inductor (i.e., Type I) shows higher Q compared with Type II. Meanwhile, when R_t increases, the quality factor degradation of Type I is less than Type II. In addition, the tunable capacitors C_t and C_{t2} are finely adjusted to tune L_{1e} and L_{2e}, respectively. The calculated Q_{1e} and Q_{2e} under the case of $L_{1e} = L_{2e}$ are shown in Fig. 4(b). The directly tuning network introduces a critical effect on Q_{2e}. Meanwhile, the proposed tunable inductor shows a little Q degradation when L_{1e} is tuned. Therefore, compared with the conventional tuning network using directly connected tunable capacitor, the proposed tunable inductor indirectly affects the winding through EM coupling, which introduces less loss.

Based on the tunable inductor, the equivalent circuit and schematic of two-port reconfigurable transformer are shown in Fig. 5(a). L_p is the primary inductor of the transformer with the parasitic resistor R_p. The secondary inductor L_s with the parasitic resistor R_s is coupled to L_p with coupling factor k_{ps}. The extra inductor L_t with the parasitic resistor R_t is coupled to L_s with coupling coefficient k_{st}. By tuning the capacitor C_t, which is connected with L_t, the equivalent secondary inductance L'_{se} can be adjusted. Note that the undesired weak coupling k_{pt} between L_p and L_t is hard to be eliminated in practical implementation. Thus, k_{pt} is considered in principle analysis, which would slightly affect the equivalent primary inductance L'_{pe} and equivalent resistance R'_{pe}. R'_{se} is the equivalent resistance of L'_{se}. k'_{pse} represents the equivalent coupling coefficient of the transformer.

$$[Z_{TA}] = \begin{bmatrix} R_p + j\omega L_p + \dfrac{\omega^2 k_{pt}^2 L_p L_t}{R_t + j\omega L_t - j/(\omega C_t)} & j\omega k_{ps}\sqrt{L_p L_s} + \dfrac{\omega^2 k_{st} k_{pt} L_t \sqrt{L_p L_s}}{R_t + j\omega L_t - j/(\omega C_t)} \\ j\omega k_{ps}\sqrt{L_p L_s} + \dfrac{\omega^2 k_{st} k_{pt} L_t \sqrt{L_p L_s}}{R_t + j\omega L_t - j/(\omega C_t)} & R_s + j\omega L_s + \dfrac{\omega^2 k_{st}^2 L_s L_t}{R_t + j\omega L_t - j/(\omega C_t)} \end{bmatrix} \tag{3}$$

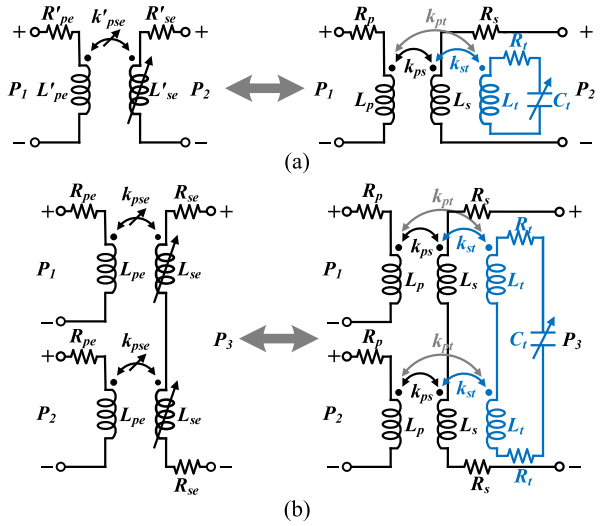

Fig. 5. Equivalent circuit and schematic of (a) two-port reconfigurable transformer and (b) reconfigurable voltage-mode power-combining transformer.

The impedance matrix $[Z_{TA}]$ of such a two-port transformer can be expressed by (3), shown at the bottom of the previous page. The derivation procedures in detail are shown in Appendix B. L'_{pe}, L'_{se}, R'_{pe}, R'_{se}, quality factors, and k'_{pse} can be evaluated by the following equations:

$$L'_{pe} = \frac{\text{imag}([Z_{TA}]_{11})}{\omega} = L_p + \frac{\omega k_{pt}^2 L_p L_t [1/(\omega C_t) - \omega L_t]}{R_t^2 + [\omega L_t - 1/(\omega C_t)]^2} \tag{4}$$

$$L'_{se} = \frac{\text{imag}([Z_{TA}]_{22})}{\omega} = L_s + \frac{\omega k_{st}^2 L_s L_t [1/(\omega C_t) - \omega L_t]}{R_t^2 + [\omega L_t - 1/(\omega C_t)]^2} \tag{5}$$

$$R'_{pe} = \text{real}([Z_{TA}]_{11}) = R_p + \frac{\omega^2 k_{pt}^2 L_p L_t R_t}{R_t^2 + [\omega L_t - 1/(\omega C_t)]^2} \tag{6}$$

$$R'_{se} = \text{real}([Z_{TA}]_{22}) = R_s + \frac{\omega^2 k_{st}^2 L_s L_t R_t}{R_t^2 + [\omega L_t - 1/(\omega C_t)]^2} \tag{7}$$

$$Q'_{pe,se} = \frac{\omega L'_{pe,se}}{R'_{pe,se}} \tag{8}$$

$$k'_{pse} = \frac{\text{imag}([Z_{TA}]_{21})/\omega}{\sqrt{L'_{se} \times L'_{pe}}}. \tag{9}$$

To achieve higher output power, the power-combining technique using transformer is usually used in integrated circuit design. The voltage-mode power-combining transformer, which requires lower impedance turn ratio compared with the current-mode power-combining transformer [43], [44], is adopted in this work. The reconfigurable voltage-mode power-combining transformer is proposed as shown in Fig. 5(b). The corresponding impedance matrix $[Z_{TB}]$ of such a three-port network can be derived and expressed by (10), shown at the bottom of the page. The weak coupling between primary inductors is ignored. The equivalent inductances L_{se}, L_{pe}, equivalent resistances R_{se}, R_{pe}, equivalent quality factors Q_{pe}, Q_{se}, and equivalent coupling coefficient k_{pse} can be calculated by the following equations:

$$L_{pe} = \frac{\text{imag}([Z_{TB}]_{11})}{\omega} = L_p + \frac{\omega k_{pt}^2 L_p L_t [1/(\omega C_t) - 2\omega L_t]}{4R_t^2 + [2\omega L_t - 1/(\omega C_t)]^2} \tag{11}$$

$$L_{se} = \frac{\text{imag}([Z_{TB}]_{33})}{2\omega} = L_s + \frac{2\omega k_{st}^2 L_s L_t [1/(\omega C_t) - 2\omega L_t]}{4R_t^2 + [2\omega L_t - 1/(\omega C_t)]^2} \tag{12}$$

$$R_{pe} = \text{real}([Z_{TB}]_{11}) = R_p + \frac{2\omega^2 k_{pt}^2 L_p L_t R_t}{4R_t^2 + [2\omega L_t - 1/(\omega C_t)]^2} \tag{13}$$

$$R_{se} = \frac{\text{real}([Z_{TB}]_{33})}{2} = R_s + \frac{4\omega^2 k_{st}^2 L_s L_t R_t}{4R_t^2 + [2\omega L_t - 1/(\omega C_t)]^2} \tag{14}$$

$$Q_{pe,se} = \frac{\omega L_{pe,se}}{R_{pe,se}} \tag{15}$$

$$k_{pse} = \frac{\text{imag}([Z_{TB}]_{31})/\omega}{\sqrt{L_{se} \times L_{pe}}}. \tag{16}$$

It can be seen that the equivalent secondary inductance L_{se} is affected by C_t, L_t, k_{pt}, and R_t. By tuning C_t, L_{se} can be controlled to tune the input impedance of the network. Therefore, it is possible to design the reconfigurable matching network for enhanced BW based on the proposed reconfigurable power-combining transformer. Following the aforementioned theories and equations, we can easily design tunable inductor and reconfigurable transformer for different requirements.

B. Implementation of Matching Network With Reconfigurable Power-Combining Transformer

As shown in Fig. 6, the proposed reconfigurable matching network is implemented by a reconfigurable power-combining transformer, four switched capacitors C_d at inputs, and fixed capacitor C_o at output. Considering the reliability problem of CMOS switch under high voltage swing after power-combining, the output capacitor C_o is set to be fixed. The switched capacitor banks C_t and C_d are used for the reconfigurable matching network. C_d is composed of a switched capacitor C_{d2} of 3.5 pF and a fixed capacitor C_{d1} of 2.7 pF. The capacitance of C_d is 6.2 pF with Q of 31.5 when C_{d2}

$$[Z_{TB}] = \begin{bmatrix} R_p + j\omega L_p + \dfrac{\omega^2 k_{pt}^2 L_p L_t}{2R_t + j2\omega L_t - j/(\omega C_t)} & 0 & j\omega k_{ps}\sqrt{L_p L_s} + \dfrac{2\omega^2 k_{st} k_{pt} L_t \sqrt{L_p L_s}}{2R_t + j2\omega L_t - j/(\omega C_t)} \\ 0 & R_p + j\omega L_p + \dfrac{\omega^2 k_{pt}^2 L_p L_t}{2R_t + j2\omega L_t - j/(\omega C_t)} & j\omega k_{ps}\sqrt{L_p L_s} + \dfrac{2\omega^2 k_{st} k_{pt} L_t \sqrt{L_p L_s}}{2R_t + j2\omega L_t - j/(\omega C_t)} \\ j\omega k_{ps}\sqrt{L_p L_s} + \dfrac{2\omega^2 k_{st} k_{pt} L_t \sqrt{L_p L_s}}{2R_t + j2\omega L_t - j/(\omega C_t)} & j\omega k_{ps}\sqrt{L_p L_s} + \dfrac{2\omega^2 k_{st} k_{pt} L_t \sqrt{L_p L_s}}{2R_t + j2\omega L_t - j/(\omega C_t)} & 2R_s + j2\omega L_s + \dfrac{4\omega^2 k_{st}^2 L_s L_t}{2R_t + j2\omega L_t - j/(\omega C_t)} \end{bmatrix} \tag{10}$$

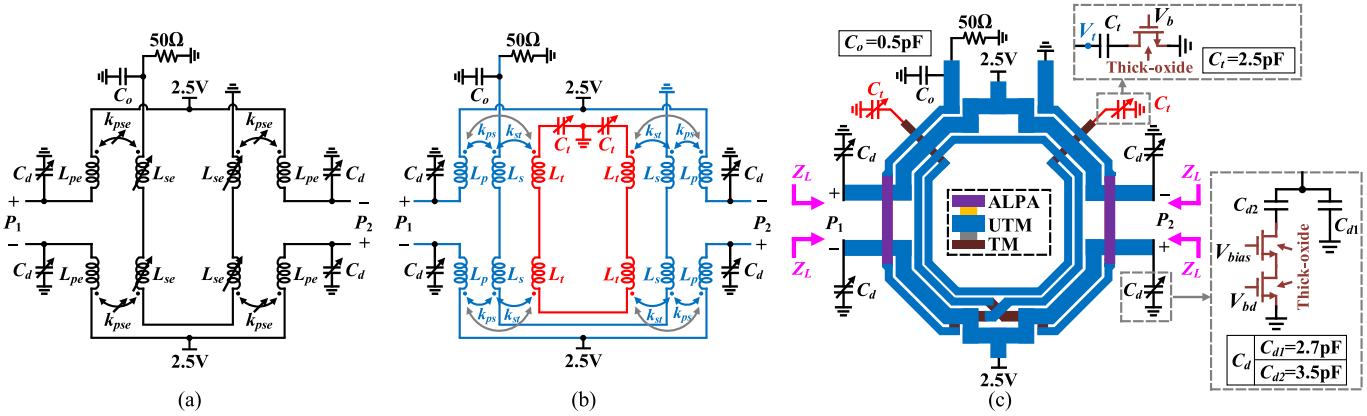

Fig. 6. (a) Equivalent circuit, (b) schematic, and (c) configuration of the proposed matching network with a reconfigurable power-combining transformer.

switched-ON at 2 GHz, while C_d is 3.4 pF with Q of 139 when C_{d2} switched-OFF at 2 GHz. The switched-ON C_t is 2.5 pF with Q of 40.1, while the switched-OFF C_t is 0.6 pF with Q of 31.7 at 2 GHz. The top three thick metal layers (i.e., ALPA, UTM, and TM) are used to implement the power-combining transformer for higher quality factors and enough current capability.

L_p and L_s are the primary and secondary inductors of the transformer, respectively. L_t connected with C_t is coupled to L_s with coupling coefficient of k_{st}. The equivalent secondary inductance L_{se} can be adjusted by tuning C_t. However, due to the undesired weak coupling k_{pt}, L_{pe} would be slightly affected when C_t is tuning. The calculated and EM-simulated L_{se}, Q_{se}, L_{pe}, Q_{pe}, and k_{pse} at 2.4 GHz are compared in Fig. 7. The calculated results are based on (11)–(16). The parameters (L_p, Q_p, L_s, Q_s, k_{ps}, L_t, Q_t, k_{st}, and k_{pt}) are extracted from the EM-simulated results. To avoid the undesired influences introduced by parasitics of practical capacitors and switches, the ideal model of tunable capacitors is used in the calculation and simulation. The calculated and EM-simulated results show good agreement. The equivalent secondary inductance L_{se} is adjusted in a relatively large range when C_t is tuning. Meanwhile, L_{pe} and k_{pse} are slightly affected by C_t. In addition, the proposed transformer shows little degradation of Q_{pe} and Q_{se} when C_t is increased.

The impedance Z_L of the matching network could be controlled by tuning C_t or C_d. Z_L is simulated at different frequencies, as shown in Fig. 8. When the capacitor C_d is tuned and C_t is switched OFF, the simulated tuning ranges of Z_L at different frequencies are expressed by the red curves. Z_L is only obtained in a small range, which could not meet the design requirement of Z_{opt} in wideband. Meanwhile, by adjusting both C_t and C_d, the tuning range of impedance Z_L (the blue region) could be further extended, which finely meets the optimum load impedance Z_{opt} in a wide frequency range. Therefore, the proposed reconfigurable matching network can enhance the operation BW of the proposed DPA.

Two optimized operation modes (i.e., Modes I and II) are used to optimize the impedance matching at different frequencies for enhanced BW. To evaluate the passive efficiency of the proposed matching network under two operation modes,

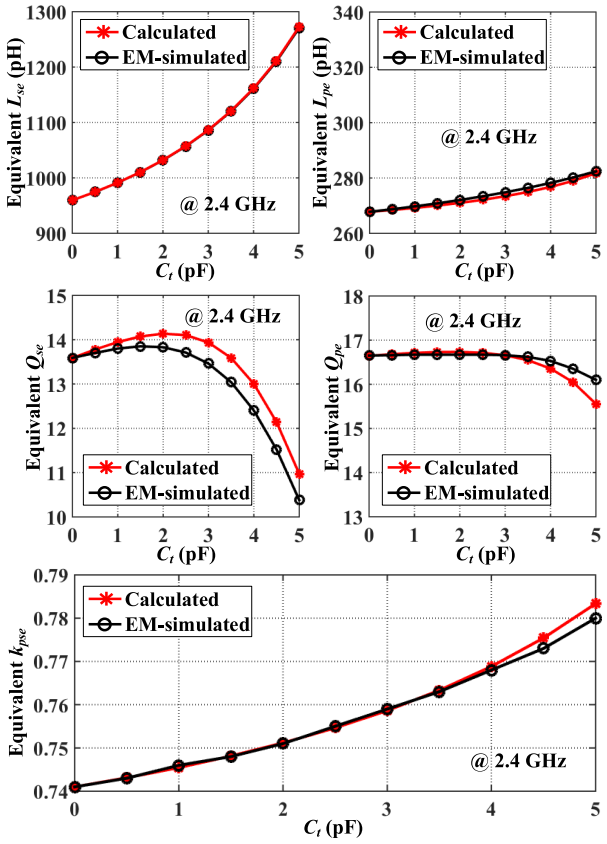

Fig. 7. Calculated and EM-simulated equivalent L_{se}, L_{pe}, Q_{se}, Q_{pe}, and k_{pse} at 2.4 GHz based on (11)–(16) (L_p = 267 pH, Q_p = 16.59, L_s = 960 pH, Q_s = 13.59, k_{ps} = 0.741, L_t = 245 pH, Q_t = 8.69, k_{st} = 0.513, and k_{pt} = 0.29 at 2.4 GHz).

the single-ended equivalent circuit of the matching network based on the reconfigurable power-combining transformer is shown in Fig. 9. The voltages and currents applied to the ports of the transformer can be presented by the following equation based on the impedance matrix $[Z_{TB}]$:

$$\begin{cases} V_1 = [Z_{TB}]_{11} \times I_1 + [Z_{TB}]_{12} \times I_2 - [Z_{TB}]_{13} \times I_3' \\ V_2 = [Z_{TB}]_{21} \times I_1 + [Z_{TB}]_{22} \times I_2 - [Z_{TB}]_{23} \times I_3' \\ V_3 = [Z_{TB}]_{31} \times I_1 + [Z_{TB}]_{32} \times I_2 - [Z_{TB}]_{33} \times I_3' \end{cases} \quad (17)$$

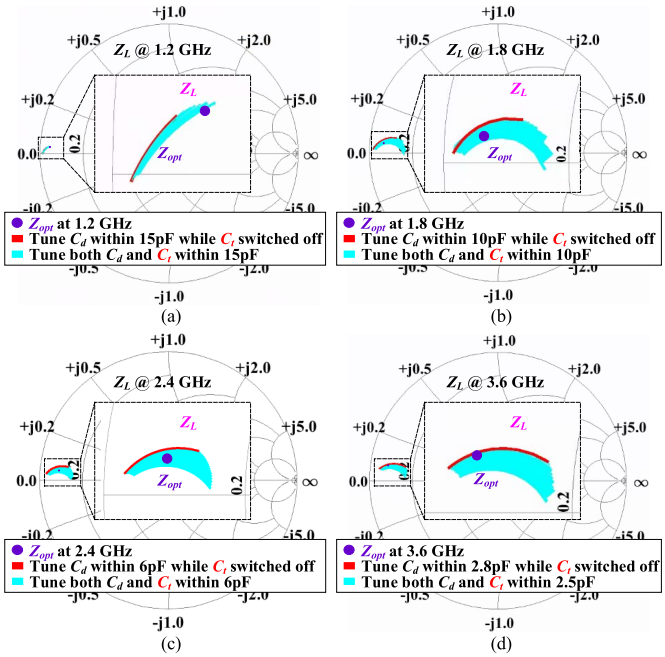

Fig. 8. Simulated tuning range of impedance Z_L at (a) 1.2, (b) 1.8, (c) 2.4, and (d) 3.6 GHz.

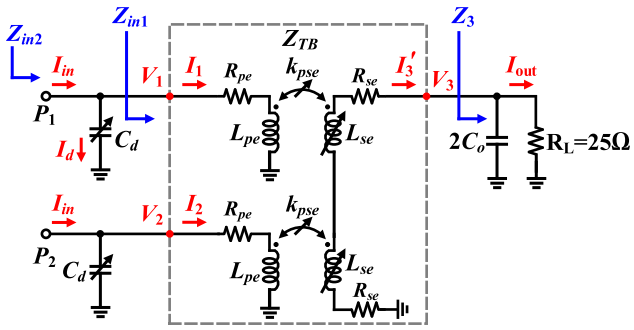

Fig. 9. Single-ended equivalent circuit of the proposed matching network with a reconfigurable power-combining transformer.

where $I_3' = -I_3$. For simple analysis, $I_1 = I_2$ and $V_1 = V_2$ are assumed. I_1 can be derived as

$$I_1 = \frac{\frac{R_L \frac{1}{2j\omega C_o}}{R_L + \frac{1}{2j\omega C_o}} + [Z_{TB}]_{33}}{2[Z_{TB}]_{31}} I_3'. \tag{18}$$

The input power of port 1 can be evaluated. First, the input impedance Z_{in1} can be expressed by the following equation based on (17) and (18):

$$\begin{aligned} Z_{in1} &= \frac{V_1}{I_1} \\ &= [Z_{TB}]_{11} - [Z_{TB}]_{13} \frac{I_3'}{I_1} \\ &= [Z_{TB}]_{11} - [Z_{TB}]_{13} \frac{2[Z_{TB}]_{31}}{\frac{R_L \frac{1}{2j\omega C_o}}{R_L + \frac{1}{2j\omega C_o}} + [Z_{TB}]_{33}}. \end{aligned} \tag{19}$$

The input current I_{in} can be derived as

$$\begin{aligned} I_{in} &= I_1 + I_d \\ &= I_1 + \frac{I_1 Z_{in1}}{\frac{1}{j\omega C_d}} \\ &= I_1 (1 + Z_{in1} \times j\omega C_d) \\ &= (1 + Z_{in1} \times j\omega C_d) \frac{\frac{R_L \frac{1}{2j\omega C_o}}{R_L + \frac{1}{2j\omega C_o}} + [Z_{TB}]_{33}}{2[Z_{TB}]_{31}} I_3'. \end{aligned} \tag{20}$$

The input power of port 1 can be calculated using the following equation:

$$P_{in} = \text{real}(I_{in} \times I_{in}^* \times Z_{in2}) \tag{21}$$

where

$$Z_{in2} = \frac{Z_{in1} \frac{1}{j\omega C_d}}{Z_{in1} + \frac{1}{j\omega C_d}}. \tag{22}$$

The output power delivered to the load R_L should be calculated. Considering the output capacitor $2C_o$, the output current I_{out} of the load R_L can be expressed by

$$I_{\text{out}} = \frac{1}{2j\omega C_o (R_L + \frac{1}{2j\omega Co})} I_3'. \tag{23}$$

The output power delivered to the load R_L can be evaluated using the following equation:

$$P_{\text{out}} = \text{real}(I_{\text{out}} \times I_{\text{out}}^* \times R_L). \tag{24}$$

The input power of port 2 is identical to port 1. Therefore, the passive efficiency of the proposed matching network can be calculated by

$$\text{eff.} = \frac{P_{\text{out}}}{P_{in} + P_{in}} \times 100\%. \tag{25}$$

To obtain more accurate calculation result of passive efficiency in a wide frequency range, the frequency-dependent parameters of the reconfigurable power-combining transformer (i.e., L_p, L_s, L_t, Q_p, Q_s, Q_t, k_{ps}, k_{pt}, and k_{st}) are considered in calculation. The simulation results of these frequency-dependent parameters versus frequency are shown in Fig. 10. It can be seen that L_p and L_s show good quality factors in a wide frequency range, which benefits the passive efficiency. The calculated and simulated passive efficiencies of the proposed matching network under two operation modes (i.e., Modes I and II) are compared in Fig. 11, which show good agreement. It can be seen that the passive efficiency of the proposed network is larger than 67% in the operation BW. The calculation results shown in Fig. 11 assume that all the input impedances of the power combiner are identical. However, due to the asymmetric layout of the voltage-type combiner when using a single-ended output, the imbalances of this type of combiner exist. Such imbalances lead to unequal impedances at each input port of the power-combining transformer [45]. Therefore, the mismatch between the simulation and calculation is mainly caused by the imbalance of the layout for the proposed transformer.

To enhance the reliability of switch, the circuits of cascode thick-oxide MOSFETs are used to implement the switched capacitor C_d. As discussed in Appendix A, to improve the reliability of C_t after power-combining, the ratio of L_t/L_s should be low, which limits the voltage swing across C_t, as shown in Fig. 6(c). When the proposed DPA delivers a saturated output power at 2 GHz in operation Mode I with

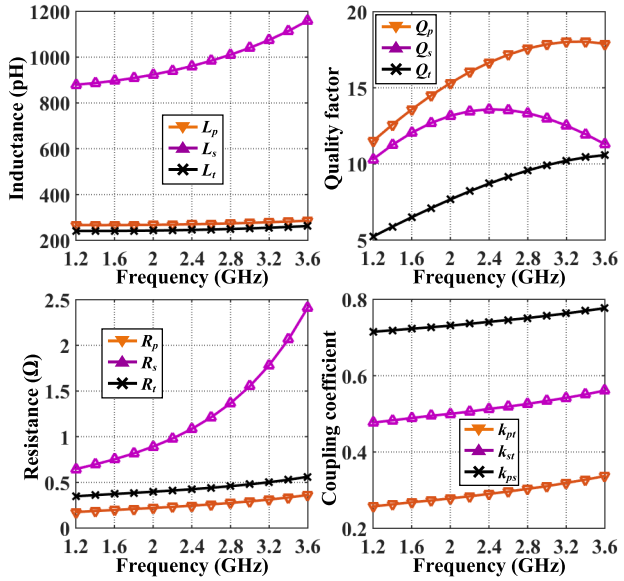

Fig. 10. Simulated inductances, quality factors, parasitic resistance, and coupling coefficients of the proposed power-combining transformer versus frequency.

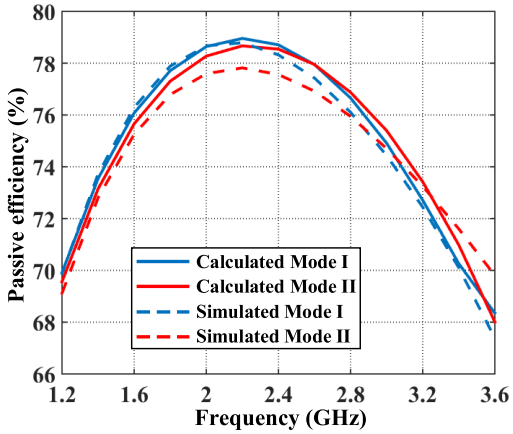

Fig. 11. Calculated and simulated passive efficiencies of operation Mode I (C_d = 6.2 pF, C_t = 2.5 pF, and C_o = 0.5 pF) and Mode II (C_d = 2.7 pF, C_t OFF, and C_o = 0.5 pF).

C_d = 6.2 pF and C_t = 2.5 pF, the simulated voltage V_t across C_t and the output voltage V_{out} of the proposed DPA are depicted in Fig. 12. V_t shows peak-to-peak voltage swing of about 5 V, which is much lower comparing to DPA output V_{out}. Thus, the single 2.5-V thick-oxide transistor is used to implement the switched capacitor C_t with good reliability.

IV. Power DAC With LO Leakage and Harmonic Suppression

The configuration of the 12-bit power-DAC with the 6-bit MSB and 6-bit LSB unit cells is shown in Fig. 13. The dimensions of each transistor for the 6-bit MSB are set to 72.5 μm/270 nm. The sizes of the cascode devices for the 6-bit LSB are 36.25, 18.13, 9.065, 4.54, 2.27, and 1.135 μm/270 nm, respectively. The outputs of sub-DPAs are connected to the reconfigurable matching network. The

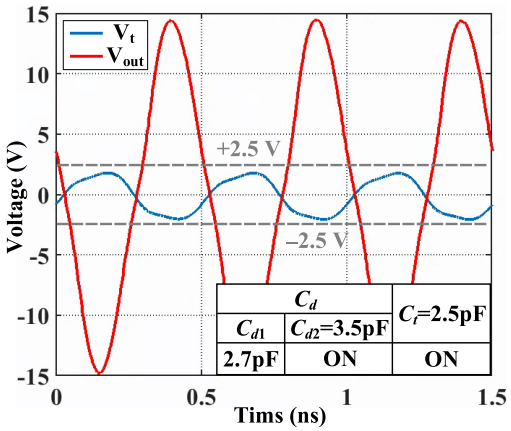

Fig. 12. Simulated voltage V_t across C_t and output voltage V_{out} of the proposed DPA under saturated output power at 2 GHz.

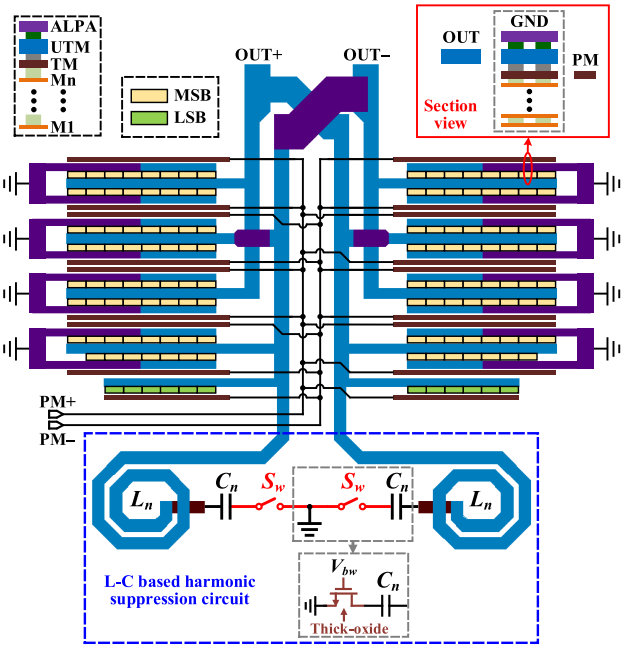

Fig. 13. Configuration of the proposed 12-bit power-DAC with harmonic suppression circuit.

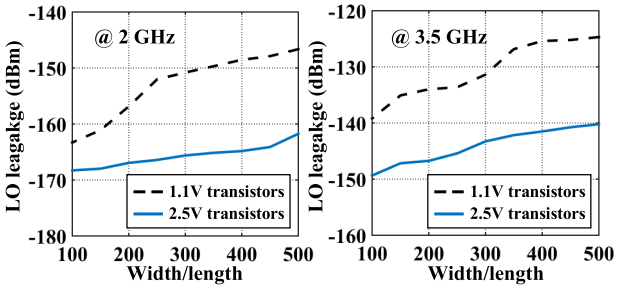

Fig. 14. Simulated LO leakage of the 6-bit MSB unit cells implemented using 1.1-V transistors and 2.5-V thick-oxide transistors versus the ratio of width/length.

simulated LO leakage of the 6-bit MSB unit cells implemented using 1.1-V transistors and 2.5-V thick-oxide transistors is compared in Fig. 14. The lengths of 1.1-V transistors and

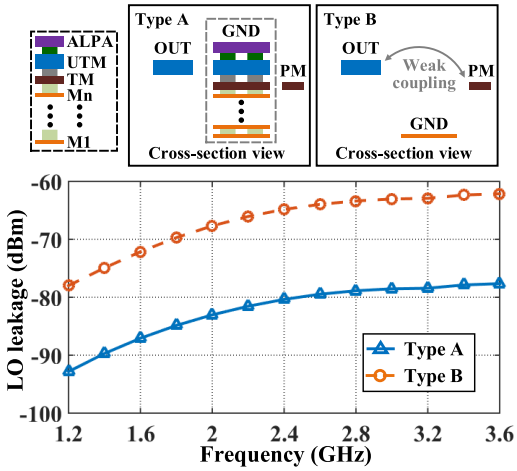

Fig. 15. Cross section view and simulated LO leakage of Types A and B.

2.5-V thick-oxide transistors are set to be minimized value of 40 and 270 nm, respectively. With identical ratio of width/length, the power DAC based on 2.5-V thick-oxide transistors features lower LO leakage. In addition, the thick-oxide transistors with 2.5-V supply shows higher output power. Therefore, the thick-oxide transistors are used to implement the 12-bit power-DAC for watt-level output power and relatively low LO leakage in this work. In addition, considering the reliability, the cascode structure is introduced in unit cell design, which handles higher voltage stress.

Meanwhile, the EM coupling introduced by routings of power DAC further deteriorates the LO leakage. The cross section views of two types of sub-PA routings are depicted in Fig. 15. Type A and Type B are the proposed and conventional routing schemes, respectively. The weak coupling between PM input routing and output routing of the sub-PA further deteriorates LO leakage. The GND implemented using stacked metal layer is introduced in this work (i.e., Type A), which improves the isolation between input–output and further decreases the LO leakage. The simulated LO leakage of Types A and B is compared in Fig. 15. Type A introduces more than 15-dB LO leakage suppression improvement compared with Type B.

The L–C circuit is introduced in each sub-DPA as shown in Fig. 13, which could generate a transmission zero at about 4 GHz to suppress the third harmonic of the fundamental signal at lower frequency. The inductor L_n, which is implemented using top thick metal layers, is 458 pH with a quality factor of 15.5. The L–C-based harmonic suppression circuit is controlled by the switch S_W. The single thick-oxide transistor is used to design the switch S_W. The simulated peak-to-peak voltage swing across the switch S_W is only about 1.4 V at 2 GHz. As illustrated in Fig. 16, when the proposed DPA operates at lower frequencies, S_W is switched ON. The third harmonics of the fundamental signals are suppressed. Meanwhile, the impedance matching is further optimized by the harmonic suppression circuit, which contributes to the improved output power of the fundamental signals. The simulated transient drain voltage of the cascode unit cell with and without harmonic suppression at 2 GHz is shown in Fig. 17.

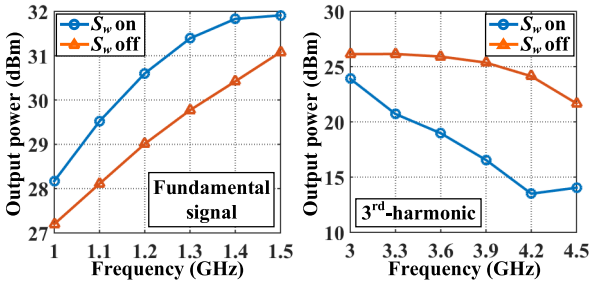

Fig. 16. Simulated effect of harmonic suppression circuit.

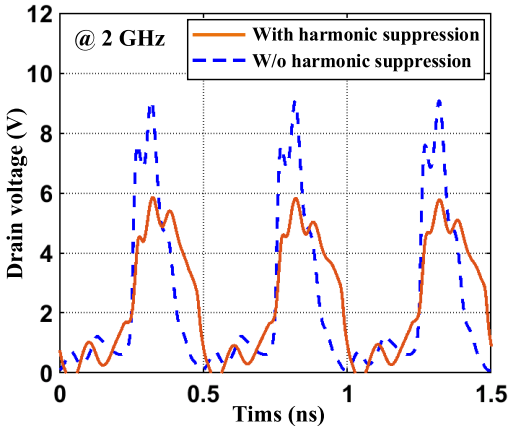

Fig. 17. Simulated transient drain voltage of cascode unit cell with and without harmonic suppression at 2 GHz.

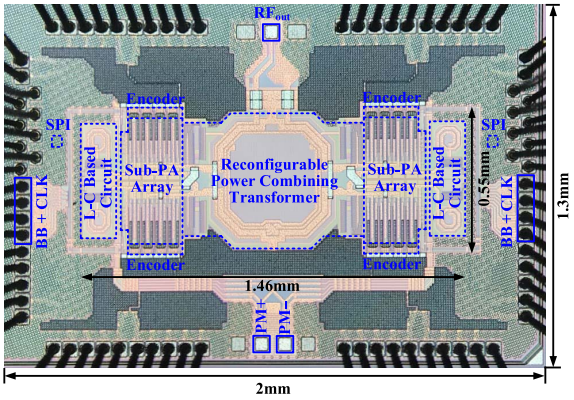

Fig. 18. Chip microphotograph.

V. Fabrication and Measurement

The proposed watt-level DPA is fabricated using a conventional 40-nm CMOS technology occupying 2 mm × 1.3 mm including all I/O pads. The core circuit is only 1.46 mm × 0.55 mm. The microphotograph of the fabricated DPA is shown in Fig. 18. The supply voltage is 1.1/2.5 V. The measurement setup is shown in Fig. 19. The chip is wirebonded on a PCB for measurement. For modulation measurement, the vector signal generator generates the PM signal. The wideband balun converts the signal of the vector signal generator into differential, which feeds the proposed DPA through GSSG probe. The baseband signals (i.e., BB_H and BB_L) and sampling clocks (i.e., CLK_H and CLK_L with $\mathrm{CLK}_H = 6\mathrm{CLK}_L$)

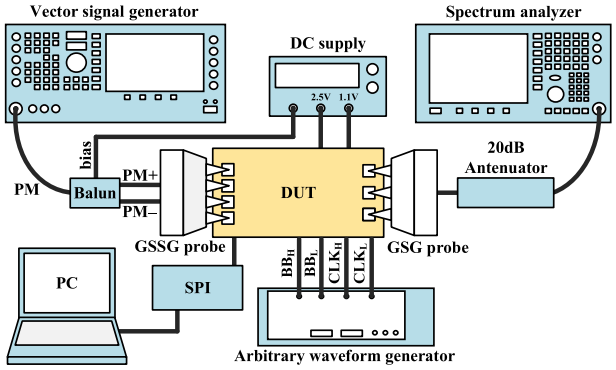

Fig. 19. Measurement setup.

are generated by the arbitrary waveform generator (AWG). Besides, the output signal of the proposed DPA is attenuated by a 20-dB attenuator and measured by the spectrum analyzer.

The measured saturated output power P_{sat}, DE, and power-added efficiency (PAE) versus frequency are depicted in Fig. 20(a). The proposed DPA features a peak P_{sat} of 32.67 dBm with 45.1% DE and peak PAE of 35.5% at 2 GHz. The power dissipation of core circuits, driving circuits, digital circuits, and all the logic blocks is considered in PAE calculation. Two optimized operation modes (i.e., Modes I and II) are adopted to optimize the output impedance of the DPA at different frequencies, which leads to BW enhancement. The 1-dB BW of operation Mode I is about 1.45–2.4 GHz. Meanwhile, the 1-dB BW of operation Mode II is about 1.7–2.85 GHz, which effectively extends the operation BW of the proposed DPA. The 3-dB BW of the proposed DPA is 1.2–3.6 GHz, i.e., 100% FBW. Besides, the proposed DPA exhibits the LO leakage of −82.97 dBm and dynamic range of 115.64 dB at 2 GHz, as shown in Fig. 20(b). The dynamic range is defined as the difference between the maximal and minimal output power of DPA [40].

The measured typical AM–AM and AM–PM distortions of the proposed DPA at 2.4 and 3.5 GHz are shown in Fig. 20(c). The AM–PM distortion is mainly caused by the varying output impedance of transistors versus code. Two 1-D digital predistortions (DPDs) with lookup table are required to enhance both the amplitude and phase linearity of the DPA. The AM–AM distortion is minimized by the DPD with AWG. Meanwhile, the AM–PM distortion of the DPA is improved by the DPD with a vector signal generator. As illustrated in Fig. 21, the constellation and spectrum of the 256-QAM signals are measured at different frequencies. Note that limited by the 200-MHz sampling rate of the vector signal generator, the maximal symbol rate is 50 MSym/s with 4 upsampling ratio. 10 000 symbols are measured in the modulation measurement. At 1.8 GHz, the 25-MSym/s 256-QAM modulation signals are measured, which exhibit the average output power (P_{avg}) of 24.85 dBm, average PAE of 16.94%, EVM of −31.37 dB, and adjacent channel leakage ratio (ACLR) of −32.05 dBc. At 2.4 GHz, the 25-MSym/s 256-QAM modulation signals are measured. They feature P_{avg} of 25.48 dBm, average PAE of 18.82%, EVM of −32.11 dB, and ACLR of −32.83 dBc. Meanwhile, at 3.5 GHz, the 50-MSym/s 256-QAM modulation signals are measured, which show P_{avg} of 22.76 dBm, average PAE of 13.45%, EVM of −31.46 dB, and ACLR of ≤−30.67 dBc.

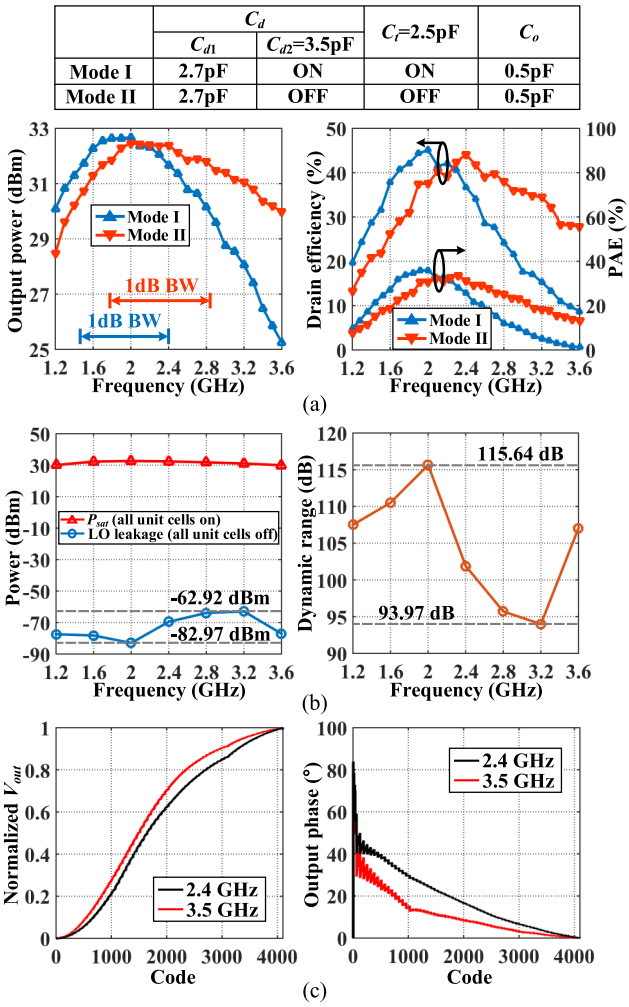

Fig. 20. (a) Measured output power, DE, and PAE of operation Mode I (C_{d1} = 2.7 pF, C_{d2} = 3.5 pF, C_t = 2.5 pF, and C_o = 0.5 pF) and Mode II (C_{d1} = 2.7 pF, C_{d2} OFF, C_t OFF, and C_o = 0.5 pF) versus frequency. (b) Measured LO leakage and dynamic range versus frequency. (c) Measured AM–AM and AM–PM distortions at 2.4 and 3.5 GHz.

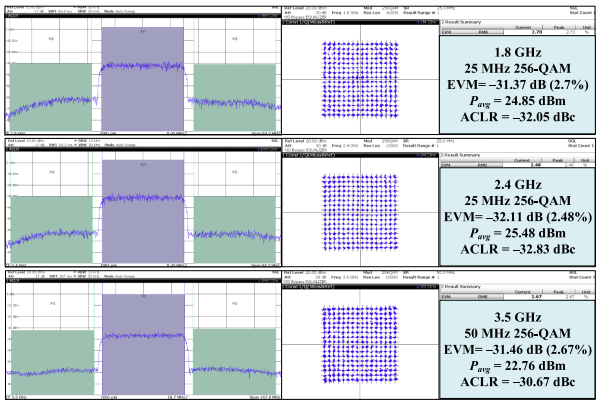

Fig. 21. Measured output spectrum and constellation of 256-QAM at 1.8, 2.4, and 3.5 GHz.

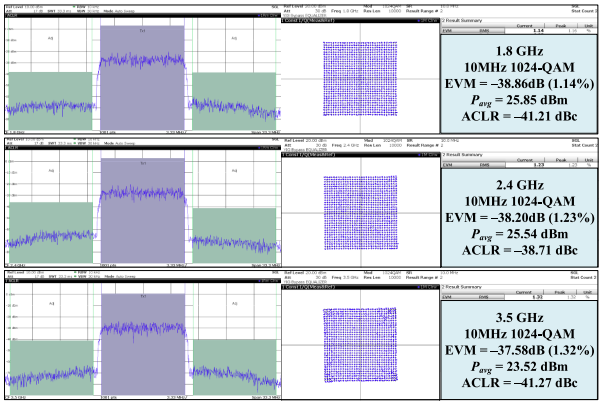

Fig. 22. Measured output spectrum and constellation of 1024-QAM at 1.8, 2.4, and 3.5 GHz.

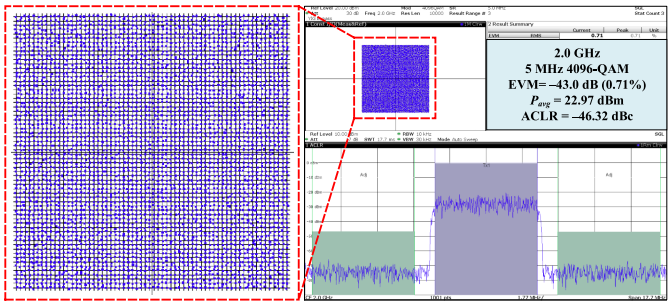

Fig. 23. Measured output spectrum and constellation of 4096-QAM at 2 GHz.

Moreover, the 10-MHz 1024-QAM signals are measured at 1.8, 2.4, and 3.5 GHz, as shown in Fig. 22. At 1.8 GHz, the measured 10-MSym/s 1024-QAM modulation signal shows P_{avg} of 25.85 dBm, average PAE of 15.35%, EVM of −38.86 dB, and ACLR of −41.21 dBc. At 2.4 GHz, the 10-MSym/s 1024-QAM modulation signals are measured, which exhibit P_{avg} of 25.54 dBm, average PAE of 16.68%, EVM of −38.2 dB, and ACLR of −38.71 dBc. Meanwhile, at 3.5 GHz, the 10-MSym/s 1024-QAM modulation signals are measured, which feature P_{avg} of 23.52 dBm, average PAE of 15.27%, EVM of −37.58 dB, and ACLR ≤−41.27 dBc.

Besides, even the 4096-QAM modulation signal could be supported by the proposed watt-level DPA. To achieve higher data rate, the higher order QAM signal (e.g., the 4096-QAM) should be supported by the future wireless transmission system. The 4096-QAM is introduced in IEEE 802.11 be (i.e., Wi-Fi 7) for peak data rate improvement. The measured EVM and spectrum of 5-MSym/s 4096-QAM at 2 GHz are shown in Fig. 23, which exhibit the EVM of −43.0 dB and ACLR −46.32 dBc with 22.97-dBm P_{avg}.

The EVM and ACLR of the 64-QAM and 256-QAM modulation signals versus symbol rate are measured at 2.4 and 3.5 GHz, as shown in Fig. 24(a) and (b). With a constant sampling rate of 200 MHz, the EVM and ACLR increase with higher symbol rate, which means a lower up-sampling rate. With higher up-sampling rate, the EVM and ACLR could be better. Moreover, the memory effect could further deteriorate the EVM and ACLR when the DPA transmits modulation

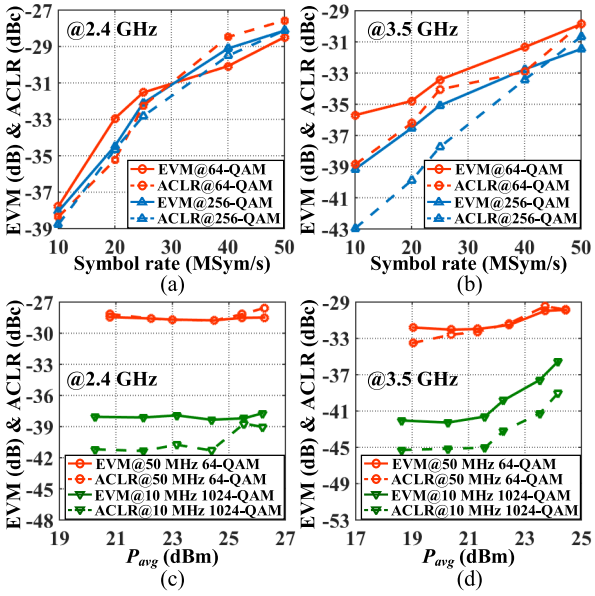

Fig. 24. Measured EVM and ACLR versus symbol rate at (a) 2.4 and (b) 3.5 GHz. Measured EVM and ACLR versus average output power at (c) 2.4 and (d) 3.5 GHz.

Fig. 25. Measured output spectrum and constellation of 20-MHz 64-QAM WLAN OFDM signal at 2.4 GHz.

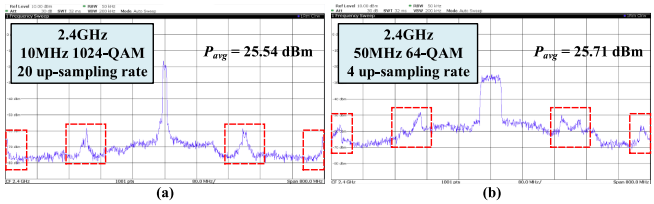

Fig. 26. Measured OOB spectrum of (a) 10-MHz 1024-QAM and (b) 50-MHz 64-QAM at 2.4 GHz.

signal with higher symbol rate. With 20 up-sampling rate, the 10-MHz 64-QAM signal at 2.4 and 3.5 GHz shows the EVM of −37.78 and −35.7 dB and the ACLR of −38.36 and −38.87 dBc, respectively. Meanwhile, the 10-MHz 256-QAM signal at 2.4 and 3.5 GHz shows the EVM of −38.06 and −39.17 dB and the ACLR of −38.78 and −42.97 dBc, respectively. Fig. 24(c) and (d) exhibits the measured EVM and ACLR of 50-MSym/s 64-QAM and 10-MSym/s 1024-QAM modulation signals versus P_{avg} at 2.4 and 3.5 GHz, respectively. As shown in Fig. 25, the measured 20-MHz 64-QAM WLAN OFDM signal exhibits P_{avg} of 24.15 dBm with −26.3-dB EVM at 2.4 GHz. The measured out-of-band (OOB) spectrum of 10-MHz 1024-QAM and 50-MHz 64-QAM at 2.4 GHz is shown in Fig. 26. The maximal sampling frequency is only 200 MHz, which limits the OOB spectrum, including

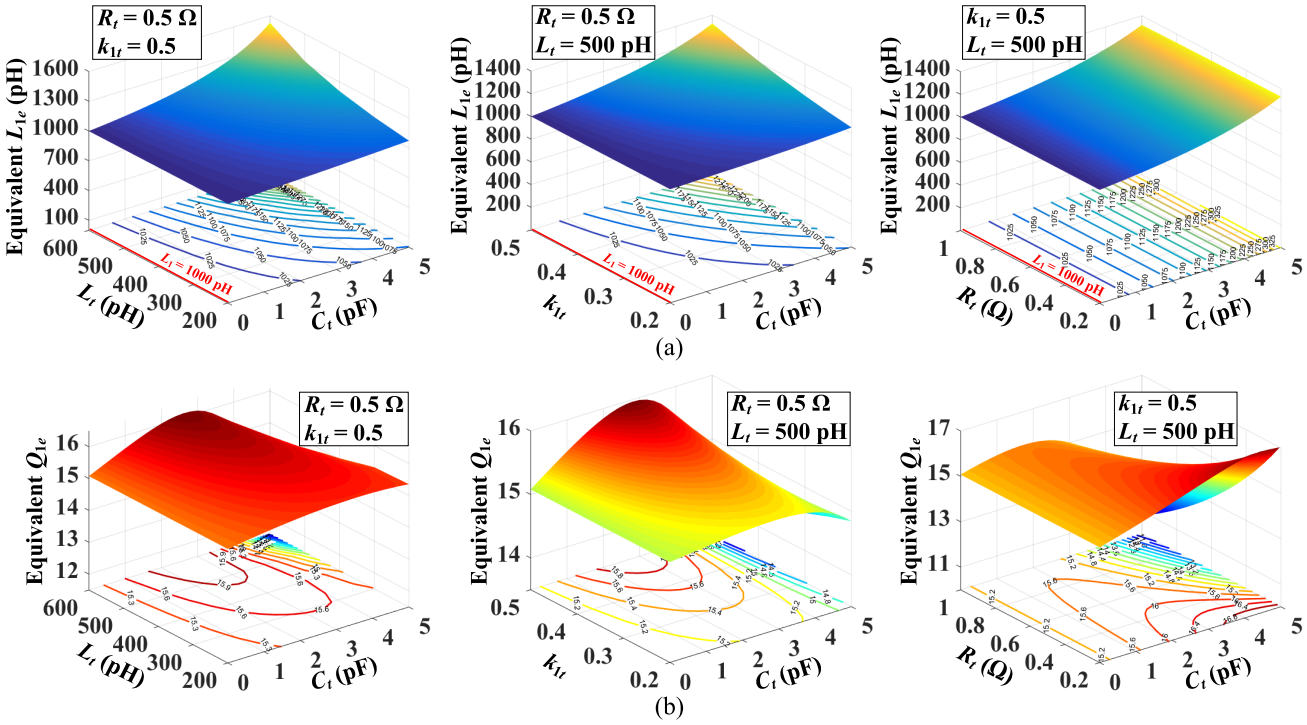

Fig. 27. Calculated (a) equivalent L_{1e} and (b) equivalent Q_{1e} at 2.4 GHz (L_1 = 1000 pH, R_1 = 1 Ω, and Q_1 = 15.08 at 2.4 GHz).

the spectral image suppression. The larger sampling frequency would move the replicas further, which enhances the spectral images' suppression.

The measured performance of the proposed DPA is summarized and compared with the state-of-the-art in Table I. Using reconfigurable power-combining transformer with harmonic suppression, the proposed watt-level polar DPA demonstrates a wide 3-dB BW of 1.2–3.6 GHz (100% 3-dB FBW) and 1-dB BW of 1.45–2.85 GHz (65.1% 1-dB FBW), which are competitive compared with other state-of-the-arts watt-level PAs. Meanwhile, the proposed DPA shows high efficiency with peak DE of 45.1% and peak PAE of 35.5%. The modulation test further demonstrates that the proposed polar DPA could support maximal 50-MHz 256-QAM signal and 5-MHz 4096-QAM signal.

VI. Conclusion

In this article, a wideband watt-level polar DPA is proposed. The reconfigurable power-combining transformer is introduced to further enhance the operation BW and improve the output power. The detailed theories and operation of the reconfigurable power-combining transformer based on tunable inductor are discussed. Meanwhile, the L–C circuit is used to suppress the harmonic. The 12-bit power-DAC featuring high resolution and dynamic range is introduced to support high-order modulation signals. The proposed DPA fabricated in the 40-nm CMOS technology shows the merits of wideband, high efficiency, watt-level output power, and low LO leakage, which are attractive for multi-standard wireless communication applications.

Appendix A

The equivalent circuit of the tunable inductor is shown in Fig. 3(a) (i.e., Type I). Z_{11} of such a one-port network can be expressed by

$$Z_{11} = R_1 + j\omega L_1 + \frac{\omega^2 k_{1t}^2 L_1 L_t}{R_t + j\omega L_t - j/(\omega C_t)}. \quad (26)$$

The equivalent inductance L_{1e} of the one-port network can be derived as

$$L_{1e} = \frac{\text{imag}(Z_{11})}{\omega} = L_1 + \frac{\omega k_{1t}^2 L_1 L_t [1/(\omega C_t) - \omega L_t]}{R_t^2 + [\omega L_t - 1/(\omega C_t)]^2}. \quad (27)$$

It can be seen that L_{1e} is affected by L_1, L_t, C_t, k_{1t}, and R_t. The equivalent quality factor Q_{1e} of the tunable inductor can be expressed by (28), shown at the bottom of the next page. To discuss the effect of C_t, L_t, k_{1t}, and R_t, the calculated L_{1e} and Q_{1e} at 2.4 GHz using (27) and (28) are shown in Fig. 27(a) and (b), respectively. The inductor with L_1 = 1000 pH and R_1 = 1 Ω at 2.4 GHz is adopted. Various values of C_t, L_t, k_{1t}, and R_t are analyzed when $1/(\omega C_t) > \omega L_t$. As shown in Fig. 27(a), L_{1e} can be adjusted in a relatively large range when C_t is tuning. L_{1e} obviously increases with larger L_t and k_{1t}. Meanwhile, the resistor R_t shows little effect on L_{1e}. As shown in Fig. 27(b), the equivalent Q_{1e} is calculated under the same conditions in Fig. 27(a). Q_{1e} is affected by C_t, L_t, k_{1t}, and R_t. The decreased R_t would lead to larger Q_{1e}. Note that when C_t is tuned to control L_{1e}, the proposed tunable inductor shows little degradation of Q_{1e}. The conventional directly connected tuning network using tunable capacitor C_{t2} is shown in Fig. 3(b) (i.e., Type II). The equivalent inductance L_{2e} and quality factor Q_{2e} of Type II can be calculated by (29) and (30), shown at the bottom of the next page, respectively.

To investigate the reliability of C_t, the voltage V_t across C_t is discussed. V_t can be calculated by (31), shown at the bottom of the next page. V_1 is the input voltage of the one-port network. To simplify the analysis, the ideal condition R_1

TABLE I
COMPARISON WITH STATE-OF-THE-ART WORKS

	This work		2020 JSSC [2]	2016 TMTT [6]	2020 JSSC [28]	2019 JSSC [29]	2017 ISSCC [31]	2012 JSSC [34]
Technology	**40-nm CMOS**		SiGe	28-nm CMOS	65-nm CMOS	65-nm CMOS	28-nm CMOS	45-nm CMOS
Topology	**Polar with reconfigurable transformer**		Linear class-AB	Triple-stack PA	Polar switched capacitor	Polar multi-subharmonic switching	Quadrature switched capacitor	Outphasing
Supply (V)	**1.1/2.5**		5	3	2.5	2.4/3.6	1.1	2.4
Operation frequency (GHz)	**1.2–3.6 (3 dB BW)** **1.45 – 2.85 (1 dB BW)**		4.9 – 5.9 (1 dB BW)	1.5–1.95* (1 dB BW)	2.4	1.65–2.2* (1 dB BW)	2.5	1.5–3.2 (3 dB BW)
P_{sat} (dBm)	**32.67**		33.0	31.2	30.0	30.0	28.6	31.5
Efficiency (%)	**45.1 (DE), 35.5 (PAE)**		35.5 (PAE)	33 (PAE)	40.2 (DE)	45.9 (DE)	35 (PAE)	27 (PAE)
Modulation	**5 MHz 4096-QAM**	**50 MHz 256-QAM**	80 MHz 802.11ax MCS11	3.84 MHz W-CDMA	10 MHz 1024-QAM	5 MHz 16-QAM OFDM	20–40 MHz WIFI	20 MHz 64-QAM
Frequency (GHz)	**2.0**	**3.5**	5.53	1.8	2.4	1.9	2.5	2.4
EVM (%)	**0.71**	**2.67**	1.0**	1.7	0.6	5.82	4.3–5.4	5.6
ACLR (dBc)	**–46.32**	**–30.67**	N/A	–33	N/A	–35	–44.7	N/A
P_{avg} (dBm)	**22.97**	**22.76**	19.4	26.5	23.2	22.8	17.3	24.8
Size (mm^2)	**2.6 (0.99‡)**		2.03	3.36	3.36	7.2	1‡	3.12

* Estimated from figures. ** Dynamic EVM.
‡ Core size.

$= R_t = 0$ is assumed. Equation (31) can be simplified as

$$V_t = \frac{k_{1t}}{1-\omega^2 L_t\left(1-k_{1t}^2\right)C_t}\sqrt{\frac{L_t}{L_1}}V_1. \tag{32}$$

It can be seen that V_t can be decreased by decreasing L_t or increasing L_1 (i.e., a smaller ratio of L_t/L_1). Therefore, it is possible to limit V_t for enhanced reliability by decreasing the ratio of L_t/L_1 even when V_1 is much higher than V_t.

APPENDIX B

The schematic of the two-port reconfigurable transformer is shown in Fig. 28. To derive the impedance matrix $[Z_{TA}]$, the three-port network of three coupled inductors including L_p, L_s, and L_t is considered. The impedance matrix of such a three-port network is represented by $[Z]$. V_n and I_n ($n = 1, 2, 3$) represent the voltage and current of the nth port, respectively, as shown in Fig. 28. The voltage at each port can be expressed by the following equation:

$$\begin{cases} Z_{11}\times I_1 + Z_{12}\times I_2 + Z_{13}\times I_3 = V_1 \\ Z_{21}\times I_1 + Z_{22}\times I_2 + Z_{23}\times I_3 = V_2 \\ Z_{31}\times I_1 + Z_{32}\times I_2 + Z_{33}\times I_3 = V_3. \end{cases} \tag{33}$$

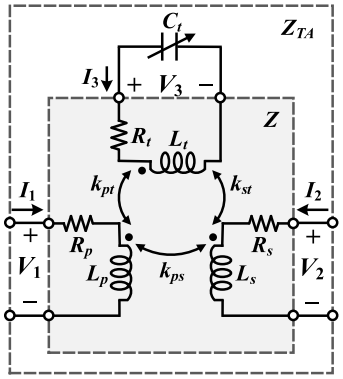

Fig. 28. Schematic of the two-port reconfigurable transformer.

When the capacitor C_t is connected to port 3 as shown in Fig. 28, V_3 can be expressed by

$$V_3 = -I_3 \times \frac{1}{j\omega C_t}. \tag{34}$$

Equation (33) can be further expressed by

$$\begin{cases} Z_{11}\times I_1 + Z_{12}\times I_2 + Z_{13}\times I_3 = V_1 \\ Z_{21}\times I_1 + Z_{22}\times I_2 + Z_{23}\times I_3 = V_2 \\ Z_{31}\times I_1 + Z_{32}\times I_2 + Z_{33}\times I_3 = -I_3 \times \dfrac{1}{j\omega C_t}. \end{cases} \tag{35}$$

$$Q_{1e} = \frac{\omega L_{1e}}{\text{real}(Z_{11})} = \frac{\omega L_1 R_t^2 + \omega L_1[\omega L_t - 1/(\omega C_t)]^2 - \omega k_{1t}^2 L_1 L_t[\omega L_t - 1/(\omega C_t)]}{R_1 R_t^2 + R_1[\omega L_t - 1/(\omega C_t)]^2 + R_t\omega^2 k_{1t}^2 L_1 L_t} \tag{28}$$

$$L_{2e} = \frac{[-R_1/(\omega C_{t2}) + \omega L_1 R_t](R_1 + R_t) - (R_1 R_t + L_1/C_{t2})[\omega L_1 - 1/(\omega C_{t2})]}{\omega(R_1 + R_t)^2 + \omega[\omega L_1 - 1/(\omega C_{t2})]^2} \tag{29}$$

$$Q_{2e} = \frac{[-R_1/(\omega C_{t2}) + \omega L_1 R_t](R_1 + R_t) - (R_1 R_t + L_1/C_{t2})[\omega L_1 - 1/(\omega C_{t2})]}{(R_1 R_t + L_1/C_{t2})(R_1 + R_t) + [\omega L_1 - 1/(\omega C_{t2})][\omega L_1 R_t - R_1/(\omega C_{t2})]} \tag{30}$$

$$V_t = \frac{k_{1t}\sqrt{L_1 L_t}}{C_t(R_1 + j\omega L_1)[R_t + j\omega L_t - j/(\omega C_t)] + C_t\omega^2 k_{1t}^2 L_1 L_t} V_1 \tag{31}$$

Finally, the impedance matrix $[Z_{TA}]$ of the two-port reconfigurable transformer can be derived as the following equations:

$$[Z_{TA}]_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} = R_p + j\omega L_p + \frac{\omega^2 k_{pt}^2 L_p L_t}{R_t + j\omega L_t - j/(\omega C_t)} \quad (36)$$

$$[Z_{TA}]_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} = R_s + j\omega L_s + \frac{\omega^2 k_{st}^2 L_s L_t}{R_t + j\omega L_t - j/(\omega C_t)} \quad (37)$$

$$[Z_{TA}]_{12} = [Z_{TA}]_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} = j\omega k_{ps}\sqrt{L_p L_s} + \frac{\omega^2 k_{st} k_{pt} L_t \sqrt{L_p L_s}}{R_t + j\omega L_t - j/(\omega C_t)}. \quad (38)$$

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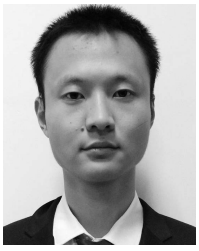

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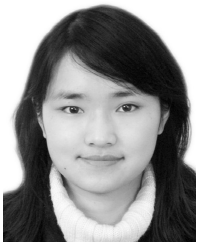

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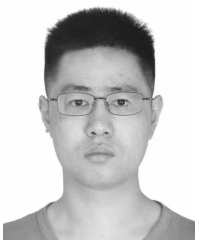

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