PIXAPP Photonics Packaging Pilot Line – Development of a Silicon Photonic Optical Transceiver With Pluggable Fiber Connectivity

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(Invited Paper)

***Abstract*—This paper demonstrates how the PIXAPP Photonics Packaging Pilot Line uses its extensive packaging capabilities across its European partner network to design and assemble a highly integrated silicon photonic-based optical transceiver. The processes used are based on PIXAPP's open access packaging design rules or Assembly Design Kit (ADK). The transceiver was designed to have the Tx and Rx elements integrated on to a single silicon photonic chip, together with flipchip control electronics, hybrid laser and micro-optics. The transceiver used the on-chip micro-optics to enable a pluggable fiber connection, avoiding the need to bond optical fibers directly to the photonic chip. Finally, the packaged transceiver module was tested, showing 56 Gb/s loop-back modulation and de-modulation, validating both the transmitter and receiver performance.**

***Index Terms*—Electrooptic modulators, chip scale packaging, demodulation, electronic packaging thermal management, electronics packaging, high-speed electronics, high-speed integrated circuits, intensity modulation, modulation, PIC, PIC packaging, photonics, semiconductor device packaging, silicon photonics, telecommunications, communication systems.**

I. Introduction

Recent decades have seen the growth of integrated photonics supported by the ever-growing information communication technology needs, as well as lidar systems, biomedical and other industrial sensing applications. The silicon Photonic Integrated Circuit (PIC) platform was created on the foundation of established CMOS (complementary metal–oxide–semiconductor) fabrication technology for silicon electronics. This native compatibility with CMOS technology, together with the ability to build compact, highly integrated photonic subsystems are the main driving forces behind Si-photonics. In recent years, the field has further grown out of the Silicon to include other integrated photonics platforms such as SOI [1], [2], InP [3], Si_3N_4 [4] and Ge [5]. These more optic-centered platforms allow for a better integration of active elements such as lasers, and are transparent in optical windows that silicon is not.

A. PIC Elements and MPWs

A wide array of Si-photonic elements has been demonstrated, and while there continues to be improvements in component performance, the technology has matured to the stage that design kits exist. These are provided as certified "building blocks" in the multi-project wafer (MPW) runs offered by various silicon foundries [6]. These include strip/rib waveguides and crossings, one-dimensional (1D) and two-dimensional (2D) grating-couplers (GCs), broadband edge-couplers, multi-mode-interference (MMI) splitters, broadband edge-couplers, integrated lasers, arrayed waveguide gratings (AWG), multiplexers/de-multiplexers, thermally tunable microring resonators, high-speed Ge photodiodes, thermo-optic phase shifters, electro-absorption modulators (EAMs), etc.

Hundreds of the unique PIC designs, together containing thousands of Photonics elements can be laid out in a single wafer. Researchers, graduate students, and Small & Medium Enterprises (SMEs) now routinely design PICs through these Multi-Project Wafer (MPW) runs which enable them to develop new devices and share costs without having to individually invest in expensive dedicated wafer runs. These PICs, a few millimeters wide, can easily contain hundreds of electrical and optical connections on a very small footprint, all of which require interfacing with other elements of the system.

The challenge for integrated photonics is no longer in fabricating photonic chips, but in fabricating photonic devices, i.e.,

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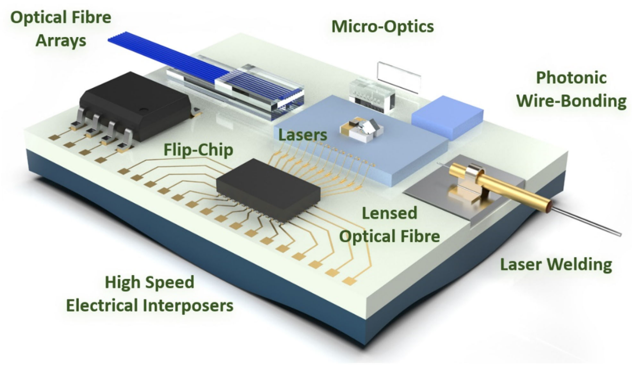

Fig. 1. Various packaging technologies available through PIXAPP.

the coupling of light and electrical signals between the 2D PIC and the 3D world outside.

B. PIC Packaging

Developing an operational PIC and demonstrating its functionality in a laboratory environment requires building a first prototype that allows accessing its inputs and outputs. PICs - being tightly integrated devices and at most a few millimeters long – need to be electrically and optically interfaced, which can be done in a variety of ways as shown in Fig. 1. They also need to be placed in a dedicated mechanical housing, that often needs to be thermally cooled. These four domains – electrical, optical, mechanical and thermal - make the core of what is known as photonic packaging. The challenges associated with photonic packaging are often underestimated and remain technically challenging [7]. The optical alignment tolerances can be sub-micron and must be carefully considered to account for the polarization requirements and thermal expansion. Small misalignments can cause large optical losses which necessitates photonics packages to be well made and accounting for all of these issues already at a lab stage [8]–[12].

However, bridging the gap from laboratory to an industrial product commonly brings in significant other issues related to reliability, which reflect in high financial cost of packaging which, at small volumes, can easily amount to about 50% of overall product cost.

A fragmented ecosystem is another reason why PIC packaging is costly. It is difficult for an SME to get a comprehensive and large volume photonic packaging service at a single company. A lack of design rules and standardization leads to SMEs holding multilateral talks with companies doing specific packaging technologies, each with its own set of processes which are not always mutually compatible.

C. PIXAPP

Technical and economic challenges of Photonic Packaging exist for all device designers, whether they are multinational companies, SMEs, or Researchers. To address those issues, the EU funded PIXAPP (Photonic Integrated Circuit Assembly and Packaging) Pilot Line was established. PIXAPP's goals are to (1) be a single point of contact for PIC Packaging, (2) Offer generic Packaging Solutions for PICs, and (3) Create a credible strategy to future full-scale PIC Manufacturing. The Pilot Line helps SMEs and industrial organizations bridge the so-called "Valley of Death", moving them from Technology Readiness Levels 5 (prototyping) to 9 (manufacturing). Different technological solutions are offered through PIXAPP in what are called building blocks – which are validated and scalable packaging processes.

To prove that multi-party assembly of photonic devices can be achieved at medium volume, to industry timescales, and at accessible cost-points, PIXAPP developed several showcase "demonstrators". These demonstrators were designed to stress-test the packaging and assembly capabilities of the pilot-line before opening the pilot-line to external users.

In this paper, we present the assembly of the Datacommunications (Datacom) Demonstrator that was established within PIXAPP using a variety of different building blocks. The goal of this demonstrator was to show how it is made in PIXAPP's distributed network, taken from design right through to testing.

II. The Datacom Specifications

The planned Datacom Demonstrator has a 200G transmitter side consisting of four channels each operating at 50Gb/s. The same was chosen for the receiver side, giving the module a total of 8 channels. An On-Off Keying (OOK) modulation format was chosen as it reflects bandwidth performance, a key figure for high-speed electronic packaging. The more advanced modulation formats usually involve more high-speed electronics [13], an added complexity which was not in scope of this packaging demonstration.

The agreed specifications for the PIXAPP Datacom demonstrator were as follows:

- single-chip transceiver
- SOI PIC platform
- 1310 nm laser integration
- Parallel Single-Mode 4 channel (PSM4) – for both Tx and Rx
- Relaxed Fiber-to-PIC tolerance through a pluggable connector
- 50Gbits (OOK) per channel

Furthermore, the packaging of this module was to address some key packaging challenges, and introduce non-standardized novel technologies:

- High degree of 3D integration including 2$\times$EICs; μOptics; Micro Optical Bench (MOB)
- Hybrid laser integration using Micro-Optical Bench (MOB) [14]
- Pluggable Fiber-to-PIC connection using micro-lenses on chip and on a fiber array cable
- High speed lines and interconnects such as LTCC electrical interposer and ribbon bonds
- Design optimized for passive cooling

The Datacom Demonstrator's tasks were divided among different packaging partners to demonstrate how the distributed network could be used. These tasks and its division could

TABLE I
DATACOM DEMONSTRATOR TASK DIVISION AMONG PARTNERS – PARTNER ENTITY'S FULL NAME ARE LISTED IN THE APPENDIX, TABLE III

	Partner	Task
System	TYN	System design
	ARG	System Design, and Electrical interconnects simulation
	IMEC	PIC design and fabrication
	ARG	Mechanical housing design and fabrication
	TYN	Thermal behaviour of laser and EICs
Optical	TYN	Zemax/Lumerical simulation
	CORD	MOB assembly and Laser Integration
	EBL	MOB assembly and 1310nm laser development
	ARG	MOB-to-PIC fixing
	KIT	Pluggable connector design and simulation
	IMEC	Pluggable connector design and simulation
	IMEC	Microlenses on PIC fabrication
	IMEC	Microlenses on MPO fiber array fabrication
	KIT	Microlenses on MPO fiber array fabrication
	TYN	MPO receptacle housing fabrication
	ARG	MPO receptacle to PIC fixing
Electrical	VTT	LTCC design and fabrication
	ARG	PCB design and fabrication
	ARG	PCB and LTCC interconnecting
	TYN	Solder ball Jetting
	TYN	Stud bumping
	ARG	Flip chip die bonding
	ARG	PIC to LTCC interconnects
Tests	III-V	S parameters - Electrical structures testing
	IMEC	Data transmission - Final modules testing

generally be divided to system, optical and electrical packaging, and are shown in the Table I.

III. FLOW OF THE DEMONSTRATOR ASSEMBLY

Adequate sequencing of packaging tasks is crucial for the success of the overall packaging and assembly. For example, elevated temperature reflows during electrical packaging can damage epoxy bonds during optical assembly. After assessing different options of the assembly, the assembly process was agreed to proceed as shown in the schematic under Fig. 2. For clarity of visualization, simulation building blocks are not shown. The packaging took place over 6 countries through 7 packaging partners, the geographical extent of different assembly strands are shown in Fig. 3.

IMEC designed and fabricated PICs in SOI platform [15], which is shown in the Fig. 4. They implemented the requirements for optical and electrical elements on the PIC (strands 1-3, shown in Fig. 5), and designed sufficient clearances for the tooling used to achieve different packaging steps.

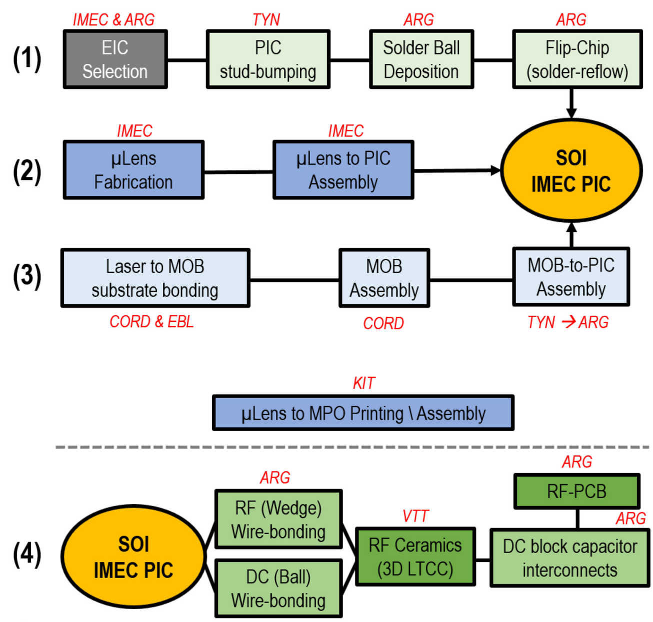

Fig. 2. Flow of Datacom Demonstrator assembly. The assembly was performed in 4 assembly strands: (1) Flip-Chip integration (2×EICs), (2) Microlenses for pluggable optical connector, (3) Laser Integration (MOB), (4) High speed LTCC, PCB, and interconnects. The KIT-led building block was technically a part of strand 2, but as it did not influence the flow of the integration, it is pictured outside of the strands.

A. Strand (1) - EICs

The first strand of the assembly dealt with Flip-Chip die bonding - the Electronic Integrated Circuit (EIC) integration. Each PIC contained 2 EICs, for the transmitter side a Driver for the Mach Zehnder Modulators (MZMs) and for the receiver side a Trans Impedance Amplifier (TIA), both in 4 channel configurations. High speed IMEC developed EICs were chosen due to their small footprint and high-speed performance. For reliable electrical connection between EICs and the PIC, the PIC was solder jetted and EICs were gold stud-bumped and were subsequently coined (flattened to have a similar height). The Driver has 69 and TIA 70 connections, which in total gives 139 bond-pads that were prepared for flip-chip die bonding by stud bump and solder jetting.

The flip-chip process was then performed with a die bonding machine where at the temperature of 245 °C the solder was reflowed, and a conductive contact was established between bondpads on the PIC and on the EICs (see Fig. 6).

B. Strand (2) - Microlenses

One of the goals in this demonstrator was to establish a pluggable fiber connection to/from the optical transceiver. The PIC has 8 grating couplers which are emitting light at 10° in the air, and with a Mode Field Diameter (MFD) of 9.2 μm at the wavelength of 1310 nm. The same MFD is on SMF28 fiber, a common fiber for telecommunications, which was chosen for coupling the light to the PIC. The connector system was developed by use of precision-fabricated components and

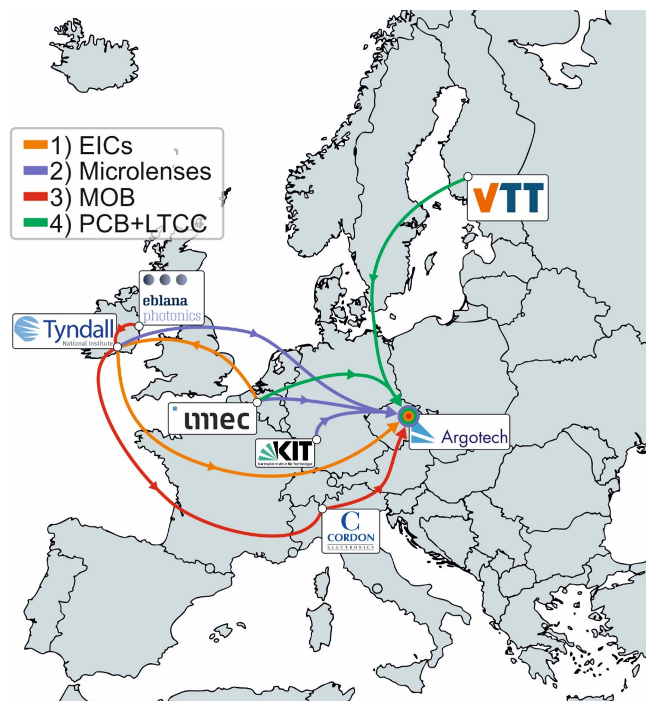

Fig. 3 Assemby sequence process flow through the PIXAPP packaging partners, for 4 different assembly strands shown in Fig. 2.

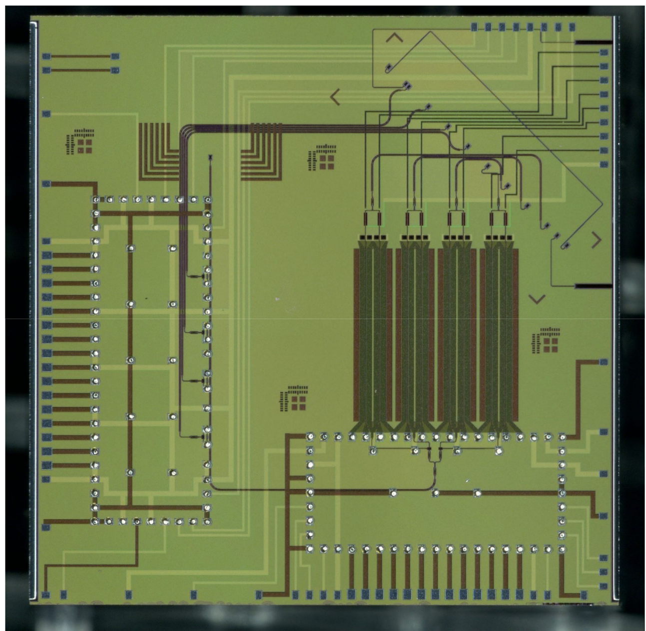

Fig. 4. Datacom PIC designed and fabricated by Belgian foundry IMEC.

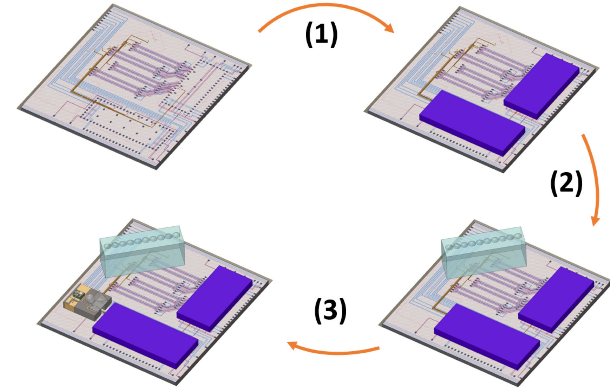

Fig. 5. Schematic of packaging the first 3 assembly strands on PIC. The (1) deals with EICs, (2) with microlenses, and (3) with the MOB.

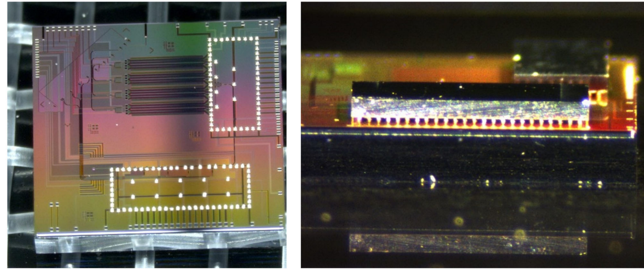

Fig. 6. Datacom PIC with solder showing as a white glow deposited on bondpads (left), and side view of die-bonded TIA and MZM Driver (right).

microlenses, that were placed on PIC and on a Multi-fiber Push On (MPO) Fiber Array (FA). The microlenses serve 2 purposes. Firstly, they can collimate diverging beams and couple the light to PIC from a distance. That way they protect the PIC from being damaged under forces due to (un)plugging. Secondly, they can expand the MFDs so that small misalignments created by plugging and unplugging result in a much smaller loss of optical power, and therefore maintain a good quality high-speed optical data link.

Polymer based microlenses were designed by IMEC in Belgium and, through their proprietary technology [16], deposited on a 980 μm thick silica glass block. The glass block was then deposited on a PIC, ensuring epoxy extends only within the allowed perimeter on the PIC. On the MPO FA side, KIT in Germany 3D printed polymer lenses on individual fibers of the MPO FA patch cable (see Fig. 7) using two-photon polymerization [17]. These freeform lenses match and couple the light to IMEC's expanded MFD. The flexibility of design and fabrication of these lenses allowed the MPO connector to come perpendicularly to the PIC's surface. This proved to be successful with a working distance of 2 mm. Additional loss per interface (IMEC+KIT microlenses) showed to be about 1.5 dB, with respect to direct Fiber to GC coupling. It is caused mainly by reflection losses at the 2 polymer lens-air interfaces; lens fabrication (shape and positioning) inaccuracies which lead to a mismatch in terms of optimal coupling angles and MFDs; as well as lens aberrations. The lenses expanded MFDs to 30 μm at a distance of about 2 mm, as shown in Fig. 8, achieving more than $3\times$ the original MFD. A mechanical connector for plugging an MPO FA was made at Tyndall in Ireland with MPO receptacles, components that are used in MTP version of MPO Fiber Array (FA) connectors, that were kindly provided by US Conec.

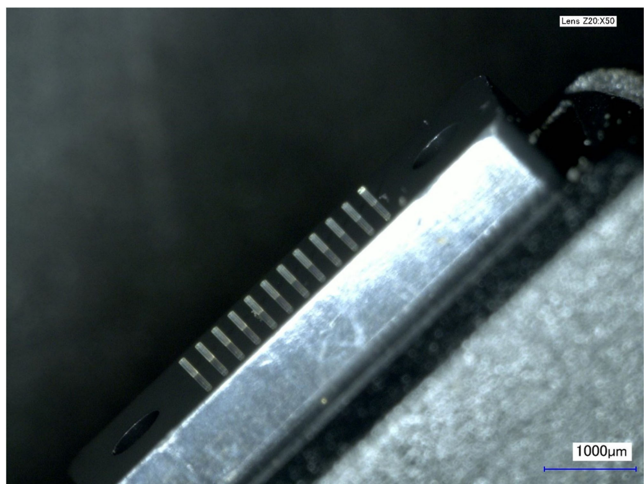

Fig. 7. Freeform lenses fabricated by two-photon polymerization on the facet of an Multi-fiber Push On (MPO) connector.

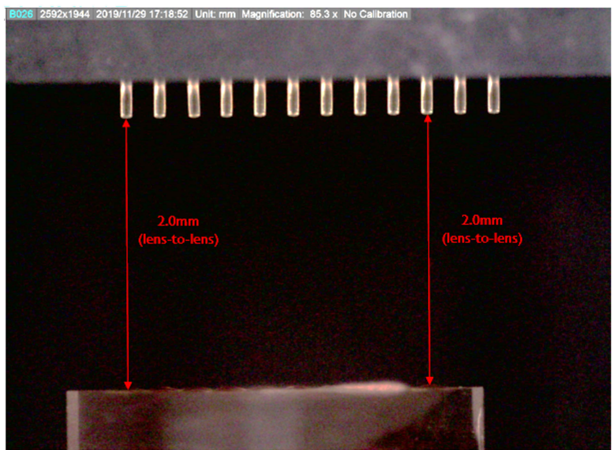

Fig. 8. Datacom Demonstrator PIC with micro-lens block (bottom) and lensed MPO connector (top). Working distance of 2 mm between the two lens surfaces.

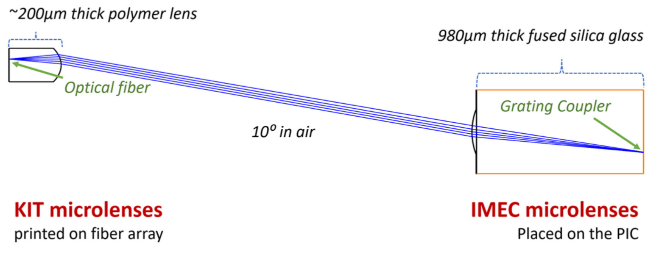

Fig. 9. A schematic graph showing the light path between MPO connector's free-form lenses (KIT lenses, left) and PIC's micro-lens block (IMEC microlenses, right), as shown in Fig. 8. Ray model only for illustration purpose, the design was optimized using the Gaussian beam propagation method.

C. Strand (3) - MOB

A Micro-Optical Bench (MOB) is a subassembly hosting a laser on a separate, dedicated substrate [14]. It was used as a hybridly integrated source on the PIC. The laser output light is focused by a ball lens, and then enters the prism which reflects it downwards at a 10° angle, through an opening in the substrate. The light is focused and reflected at an angle for optimal coupling to the GCs on the PIC.

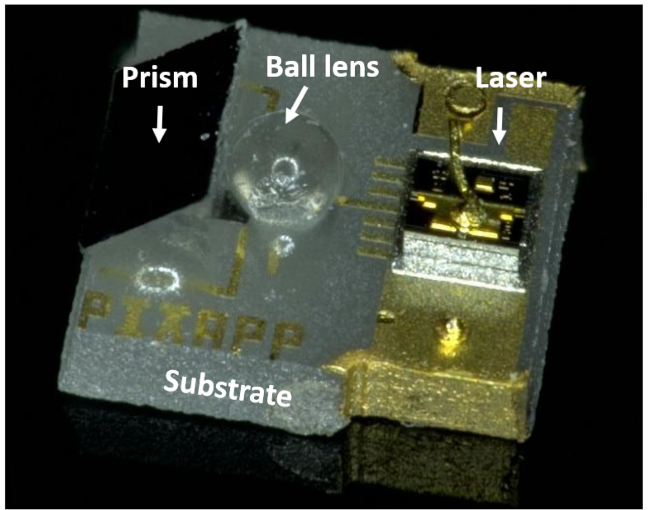

Fig. 10. Micro-Optical Bench (MOB) supports a laser, whose output is focused via ball lens and directed at 10° angle to couple to the GC, on the surface of the Datacom PIC.

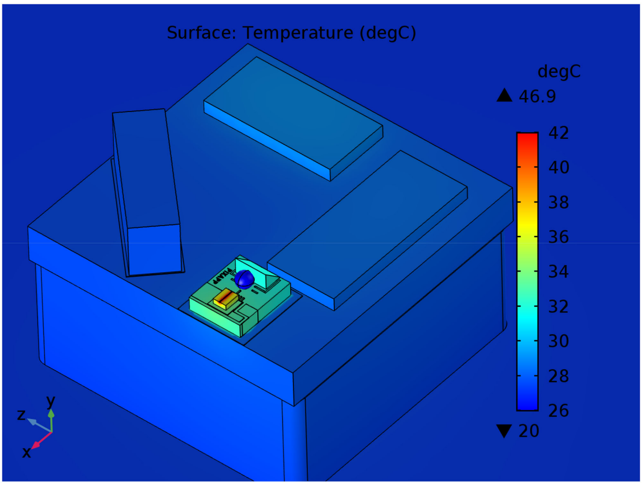

Fig. 11. Tyndall performed steady state heat dissipation simulation of the PIC, and its top-surface elements, positioned on aluminum submount. TIA and Driver produce significant heat, but due to low thermal conductivity of substrate and epoxy, high power laser on the MOB heats up the most averaging 36 °C, and reaching up to 77 °C in the laser's active region. MOB's height and the amount of low conductivity epoxy holding it significantly impact laser performance. Simulations indicated that no active cooling is necessary.

The benefit of an MOB is in its very small footprint and in ability to be independently placed on the PIC, to which it has to be bonded. The MOB was designed in Tyndall and was thermally simulated to ensure sufficient heat dissipation that can lower laser's output power (see Fig. 11). It was assembled at Cordon Electronics in Italy as shown in the Fig. 10, with lasers and guidance from Eblana Photonics in Ireland.

Tyndall and Argotech both placed MOBs on PICs using a UV curable glue, as shown in Fig. 12, with former partner developing

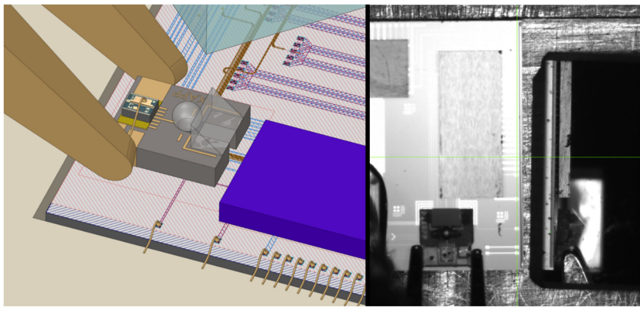

Fig. 12. MOB placement 3D design (left), and microscope image (right). Besides sequencing packaging steps in a way that is the least hazardous to other packaging processes, the successful packaging of complex systems requires establishing clearances for the tooling – such as for the MOB placement shown.

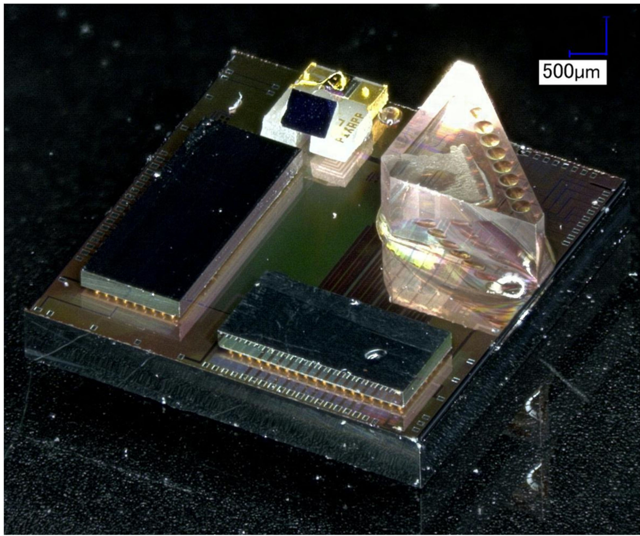

Fig. 13. Microscope photo of a fully assembled Datacom PIC. On-PIC elements involve 2 EICs, IMEC's microlens array, and an MOB.

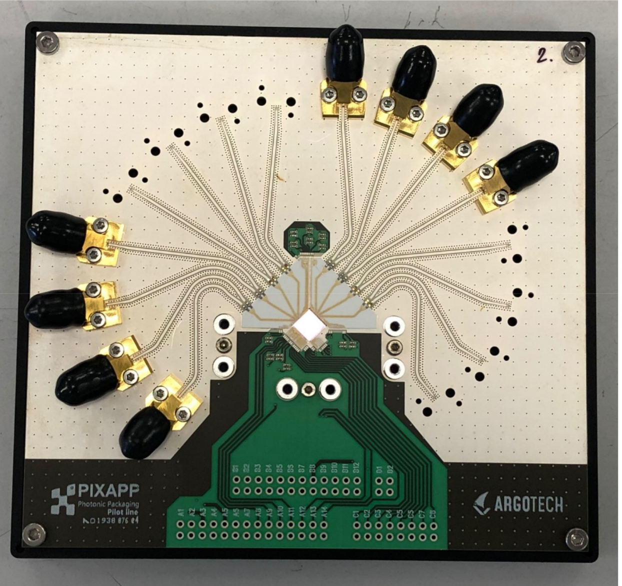

Fig. 14. Datacom Demonstrator's housing with several Rosenberger connectors being attached to the PCB, that is connected to the LTCC interposer close to the central opening where the PIC comes in. This PCB-LTCC assembly was assembled together, and the PIC was placed in the centre once assembled PIC (passing through strands 1-3) was ready.

the process and the latter adopting it for production at scale. The complete coupling losses (from laser output – ball lens - prism to GC) were measured with multiple MOBs on test structures to be in the range of 8.9-9.5dB. Higher loss was mainly due to discrepancies between the mode size, shape and angle required by GCs. Placement and gluing process introduced additional loss on the order of 0.5 dB ($\pm 1\mu$m).

With the first 3 assembly strands completed, all on-PIC components were integrated, as shown in Fig. 13.

D. Strand (4) – PCB, LTCC and Other Electrical Interconnects

The PIC has a footprint of 5.1 mm $\times$ 5.1 mm, and with 139 flip-chip electrical connections for the 2 EICs, that required a significant amount of electrical interfacing - much of it high speed. High bandwidth for 50G operation required careful design of the electrical lines leading away from the PIC and to the electrical connectors on the PCB. Connectors chosen are solderless, surface mount SMA connectors by Rosenberger (RPC 1.85). They were selected for their high-speed performance and the ability to be easily taken off and reused on multiple test structures and final modules.

The PIC required 75 closely placed bond pads and precision-made electrical waveguides that would fan out high speed electrical signal with minimal losses. Closely spaced RF bondpads and carefully designed fan-outs were the factors entailing an electrical interposer. VTT in Finland develops interposers in Low Temperature Cofired Ceramic (LTCC) technology [18]. Their laminated multilayer structures of high precision allow 3D guiding of multiple high-frequency electrical lines to be brought close to the PIC (and to fan-out from it) with a reduced pitch spacing, what normally would not be possible with PCB.

Argotech designed and simulated the complete mode propagation in all 8 GSSG lines, from the connector pads on the PCB, through the interposer, and onto the bondpads of the PIC. Their design was translated into LTCC fabrication design for VTT, and a PCB design which was finalized again by Argotech, and subsequently fabricated by an external supplier.

Upon fabrication of both the PCB and LTCC, the two were joined together in mechanical housing, and were electrically interfaced with DC blocking capacitors [19]. Image of that assembly is shown in Fig. 14.

The PIC is then placed on a dedicated submount in-between LTCC interposer, and it's 75 bondpads were wirebonded (DC signal) and ribbon bonded (RF signal) to the interposer, as shown in Fig. 15.

For operation, a pluggable optics had to be placed on top of the PIC, ensuring free space connection to the on-PIC microlenses. A 2.2mm thick top (connector-holding) plate was placed on the mount, just about a millimeter above the PIC. The plate was positioned and secured, with central opening in it being over

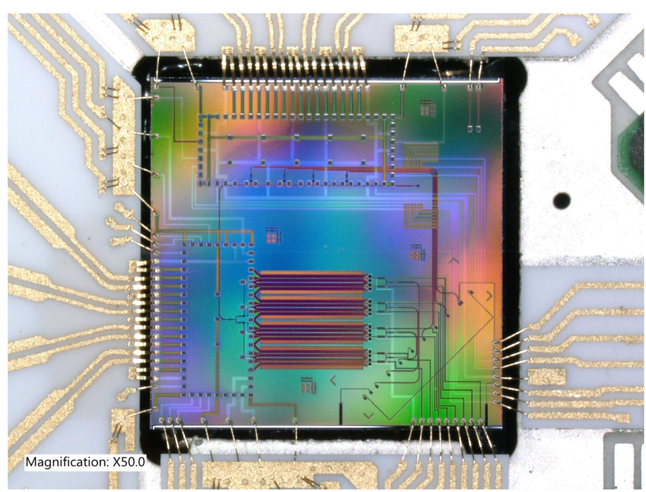

Fig. 15. Datacom test PIC (centre) used for verifying DC wire- and RF ribbon-bonding to the LTCC (around). This PIC is without on-PIC elements, and was used to test the electrical integration processes, as well as to asses the electrical line's signal losses.

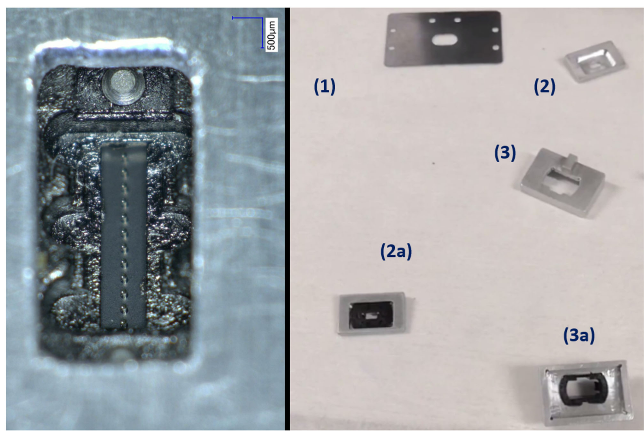

Fig. 16. Left - KIT-made microlenses on an MPO FA patch-cord slotted in, and visible through the MTP/MPO receptacle from US Conec. Right – Tyndall made connector parts used in Datacom Demonstrator with top plate (1) on top of which goes MPO connector (2 and 3) that contains MTP/MPO receptacle and holder (2a and 3a).

the PIC's microlens. The Tyndall-made connector using US Conec components, shown in the Fig. 16, and with the MPO FA containing microlenses already plugged into it, was placed on the top plate, and subsequently fixed with an epoxy (see cross sectional view in Fig. 17). The complete module is shown in the Fig. 18.

IV. Testing

The testing of Datacom Demonstrator took place at IMEC in Belgium. The results presented here are from a version of the demonstrator that had IMEC lenses both on PIC and on MPO connector, instead of KIT 3D printed ones. This change was made to ensure longer working distance between FA and PIC, mitigating the risk of a connector touching the PIC.

Firstly, the optical power emitted by the module's laser was evaluated. The laser was saturating between 80 mA and 100 mA, and the optical spectrum of the laser was measured

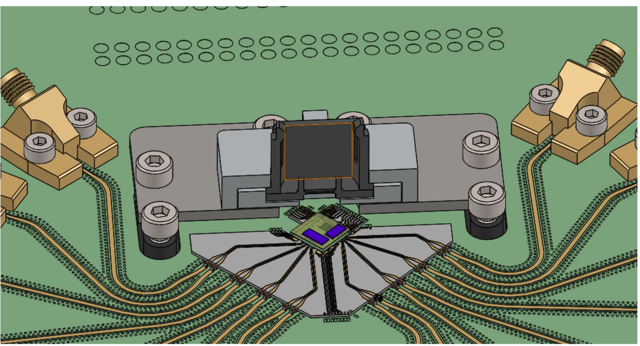

Fig. 17. Scheme of the Datacom Demonstrator. Rosenberger RPC 1.85 connectors on the PCB are shown at the extreme left and right, from which electrical lines are going over PCB and LTCC to reach the PIC, a cross sectional view of the top (connector-holding) plate with the connector.

Fig. 18. Fully assembled Datacom Demonstrator.

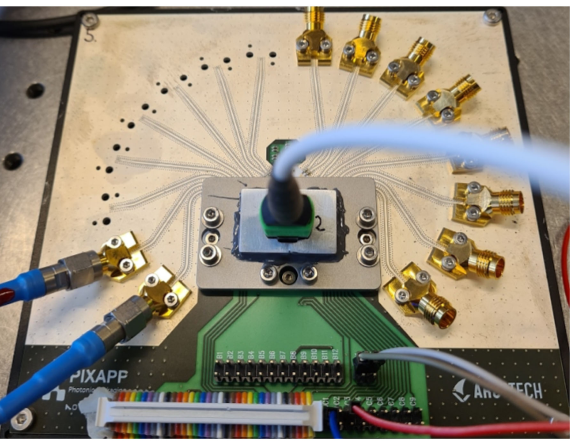

Fig. 19. Datacom Module with RF cables connected to the transmitter side only, and the MPO FA with microlenses being plugged in the centre.

showing peaks at 1308.2 nm and 1310.2 nm respectively. That was a longer wavelength than what was found optimal for the modulator itself, which was 1289 nm. With the Mach-Zehnder Modulator biased both for heater and electrodes at maximum transmission point, and at a laser bias current of 80mA, the light emitted was between −12.1 dBm and −13.2 dBm.

With module connected as shown in the Fig. 19 and the setup as shown in schematic Fig. 20, the high-speed time-domain

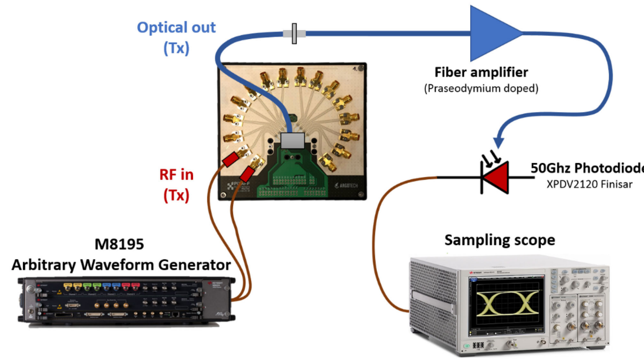

Fig. 20. Measurement setup for high-speed time-domain tests of the transmitters.

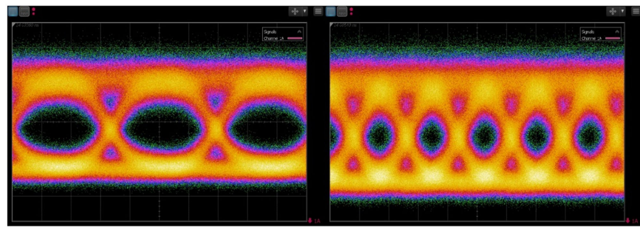

Fig. 21. 28Gb/s transmitter eye diagram (left) and 56Gb/s eye diagram (right).

TABLE II
TRANSMITTER LOSSES

Component	Loss [dB]
Micro optical bench	2.0
Input grating coupler	2.6
Waveguide routing from GC to splitter	1.7
Splitter loss	6.10
Modulator loss at quadrature point	7.30
Waveguide routing from MZM to GC	0.67
Output grating coupler	2.57
TOTAL	**22.94**

transmission test was conducted and the eye diagrams showed good performance for both 28Gb/s and 56Gb/s. Resulting open eye diagrams are presented in the Fig. 21. The corresponding transmitter losses are shown in Table II. The average insertion loss value of the full electrical transmission line, excluding the PIC, for 42 GHz (∼56Gb/s) was about 3 dB, which was close to the value of 2.5 dB obtained from RF simulation. When PIC line is considered, the loss value increased for 2 dB to a total of about 5 dB, which nearly doubled the insertion loss of the full electrical line. Variations in linewidths, effects of ground pattern and matching circuits at the end of LTCC lines make LTCC-only measurements less reliable at high frequencies. However, longer than desired PIC lines also caused significant increase in losses. Therefore this 2 dB increase in losses reflects combined PIC and LTCC line performance. Typical LTCC microstrip line losses have been 0.29 dB/cm at 10 GHz, and PCB line was measured to be about 1 dB at 42 GHz.

TABLE III
ABBREVIATIONS AND FULL NAMES OF PIXAPP PARTNERS INVOLVED IN DATACOM DEMONSTRATOR WORK

Abbreviations	Full name	Country
TYNDALL, TYN	Tyndall National Institute	Ireland
ARGOTECH, ARG	Argotech A.S.	Czech Republic
IMEC	IMEC - Interuniversity Microelectronics Centre	Belgium
CORDON, CORD	Cordon Electronics Italia	Italy
EBLANA, EBL	Eblana Photonics Ltd.	Ireland
KIT	Karlsruhe Institut of Technology	Germany
VTT	VTT Technical Research Centre of Finland Ltd	Finland
III-V Lab, III-V	III-V Lab	France

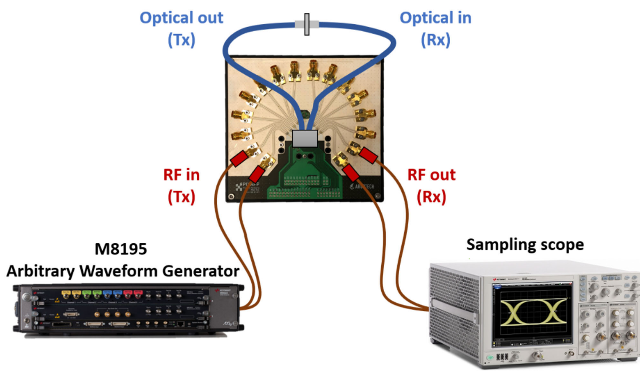

Fig. 22. Measurement setup for high-speed time-domain measurements of the transmitter's (Tx) modulation and receivers's (Rx) demodulation simultaneously.

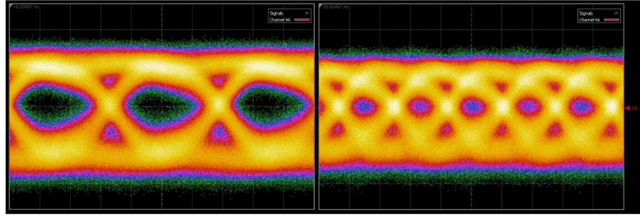

Fig. 23. 28Gb/s loopback (transmitter + receiver) eye diagram (left), and 56Gb/s eye diagram (right).

The final test on the Demonstrator involved connecting the transmitter part of the PIC to the receiver one, as presented in the Fig. 22. The back-to-back measurement, involving modulation and de-modulation, was shown to be successful.

As shown in Fig. 23, at 28Gb/s open eyes can still be clearly observed, however, at 56Gb/s the signal-to-noise ratio is reduced due to the non-optimum laser wavelength with respect to the central wavelength of the modulator.

V. CONCLUSION

In this paper we presented how the Pilot Line enables complex assemblies to be made with building blocks - packaging technologies that are scalable and suitable for volume manufacturing. The use of these building block processes was showcased by

the development of a truly one-chip optical transceiver package, which was assembled using inputs from across the PIXAPP supply chain. The demonstrator covered the key PIC packaging processes from the PIC design phase, to optical, electrical, thermal and to the mechanical packaging – successfully integrating different technologies together into a functional module.

Results showed successful 56Gb/s per channel, OOK high-speed data modulation and de-modulation - resulting from carefully designed and packaged electrical and optical lines. PIXAPP is an important step forward in linking the fragmented value chain, greatly enhancing industrial competitiveness, and Europe's leading position in advanced photonics technology. The Datacom Demonstrator showed successful distributed packaging through PIXAPP - it validates how Pilot Line's building blocks and interdisciplinary coherent technology chain unite multiple European companies and Research Centers.

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