Low Dark Current and High Speed InGaAs Photodiode on CMOS-Compatible Silicon by Heteroepitaxy

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***Abstract*—Top-illuminated proof-of-concept indium gallium arsenide (InGaAs) photodiode (PD) array and high speed InGaAs PDs were realized on (001) silicon (Si) substrate by direct heteroepitaxy using metal–organic chemical vapor deposition. The PDs containing InGaAs active layer lattice-matched to InP were grown on Si substrates employing InP-on-Si template with growth technique including GaAs on V-grooved Si, thermal cycle annealing and strained layer superlattice defect filters. Dry etched mesa structure with polyimide passivation was implemented. 8 × 8 InGaAs PD arrays with mesa diameters of 20, 30 and 40 μm were realized on (001) Si, and their performances were benchmarked with identical devices on a native InP substrate. A low dark current density of 0.45 mA/cm^2 and a responsivity of 0.72 A/W at 1550 nm were measured for 40-μm-diameter device on Si. Directly modulation has also been performed showing a 3-dB bandwidth up to 11.2 GHz and open eye diagram up to 25 Gbps. The imaging performance of InGaAs PD arrays on Si were also demonstrated for the first time by capturing the output beam profile of a single mode fiber at 1550 nm.**

***Index Terms*—Detector materials, optical interconnects, photodetectors, sensor arrays.**

I. Introduction

SILICON (Si) detectors have been widely used in the visible and near infrared regime, yet the sensitivity rolls down rapidly for the detection wavelength above 1 μm. On the other hand, indium gallium arsenide (InGaAs) detectors demonstrated superior performances in the short wave infrared (SWIR) regime (900 nm to 1700 nm), where Si detector is no longer applicable. Unlike mid-wave and long-wave infrared where light is emitted from the object, SWIR photons are either reflected or absorbed by the object, providing strong contrast for high resolution that is similar in visible region [1]. A large number of applications that are difficult or even impossible to perform in visible regions are enabled by using SWIR cameras, such as such as defects detection in silicon wafers [2], agriculture quality control [3], detection of contaminations [4] and hyperspectral surveillance [5]. Light detection and ranging (LIDAR) technology has seen explosive growth in the last few years primarily driven by the realization of high-performance automatic driver-assistance systems and fully autonomous vehicles [6]. Human eyes are not harmed bywavelengths longer than 1400 nm [7], allowing significant optical power budget increase for the LIDAR system. Longer detection range therefore can be achieved by utilizing InGaAs detectors and longer wavelength lasers [8]. InGaAs detectors are also comprehensively used in optical communication [9]. They are mainly used as receivers in C-band and O-band links in long haul, access network and data centers. We have seen rapid demand increase for high speed photodiodes (PDs) recently, fueled by maturation of 5G technology, Internet of things and increasing intra- or inter- data centers links [10].

Although extensively used in sensing and optical communications, the cost of InGaAs detectors is still significantly higher than Si detectors. The reason for this is threefold. Firstly, the substrate material used to fabricate InGaAs detectors is indium phosphide (InP). Compared to Si, InP wafers are much more fragile, expensive and have limited diameters up to 4-inch, with 2- or 3-inch wafers being the most common. On the contrary, Si substrates are 8- or 12-inches enabling lower costs due to increased devices per wafer and higher yield. This will lead to significant reduction of the cost per chip. Secondly, conventional SWIR image sensors are generally produced with hybrid integration process that flip-chip bonds an InGaAs-based PD array to a silicon readout circuit. This setup is expensive to manufacture with limitations in pixel size and density that impede high volume applications of InGaAs PD array. Lastly, packaging with lens arrays and drivers occur at the die-level for InGaAs detectors, while for Si wafer-level assembly is becoming mainstream [11].

The high manufacturing cost issues can be addressed by fabricating SWIR detectors directly on silicon wafer, leveraging complementary metal oxide semiconductor (CMOS) processes that feature high yield, high volume and low cost. Over the years, there are mainly three strategies of SWIR photodetectors on silicon technology that have been proposed. The first approach is based on the growth of high-quality germanium (Ge) epitaxial films on Si. Ge based photodetector on large silicon wafer has been commercialized primarily for the telecommunications in

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O-band [12], [13]. However, the responsivity of Ge reaches a peak at about 1530nm and decreases sharply at longer wavelengths [14]. The notably higher dark current levels compared to their III-V incumbent also limit their applications in longer wavelengths. The second approach is heterogeneous integration via wafer bonding. This has been used to integrate InGaAs epilayers grown on native InP substrates onto large Si wafers. Photodetectors are thus processed using Si as the handling wafer. Although an InGaAs array detector was demonstrated [15], the sensitive bonding process and wafer size mismatch hinder the yield and scalability of this technology.

The third approach is direct heteroepitaxy of III-V semiconductors on Si substrates [16]. It has gained significant attention recently, especially for monolithically integrating high quality active optical components into silicon photonics [17], [18]. We have previously demonstrated 1550 nm InP lasers on CMOS-compatible (001) Si substrates [19]. InP-on-Si templates with record low surface defect density were achieved by combining nano-V-groove patterned Si, dislocation filters, and thermal cycle annealing [20]. In this work, we push the InP-on-Si template technology forward and have successively demonstrated mesa InGaAs PDs with both low dark current and high bandwidth. We previously reported single InGaAs PIN PDs on non-compatible miscut Si [21]. Here, top-illuminated proof-of-concept 8×8 InGaAs PD arrays were first realized on CMOS-compatible (001) Si by heteroepitaxy, and identical devices were also fabricated on a native InP substrate for comparisons. PDs on Si with 40 μm diameter demonstrate a dark current as low as 5.71 nA at 1 V reverse bias, corresponding to a dark current density of only 0.45 mA/cm^2. A responsivity of 0.72 A/W was measured at 1550 nm. Identical devices on InP yield a dark current density of 0.20 mA/cm^2 and responsivity of 0.57 A/W. High speed InGaAs PDs with ground single ground pads were also demonstrated on Si. A bandwidth of 11.2 GHz and up to 25 Gbps eye diagrams were measured with a clear eye opening. The comparable device performances on both InP and Si suggest the potential for realizing high performance InGaAs PDs using CMOS fabrication techniques.

The paper is organized as follows. In Section II, we introduce the heteroepitaxy on silicon process by metalorganic chemical vapour deposition (MOCVD) including InP pseudo template development and the InGaAs detectors epitaxy design. Subsequently, we present the device structure and fabrication process in Section III. The device characterization results follow in Sections IV. In Section V, we discuss the results with a focus on the dark current density and bandgap energy estimation. Finally, this work is concluded in Section VI.

II. Heteroepitaxy on Silicon Substrate

A. III-V Heteroepitaxy on Silicon

There have been substantial interests in integrating III–V materials on Si, due to the potential to use CMOS-compatible silicon photonics (SiPh) platform with III–V components. Such integration enables large-scale photonic integrated circuits (PICs) production with low cost and flexibility. Hybrid integration solutions including co-packaging [22], wafer bonding [23] and 3D flip-chip bonding [23] have been proposed to integrate III–V semiconductors on SiPh demonstrating a host of novel active PICs on silicon. However, devices made with hybrid integration still endures limited scalability, lower yield and large footprint.

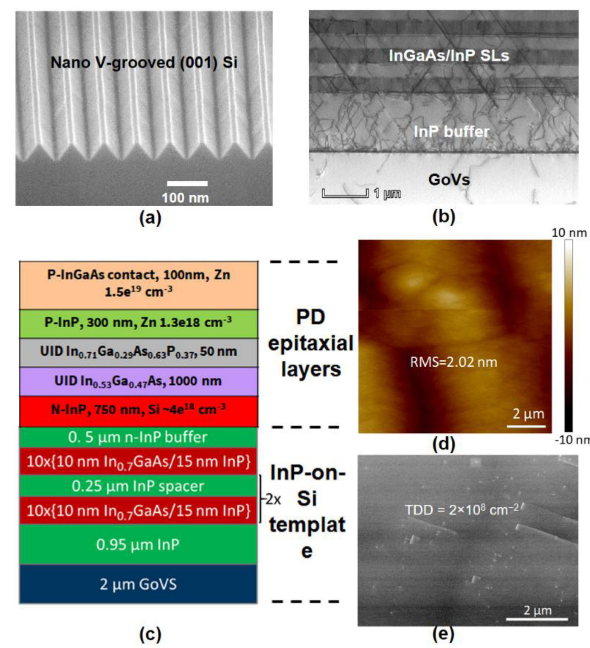

Fig. 1. (a) Tilted scanning electron microscope image of fabricated nano V-grooved (001) Si substrate. (b) Cross-sectional scanning transmission electron microscope image of the InP-on-Si template. (c) Epitaxial structures of PD on Si. Corresponding (d) 10×10 μm^2 AFM scan and (e) ECCI measurement of the as-grown PD surface.

The ultimate solution for monolithic integration III–V materials on (001) Si is heteroepitaxy. Although crystalline quality is still fundamentally challenged with threading dislocations (TDs), stacking faults and antiphase boundaries (APBs), prominent progress has been achieved by growing gallium arsenide (GaAs) on offcut Si [25]. Generally, a 2°–6° miscut Si (001) substrate is used to eliminate the formation of APBs. Other techniques to prevent APBs are based on treatments on Si substrates prior to III-V growths, including high temperature (HT) annealing [26], Si homoepitaxy [27] and nano-patterned Si substrate [28]–[31]. Additionally, thermal cycle annealing (TCA), strained interlayers and strained layer superlattices (SLSs) have been proven effective in lowering the dislocation densities for III-V buffers grown on Si substrates.

B. InP-on-Si Template

In this work, high quality InP-on-Si template was grown by MOCVD in two steps. A 2-μm-thick GaAs layer was first grown on a 12-inch (001) nano-patterned V-grooved silicon wafer, as shown in Fig. 1(a). The 65 nm nano-pattern openings were formed by CMOS-compatible dry etch and wet etch processes. Compared with GaAs directly grown on planar Si, the use of GaAs on V-grooved Si (GoVS) avoids the formation of APBs and leads to less defects by aspect ratio trapping (ART) mechanism. Details of the Si substrate preparation and the GaAs buffer growth are available in [32]. APB free GaAs film with a smooth

surface morphology was achieved with a TD density on the order of 10^7/cm^2.

Next, the 12-inch GoVS wafer was diced into 2 × 2 cm^2 coupons for InP buffer growth in a horizontal Thomas-Swan MOCVD system. The InP buffer was grown in three primary steps. A 30 nm low temperature InP was grown at 435 °C to form a nucleation layer and to accommodate the high density of generated misfit dislocations (on the order of 10^{10}/cm^2). A 45 nm middle temperature InP layer was then grown at 540 °C for coalescence and to planarize the InP growth surface. Afterwards, a 1-μm-thick HT InP primary buffer layer was grown at 600 °C –630 °C to enhance TD self-annihilation and subsequently improve the buffer quality. Next, three periods of $In_{0.7}Ga_{0.3}As$/InP SLSs were grown to filter the dislocations. The total thickness of the InP buffer layer is around 2.7 μm. The cross-section scanning transmission electron microscopy (STEM) image shown in Fig. 1(b) clearly illustrates the generation, propagation, and interaction of the defects. A significant number of TDs are either redirected or terminated at the interfaces of each stack of SLSs. Further details on the InP buffer and SLSs growth optimization are reported in [19]–[20].

C. InGaAs Photodetector Epitaxy

The epitaxial structure for the conventional InGaAs p-i-n (PIN) PD grown on the InP-on-Si template is presented in Fig. 1(c) showing the layers thicknesses. Fig. 1(d) and (e) demonstrate the surface morphology and surface defects of the as-grown PD on Si, characterized by atomic force microscopy (AFM) and electron channeling contrast imaging (ECCI) respectively. A smooth surface was obtained with the roughness as low as 2 nm RMS (root mean square roughness). The final surface defect density is 2×10^8 cm^{-2}, indicating no extra misfit dislocations generated within the 1-μm-thick InGaAs absorption layer. Identical InGaAs PIN epitaxy was grown on a premium n-type InP (001) substrate for direct comparisons.

III. Device Design and Fabrication

Surface normal PIN PDs were realized using etched mesa structure. Identical InGaAs PDs were fabricated both on Si and InP. A cross-section schematic diagram of the mesa PD structure on Si is shown in Fig. 2(a). It was reported that inductively coupled plasma - reactive ion retching (ICP-RIE) etched InGaAs PD generates lower dark current compared to the wet-etched mesa [33]. In this work, the mesa structure was defined by chlorine-based ICP-RIE etching using silicon dioxide (SiO_2) mask. The mesa etch stops at the n-type InP contact layer where the top n-type electrode was deposited.

The etched sidewall of the mesa is passivated by a combined process of polyimide coating and silicon nitride (SiN_x) deposition. After removal of the oxide mask, positive tuned photosensitive polyimide was directly spin coated and patterned with an i-line stepper to form the footprint surrounding the mesa. The sample was then cured at elevated temperature to assure adequate mechanical and electrical properties of the polyimide. SiN_x deposited by plasma-enhanced chemical vapor deposition encapsulates the whole wafer after the polyimide was cured.

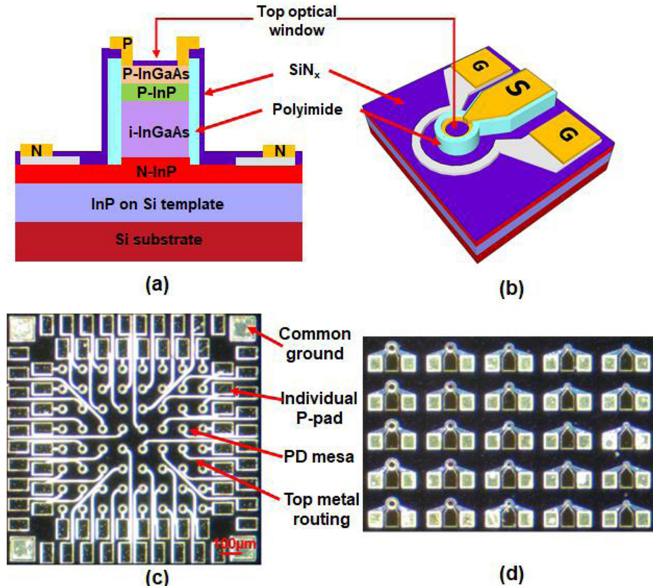

Fig. 2. (a) Cross-section schematic of a mesa PD structure. (b) 3D schematic of the high speed InGaAs PD on silicon. Microscope image of fabricated top-illuminated (c) 8 × 8 InGaAs PIN array with pixel diameter of 40 μm and (d) high speed PIN PDs with GSG pads on Si.

This layer of SiN_x on top of polyimide seals micro-cracks in the polyimide films, contributing to the device lifetime improvement and dark current reduction [33]. The thickness of SiN_x is also chosen to enhance photo sensitivity as a mono-layer AR coating. To allow sufficient top-side illumination, ring shaped p-metal contacts were used. Ti/Pt/Au was used as p-metal and Ni/AuGe/Ni/Au was employed as n-metal contact. The 3D schematic of the high speed InGaAs PD with ground-signal-ground (GSG) pads on silicon is shown in Fig. 2(b). The P pads metal were deposited on a 5 μm-thick cured polyimide layer to reduce parasitic capacitance.

InGaAs PD array with individual mesa diameter of 20, 30 and 40 μm were fabricated on both InP and Si substrate. A top-view microscope image of a fabricated 64-pixel InGaAs array on Si with 40 μm mesa diameter and 100 μm pitch is shown in Fig. 2(a). Common ground pads are located at the corner of the chip while individual P pads for each PD of array are routed to outside the photosensitive region. This configuration allows probing individual PD without disturbing the top illumination region Fabricated high speed InGaAs PDs are shown in Fig. 2(d) with various mesa diameters ranging from 10 to 40 μm and GSG pads for high speed measurement.

IV. Device Characterization

A. Dark Current

Fabricated devices were characterized at room temperature (∼22 °C) without cooling. The dark current at 1 V reverse bias was extracted for all 64 pixels of array with individual mesa diameter of 20 30 and 40 μm on both InP and Si. Statistics histogram for each data set are summarized in Fig. 3(a), (b) and (c). A normal distribution fitting was applied to each dataset

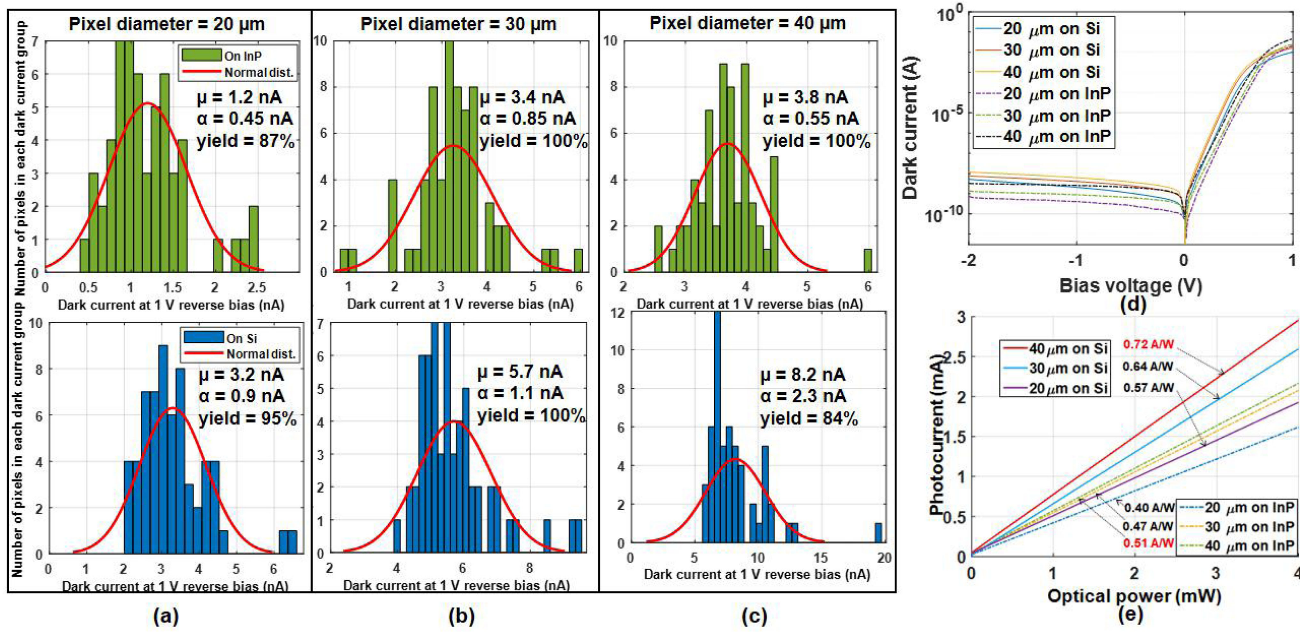

Fig. 3. Histogram plot of array on InP (left) and on Si (right) with pixel diameter of (a) 20 µm, (b) 30 µm, and (c) 40 µm. (d) IV characteristics. (e) Responsivity characteristics at 1550 nm at 1 V reverse bias.

with the distribution curve plotted in red. The mean value (µ), standard deviation (α), and yield are labeled in each figure. The dark current for the arrays on Si is generally higher than on InP. However, the general performance, distribution, and yield are fairly comparable. Fig. 3(d) shows the current-voltage (IV) characteristics for PDs with the lowest dark current on Si and InP substrates for etch mesa diameter. For the devices on Si, the corresponding dark current density at 1 V reverse bias for 20, 30 and 40 µm diameter devices are 0.69, 0.56 and 0.45 mA/cm^2, respectively. For devices on InP, those numbers are 0.13, 0.14 and 0.20 mA/cm^2, respectively. The dark current density is lower for PDs on InP substrate probably due to the fact that dry etch processes were not optimized for InP-on-Si pseudo template.

B. DC Responsivity

DC optical response of the InGaAs PD was characterized using an external 1550 nm laser. A cleaved single mode fiber (SMF) was used to couple laser light through the top of the mesa vertically. With the laser turned on, the photocurrent of PD was maximized by aligning the fiber facet to the mesa. After the coupling was optimized, photocurrent at several different input power levels was recorded. Linear interpolation was used to estimate the value of DC optical response with the results shown in Fig. 3(e). For PDs on Si, the typical responsibilities at 1550 nm are generally higher than those on InP substrate. The light reflection at the III-V/Si interface could contribute to the increasing responsibilities for devices on Si.

C. Imaging Characterization of PD Array on Si

The imaging performance of the 8 × 8 InGaAs PD array on Si was characterized by capturing the output beam of SMF. Array with an individual mesa diameter of 20 µm is used in this measurement. The experiment setup is shown in Fig. 4(a). A vertical cleaved facet SMF was fixed at around 4 mm above the array. The fiber was fed with a 1550 nm laser at an input power level of 0.25 mW. In order to plot the beam profile, the photo current of each PD of the array was automatically measured using a DC probe mounted on a programmable motorized linear stage. The measured photocurrent array was then normalized to the average dark current as an indicator of light intensity. As a result, each element of the array specifies photo intensity of one pixel within an 8 × 8 image representing the beam file of the SMF. The output beam of the SMF was captured by the InGaAs PD array on silicon as shown in Fig. 4(b). Grayscale color map is applied with intensity value for each pixel labeled. Malfunctioning pixels are labeled with "0" with the lowest intensity level. Image processing is used to enhance the low resolution raw image. Here, bi-cubic interpolation algorithm [35] is used to enlarge the raw image captured by the 8 × 8 InGaAs array on Si with the results shown in Fig. 4(c). The edge transition beam profile is smoother so that the beam profile can be easily identified. By swapping the InGaAs PD on Si array with a commercial SWIR camera, the beam profile of the SMF is captured at high resolution under identical conditions with the grayscale image shown in Fig. 4(d). A comparable beam file is shown in Fig. 4(c) and (d) indicating that the InGaAs PD array on Si has the potential to be used in SWIR imaging.

D. Radio Frequency Bandwidth

Radio frequency (RF) response was evaluated using a network analyzer with integrated laser source. The output 1550 nm laser from the network analyzer couples to the device through SMF. A high-speed microwave GSG probe was used to measure the

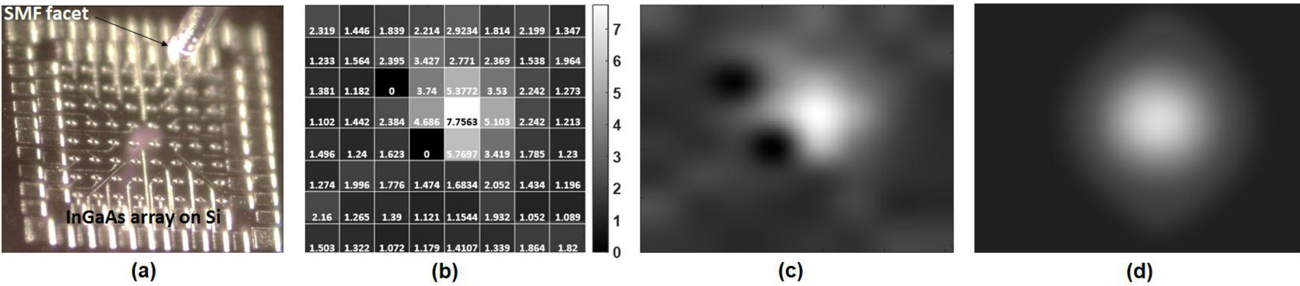

Fig. 4. (a) Experimental setup of SMF beam profile measurement. (b) Bit map plot of the beam profile of the SMF using 8 × 8 InGaAs PD array on Si with relative intensity value shown in etch pixel. (c) Enhanced image of the beam profile of the SMF based on low resolution image captured by InGaAs PD array on Si. (d) Beam profile of SMF measured with commercial SWIR camera.

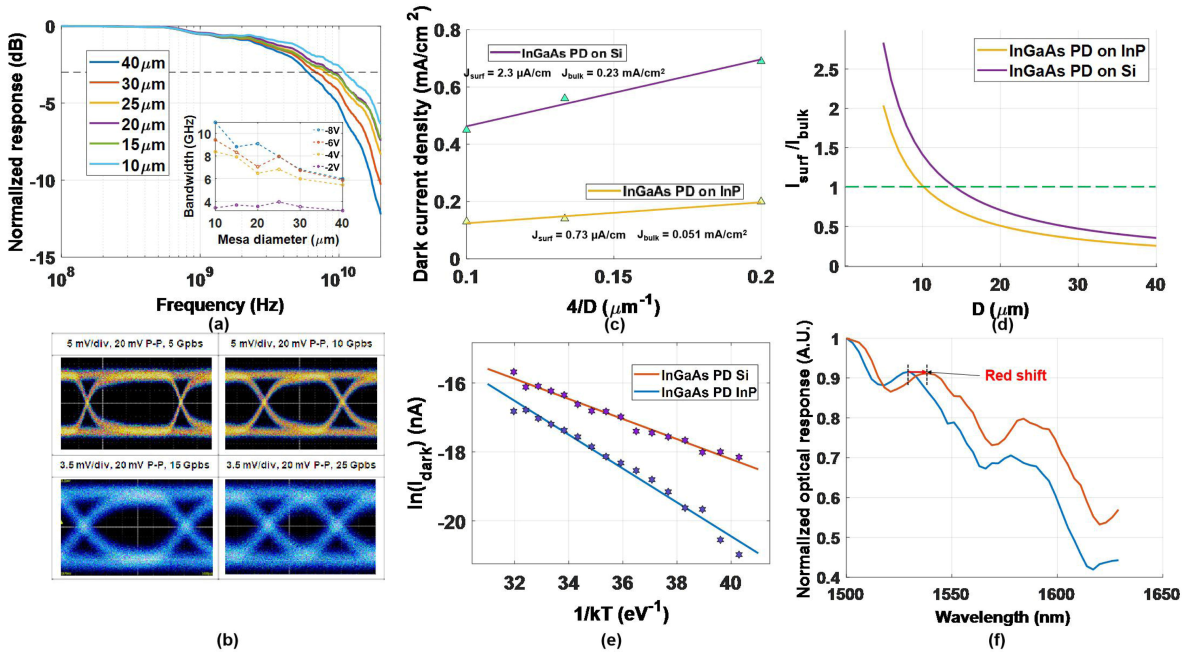

Fig. 5. (a) Measured RF frequency response at 8 V reverse bias. (b) Eye diagrams of high speed PD with mesa diameter of 15 μm at data rate ranging from 5 Gpbs to 25 Gbps. (c) J_{dark} versus 4/D characteristics of InGaAs PDs on both InP and Si substrate. (d) The ratio of I_{surf} to I_{bulk} versus mesa diameter. (e) The natural logarithm of dark current versus reciprocal of temperature and (f) normalized DC responsivity versus wavelength for PD on both InP and Si substrate with mesa diameter of 20 μm at 2 V reverse bias.

electrical output of the InGaAs photodetector. The RF response at 8 V reverse bias for photodetectors with different mesa diameters are reported in Fig. 5(a) and corresponding the DC dark current for device with mesa diameter of 10, 15, 20, 25, 30, 40 μm are 36, 41, 68, 76, 123 and 160 nA respectively. A 3-dB bandwidth of up to 11.2 GHz was measured for the InGaAs PD on silicon with a mesa diameter of 10 μm. The 3 dB bandwidth of the PDs on Si here is actually transit-time limited based on the fact that the InGaAs absorption layer is 1 um thick.

E. Optical Data Transmission

Non-return-to-zero eye patterns were measured to demonstrate the high-speed performance of the InGaAs on Si detector for optical data transmission. The RF signal from a pseudo-random bit sequence generator with $2^{31} - 1$ pattern length was used to modulate the 1550 nm single mode laser source through a $LiNbO_3$ modulator. The peak-to-peak (P-P) voltage of the RF signal applied on the modulator is 2 V with data rates ranging from 5 Gbps to 25 Gbps. The bias voltage and polarization are adjusted to maximize the optical power fed into the devices under test. The total optical power received at the detector was kept at around −3 dBm. As an example, the high speed eye diagrams of devices with mesa diameter of 15 μm with data rate from 5 to 25 Gpbs were reported in Fig. 5(b).

V. Discussion

A. Dark Current Analysis

By analyzing the total dark current density (J_{dark}) characteristics for PD with various mesa diameters (D), the J_{dark} of a InGaAs PD can be decomposed into bulk (J_{bulk}) and surface (J_{surf}) leakage components [35]. The total dark current of a PD (I_{dark}) can be expressed as $I_{\mathrm{dark}} = J_{\mathrm{bulk}} \cdot \pi D^2/4 + J_{\mathrm{surf}} \cdot \pi D$. By

dividing both sides of the equation by mesa area ($\pi D^2/4$), we can have $J_{dark} = J_{bulk} + 4 \cdot J_{surf}/D$ where J_{dark} is linearly related to $4/D$. The J_{dark} versus $4/D$ figures are shown in Fig. 5(c). The value of J_{bulk} and J_{surf} for both InGaAs PD on Si and InP are calculated by using linear interpolation. As a result, bulk dark current (I_{bulk}) and surface leakage dark current (I_{surf}) can be separately given with arbitrary mesa diameters.

To identify the dominant component of dark current, the ratio of I_{surf} to I_{bulk} is calculated for different mesa diameters for InGaAs PD on both InP and Si. The ratio versus diameter curves are shown Fig. 5(d). The ratio is generally higher for PDs on Si, indicating that it is more sensitive to surface leakage effect probably due the high dislocation density. For mesa diameter less than 10 μm, the radio is higher than 1 for both PDs on InP and Si, suggesting that the dark current density can be improved significantly by using planar device structure where surface leakage effect can be eliminated.

B. Activation and Band Gap Energy Analysis

Crystal defects create traps in the depletion region with energy levels between the valence band and the conduction band that can facilitate the formation of electron-hole pairs through indirect transition of an electron to the conduction band (or a hole to the valence band). As a result, carriers in traps would have to overcome a smaller energy barrier to become conductive. Therefore, smaller activation energies (ΔE_a) indicates larger crystal defects present within a particular device that leads to larger dark currents. It has been reported that the ΔE_a can be extracted from temperature dependent dark current measurement [37]. The ΔE_a can be calculated based on the Arrhenius plot shown in Fig. 5(e) where the dark current was measured from 15 to 90 °C with a diameter of 20 μm on both InP and Si at -2 V bias. The derived ΔE_a for InGaAs on InP and Si are 0.49 eV and 0.30 eV respectively. The normalized optical response versus wavelength plot for PDs on Si and InP shown in Fig. 5(f) also indicate that there is a minor red-shift of the InGaAs absorption spectrum on Si substrates. The red-shift emission of InGaAs absorption layer grown on InP-on-Si templates could be attributed to both the residual tensile stress inside the InP buffer (103% relaxed), and the slightly higher Indium composition of the InGaAs absorption layer ($In_{0.529}Ga_{0.471}As$ on native InP substrates vs. $In_{0.533}Ga_{0.467}As$ on InP-on-Si templates). The derived ΔE_a for InGaAs on Si is lower than InP may relate to the red-shift of the InGaAs absorption on Si and high TDD introduced by heteroepitaxy [38].

VI. Conclusion

In this work, top-illuminated InGaAs PDs on CMOS-compatible (001) Si have been demonstrated by direct heteroepitaxy. InGaAs absorption layers were grown on InP-on-Si templates with record low surface defect density by leveraging advanced growth technology including GoVS, TCA in the GaAs buffer and SLSs dislocation filters in both GaAs and InP buffers. Identical 8 × 8 InGaAs PD arrays with mesa diameters of 20, 30 and 40 μm and 100 μm pitch were fabricated and measured on both Si and InP substrates. A benchmark of PDs on Si by realized by heteroepitaxy in recently publication are shown in Table I. Our InGaAs PD on Si with 40 μm diameter demonstrates a dark current density of 0.45 mA/cm^2 with DC responsivity of 0.72 A/W at 1550 nm at 1 V reverse bias. For high speed InGaAs PDs on Si, a 3 dB RF bandwidth up to 11.2 GHz with mesa diameter of 10 μm and up to 25 Gbps eyes diagram were achieved.

TABLE I
Comparison InGaAs PDs on Si Substrates by Heteroepitaxy

Ref.	J_{dk} (mA·cm^{-2})	Responsivity(A/W)	BW(GHz)[a]
This work	0.45	0.72	6.8
[21]	0.8	0.79	9
[39]	40	0.6	15
[40]	64	0.5	10
[41]	625	0.22	9

[a] J_{dk} is dark current density; Responsivity refers to DC optical responsivity; BW refers to 3-dB RF bandwidth.

SWIR imaging experiment was also carried by using an 8 × 8 InGaAs PD array on Si with mesa diameter of 20 μm and 100 μm pitch. The output beam profile of a cleaved facet SMF was captured by the PD array on silicon. A 1550 nm laser with power level of 0.25 mW was connected to the SMF. Low resolution 8 × 8 grayscale intensity as well as enhanced beam profile image was generated. The beam profile was also captured by a commercial SWIR camera and matched to the one by InGaAs array on Si. The comparable beam profile demonstrates the SWIR imaging functionally of the InGaAs PD array on Si. Statistical measurements of dark current of 8 × 8 InGaAs PD arrays on both Si and InP shows the overall dark current distribution and yield are competitive for devices on Si and InP, indicating the potential for realizing advanced InGaAs detectors on Si substrates by heteroepitaxy.

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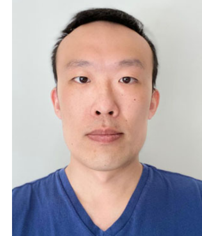

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