Engineering Breakdown Probability Profile for PDP and DCR Optimization in a SPAD Fabricated in a Standard 55 nm BCD Process

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Abstract—CMOS single-photon avalanche diodes (SPADs) have broken into the mainstream by enabling the adoption of imaging, timing, and security technologies in a variety of applications within the consumer, medical and industrial domains. The continued scaling of technology nodes creates many benefits but also obstacles for SPAD-based systems. Maintaining and/or improving upon the high-sensitivity, low-noise, and timing performance of demonstrated SPADs in custom technologies or well-established CMOS image sensor processes remains a challenge. In this paper, we present SPADs based on DPW/BNW junctions in a standard Bipolar-CMOS-DMOS (BCD) technology with results comparable to the state-of-the-art in terms of sensitivity and noise in a deep sub-micron process. Technology CAD (TCAD) simulations demonstrate the improved PDP with the simple addition of a single existing implant, which allows for an engineered performance without modifications to the process. The result is an 8.8 μm diameter SPAD exhibiting $\sim$2.6 cps/μm^2 DCR at 20 °C with 7 V excess bias. The improved structure obtains a PDP of 62% and $\sim$4.2% at 530 nm and 940 nm, respectively. Afterpulsing probability is $\sim$0.97% and the timing response is 52 ps FWHM when measured with integrated passive quench/active recharge circuitry at 3 V excess bias.

Index Terms—Single-photon avalanche diodes (SPADs), photon counting, depth-sensing, BCD, time-correlated single-photon counting(TCSPC), LIDAR, three-dimensional (3-D) ranging, FLIM, QRNG.

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I. INTRODUCTION

LARGE-FORMAT single-photon avalanche diode (SPAD) arrays [1]–[3] are becoming ubiquitous in the time-resolved imaging domain for their utility in applications such as fluorescence lifetime imaging microscopy (FLIM), LiDAR/Time-of-flight (ToF), and also emerging domains, such as quantum random number generation (QRNG). Technology scaling allows for an increased number of pixels, resulting in higher spatial resolution, more data, and further enabling the integration of complex logic functionality [4]. However, on the detector side, the higher relative doping levels, along with reduced annealing, cause a much higher order defect concentration in SPADs, which results in high noise and reduced sensitivity. The advent of 3D-stacking in IC design has provided a potential remedy, as a custom process for the detector can be bonded to a separate CMOS IC that contains the core circuitry [5]. These system-on-chip designs [6]–[12] provide a best-of-both-worlds outlet. However, this can result in high cost and additional design complexity. A good compromise between the benefits of older standard processes with reliable SPAD performance and the 3D approach is to develop high-performing SPADs in a standard deep sub-micron node.

In [13], the concept of exploiting the process flow and high power design aspects of smart power technologies, such as Bipolar-CMOS-DMOS (BCD), was demonstrated. In that work, SPADs with excellent performance in terms of timing and noise characteristics were experimentally verified in a 160 nm ST BCD technology. In this work, we push the bounds on scaling with SPAD designs by exploiting the highly commutable GF 55 nm BCDL process. Moreover, through analytical modeling and TCAD simulation of the implant concentration and depth, we iterate through two versions of the deep-junction SPAD by only adding already available masks in order to improve overall performance. This simple-to-understand approach, grounded in device physics, can be used by designers to improve sensitivity. Experimental validation of the devices shows comparable noise and sensitivity to the published state-of-the-art.

II. DESIGN BACKGROUND

A. Fundamentals of Deep-Junction SPADs

The fundamental operation of SPADs, process methods, and inherent design trade-offs are well described in the literature [14]–[16]. A general description of the operating behavior can be understood by analyzing the device cross-section, which consists of the neutral/quasi-neutral and multiplication (space charge) regions [17]. Furthermore, the relative geometries of these regions are used to distinguish between 'deep' and 'shallow' SPADs. While shallow junctions can be advantageous for their typically lower breakdown voltages, they suffer from lower photon detection probability (PDP), particularly at the longer wavelengths which are used for applications such as LiDAR. Moreover, detectors can be discriminated between whether they provide substrate isolation, which is desirable when integrating circuits on the same silicon.

For monolithic-based systems, i.e. where the SPADs and circuits co-exist on the same substrate, a way of isolating the circuits from the SPADs can be designed using 'deep' or 'buried' n-well layers [18]. The physical construction of this buried layer has direct consequences for the timing response. Considering the light absorption length of the silicon, the thickness of the n-well region contributes to the diffusion tail while the overall resistivity of the path to the cathode contact and avalanche spreading dynamics determines the full-width at half-maximum (FWHM) of the timing jitter [19], [20]. Furthermore, the buried n-well, which can be designed with retrograde doping, aids in the design of the multiplication and space-charge regions which is key for low-noise operation [21].

The PDP is defined by the product of the breakdown probability and quantum efficiency, as shown in (1).

$$\text{PDP}(\lambda) = P_b(\lambda) \cdot QE(\lambda) \qquad (1)$$

Quantum efficiency is a function of the surface transmission, relative depth, and width of the space charge region. In any given process, it may be difficult for a designer to improve the quantum efficiency of a SPAD structure, particularly for deep junctions, as it can substantially be limited by the capabilities of the foundry. Nevertheless, it is possible to improve PDP across the spectrum by engineering the photo-collector regions for higher breakdown probability [22].

Owing to the fact that electrons have higher ionization coefficients than holes for silicon, it is desirable to have electrons drift from the depletion region to the multiplication region [23]. The premier and intuitive step for enabling this principle is to bury the junction deep inside the silicon, allowing for the minority electrons to be swept into the high-electric field where an avalanche can be initiated. A well-established design technique allowing for practical realization of this deep junction is to implant high energy Boron ions, [13], [24], [15]. This ensures that low-energy red/NIR photons are detected with higher efficiency. However, while the junction depth plays an essential role in SPAD performance, small differences in the design of the quasi-neutral (photo-collector) region i.e. the net implant profile approaching the junction can produce considerably varied results in terms of PDP. In an ideal structure, a designer would engineer the net doping in order to fully deplete the depth range where photons are absorbed, allowing for the drift of generated charge carriers to the multiplication region. This increases the breakdown probability and allows for maximum PDP. However, in a standard process, there are only a limited, number of masks available, which create variations in net doping when combined. A method through which the effect these variations have on detection efficiency can be examined by observing the band diagram in a TCAD simulation and, by extension, simulation of the corresponding breakdown probability.

B. Device Physics and TCAD Simulation

The general structure of the proposed SPADs is shown in Fig. 1. The only difference between the variants is the additional p-well (PW) implant in SPAD2. Modelling of the junction in a single dimension enables quick evaluation of a SPADs detection efficiency [22], [25]. Oldham *et al.* described the voltage-dependent triggering probability with (2), (3) [23], where P_e and P_h are the probabilities that an electron and hole initiate an avalanche, respectively. The ionization coefficients are denoted by α and β, respectively.

$$\frac{dP_e}{dP_x} = -(1-P_e)\alpha(P_e + P_h - P_e \cdot P_h) \qquad (2)$$

$$\frac{dP_h}{dP_x} = (1-P_h)\beta(P_e + P_h - P_e \cdot P_h) \qquad (3)$$

McIntyre extended the analysis by formulating a history-dependent ionization coefficient [26]. In TCAD, the McIntyre model is used to simulate these quantities along with the band diagram and doping profile.

The relative concentration of majority carriers (holes) in two demonstrated deep SPADs for a section close to the surface, which corresponds to the transition from the P+ to PW implants, is plotted in Fig. 2 with the corresponding conduction band diagram illustrated by Fig. 3. It can be seen that for SPAD2, the hole concentration monotonically decreases towards the junction after a certain depth (highlighted by point A) while there is a region of increased concentration in SPAD1. The increase in holes is a result of the net concentration caused by the profile from all the implants used. We note that this depth range of interest (A-B), is outside the high-field multiplication region, which can be observed in Fig. 4(a) and Fig. 4(b). There are multiple analytical manifestations that can help elucidate the consequence of this doping variation. From the energy band diagram in Fig. 3, there is an evident barrier created, which inhibits electron diffusion towards the multiplication region caused by photons absorbed close to the surface. This is in contrast to SPAD2, where the effective photo-collector region becomes much wider, enabling the photo-generated electrons in the charge-neutral region to transit to the multiplication region. The result is a greatly improved breakdown probability. In simulation, the combined breakdown probability of holes and electrons confirms this principle with the results displayed in Fig. 4(c). Carriers that are injected into SPAD2 possess a higher probability of igniting an avalanche breakdown within a wider range of depths, which corresponds to a wider spectral response.

(a) SPAD1.

(b) SPAD2.

Fig. 1.   Cross-sections of proposed 55 nm BCD SPADs. A single implant (PW) highlights the difference between structures.
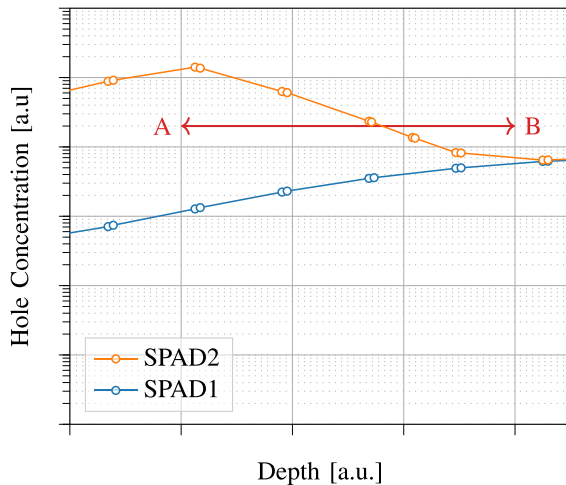

Fig. 2.   Doping comparison showing decrease of hole concentration for SPAD2 in contrast with increase shown for SPAD1 level. Net relative doping levels after all implants are placed is displayed at 5 V_{EX}.
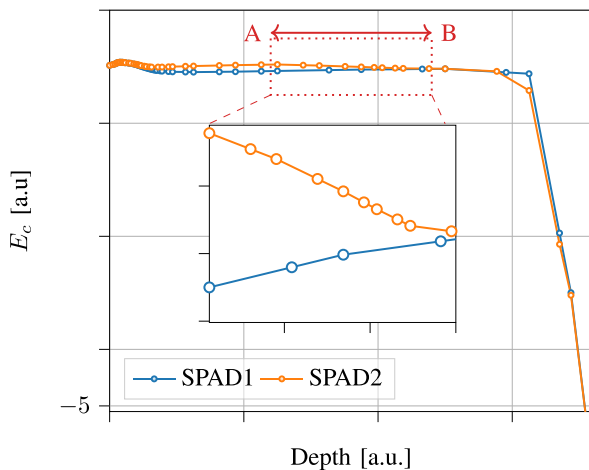

Fig. 3.   Simulated conduction band diagram of SPADs. Inset illustrates the drift barrier resulting from the net concentration difference between the proposed SPADs.

It is clearly shown by simulation that the space charge regions and electric field magnitude of the two devices are nearly identical in the multiplication region. Therefore, it is reasonable to conclude that differences in measured PDP would, to a great extent, arise from the doping variation in the photo-collector region.

III. MEASUREMENT RESULTS

A. I-V Characteristics

The diode I-V curves were measured using the Keysight B1500 A semiconductor analyzer with the resulting dark currents and breakdown voltages ($\sim$32 V) matching well the simulation carried out in TCAD and are displayed in Fig. 5. It is clearly shown that SPAD2 achieves higher photo-current near the breakdown voltage, as predicted by TCAD. Light emission testing was performed as an initial qualitative measure to ensure the absence of edge breakdown from either of the two devices. Micrographs of SPAD1 and SPAD2 along with the LET image showing good uniformity around an active diameter of $\sim$ 4.4 μm are shown in Fig. 6.

B. Photon Detection Probability

PDP measurement results for the two proposed SPADs at excess bias voltages of 1-7 V are displayed in Fig. 7(a) and Fig. 7(b). These measurements were taken at room temperature with 10 nm intervals using the continuous light technique [27]. In our setup, a monochromator and integrating sphere are used to select a temporally coherent and uniform spatial distribution. A reference photodiode (PD) (Hamamatsu s2281) along with the device under test (DUT) are placed at a calibrated distance from the light output. The output is monitored with a universal counter (Keysight 53230 A) and by an oscilloscope to verify the proper response of the SPAD.

A distinct performance difference, as initially postulated by simulation, is outlined by the overall improved sensitivity of SPAD2 along with the very low detection efficiency of blue wavelength photons in SPAD1, which has a peak PDP of 26% (580 nm). Conversely, SPAD2 is capable of an enhanced performance of 62% (530 nm) at 7 V excess bias and maintains >19% PDP up to 800 nm.

A more direct comparison of the relationship between the two SPADs' performance across excess bias and wavelength can be drawn by observing Fig. 8(a) and Fig. 8(b), which show the results of the devices on the same plot for sample excess biases and wavelengths. These graphs clearly illustrate how the performance of the two SPADs trends towards similarity at longer wavelengths, as lower energy photons, which are absorbed deeper inside the silicon, ignite avalanches with a similar probability. The standing wave pattern across the visible spectrum is a result of a non-optimized optical stack designed on top of the silicon.

(a) Space charge illustrating nearly identical multiplication regions.

(b) Electric field magnitude, $|E|$, showing depth range of interest is outside the multiplication region.

(c) Simulated breakdown probability for each SPAD which culminates in the dramatic difference in performance between the two devices.
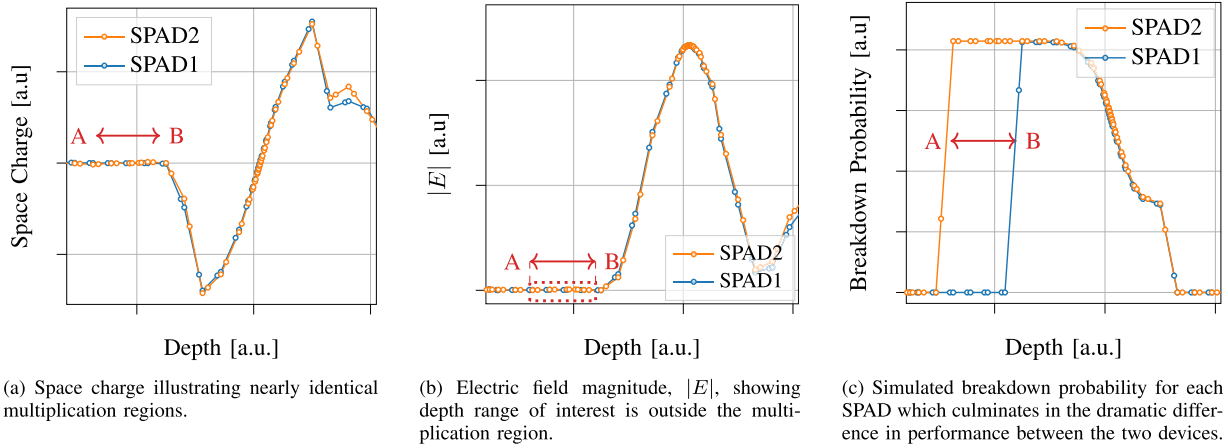
Fig. 4. Comparison between the simulated junction parameters of SPAD1 and SPAD2 at breakdown. Space charge and E-field highlight nearly-identical junction parameters. Normalized values are shown at 5 V_{EX}.
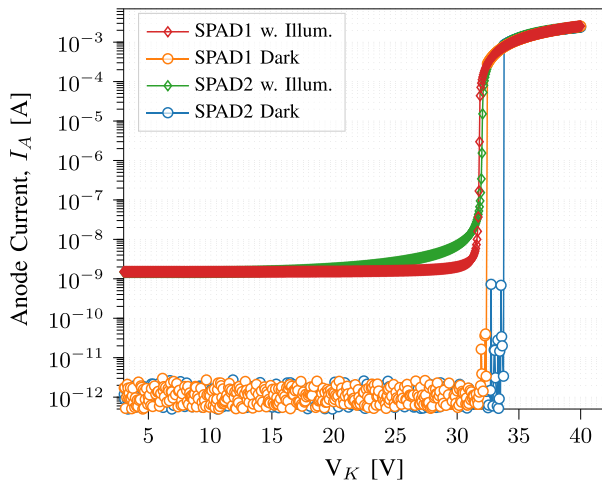

Fig. 5. I-V curves for proposed SPADs in dark and illuminated conditions at room temperature.
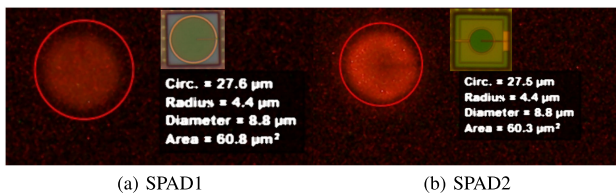

(a) SPAD1   (b) SPAD2

Fig. 6. Light emission test images with micrographs of SPAD1 (left) and SPAD2 (right) taken at V_{EX} = 3 V.

C. Noise Performance

1) DCR: The noise of a single-photon avalanche diode is characterized by its primary and secondary pulses, which combined constitute the dark count rate (DCR) in the absence of impinging photons. Thermally generated carriers and band-to-band tunneling are the main contributors to primary pulses. When there is either an initiated avalanche or thermal generation, carriers become trapped in 'deep' levels caused by defects in the silicon process. The release of and subsequent avalanche caused by these carriers are the secondary pulses known as afterpulses.

An oscilloscope (Teledyne LeCroy WaveMaster 813 Zi-B) was used to analyze the DCR. The median result for both SPADs across 10 dies at an excess bias voltage range of 1-7 V are plotted in Fig. 9. The SPAD2 results demonstrate ~1 cps/μm^2 at 4 V excess bias and ~2.6 cps/μm^2 at 7 V excess bias. As both SPADs show relatively low DCR, the remainder of the focus was the characterization of SPAD2 because of its superior PDP. Measurements were taken for a single SPAD2 die from -60 °C to 60 °C and the results are displayed in Fig. 10. The data demonstrates excellent performance even at high temperature and excess bias with a value of <10 kcps at @ 60 °C and V_{EX} = 7 V. Trap-assisted thermal generation is the main source of noise, as the DCR shows a strong temperature dependence.

2) Afterpulsing: Characterization of the afterpulsing for silicon SPADs is typically conducted by histogramming the inter-arrival time between dark counts, although it can also be indirectly obtained by estimating the lifetime and density of traps using the time-correlated carriers counting (TCCC) technique [28], which is typically more useful for III-V SPADs where the afterpulsing probability can be relatively high.

The inter-arrival histogramming technique was employed using a passive quench active recharge (PQAR) circuit, similar in design to the work presented in [29], [30], which is integrated on the same die at 3 V $_{EX}$ and 50% level of the signal swing, and is displayed in Fig. 11. The excess bias is limited to 3 V by the chosen high-voltage transistor inside of the pixel circuit. In this setup, the dead time at the 50% level was ~4.5 ns. Data are binned at 200 ns intervals, with a total of ~10.6 million counts observed. The multi-exponential behavior arising from afterpulsing is typically fitted using 3 deep-level traps [31]. The afterpulsing probability is calculated by fitting the arrival data points after 10 μ s, which typically exceeds the maximum trap lifetime in silicon [31], and then dividing the secondary pulses (above the fit) by the primary pulse count (below the fit). The calculated afterpulsing probability is ~0.97%. This low afterpulsing probability is consistent with the overall low DCR rate, suggesting that there is a relatively low defect concentration.
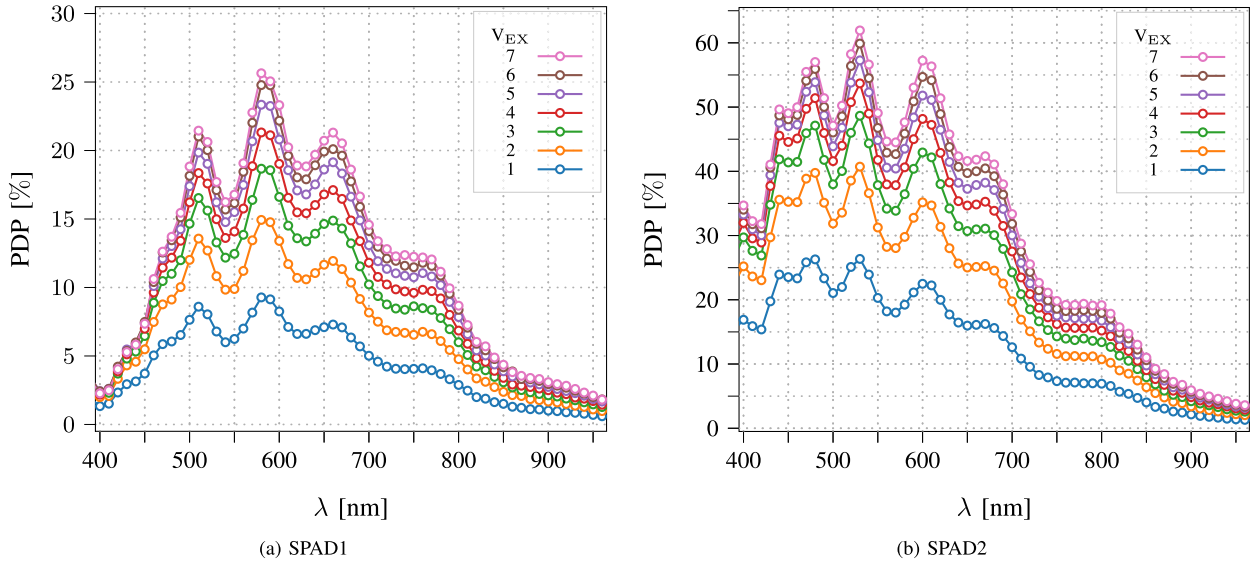
(a) SPAD1

(b) SPAD2

Fig. 7. PDP measurements for several excess bias voltages, measured with a 220 kΩ ballast resistor at 20 °C for both SPAD designs presented in this work.

(a) Measurements at 1, 4, 7 V excess biases.
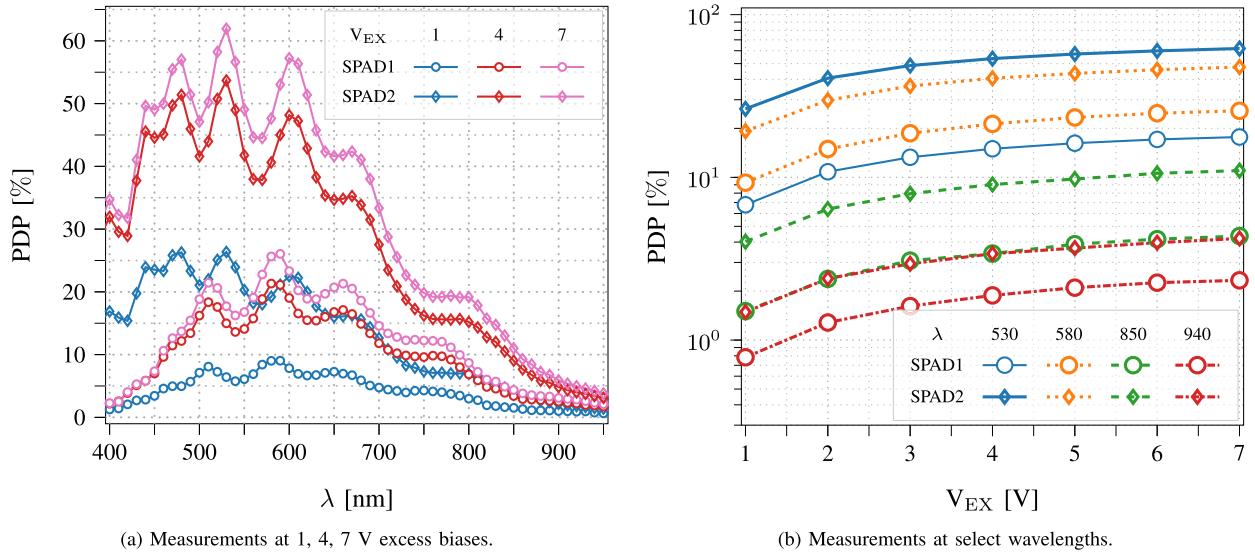

(b) Measurements at select wavelengths.

Fig. 8. PDP comparison between the two proposed SPADs highlighting variation across wavelength and excess bias.
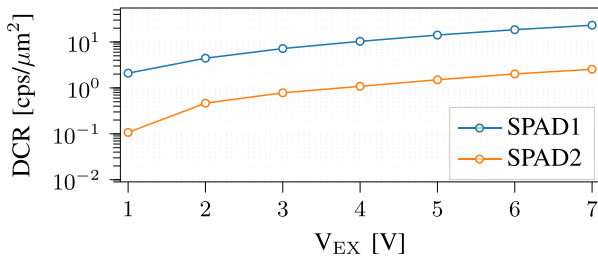

Fig. 9. Normalized DCR comparison at room temperature across excess bias values. Median value shown for 10 dies of each SPAD.

Assuming that thermal generation is the main component of DCR, activation energies can be extracted from their temperature dependence [32]. In our case, this is a justified premise because of the low relative doping of the deep junction, which results in a lower electric field at the breakdown (<1 MV/cm) along with the strong dependence of the DCR on temperature previously outlined in Fig. 10. The Arrhenius plot is shown in Fig. 12. At high temperature and low excess bias, where SRH effects are more dominant, this qualitative analysis is used to extract the activation energies of traps. The 0.46 eV value displayed at 1 V_{EX} can likely be explained by phosphorus-vacancy defects [33], with the change in slope illustrating how at higher excess bias the tunneling effects become more prevalent.

D. Timing Jitter

The timing performance of SPADs can be a critical parameter for applications requiring precise sensing. The results for the jitter of SPAD2 are displayed in Fig. 13. The time-correlated single-photon counting (TCSPC) acquisition technique was utilized to obtain data using the same oscilloscope used for the afterpulsing measurement, operating as a time-to-digital

(a) Sweep of temperature from -60 to 60 °C.

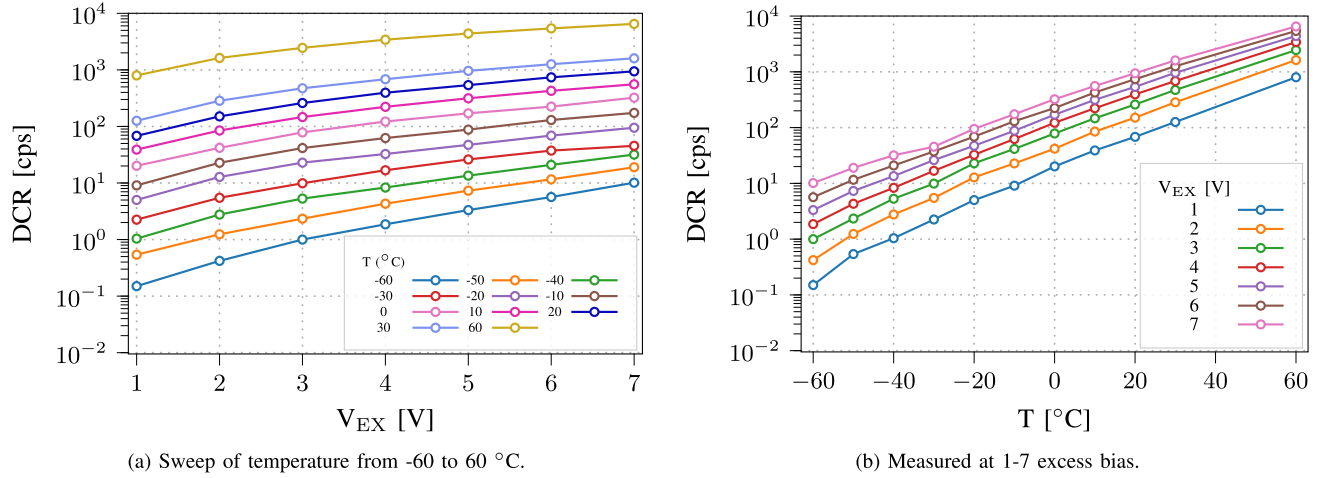(b) Measured at 1-7 excess bias.

Fig. 10. Temperature dependence of DCR for a single randomly selected SPAD2 die illustrating strong temperature dependence of DCR.
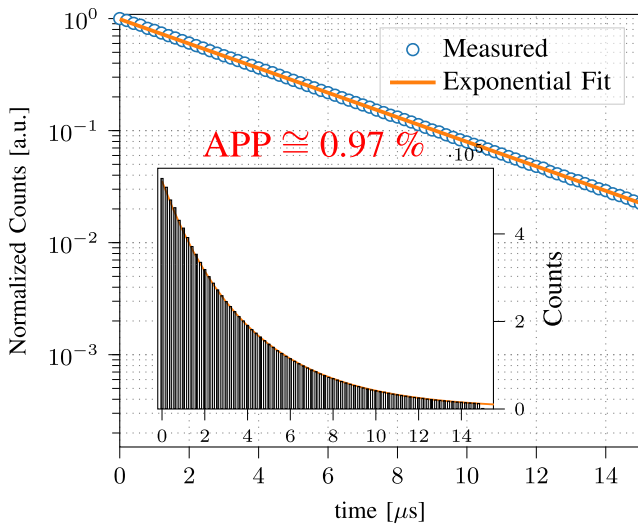

Fig. 11. Inter-arrival histogram of SPAD2 with fitted exponential measured at 50% level and room temperature at 3 V excess bias with integrated PQAR circuit and a dead time of ∼4.5 ns.
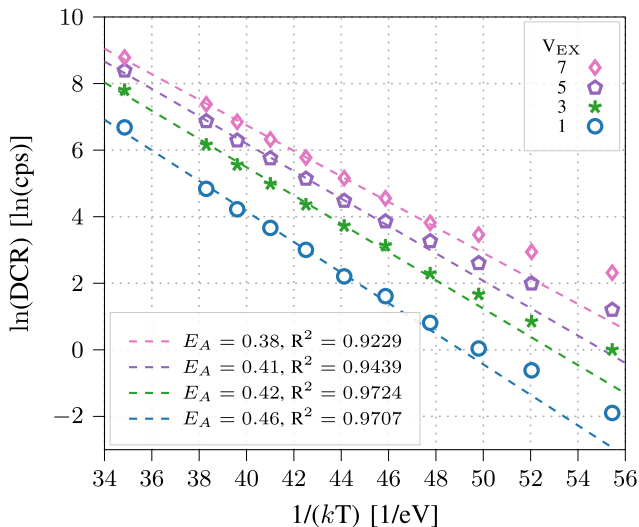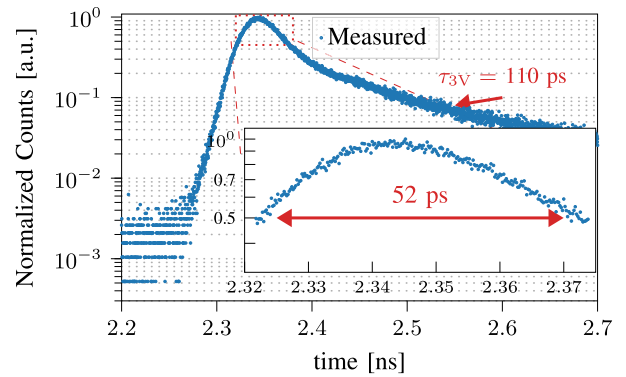

Fig. 13. Jitter measurement of SPAD2 performed with a 780 nm pulsed laser. FWHM is 52 ps and a diffusion tail time constant of 110 ps at $V_{EX} = 3$ V using integrated PQAR circuitry.

converter (TDC). The setup used for characterization is analogous to the one reported in [30]. A 1560 nm laser (NKT Onefive ORIGAMI-08) with second harmonic generation was used to output pulses at a wavelength of 780 nm containing a pulse-width of 150 fs pulsed at a repetition rate of 50 MHz. A 45 GHz optical receiver was inserted as a trigger on the 1560 nm branch. Moreover, neutral density filters were placed for attenuating the light intensity in order to avoid pile-up and ensure operation in the single-photon detection regime. Utilizing the same PQAR circuitry at 3 V_{EX} we achieved a full width at half-maximum of 52 ps, which is commensurate to other CMOS SPADs in the literature that performed this measurement using integrated pixel circuits. The exponential time constant of the diffusion tail is 110 ps. Further improvements by adding active quench/recharge circuitry and optimizing the measurement setup are ongoing.

IV. DISCUSSION AND COMPARISON WITH THE STATE-OF-THE-ART

A summary table outlining the relevant front-side illuminated (FSI) SPADs demonstrated in literature is shown in Table I. The literature is organized in chronological order to achieve a visualization of the advancements over the course of time. In

Fig. 12. Arrhenius plot of the DCR for SPAD2 at the excess bias voltages of 1, 3, 5, and 7 V.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TO FSI STATE-OF-THE-ART

Reference		Year	Tech. [nm]	Junc.	Guard Ring	Active Diam. [μ]	V_{EX} / V_{BD} [V]	Peak PDP [%] @λ [nm]	PDP [%] @940 [nm]	DCR / area [cps / μm^2]^{a,f}	DCR @V_{EX}^{f} [V]	AP [%]	Jitter [ps]	Jitter λ[nm]	Jitter V_{EX} [V]
Niclass et al.	[34]	2007	130	p+/n	pw	10	1-2.7 /10	31-41 @450	1	1300	100k @1.7	N.A.	144	637	1.7
Gersbach et al.	[35]	2008	130	p+/nw	STI^m	8.6	1-2 /9	18-30 @480	2	1.5k - 11.5k	670k @2	<1^g	125	637	1
Richardson et al.	[36]	2009	130	pw/ DNW	N.A.^{c}	8	0.6-1.4 /14	18-28 @500	2	0.24 - 0.6	30 @1.4	0.02^h	200	815	N.A
Richardson et al.^{y}	[15]	2011	130	pw/ DNW^v p+/nw	N.A.^{c}	8^x	0.2-1.2 /12-18	18-33 @450-560	2-3	0.5-0.97	40-47 @0.8	0.02^i	183 - 237	470	1.2
Webster et al.	[37]	2012	90	DNW/ p-epi^k	N.A.^{c}	6.4	2.46 /14.9	44 @690	12	∼ 4.6	∼150 @1	0.38^l	51	470	2.46
Webster et al.	[38]	2012	130	p-epi^k	N.A.^{c}	8	2-12 /20	72 @560	12	0.36	18.0 @2	<4	60	654	12
Leitner et al.	[39]	2013	180	p+/nw	N.A.^{c}	10	1-3.3 /21	35-47 @450	N.A.	0.3-1.8	∼180 @4	N.A.	N.A.	N.A.	N.A.
Charbon et al.	[40]	2013	65	n+/pw	nw	8	0.05-0.4 /9	2-5.5 @420	0.2	340-15.6k	105 @.05	1^n	235	637	0.4
Villa et al.	[41]	2014	350	p+/nw	pw	10-500	2-6 /25	37-55 @420	2	0.05	1.0 @4	1°	56-4470	780	6
Veerappan et al.	[18]	2014	180	p+/nw	pw	12	2-10 /23.5	24-48 @480	N.A.	0.16-12.8	20 @2	0.03-0.3^p	86	637	10
Lee et al.	[42]	2015	140^d	p+/nw	pw	12	0.5-3 /11	10-25 @500	1-3	0.9-244	30k @3	1.7^p	65	405	3
Veerappan et al.	[43]	2015	180	p+/nw	pw	12	1-4 /14	23-47 @480	N.A.	16	2k @4	0.2^q	95	405	4
Veerappan et al.	[24]	2016	180	p-epi/ DNW	N.A.^{c}	12	1-12 /25	18-47 @520	N.A.	1.5	200 @11	7.2^q	97	637	11
Takai et al.	[44]	2016	180	n/p^r	N.A.^{c}	16	1.5-5 /20.5	62 @210	8	0.5	100 @5	0.35	161	635	5
Pellegrini et al.	[45]	2017	130	pw/ DNW	N.A.^{c}	8	0.5 /14.2	43 @480	1.4	1.6	80 @0.5	0.08	100	N.A.	2.4
Xu et al.	[46]	2017	150	p+/nw	N.A.^{c}	10	5 / 18.0	31 @450	2	0.4	200 @5	0.85	42	831	4
Pellegrini et al.	[47]	2017	40	pw/ DNW	N.A.^{c}	N.A.	1.0 /15.5	45^s @500	3	N.A.	50 @1.0	0.1	140	850	1
Sanzaro et al.^{y}	[13]	2018	160^e	p+/n p/ DNW	N.A.^{c}	10-80	3-9/ 25-36	58-71 @450-490	3	0.1-0.2	100 @5	0.02-1.59	28-41	820	5
This Work (SPAD2)		-	55^e	DPW/ BNW	N.A.^{c}	8.8	1-7/ 31.5	26-62 @530	4.2	0.1-2.6	6.1-156 @1-7	∼0.97^t	52	780	3

^{a}Taken at max excess bias if not range of excess bias values not specified. ^{c}Virtual guard ring structure. ^{d}Silicon-on-insulator. ^{e}BCD. ^{f}At 20 °C. ^{g}180 ns dead time. ^{h}200 ns dead time. ^{i}50 ns dead time. ^{k}Not substrate isolated. ^{l}15 ns dead time. ^{m}Shallow trench isolation with passivation implants to create p-type glove structure. ^{n}At 1 μs dead time. ^{o}30 μm diameter. ^{p}200 ns dead time. ^{q}300 ns dead time. ^{r}Surface-isolated n-spad/p-spad junction. ^{s}With microlens. ^{t}4.5 ns dead time with 50% level @ 3 V $_{EX}$. ^{v}Two different deep structures presented one with an epi layer and one with a pw implant. ^{x}Multiple diameters demonstrated. ^{y}3 SPAD structures proposed.

general, the research and development focus has been to try and achieve improved PDP and lower noise while experimenting with a number of junction and guard ring structures. Although it can be difficult to draw a direct comparison, given that there are many figures of merit and technologies, some key conclusions can be drawn from this work.

It can be seen that there have been few published designs in process nodes lower than 100 nm. Industrial SPADs in a 40 nm process have been developed [47], although with lower PDP than this work. SPADs in a standard 28 nm FDSOI [48], were presented recently, however, the results do not achieve comparable levels of performance to those displayed by Table I. Our SPADs demonstrate the highest peak sensitivity and lowest noise for SPADs in an advanced technology (<65 nm). A visual comparison of the DCR and PDP for relevant works is depicted in Fig. 14. Finally, a key exposition from our work was that performance could be dramatically improved with only a single additional implant close to the surface of the SPAD. TCAD was used to explain the reasoning behind this, and the principle was then subsequently validated in silicon.
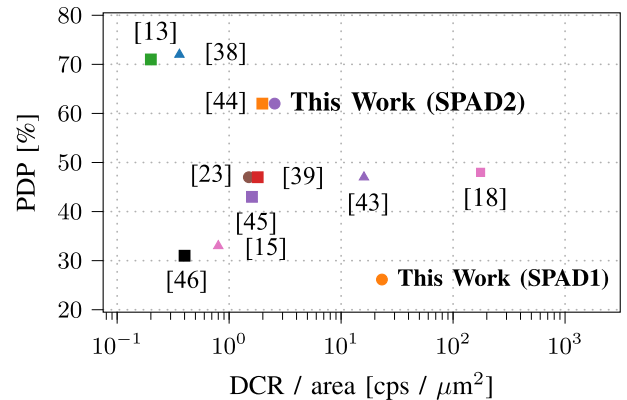

Fig. 14. State-of-the-art comparison of noise and sensitivity performance. DCR taken at max excess bias reported.

Engineering of the dopant profiles, improving the optical stack, and the addition of circuitry are our main focus going forward, which is required to improve performance. Overall, the excellent figures achieved in our work demonstrate the

possibility of designing high-performance SPAD-based systems in a modern MPW technology without the need for 3D-stacking.

V. Conclusion

This work has reported SPADs in a 55 nm process which demonstrates comparable noise and sensitivity characteristics to the state-of-the-art. The SPAD photocollector region was optimized with the addition of a single implant, resulting in greatly improved performance. Furthermore, these SPADs are highly amenable to the design of fully integrated SPAD-based system-on-chips in a standard process.

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