The AIM Photonics MPW: A Highly Accessible Cutting Edge Technology for Rapid Prototyping of Photonic Integrated Circuits

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***Abstract*—Silicon photonics has been heralded for a number of high technology fields, but access to a high quality technology has been limited to vertically integrated design/fabrication companies, or fabless companies with significant resources to engage high volume fabs. More recently, research and development hubs have developed and released process design kits and multi-project wafer programs to lower the barrier. We present the first silicon photonics multi-project wafer (MPW) service produced in a state-of-the-art 300 mm fabrication facility. The MPW service is enabled by a best-in-class process design kit (PDK) which allows designers to layout and obtain photonic integrated circuits (PICs) that work properly on the first run. The fabrication of these circuits is carried out at the SUNY Polytechnic Institute which operates a world class 300 mm cleanroom that, besides silicon photonics, develops sub-7 nm CMOS architectures. The industrial-level management of this facility and its equipment provides high quality photonic devices which are repeatable from run-to-run along with rapid turnaround time. The devices that are available to designers via the process design kit are produced by Analog Photonics and have been verified on actual runs. The performance of these devices is comparable to the state-of-the-art and enables a wide variety of silicon photonic applications.**

***Index Terms*—Photonic integrated circuits, silicon photonics, foundries.**

I. Introduction

OVER the past twenty years the popularity of silicon photonic integrated circuits (PICs) has increased as their reported performance improves. This popularity is partially driven due to the potential cost benefits that silicon-based PICs possess over alternative material platforms (ie, III-V). Specifically, PICs fabricated using a silicon-based platform are able to take advantage of the unsurpassed infrastructure of silicon-based electronic integrated circuits (ICs). In many cases the same fabrication facilities ("fabs"), process equipment ("tools"), chemicals, materials, and supply chains that have been established for high volume silicon ICs can be applied towards PICs [2]. In addition, the raw material cost of a silicon wafer is significantly less than GaAs or InP wafers that are used for III-V PICs. With an established infrastructure and a lower starting cost, silicon-based PICs are therefore an attractive platform for commercialization.

Silicon PICs have been produced in volume primarily for the telecommunications and data center communications markets. These products are fabricated by large commercial silicon foundries which require large manufacturing agreements in order to justify the process development and fab time [3], [4]. Telecom/Datacom applications are able to clear this hurdle while most of the early-stage applications of silicon photonics (free space communications, LiDAR, biological/chemical sensing, quantum computing, etc.) are limited by this high barrier to entry [5].

Instead, researchers or start-up companies in these application spaces must work in smaller scale fabs which may not be able to take advantage of the economies of scale a high-volume silicon fab has. Bridging the gap between closed high volume fabs and smaller boutique fabs (or academic labs) are larger research and development consortia such as IMEC, CEA-Leti, AMR, and (in the United States) the American Institute for Manufacturing Integrated Photonics (AIM Photonics) at the SUNY Polytechnic Institute [6]. Each of these organizations operate a multi-project wafer (MPW) service which allows small to medium sized businesses, academic researchers, and government labs to access the silicon photonics integrated circuits by sharing the development and fabrication costs in their state-of-the-art cleanroom facilities [7].

II. Foundry Model

A. AIM Photonics

Established in 2015 as the American Institute for Manufacturing Integrated Photonics, "AIM Photonics" is an Institute for Manufacturing Innovation funded by the US federal government, some state governments, and member companies [8]. The mission of AIM Photonics is in part to "advance integrated photonic circuit manufacturing technology development while

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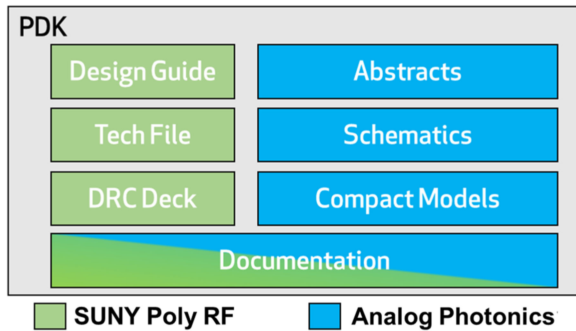

Fig. 1. Components of the APSUNY process design kit.

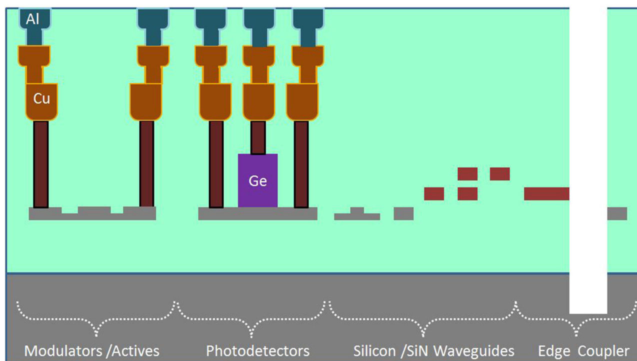

Fig. 2. Schematic cross section of the SUNY Poly/AIM Photonics MPW technology. On the left are the active devices in silicon connected to the copper BEOL. On the right are the different passive waveguiding layers that are available to designers.

simultaneously providing access to state-of-the-art fabrication, packaging, and testing capabilities." Besides the signature MPW program, AIM also funds various research and development projects at member universities across the country, and is bringing online a first of its kind photonics test, assembly and packaging (TAP) facility in Rochester, NY. AIM Photonics' MPW service and TAP facility are the only ones in the world to run on advanced tooling for 300 mm wafers.

B. Process Design Kit

The AIM Photonics MPW program fabricated at the SUNY Polytechnic Institute (SUNY-Poly) is enabled by an extensive process design kit (PDK) [8], [9] produced by Analog Photonics (Boston, MA). Analog Photonics (AP) draws upon years of experience with the SUNY-Poly fab and silicon photonics technology to provide devices that have been verified on wafers. The organization of the APSUNY PDK is shown in Fig. 1. The information provided by SUNY-Poly includes design guide, technology file, and design rule check (DRC) deck which will provide sufficient information about the foundry process to design, layout, and tapeout. The design guide includes mask layer names, types (negative or positive), opacities, thicknesses, purposes, stress gradients, and tolerances. The technology file provides the layer map that transfers the design intent layers to fabrication ready layer numbers and shows interactions between these layers. This layermap is used to convert the designs to a graphic database system (GDSII) or OASIS file formats that are recognized by the design rule check (DRC) deck. After passing the DRC, designs will be ready to submit to SUNY-Poly for mask generation. This submission process is typical referred as the tapeout.

Although primitive elements are sufficient for a custom design tapeout, a fully functional design requires expertise in process, design, test, and layout. Therefore, a photonic design typically takes multiple fabrication runs (iterations) to meet certain specifications, which increases the cost of development and slows down the development of a product. The added cost and development time can lead to a loss of competitive advantages that came with the custom design. Instead, a PDK component library aided design is preferred to accurately predict PIC behavior and iterate at a rapid pace, which reduces the risk and time to market. In addition, the overall cost of licensing a component library can be less than the custom development of those components. The PDK component library, shown in Fig. 1, typically includes the abstracts, schematics, and compact models. The abstracts allow the PDK developer to obstruct parts of true geometries that contain design IP while enabling the user to interact with the designated optical and electrical ports of components. The abstracts are then replaced with true geometries for fabrication ready files at a broker or foundry. The schematics and compact models of these components are used to predict the performance of the design, including the custom designed elements. The current APSUNY PDK component library provides state-of-the-art verifiable performance and high yield, and includes documentations of both primitive elements and component library. These documentations guide and inform the designers about PDK hierarchy, changes, design methodologies, supported EPDA tools, component library performances, application notes, and instructions (installation, licensing, and tapeout of the PDK).

At present, passive devices in the APSUNY PDK include vertical and edge couplers, splitters, crossings, directional couplers, interlayer transitions (silicon to silicon nitride waveguides), and polarization rotators/splitters.

Highlights of the active device library include high speed switches, microdisk modulators, Mach-Zehnder modulators and photodetectors. The PDK is divided into elements designed for O-band or C- and L- band applications, supporting both digital and analog circuit architectures. The APSUNY PDK is designed for the MPW program, and therefore provides support for a wide range of applications that use the program. To that end, new devices are constantly being developed and implemented to extend the PDK/MPW's use beyond Datacom/Telecom and into applications such as RF, 5G, bio/chem sensors, quantum computing, LiDAR, and more.

C. MPW Service

Fabrication runs of the AIM Photonics MPW are aggregated by The MOSIS Service (Marina del Rey, CA) which also hosts and distributes the PDK, and runs the final design rule check

(DRC). Customer designs are due to MOSIS in advance of the fabrication run to allow time for the fab to review DRC results, for MOSIS to insert IP blocks from the PDK component library and assemble the designs, and for the mask house to fabricate the reticles. These processes take approximately 30–40 days depending on issues found during DRC that might require redesign.

Once masks arrive at the fab and wafers start in the line the fabrication process takes approximately 90 days to manufacture a full wafer. After fabrication each wafer undergoes final quality assurance inspections and testing. The wafer is then diced and the chips are distributed to individual riders. This work takes approximately 3-4 weeks which brings the turnaround time for the active silicon photonics MPW run to 150 days from design drop to delivered chips.

III. Fabrication

The AIM Photonics MPW Service operates within the advanced 300 mm research and development fab located at the SUNY Polytechnic Institute. The fab at SUNY-Poly is a state-of-the-art 300 mm facility that is also used to develop sub-7 nm advanced CMOS nodes, and therefore the tools and processes are very precisely controlled. The operational infrastructure at SUNY Poly is more similar to an industrial fab than a typical academic user facility. These benefits allow for this program to achieve fast turnaround time and stable device performance.

Commercially available, photonics grade 220 nm silicon-on-insulator (SOI) wafers are used with a thick buried oxide to isolate the photonics devices from the substrate silicon. The SOI is patterned with multiple masks to create thinned silicon and to define full thickness silicon. Industry standard 193 nm immersion lithography is used to define the silicon patterns on the wafer with critical dimension control down to 100 nm and negligible interlevel misalignment. Advanced reactive ion etching (RIE) is used to obtain nearly vertical sidewalls and post etch chemical treatments produce sidewalls that are ultra-smooth. The patterned silicon enables the APSUNY PDK's silicon waveguides, couplers, and various other passive elements. In addition, the silicon levels form the basis for the active components. The patterned silicon is buried with a low loss dielectric cladding material, such as plasma-enhanced tetraethyl orthosilicate (pTEOS). Specifically, a non-conformal deposition is used to minimize pinch-off of the dielectric which can lead to defects. Two low-loss silicon nitride (SiN) waveguide levels are available for use by designers and are fabricated similar to the silicon waveguide. Notably, a unique low temperature plasma enhanced chemical vapor deposition (PECVD) SiN is used in order to enable co-integrate SiN waveguides with active components. As with the silicon waveguide, the RIE patterning and post etch treatment have been optimized to yield low loss waveguides that are then cladded with pTEOS.

Riders have access to six standardized ion implantation design levels–three each for N-type and P-type implants. These implants enable the APSUNY PDK's filters, switches, phase shifters, modulators, and detectors as well as allow advanced designers to create their own devices using the six design levels, if desired.

The PDK offers different types of photodetectors depending on the designer's application. All are based on p-i-n Ge diodes that are fabricated in photolithographically defined trenches in the pTEOS. The germanium is grown via CVD with specially tuned growth rates and temperatures to minimize defects in the material. The Ge is then planarized, capped and the top contact area is defined. The contact to the Ge is made from CMOS-compatible materials that are specifically chosen for optimal detector performance. Another contact is made to the various active components using a deep via etched to the implanted silicon. After the two contact levels are finished, standard Cu-based CMOS back-end-of-the-line (BEOL) processing is carried out. The first metal routing level is single damascene in nature, while the next two metal levels include vias with dual damascene processing. The final metal level is finished with aluminum to allow for wire bonding. The final process module is a deep trench to facilitate low-loss edge coupling. After the deep trench, the wafers are sent to an external vendor for dicing, and the individual chips are shipped to riders for testing.

The AIM Photonics MPW service is able to take advantage of the advanced semiconductor fabrication facility at SUNY-Poly which includes tool, process, and product controls. Each tool in the fab is subjected to regular monitoring ("quals") for physical contamination (foreign material) or chemical contamination (via trace X-ray fluorescence, or TXRF, measurements). In addition, each tool's critical processes are measured on a regular basis to ensure the equipment is operating properly. For example, a dielectric deposition tool would have multiple representative films monitored for thickness, refractive index, stress, and uniformity, while a lithography tool's critical dimension (CD), across wafer variability, and interlayer misalignment (or overlay) would also be monitored. Tools that fail these cleanliness or process quals are proactively made unavailable for use until they successfully pass all the appropriate checks. Furthermore, full process flow wafers are fabricated on a rolling basis in order to preemptively identify any issues with process integration or any unique processes that might not be discovered by the tool quals. Finally, all of the data collected from these measurements and monitors are processed and scrutinized with statistical process control (SPC) which allows the engineering staff to identify and remedy potential issues before they impact wafer yield or device performance.

On top of the tool, process, line, and integration controls and monitors described above, every MPW wafer is tested and inspected multiple times during the fabrication process for added quality control. Electrical testing is done at each metal level to measure standard CMOS-related parametrics and to confirm basic behavior of the active photonics components. AIM Photonics has also sponsored, installed, and implemented an inline electro/optical prober which is used to measure key passive and active photonic device performance. Both the standard electrical testing and the electro/optical testing results are used for wafer acceptance decisions. Finally, at critical steps, including at the

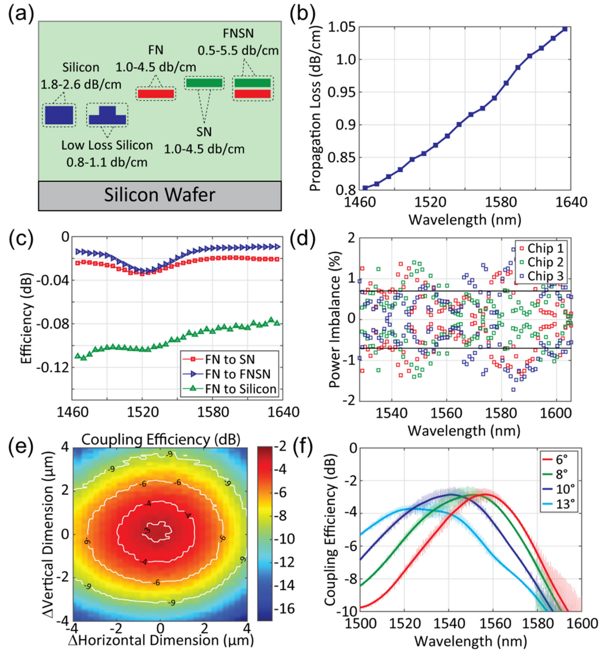

Fig. 3. (a) Waveguide types and propagation losses. (b) Propagation loss of the low-loss silicon waveguide. (c) Layer transition efficiencies. (d) Power imbalance of the SiN 3-port splitter. (e) SMF-28e fiber to TE edge couplers coupling efficiency and alignment tolerance. (f) SMF-28e fiber to TE vertical coupler efficiency and angle dependence.

end of the fabrication flow, both manual and automated inspections are used to check for random defects as well as assess wafer quality. Wafers that do not pass the wafer acceptance criteria are not used to ship to riders, and any die that has unacceptable defect sizes or counts are excluded from the dicing plan.

IV. Results

A. Passive Library Highlights

The passive components in current APSUNY PDK include waveguides, edge couplers, vertical couplers, 1% and 10% power taps, 3-and 4-port splitters, layer transitions (escalators), polarization rotators, polarization splitter/rotators, and waveguide crossings. The use of both silicon and silicon nitride waveguides is unique to this PDK and essential for supporting low PIC-to-fiber coupling losses, low propagation losses at diverse operation wavelengths, tight bend radii, low polarization dependence, and active functionality for applications ranging from optical computing and interconnect, to sensors and nonlinear optics (Fig. 3(a)). In addition to the standard silicon and silicon nitride waveguides, a low-loss silicon waveguide is also provided with a propagation loss of 0.8–1.05 dB/cm over a wavelength range of 1460 to 1640 nm (Fig. 3(b)). The propagation loss is limited by roughness at the edges of the waveguide. The increased waveguide loss at longer wavelengths agrees well with increased interaction with waveguide edges. The transition between these waveguide layers is supported with escalators that have <0.1 dB/transition losses over a broad wavelength range (Fig. 3(c)).

The splitting ratio between the output ports of optical splitters is key to maximize the extinction ratio in a Mach-Zehnder interferometer or the common mode rejection ratio in a balanced photodetector. APSUNY PDK offers silicon and silicon nitride splitters with a small power imbalance between the two outputs. For instance, the power imbalance of the silicon nitride 3-port splitter has a standard deviation of ∼0.7% (Fig. 3(d)).

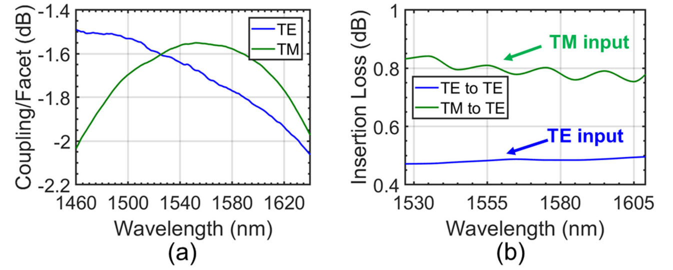

Fig. 4. (a) Efficiency of TE/TM edge coupler. Device loss of (b) polarization splitter/rotator.

To facilitate PIC packaging, TE edge couplers are provided to couple TE polarized light from a standard SMF-28e fiber with a loss of ∼2.5 dB/facet. These devices have a 3 dB alignment tolerance of 6.2 μm and 4.6 μm in the horizontal and vertical directions, respectively (Fig. 3(e)). The large alignment tolerance offers compatibility with standard pick-and-place tools.

A part from an edge coupling solution, TE vertical couplers are also supported with a peak coupling efficiency of ∼2.8 dB/facet to an SMF-28e fiber at $\lambda \sim 1550$ nm with a 1 dB bandwidth of $\Delta\lambda \sim 30$ nm (Fig. 3(f)). The vertical coupler is optimized to at 8° launch angle and works at peak efficiency in a ±2° around this design point. When the launch angle is 13°, the peak efficiency is reduced by 1 dB due to non-optimized up down emission rate for this launch angle. However, TE-only couplers can require costly polarization-maintaining (PM) fibers and are not compatible with communication standards that require dual polarizations or applications that favor TM polarization. A TE/TM compatible edge coupler is supplied to couple light from a 3.5 μm mode-field diameter lensed fiber with a loss of ∼1.8 dB/facet (Fig. 4(a)). Moreover, a polarization splitter/rotator (Fig. 4(b)) is offered with low polarization dependent loss (<0.45 dB) and low insertion losses (∼0.2–0.9 dB) to enable on-chip polarization manipulation. This functionality is a unique PDK offering.

B. Wavelength-Selective Library Highlights

The wavelength-selective components in APSUNY PDK include 4-channel tunable and resonant wavelength division multiplexed microdisk switches, microdisk modulators, and microring filters that share the same free-spectral-range (FSR) of ∼26 nm over the C-band and contain integrated heaters to compensate for fabrication variations. The resonance of the tunable microdisk switch can be rapidly detuned by applying 1 V (1 mW) across the embedded forward-biased p-i-n junction. This detuning switches the optical routing from the through to the drop port with 1.0 dB insertion loss and 16 dB dynamic extinction ratio at a nano-second scale switching speed (Fig. 5(a)). The tunable microring filter has an insertion loss of <0.2 dB and can be tuned using an integrated heater with a tuning efficiency of 1 nm/mW (7.5 μW/GHz) (Fig. 5(b)).

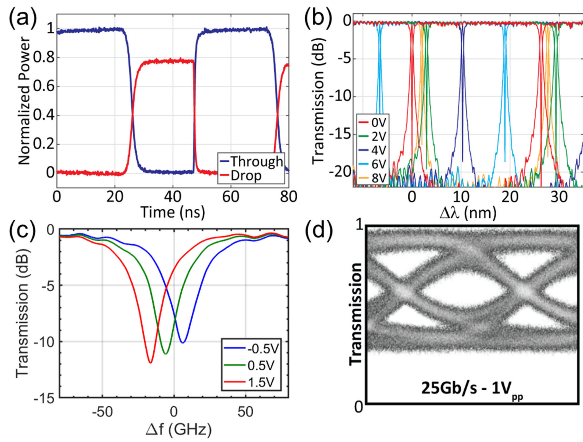

Fig. 5. (a) The tunable microdisk switch dynamic drop and through port response, showing nano-second scale switching times. (b) The microring filter tunes across its FSR of 26 nm. (c) Transmission spectra of microdisk modulator under different bias voltage. (d) 25 Gb/s transmission eye diagram from the microdisk modulators.

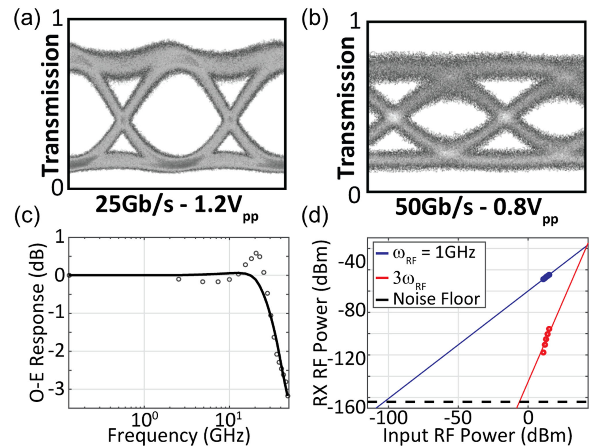

Fig. 6. (a) 25 Gb/s and (b) 50 Gb/s transmission eye diagrams from the digital MZM. (c) Optical-electrical response of the digital germanium photodetector with a 50 GHz bandwidth. (d) The dynamic range and linearity measurement of the analog MZM.

The microdisk modulator has an integrated reverse-biased p-n junction for electro-optical modulation. The current device can be detuned with an efficiency of 8 GHz/V and is capable of transmitting 25 Gb/s non-return-to-zero (NRZ) data with >4 dB dynamic extinction ratio and <0.1 dB insertion loss using only a 1 V_{pp} drive (Fig. 5(d)). Broadband Library Highlights

C. Broadband Library Highlights

In APSUNY PDK, there are also other key active components such as broadband thermo-optic switches and phase shifters, analog and digital Mach-Zehnder modulators (MZM), and photodetectors. These components offer high yields and large tolerance to fabrication variations. The digital MZM has a 1mm long reverse-biased p-n junction for electro-optical modulation and a thermo-optic phase shifter for adjusting the operation point, for example to quadrature. The electro-optic effect is also referred as plasma-dispersion effect [10], [11]. The device is characterized to have an optical loss of 2.7 dB and a $V_\pi L$ of 0.8 Vcm at -1 V bias and can transmit 25 Gb/s (50 Gb/s) NRZ data with 7.2 dB (6 dB) dynamic extinction ratio and 1.0 dB (1.4 dB) additional insertion loss using only 1.2 V_{pp} (0.8 V_{pp}) differential dual drive (i.e., 0.6 V_{pp} (0.4 V_{pp}) per MZ arm), as shown in Fig. 5(a) and (b). The digital photodetector uses a vertical p-i-n junction within the germanium layer for photocurrent generation. At -1 V bias, the detector offers >1 A/W responsivity at 1550 nm and ~50 GHz optical-electrical bandwidth (Fig. 6(c)). The analog MZM has a reverse-biased p-i-n junction designed to offer a linear electro-optic response, as is shown to have a spurious free dynamic range of >90 dB/Hz$^{2/3}$ (Fig. 6(d)). The analog photodetector increases the total absorption area to minimize saturation and nonlinear effects that also have a spurious free dynamic range of >90 dB/Hz$^{2/3}$.

D. Library Maturity

In addition to the die-level tested performance, the PDK components were also verified in wafer-scale and across multiple fabrication runs [32]. The wavelength distribution of the

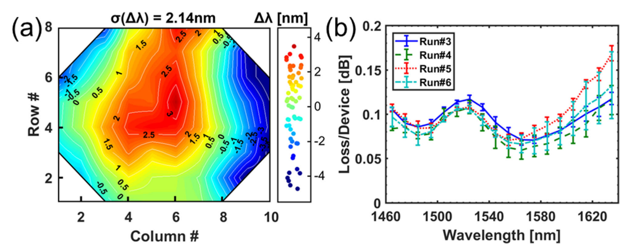

Fig. 7. (a) Wavelength variations of the PDK microdisk modulator across the 300 mm wafer, showing a wavelength standard deviation of 2.14 nm. (b) Transmission loss of the PDK SiN 3-port splitter over multiple MPW runs. Multiple dies were measured for each run.

PDK microdisk modulator across the whole wafer is shown in Fig. 7(a). The standard deviation of the peak wavelength due to across wafer fabrication variability is 2.14 nm, which can be easily compensated by the integrated heater within the component. The transmission loss of the SiN 3-port splitter over multiple dies across several MPW runs are shown in Fig. 7(b), demonstrating a repeatable low-loss performance and a reliable and high-yield fabrication process of SUNY-Poly.

The APSUNY PDK is continuing its evolving path, adding O-band support [32] to complement the verified C and L band silicon photonics library that provides state-of-the-art, repeatable performance and enables a wide range of applications using AIM MPW runs with CMOS-compatible voltages. Continued semi-annual updates will improve component performances and offer verified sub-system performance to further reduce the product time to market.

V. Conclusion

The AIM Photonics institute has assembled a state-of-the-art multi project wafer (MPW) service through the 300 mm fabrication facility at the SUNY Polytechnic Institute and enabled by the Process Design Kit developed by Analog Photonics. Here we have presented the fabrication process flow and the APSUNY PDK. Within the PDK is a comprehensive active and passive silicon photonics library that provides verified state-of-the-art

performances and enables a wide range of silicon photonics applications with CMOS compatible voltages. With the help of the mature PDK and its integrated electronics-photonics design automation software support, the process of designing a photonic system is further simplified and the number of design rule violations is greatly reduced, which reduces the time cost on both designers and fabrication facilities. Future PDK updates will focus on further improving component performances and offering verified sub-system performance to further reduce time to market.

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