Scalable Microring-Based Silicon Clos Switch Fabric With Switch-and-Select Stages

Qixiang Cheng , *Member, IEEE*, Meisam Bahadori , Yu-Han Hung, Yishen Huang, Nathan Abrams, and Keren Bergman , *Fellow, IEEE*

(Invited Paper)

Abstract—We propose and analyze a scalable microring-based Clos switch fabric architecture constructed with switch-and-select switching stages. A silicon 4×4 building block that was designed and fabricated through American Institute for Manufacturing Integrated Photonics is used for the proof-of-principle demonstration of a 16×16 Clos switch fabric. By fully blocking the first-order crosstalk, the 4×4 device is measured to show a crosstalk ratio in the range of –57 to –48.5 dB, enabling better than –39 dB crosstalk for the 16×16 switch. Our study shows that the three-stage Clos design enables up to a factor of 4 in the reduction of the number of switching cells compared to single-stage switch-and-select fabrics. We further explore the design space for both first-order and second-order switching elements using the foundry-validated parameters and how these factors impact the performance and scalability of the three-stage Clos switch. A detailed power penalty map is drawn for Clos switch fabrics with various scales, which reveals that the ultimate key limiting factor is the shuffle insertion loss. An optimized 32-port Clos switch fabric using foundry-enabled parameters is shown to have a less than 10-dB power penalty.

Index Terms—Optical switches, switch architectures, photonic integrated circuits, silicon photonics, microring resonators.

I. INTRODUCTION

PHOTONIC switch fabrics are emerging as a key technology for enabling direct optical connectivity toward addressing the growing interconnection performance requirements in datacenter architectures [1]. Optical switching technologies can be generally divided into two categories: free-space optics and integrated optics. Free-space optical switches have been realized by a number of competing technologies, such as microelectromechanical systems (MEMS) [2], beam-steering [3], and liquid crystal on silicon (LCOS) [4]. Free-space optics represents the most mature and commercial technologies; however, their rigorous calibration and installation of discrete components introduce significant complexity that is ultimately reflected in

the cost per port. To ensure low cost for eventual datacenter adoption, lithography-based high-level integration technologies are favored [5]. While initial demonstrations included silica platform [6], indium phosphide and silicon based integrations are more widely explored [7]–[11]. In particular, silicon photonic switch fabrics can offer further benefits of small footprint, energy efficiency, and CMOS manufacturing compatibility.

The last decade has witnessed significant advancement in silicon photonic switch fabrics with tens of port counts being monolithically integrated [5], [10], [11]. The primary switching cells that are explored are Mach-Zehnder interferometers (MZIs) [10], MEMS-actuated couplers [11], and microring resonators (MRRs) [9]. While the resonant devices have shown great potential for ultra-compact and energy-efficient applications [12], [13], they have not yet been scaled to high-port count for optical switch fabrics. The wavelength-selective nature of the MRR unit requires wavelength alignment across the switching circuit, for which various schemes for fast and efficient wavelength locking have been demonstrated [14]–[16]. Higher-order MRR elements enable broadened passband, relaxing the wavelength registration requirement [9], but at the cost of higher insertion loss and fabrication complexity. To date, MRR-based optical switch fabrics tend to employ crossbar-based topologies, with the port count of up to 8×7 [9]. Other notable demonstrations include the hitless design [17] and the recent Omega switch with dual-ring crosspoints [18]. In addition to the insertion loss, the first-order crosstalk significantly deteriorates the signal quality that compromises the link budget. We recently demonstrated a monolithic Si/SiN MRR-based switch circuit in the switch-and-select topology, cancelling the first-order crosstalk [19]. Integrating a multi-layer passive shuffle offers a promising approach to low insertion loss, but the scale of $2 N^2$ switching cells for an $N \times N$ network becomes prohibitive and managing the $N^2 \times N^2$ perfect shuffle is increasingly difficult at high port counts. In this paper, we propose and analyze an MRR-based Clos switch fabric architecture constructed with switch-and-select stages. This design keeps the number of stages to the modest value of *three* while significantly reducing the required number of switching elements, and inheriting the immunity to first-order crosstalk from the switch-and-select stages. A silicon 4×4 building block was designed and fabricated using standard process design kit (PDK) elements through the American Institute for Manufacturing Integrated Photonics (AIM Photonics) multi-project wafer (MPW)

TABLE I
NOTABLE DEMONSTRATIONS OF MICRORING-BASED SILICON OPTICAL SWITCH FABRICS

Port Count	Architecture	Elementary switching cell	On-chip loss [dB]	Crosstalk [dB]	Optical power penalty [dB]	Group
4×4	Hitless router	1st-order MRR	-	>20*	-	N. Sherwood-Droz1 *et al*, 2008 [17]
5×5	Bidirectional optical router	1st-order MRR	~8	>16*	< 1.75 @12.5 Gb/s	R. Ji *et al*, 2011 [21]
8×7	Crossbar	5th-order MRR	2 to 10	19.5 to 23.4*	< 1 @10 & 40 Gb/s	P. DasMahapatra *et al*, 2014 [9]
8×8	N-stage planar	1st-order dual MRR[1]	~4	<-10	-	G. Fan *et al*, 2017 [22]
8×8	Crossbar	2nd-order MRR	>5	>-20	-	A. Khope *et al*, 2017 [23]
4×4	Benes	2nd-order MRR	≤6.9	<-13.6	-	Q. Zhu *et al*, 2018 [24]
4×4	Switch-and-select[2]	1st-order MRR	>1.8	-51.4 to -31.6	-1 @ 12.5 Gb/s	Q. Cheng *et al*, 2019 [25]
8×4	Crossbar	2nd-order MRR	6 to 14	<-32	0.2 @ 40Gb/s	A. Khope *et al*, 2019 [26]
8×8	Omega	1st-order dual MRR	4.4 to 8.4	-18.8 to -14.7	< 2.5 @12.5 Gb/s	Y. Huang *et al*, 2019 [18]

*Extinction ratio reported instead of crosstalk ratio.
[1] Passive wavelength router without on-chip phase shifters.
[2] The device implemented in a Si/SiN two-layered structure.

run. This device is characterized to extract key parameters for evaluating the insertion loss, aggregated crosstalk, scalability and power consumption of the Clos design.

The paper is structured as follows. We review the state-of-the-art of MRR-based optical switch fabrics in Section II. The design and architectural evaluation of the proposed Clos switch fabric constructed with switch-and-select stages is described in Section III. The design and characterization of the silicon 4×4 switch building block is presented in Section IV, along with the performance emulation of the 16×16 Clos switch fabric. In Section V, we explore the design space for microring switching cells and discuss how their parameters impact the performance and scalability of a three-stage Clos switch fabric. Finally, conclusions are drawn in Section VI.

II. STATE-OF-THE-ART OF MICRORING-BASED SILICON OPTICAL SWITCH FABRICS

The highly advanced CMOS industry, with mature fabrication and manufacturing infrastructures as well as advances in silicon photonic manufacturing capabilities, has triggered considerable development in silicon photonic switch fabrics. The first demonstration of a μm-scale silicon ring resonator by Xu *et al.* stimulated the research of MRR-based photonic integrated circuits [20]. There have been a number of demonstrations of microring-based optical switch fabrics, scaling from 2 to 8 ports [9], [17], [18], [21]–[26]. Table I summarises notable demonstrations of microring-based optical switching circuits chronologically. Key metrics, such as port count, insertion loss, crosstalk, and optical power penalty are highlighted and compared. This type of switch tends to utilize the MRR element as a 1×2 spatial add-drop unit assembled in certain topologies, such as the hitless [17] and five-port [21] routers, the crossbar switches [9], [23], [26], and the Omega switch with dual-ring intersections [18]. In these configurations, while each 1×2 elementary cell is only

traversed by one signal, the crosstalk leakage gets aggregated with adjacent channels. This situation is referred as the first-order crosstalk and generally imposes stringent requirements on the design of the elementary switch units for an $N \times N$ network. Even for these reported MRR switch fabrics of modest scales, the crosstalk ratios are too high to be applied in a practical system [5].

It would therefore be beneficial to obtain lower crosstalk by topological modification to cancel the first-order crosstalk, such as in the dilated approach [27]. Special attention should also be paid to the number of stages in such a multistage network, which correlates to the aggregated crosstalk ratio as well as switch insertion loss. We proposed a modified switch-and-select architecture using microring resonators [19]. The $1 \times N/N \times 1$ switching units are replaced by an array of MRR add-drop filters assembled in a 1-D bus structure acting as spatial (de)multiplexers. This design effectively maintains the number of resonating rings in any path at two, while the two-stage configuration fully blocks the first-order crosstalk by dropping the crosstalk leakage at the output stage. For such an $N \times N$ switch fabric with large port counts, the number of required MRR switching cells ($2 N^2$) and the management of the central $N^2 \times N^2$ perfect shuffle stand out as two key challenges. Though a multi-layer platform can be leveraged [19], the footprint and complexity of such an $N^2 \times N^2$ shuffle increases exponentially.

In this work, we propose a microring-based Clos switch fabric architecture constructed with switch-and-select switching stages. This design allows for the construction of large-scale MRR-based switch fabrics while maintaining low crosstalk and low loss. The bounded number of required MRR switching cells is significantly reduced while the number of stages is kept at a modest value of three. A 4×4 silicon building block is designed, fabricated and characterized to verify the 16×16 Clos switch performance, along with a detailed design space exploration.
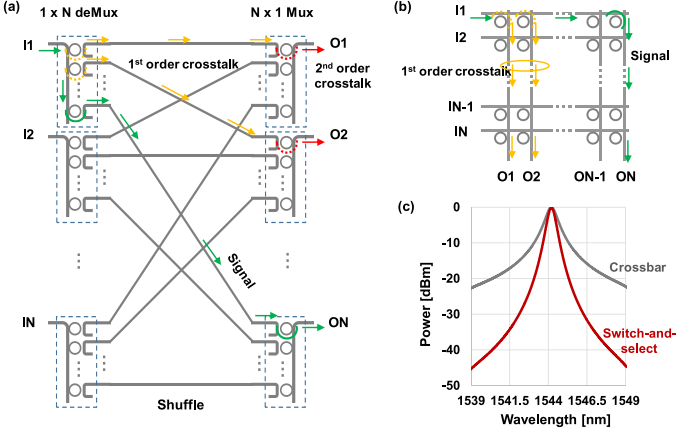
Fig. 1 (a) Schematic of the microring-based switch-and-select topology. Signal (green lines) routes from input 1 to output N. (b) Schematic of the microring-based crossbar topology. Signal (green lines) routes from input 1 to output N. (c) Comparison of simulated drop spectrum of a crossbar switching device and the switch-and-select structure.

III. MICRORING-BASED CLOS SWITCH ARCHITECTURE

In this section, we propose and analyse the Microring-based Clos switch architecture with microring-based switch-and-select stages.

A. Microring-Based Switch-and-Select Building Block

The microring-based switch-and-select architecture is shown in Fig. 1(a). An $N \times N$ device comprises two linear arrays of $1 \times N/N \times 1$ spatial (de)multiplexers, connected by a perfect shuffle network, with a total of $2 N^2$ MRR switching cells. This architecture provides strictly non-blocking connectivity as each pair of input and output switching arrays dedicates a specific path. The design also significantly reduces the scaling overhead in loss, since the scale-up of such a design only requires adding bypass rings in the linear switching arrays. The first order crosstalk leakage (outlined by yellow arrows) from the input switching arrays will get dropped by the off-resonance microrings at the output stage; hence only *second-order crosstalk* occurs (represented by red arrows), as illustrated in Fig. 1(a). By contrast, the crossbar topology suffers from the *first-order crosstalk*, as shown in Fig. 1(b), though a smaller number of switching cells are required (N^2). Fig. 1(c) compares the simulated drop spectrum of a crossbar switching device, and the switch-and-select structure. The latter exhibits a much sharper spectral edge due to the cascading of two add-drop elements.

B. Clos Switch Design and Topological Evaluation

The Clos architecture is a three stage network that was first studied by Clos in the early 1950s [28]. The Clos topology is attractive since fewer switching cells are required leading to a reduction in cost. While the center stages can be replaced by smaller size Clos networks recursively, trading off more stages, such as the Beneš with $n = m = 2$, the three-stage implementation offers a suitable balance between the number of stages and the number of switching cells [29]. Fig. 2(a) shows a generic Clos
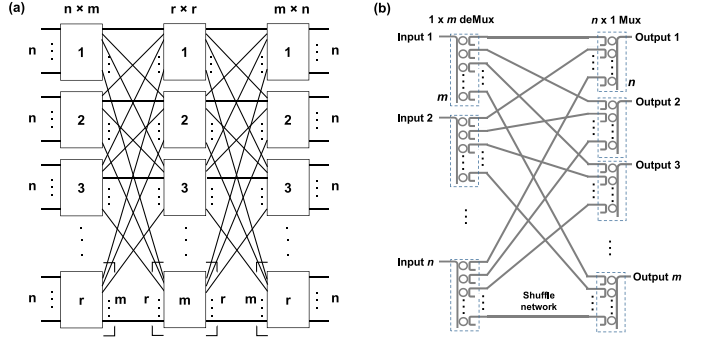

Fig. 2. (a) Layout of a generic three-stage Clos network building from $r \, n \times m$, $m \, r \times r$, and $r \, m \times n$ blocks. (b) Schematic of an $n \times m$ microring-based block in the switch-and-select topology.

network, comprised of $r \, n \times m$, $m \, r \times r$, and $r \, m \times n$ blocks, in the first, second and third stage, respectively. The microring-based switch-and-select topology offers great flexibility in defining $n \times m$ connectivity by applying $n \, 1 \times m$ spatial de-multiplexer arrays and $m \, n \times 1$ spatial multiplexer arrays, as shown in Fig. 2(b), with a total of $2n \times m$ microrings. The worst-case crosstalk is given by:

$$C = X + 10 log_{10} \left(n + r + m - 3 \right) \tag{1}$$

where X represents the second-order crosstalk ratio of the switch blocks.

The blocking properties of the Clos switch fabric architecture can be described by the following equations [28]:

$$m \geq (2n - 1) \tag{2}$$

$$m \geq n \tag{3}$$

Equations 2 and 3 define strictly non-blocking (SNB) and rearrangeably non-blocking connectivity (RNB) architectures, respectively. To minimize the redundancy in connections, which translates to number of required microrings, $m = (2n-1)$ and $m = n$ are chosen for SNB and RNB Clos networks, respectively. As $r = N/n$, the number of required switching cells is thus given by:

$$SC\left(SNB\right) = 4\left(2n - 1\right)N + 2\left(\frac{2}{n} - \frac{1}{n^2}\right)N^2 \tag{4}$$

$$SC\left(RNB\right) = 4nN + \frac{2}{n}N^2 \tag{5}$$

where N is the switch port count. We then define α as the ratio between the number of switching elements in the Clos design and the single-stage switch-and-select ($2 N^2$):

$$\alpha\left(SNB\right) = \frac{2\left(2n - 1\right)}{N} + \left(\frac{2}{n} - \frac{1}{n^2}\right) \tag{6}$$

$$\alpha\left(RNB\right) = \frac{2n}{N} + \frac{1}{n} \tag{7}$$

Figure 3(a) and 3(b) plot the α for SNB Clos and RNB Clos switch fabrics, respectively, when $n = 2, 3, 4, 5, 6, 7, 8$. It can be seen that for $N \leq 16$, the single-stage switch-and-select
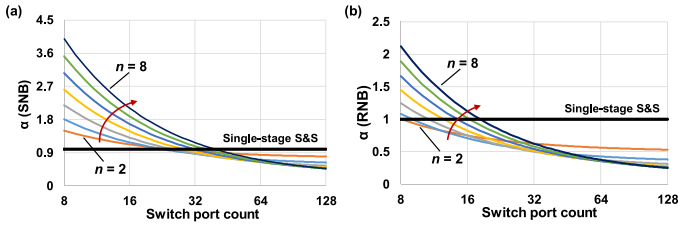
Fig. 3.   Ratio between the number of switching elements in the (a) SNB Clos design and the single-stage switch-and-select, and (b) RNB Clos design and the single-stage switch-and-select, for n = 2, 3, 4, 5, 6, 7, 8.
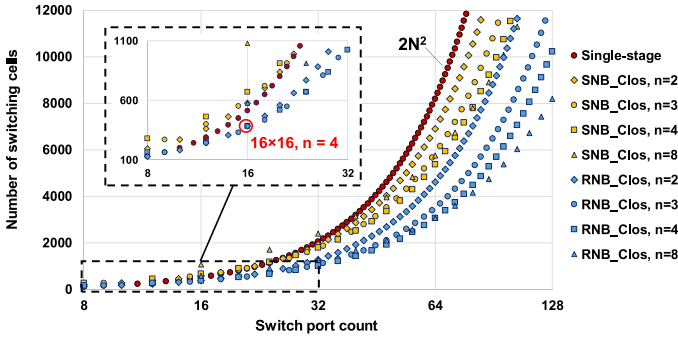

Fig. 4.   Number of switching cells as a function of the switch port count N for both SNB and RNB Clos networks, with n = 2, 3, 4, and 8, as well as single-stage switch-and-select devices. Individual marker represents a valid switch configuration.
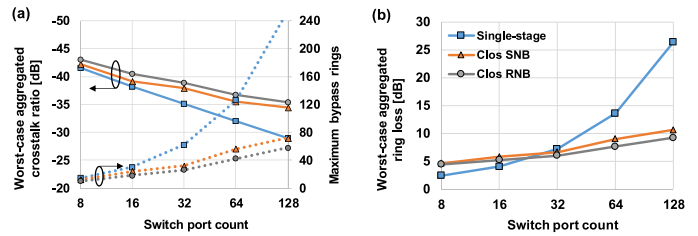

Fig. 5.   (a) Worst-case aggregated crosstalk ratio, number of maximum bypass rings and (b) worst-case aggregated ring loss, as a function of the switch port count N for both SNB and RNB Clos networks, as well as single-stage switch-and-select devices. Calculations based on the measured results reported in [25].

stands out as the best candidate for strictly non-blocking connections (Fig. 3(a)). The reduction in the number of switching cells for the Clos design becomes evident when N is larger than 64. At the port count of 128, the α(SNB) is lower than half when $n = 8$. Larger reductions in the number of switching cells are expected for RNB Clos switch fabrics, though at the expense of a more complex control plane. As expected, Fig. 3(b) shows that the RNB Clos switch fabric saves over 25% switching cells compared to the single-stage design, even at a moderate port count of 16. A factor of 4 in reduction can be achieved for a 128 port count switch fabric with $n = 8$.

The total number of switching cells, as a function of the switch port count N for both SNB and RNB Clos switch fabrics, is plotted in Fig. 4, with $n = 2$, 3, 4 and 8, along with the numbers for the single-stage switch-and-select ($2N^2$) devices. Note that each marker represents a valid switch configuration. While at moderate scales, switch fabrics with smaller n tend to have fewer switching cells, it will be more efficient in terms of switching cells to apply larger sub-stages (with larger n) at high port counts.

The three stage arrangement in the Clos topology also brings about a further benefit of reducing the number of crosstalk sources, since the crosstalk leakage only aggregates within each switching blocks. As indicated by equation 1, the number of crosstalk sources is bounded at $(n + r + m - 3)$ for the Clos design, whereas the number goes up to $(N - 1)$ for the single-stage switch-and-select design. This directly translates into the worst-case aggregated crosstalk ratio as shown in Fig. 5(a). The same is the case for the number of maximum bypass rings (Fig. 5(a)), which leads to a sharp increase in the aggregated ring loss for

the single-stage switch-and-select device at large switch scales, as illustrated in Fig. 5(b). The aggregated ring through loss dominates over the drop loss at large port counts, leading to a large discrepancy between the Clos design and the single-stage switch-and-select switch.

C. Bandwidth Narrow-Down in a Multi-Stage MRR Switch

The bandwidth narrow-down factor for ring-based multi-stage switch is frequently ignored in the literature studies [24], [30], [31]. It, however, stands out as another key factor which bounds the switch performance for high speed data routing capability. The drop spectrum of a first-order add-drop ring resonator can be simply described by [32]:

$$D\left(\lambda\right) = \frac{D_0}{1 + \left(\frac{2}{\pi}\frac{FSR}{\Delta\lambda_{3dB}}\sin\left(\pi\frac{(\lambda - \lambda_{res})}{FSR}\right)\right)^2} \tag{8}$$

where D_0 is the drop attenuation at the resonance, $\Delta\lambda_{3dB}$ is the 3 dB optical bandwidth, FSR is the free spectral range of the cavity, and λ_{res} is the particular resonance of interest. The drop spectrum at wavelengths close to its resonance can be approximated as:

$$D\left(\lambda\right) \approx \frac{D_0}{1 + \left(\frac{2}{\Delta\lambda_{3dB}}\left(\lambda - \lambda_{res}\right)\right)^2} \tag{9}$$

If the optical signal is consecutively dropped by k add-drop elements, the overall spectral response is $D_k(\lambda) = [D(\lambda)]^k$. The 3 dB optical bandwidth of the optical path is therefore given by:

$$\Delta\lambda_{3dB,k} \approx \Delta\lambda_{3dB} \times \sqrt{2^{\frac{1}{k}} - 1} \tag{10}$$

It should be noted that this equation also holds approximately true for the higher order add-drop elements under the *maximally flat* passband condition [33]:

$$\kappa_{RR} = \frac{\kappa_{RW}^2}{2 - \kappa_{RW}^2} \tag{11}$$

where κ_{RW} is the ring-bus field coupling and κ_{RR} is the ring-ring coupling coefficient.

The bandwidth narrow-down factor as a function of the number of drop rings per path can thus be plotted, which is shown in Fig. 6. The number of drop stages at 1, 2, and 6 corresponds to the crossbar, single-stage switch-and-select, and Clos of switch-and-select topologies, respectively. Whereas it is shown that
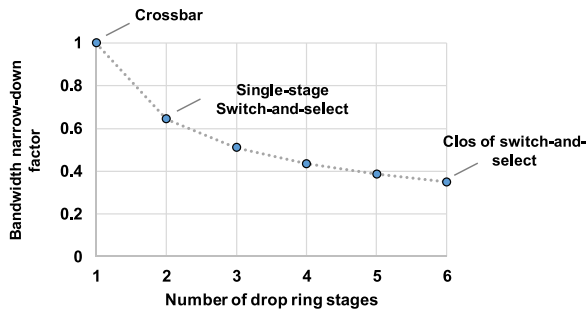
Fig. 6. Bandwidth narrow-down factor as a function of the number of drop rings per path.
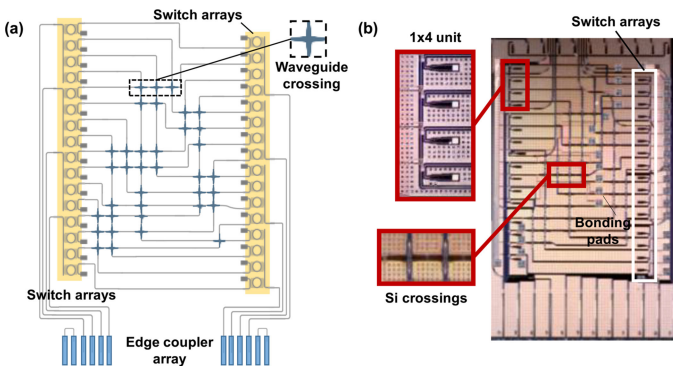

Fig. 7. (a) Schematic of the 4 × 4 microring-based switch-and-select layout with inset showing the silicon waveguide crossing. (b) Microscope photo of the fabricated device with insets showing the enlarged 1 × 4 spatial de-multiplexer and the silicon waveguide crossing.
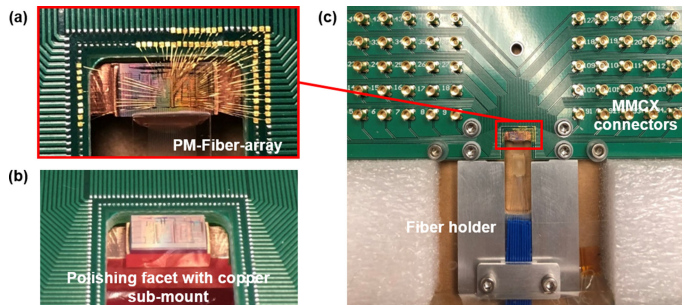

Fig. 8. (a) Enlarged photo of the wire-bonded chip with UV-curved PM fiber array. (b) Enlarged photo of the copper sub-mount, which was polished together with the chip facet for fiber attachment. (c) Photo of the packaged 4 × 4 switch-and-select device.

MRR elements can be easily engineered to have over 100 GHz bandwidth [32], the Clos design clearly trades off the bandwidth with a narrow-down factor of 0.35 comparing to a single MRR element. We verify the bandwidth narrow-down factor for ring resonators experimentally in the next section and demonstrate a 6-stage drop ring structure with 42 GHz passband.

IV. SILICON 4 × 4 BUILDING BLOCK FOR A 16 × 16 CLOS SWITCH FABRIC

In this work, a 16 × 16 RNB Clos switch fabric is chosen as the initial demonstration for such a Clos design. While, both ($n = m = 2$, $r = 8$) and ($n = m = r = 4$) configurations have the same number of microrings (384), we select the latter as it consists of 12 4 × 4 building blocks and therefore, a modular approach can be leveraged by studying the performance of a single 4 × 4 element. A detailed description of the design, fabrication and characterization of the 4 × 4 Clos building block is presented in this section, which is used to emulate the performance of a 16 × 16 Clos switch fabric.

A. Device Design, Fabrication, and Packaging

The silicon 4 × 4 microring-based switch-and-select layout is shown schematically in Fig. 7(a). This device is similar to the one reported in [19], but with all elements fabricated in the silicon layer. It has 32 thermo-optic microring resonators with

optical terminations placed at each through port to eliminate reflections. A perfect shuffle is used to connect the 16 (4 × 4 arrays) microrings at the input stage to the 16 microrings at the output stage. Multi-mode based waveguide crossings are placed at the intersections for low-loss and low-crosstalk. The input and output MRR switching arrays are staggered by an offset of ~130 μm to avoid symmetrical shuffle networks. This reduces waveguide overlaps and thus reduces the number of waveguide bending structures. An edge coupler array is used to couple light in and out of the chip. Two pairs of looped couplers are used to facilitate the coupling process. The chip is designed for TE-mode operation only.

The device was taped out using standard PDK elements through the AIM Photonics MPW run [34]. A microscope photo of the fabricated device is shown in Fig. 7(b). The thermo-optic microring resonators are placed at a pitch of 100 μm to minimize thermal crosstalk. Their measured resonance shift shows a thermal efficiency of 1 nm/mW [35]. The switch fabric has a compact footprint of 1.6 × 2.5 mm^2 with 34 electrical bonding pads. The edge coupler array has a standard pitch of 127 μm.

The fabricated device was wire-bonded to a co-designed printed circuit board (PCB) for electrical fan-out, as shown in Fig. 8(a). The silicon chip was first die-bonded onto a customized copper sub-mount with the edge slightly overhung. Then, the facet of the chip was polished together with the copper mount to remove the chip ledge that is residual from the dicing trench (Fig. 8(b)). This allows a standard polarization-maintaining (PM) fiber array to be attached using a UV curable epoxy. MMCX connectors are used for a compact footprint. The packaged device was mounted with an aluminum fiber holder and the completed package is shown in Fig. 8(c).

B. Device Characterization

Figure 9 shows the switch test-bed. The optical input to the switch is connected to a tunable laser operating at 1542.2 nm. The selection of operating wavelength is close to the half free spectral range (FSR) of MRRs, which ensures the minimum interaction with the bypass ring resonators, and thus minimum power consumption. Initial device evaluation is performed by characterizing switch power transfer functions, for input 1 and 4, to all four output ports. The measurement covers the best (shortest path) and worst (longest path) cases, which will be used
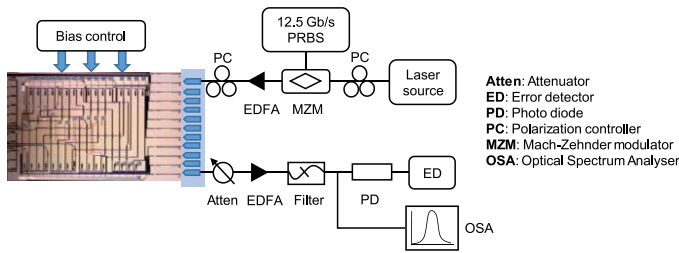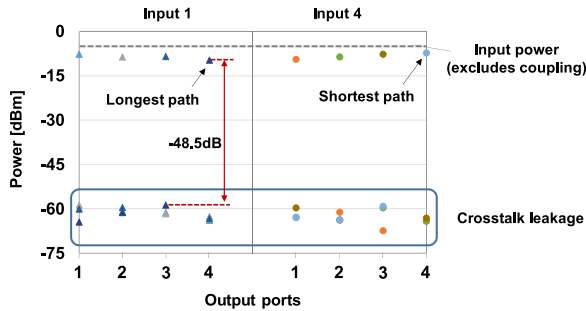
Fig. 9.   Schematic of the device test-bed.

TABLE II
ESTIMATED COMPONENT LOSS

Item	Loss
Waveguide propagation loss	2 dB/cm
T-O microring drop	0.5 dB
T-O microring through	0.1 dB
Waveguide crossing	0.2 dB
Edge coupler	6 dB/facet

Fig. 10.   Measured insertion loss and crosstalk for paths from input 1 and 4 to all four outputs.
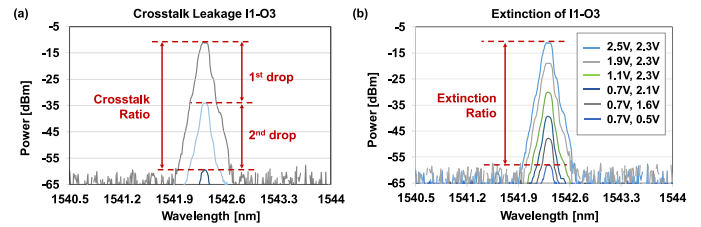

Fig. 11.   (a) Breakdown measurement on the worst-case crosstalk. Data routed from input 1 to output 4 and the crosstalk leakage to output 3. (b) Power tuning for path 1–3 with various bias voltages.
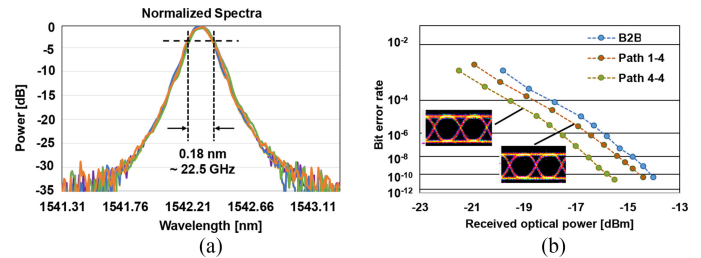

Fig. 12.   (a) Normalized spectra with resolution at 0.1 nm. (b) BER as a function of received optical power at 12.5 Gb/s for path 1–4 and 4–4. Insets show the measured eye diagrams.

in the three-stage Clos switch fabric emulation. The on-state and off-state are verified by searching for the highest and lowest output power, respectively. An optical spectrum analyzer (OSA) is used to record both the transferred power and the spectrum. Fig. 10 shows the measured results, illustrating the switch on-chip insertion loss and crosstalk ratio. The on-state and off-state bias lies in the range of 2.2 to 2.7 V and 0.2 to 0.7 V, respectively. The power consumption per path (including both on-state and off-state tuning) is estimated at 20 mW (roughly 10 mW for each switching array).

The measured on-chip loss is in a range of 2.3 to 4.8 dB. The path-dependent loss mainly comes from the central shuffle network. The passive loss of each path is a linear combination of different loss sources: microring drop and through loss, waveguide propagation and crossing loss, and the chip coupling loss. The coupling loss can be determined by measuring the looped pair of edge couplings, at 6 dB/facet. Referring to Fig. 7(a), both path 1–1 and 4–4 incorporate three off-resonance microrings, two on-resonance ones and straight waveguide sections, and therefore, the loss difference is attributed to the different waveguide propagating lengths. This results in a silicon waveguide propagation loss of ∼2 dB/cm. The microring drop-state and through-state loss, along with silicon waveguide crossing loss, can be found and averaged by solving the combination of measurements, as summarized in Table II.

As shown in Fig. 10, the measured switch crosstalk ratio is in the range of −57 dB to −48.5 dB, benefitting from the first-order crosstalk cancellation in the switch-and-select architecture. The worst-case (−48.5 dB) occurs in path 1–4 as marked in red. The slight degradation is believed to come from the higher path insertion loss. A detailed breakdown of the measurement is shown in Fig. 11(a), showing that the on-off extinction of single

ring elements is more than 23 dB. A detailed measurement on the extinction ratio of path 1–3 is also presented in Fig. 11(b) with a set of bias voltages, revealing an extinction ratio of 49 dB.

An Erbium-doped fiber amplifier (EDFA)-based broadband source is injected to measure the passband of the optical paths. The spectra are recorded for the measured eight optical connections using the OSA with a resolution of 0.1 nm. The normalized spectra are shown in Fig. 12(a), indicating a passband of ∼22.5 GHz. However, the pre-defined microring resonator targets a 3 dB passband of ∼70 GHz. This should allow the switch-and-select device to operate with a 45 GHz passband after two drops (the effective passband of k consecutive microring drops is given by Equation 10). The degraded passband could be a result of imperfect fabrication, which is expected to be improved in future runs with better fabrication uniformity.

Measurements of the switch BER performance are performed. An optical input to the switch is generated using a tunable laser that is modulated by a Mach–Zehnder modulator (MZM) driven by an electrical non-return-to-zero (NRZ) signal at a rate of 12.5 Gb/s. Test results for the longest and shortest paths–1-4 and 4–4–are shown in Fig. 12(b), with a power penalty of −0.5 dB
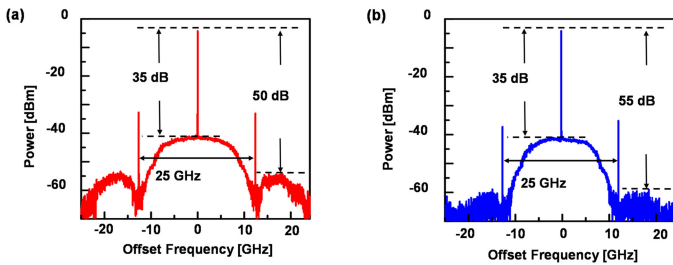
Fig. 13. Optical spectra of the NRZ-encoded optical signal recorded (a) at the switch input and (b) output for path 4–4.
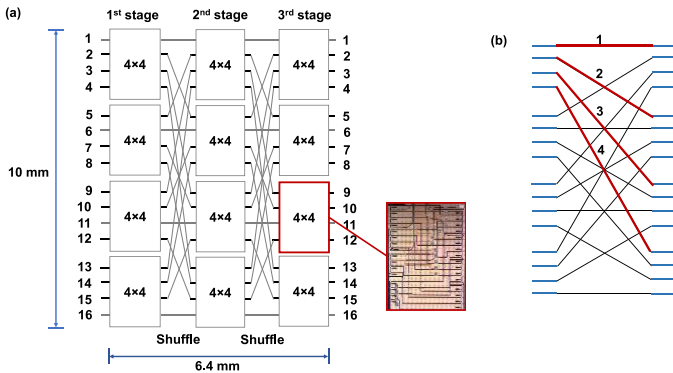
TABLE III
ESTIMATED SHUFFLE LOSS

Path	Waveguide propagation length [mm]	Number of waveguide crossings	Loss [dB]
1	0.8	0	0.2
2	2.7	3	1.1
3	4.6	6	2.1
4	6.5	9	3.1

Fig. 14. Schematic of (a) the 16 × 16 Clos switch fabric and (b) the inter-stage shuffle network. Path loss of the shuffle is estimated in Table III.
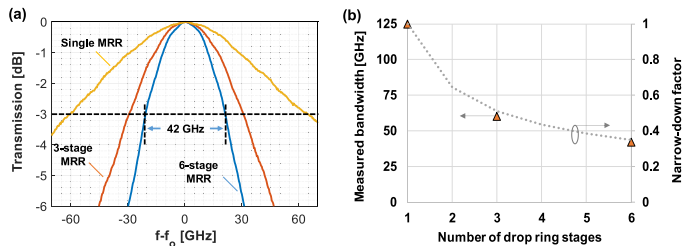

Fig. 15. (a) Measured optical spectra for single, 3-stage, 6-stage drop rings. (b) Measured optical bandwidth with fitted narrow-down factor from Fig. 6.

and −1.6 dB, respectively. Note that the power penalty is calculated as the difference in received power required to achieve a BER of 10^{-9}. For a fair comparison, an optical attenuator is used to emulate the switch insertion loss for back-to-back (B2B) BER measurement. The slope of the BER data remains nearly unchanged for the three measurements, indicating that the device induced inter-symbol-interference is negligible. The negative power penalty could be attributed to the filtering nature of microrings that suppress the signal distortion due to the nonlinearity of the optical modulator [36]. The NRZ-encoded electrical signal is first pre-amplified using a driving amplifier and then imprinted on the optical carrier via an external MZM. It can be seen in Fig. 13(a) that the modulated optical signal carries harmonic distortion components on the side band, which get suppressed by passing through the microring-based switch circuit (Fig. 13(b)), improving the signal quality. The additional power penalty from path 1–4 is predominantly incurred by higher insertion loss.

C. 16 × 16 Clos Switch Fabric Emulation

A schematic of the 16 × 16 Clos switch is shown in Fig. 14. It consists of 12 4 × 4 building blocks in three stages, connected via two inter-stage shuffle networks. The footprint width of the shuffle network is inherently limited by the number of cascaded waveguide crossings, as seen in Fig. 7(a). Since the inter-stage shuffle connects the 16 outputs of one stage to the 16 inputs of the following stage, its width is roughly the same as that of the inner shuffle within the 4 × 4 block (∼0.8 mm). For each building block, electrical pads can be placed right next to the

MRR unit and electrical fan-out will be taken care of using a PCB or an interposer with flip-chip bonding technique as the one demonstrated in [25]. The dimension of the 16 × 16 Clos switch fabric with the fabricated 4 × 4 blocks can thus be estimated as 10 mm long by 6.4 mm wide.

The inter-stage shuffle loss can be then estimated based on the experiment-validated component-level loss listed in Table II. By verifying the detailed shuffle parameters, the shuffle path loss is calculated and shown in Table III. The shortest path travels directly from input 1 to output 1, while the longest path travels from input 1 to output 16 via two inter-stage shuffles (Fig. 12). The on-chip insertion loss for the 16 × 16 Clos switch fabric can thus be summed, in the range of 7.3 dB to 15.2 dB. The path-dependent loss is primarily a result of the loss variation in the shuffles. Taking the measured worst-case crosstalk ratio of −48.5 dB for the 4 × 4 building block into Equation 1, a worst-case crosstalk ratio of −39 dB can be achieved for the 16 × 16 Clos switch fabric at a full load. However, the degraded 3 dB bandwidth here is a limiting factor for the three-stage Clos switch fabric.

We thus verify the bandwidth narrow-down factor with a test structure that can set 1–6 drop rings in one path. The add-drop ring resonator employs a first-order structure and is measured to show a 3 dB optical bandwidth of 125 GHz. Its measured drop spectrum is normalized and shown in Fig. 15(a). The bandwidth consequently shrinks to 60 GHz and 42 GHz, when the number of drop rings per path goes to 3 and 6 stages, respectively. The spectra of both are included in Fig. 15(a). The measurement agrees very well with the calculated bandwidth narrow-down factor from equation 10, as illustrated in Fig. 15(b). Further design considerations and performance trade-offs for the add-drop switch elements will be included in Section V.
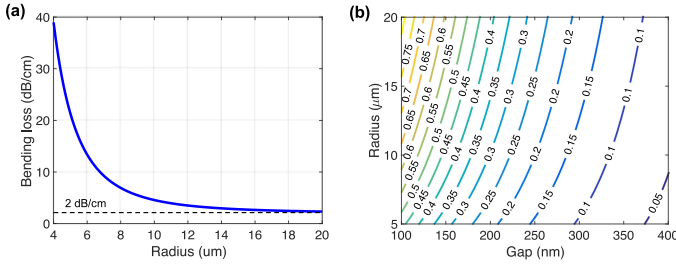
Fig. 16.   (a) Bending loss model for 400 nm × 220 nm silicon strip waveguides. (b) Contours of electric field coupling coefficient between the bus waveguide and the ring resonator.

The power consumption of the Clos switch fabric is the sum of each switch-and-select building block. This results in ∼60 mW per path for a total power consumption of 720 mW at a full load. It should be noted that the microring on-off tuning power directly relates to its FSR, which can be reduced by redesigning the microring filters.

V. CLOS SWITCH FABRIC PERFORMANCE EXPLORATION

In this section, we start from the design space exploration of individual microring switching cells with foundry-validated data, followed by the Clos switch fabric performance exploration. Special attention is paid to the drop and through loss, out-of-band extinction ratio, as well as the, frequently ignored, 3 dB bandwidth from a single microring element, and how these factors impact the performance and scalability of a three-stage Clos switch fabric.

We have extracted a set of key foundry related parameters on the bending loss of the ring resonators as a function of radius through AIM MPW runs, as plotted in Fig. 16(a). It can be seen that the bending loss converges at ∼2 dB/cm (close to straight waveguide propagation loss) when approaching large radii. All structures are defined with 400 nm × 220 nm silicon strip waveguides. The radius of the microrings also affects the coupling efficiency to the bus waveguide, which can be seen from the non-vertical contours on the coupling coefficient in Fig. 16(b). We then establish a compact, yet highly-accurate, model exploring the design space of microring cells [32], and link them to the Clos switch fabric performance exploration. Designs with both first-order and second-order ring resonators are presented.

A. First-Order Thermo-Optic Microring Unit

Equation 10 yields a bandwidth narrow-down factor of 0.35 for the 6 drops in the Clos switch design. We set the lower bound of 3 dB bandwidth on a single switching cell to be 70 GHz to maintain over 25 GHz operating bandwidth. Detailed performance contours of the first-order add-drop microring unit as a function of ring radius and ring-bus gap are plotted to explore the drop loss, out-of-band extinction ratio, and 3 dB bandwidth in Fig. 17(a), (b) and (c), respectively. It assumes that the rings are operating close to critical coupling. It can be seen that the
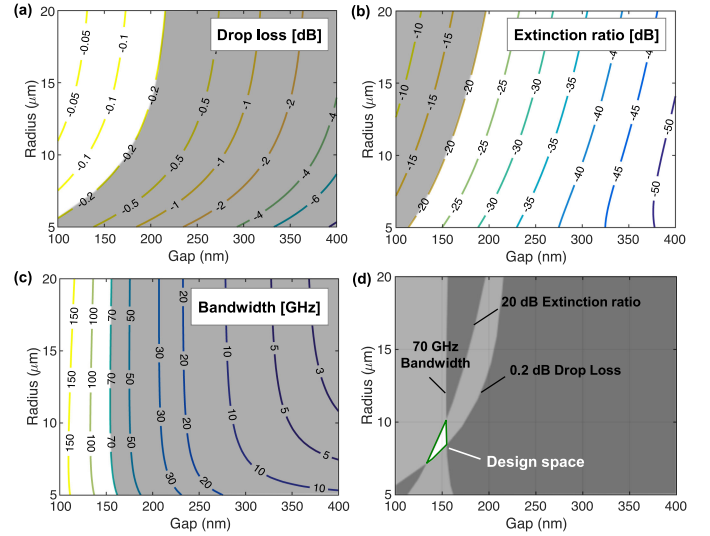

Fig. 17.   Design space exploration of first-order add-drop microrings based on 400 nm × 220 nm silicon strip waveguides for (a) drop-state insertion loss, (b) out-of-band extinction ratio, (c) 3 dB optical bandwidth, and (d) overall design space.

requirement on bandwidth of over 70 GHz calls for narrow ring-bus gaps for tight coupling (Fig. 17(c)). The optimization of extinction is restricted as their values are coupled to the bandwidth in the first-order microring designs. We target a lower drop loss in this case, i.e., 0.2 dB (Fig. 17(a)), while maintaining a reasonable out-of-band extinction ratio of >20 dB (Fig. 17(b)). These performance bounds outline the overall optimal design space as outlined in Fig. 17(d), yielding a drop loss of 0.15-0.2 dB, out-of-band extinction ratio of 20–22 dB, and 3 dB bandwidth of 70–100 GHz. The design space not only defines the range of required geometric parameters, but it also illustrates the design and fabrication tolerance.

While the microrings that fall into the defined design space are expected to have better performance than the boundary values, we use these boundary values (drop loss of 0.2 dB, extinction ratio of 20 dB) in the Clos switch fabric performance exploration to secure design margins. The through state loss is simulated ∼0.05 dB. Waveguide propagation loss will refer to the measured result listed in Table II as it is an important foundry-relevant parameter. AIM Photonics predicts the waveguide crossings to have lower than −50 dB crosstalk with insertion loss of ≤0.25 dB. As a standalone component, we however take the value of 0.05 dB for the waveguide crossing loss, since a number of groups have demonstrated <0.05 dB loss using CMOS-compatible fabrication [37]–[39]. Given that thermal isolation structures, for example deep trenches, can be added on-chip to suppress thermal crosstalk, the pitch of the microrings can be brought down in order to reduce the length of the shuffles. We use 50 μm as the pitch here, due to the small radius of the microrings. A detailed analysis on the power penalty map (for the longest path at full load) for various Clos switch scales is performed and summarized in Fig. 18. The combination of (n, r, m) is selected to be (2, 4, 2), (4, 4, 4), (4, 8, 4), (8, 8, 8), and (8, 16, 8) for the lowest number of switching cells in 8 × 8,
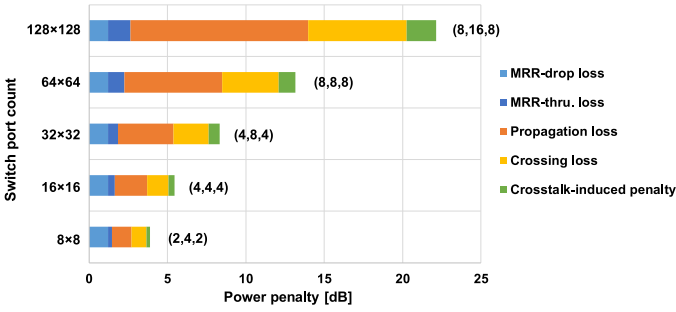
Fig. 18. Power penalty map (for the longest path) for various Clos switch scales using first-order microring units. The combination of (n, r, m) is shown next to each bar.

16×16, 32×32, 64×64, and 128×128 port count switch fabric, respectively (referring to the discussion in Section III).

The power penalty map shown in Fig. 15 consists of 5 elements, i.e., microring drop and through loss, waveguide propagation loss, waveguide crossing loss and crosstalk-induced penalty [40]. It can be seen that applying the switch-and-select stages as building blocks is highly scalable as the ring drop loss keeps constant (6 drops), while adding bypass rings only add a 0.05 dB/ring penalty. In addition, the immunity to first-order crosstalk ensures that the aggregated crosstalk-induced penalty remains at a modest level. This simulation assumes −50 dB crosstalk at each waveguide crossing. Further signal degradation can be expected with higher crosstalk. The 3 dB bandwidth of the Clos switch can be obtained by multiplying the bandwidth of a single switching cell by the narrow-down factor, which is in the range of 25–35 GHz. This number can be further increased by trading off the extinction ratio. Higher-order ring resonators can be used to relax this constraint as will be shown in the next sub-section. The limiting factor on the switch fabric performance, and thus the scalability, is shown to be the insertion loss of shuffle networks, comprising of waveguide propagation loss and waveguide crossing loss, as presented in Fig. 18. The Si/SiN multi-layer platform can be leveraged [25], [41]; however, additional considerations should be taken to examine the trade-offs among design complexity, device footprint and yield, and the performance enhancement.

B. Second-Order Thermo-Optic Microring Unit

Higher-order microring resonators can be used to decouple the values of extinction ratio and optical bandwidth, relaxing optimization restrictions. We choose to use the second-order elements as a balance of complexity and performance. The second-order add-drop elements are assumed to operate at their *maximally flat* response [33].

Similarly, Fig. 19(a), (b) and (c) plot performance contours of the second-order add-drop microring unit as a function of ring radius and ring-bus gap to explore the drop loss, out-of-band extinction ratio, and 3 dB optical bandwidth, respectively. The ring-ring coupling is determined under the *maximally flat* passband condition as shown in Equation 11. It can be seen in Fig. 19(b): that the lower bound on the ring-bus gap is much relaxed comparing to that in Fig. 17(b) to achieve extinction ratios
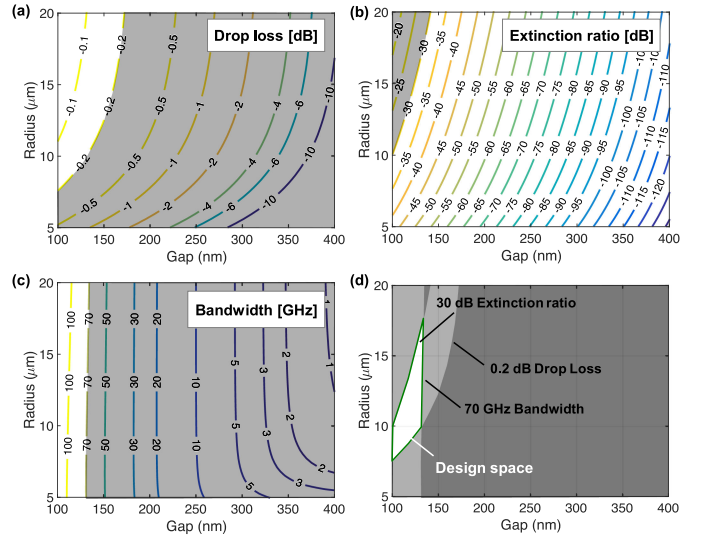

Fig. 19. Design space exploration of second-order add-drop microring based on 400 nm × 220 nm silicon strip waveguides for (a) drop-state insertion loss, (b) out-of-band extinction ratio, (c) 3 dB optical bandwidth, and (d) overall design space.
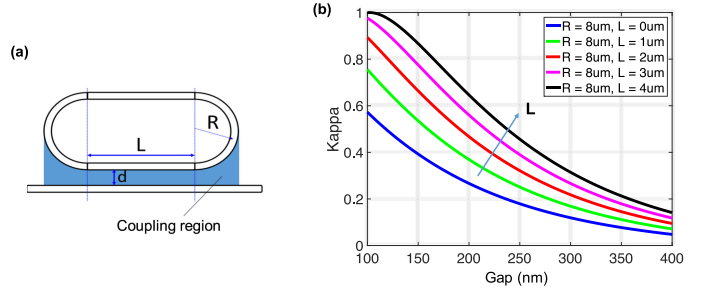

Fig. 20. (a) Schematic of a race-track ring resonator with straight section length of L, gap of d, and radius of R. (b) Comparison of ring-bus coupling coefficient between $L = 0$, 1, 2, 3, and 4 μm, as a function of ring-bus gap.

of over 20 dB, though a slightly higher loss is induced. This, consequently, allows a more relaxed design space with higher performance bounds on the extinction ratios. Fig. 19(d) outlines the defined design space for drop loss of ≤ 0.2 dB, extinction ratio of ≥ 30 dB, and 3 dB bandwidth of ≥ 70 GHz. We restrict the ring-bus gap to be larger than 100 nm as the fabrication becomes difficult at smaller gaps. This yields a drop loss of 0.1–0.2 dB, out-of-band extinction ratio of 30–40 dB, and 3 dB bandwidth of 70–120 GHz.

It can be seen that the achievable 3 dB bandwidth is bounded by the ring-bus gap. This restriction can be effectively relaxed by utilizing the race-track structure or a curved bus [32] which offers an extra degree of freedom for ring-bus coupling optimization. The schematic of a race-track structure is shown in Fig. 20(a), with straight section length of L, gap of d, and radius of R. Fig. 20(b) plots the ring-bus coupling coefficient as a function of ring-bus gap for $L = 0$, 1, 2, 3, and 4 μm. The coupling coefficient can be flexibly set by adjusting the length of the straight coupling section. Note that the longer of the straight section, the larger of the effective ring radius and thus smaller FSR. We set $L = 2$ μm and plot performance contours of the
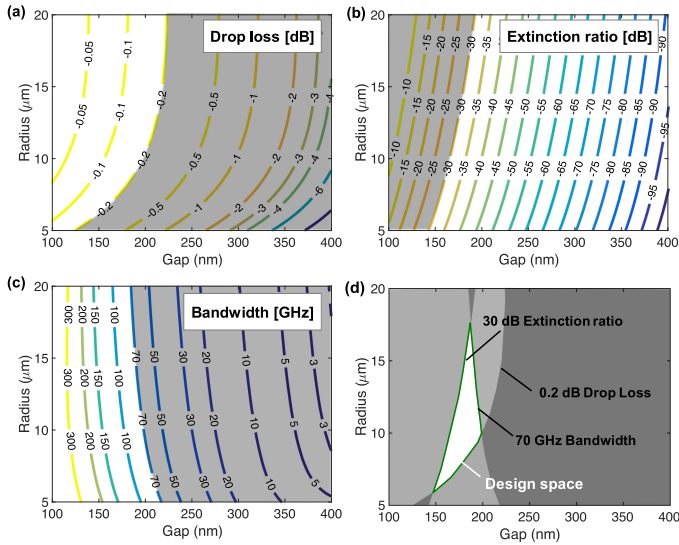
Fig. 21. Design space exploration of second-order add-drop microring in race-track structure with $L = 2$ μm for (a) drop-state insertion loss, (b) out-of-band extinction ratio, (c) 3 dB optical bandwidth, and (d) overall design space.
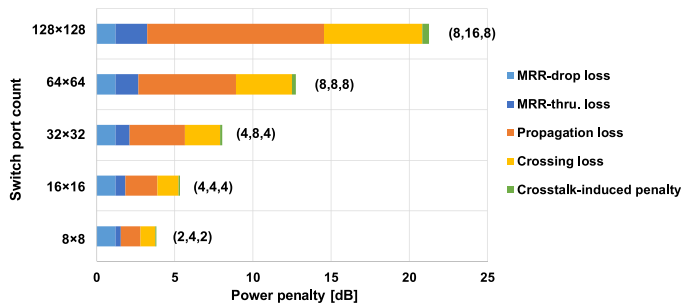

Fig. 22. Power penalty map (for the longest path) for various Clos switch scales using second-order microring units. The combination of (n, r, m) is shown next to each bar.

second-order race-track MRR unit as a function of ring radius, R, and ring-bus gap, d, to explore its drop loss, out-of-band extinction ratio, and 3 dB optical bandwidth in Fig. 21(a), (b), and (c), respectively. The defined design space shown in Fig. 21(d) indicates a drop loss of 0.1–0.2 dB, out-of-band extinction ratio of 30–40 dB, and a significantly improved 3 dB bandwidth of 70–200 GHz, benefitting from the race-track structure.

The through state loss is calculated at ~0.07 dB. The same component-level performance is applied as those used in Section V. A. Setting these parameters, a detailed breakdown of the power penalty as a function of switch scales can be determined and is shown in Fig. 22. The 30 dB out-of-band extinction offers a higher suppression on the switch crosstalk, and therefore the crosstalk-induced penalty can be further reduced, as shown in Fig. 22. While the penalty on device insertion loss remains almost unchanged compared to the design using first-order elements, the much relaxed design space for the second-order elements offers a higher fabrication tolerance, which enables a more robust design. Moreover, the second-order race-track MRRs support a 3 dB bandwidth of up to 70 GHz in the Clos switch fabrics. The selection of geometrical parameters on the

microring switching elements depends on exact switching applications.

VI. CONCLUSION

We propose a highly-scalable microring-based Clos switch fabric architecture constructed with switch-and-select stages. We analyse the key design parameters for both SNB and RNB implementations, emphasizing the factor of switching cell numbers. Inheriting the immunity to first-order crosstalk from the switch-and-select stages, the Clos design also fully blocks first-order crosstalk. We establish the feasibility of a microring-based 16×16 Clos switch fabric by using the 4×4 silicon switch-and-select building block, taped out at AIM Photonics. Furthermore, using the foundry-validated data, we conduct a detailed design space exploration on the insertion loss, out-of-band extinction ratio, as well as the frequently ignored 3 dB bandwidth for microring-based switching cells and exploit the feasibility of building large-scale MRR-based switch fabrics in the Clos architecture. The design with second-order microrings is shown to have a larger design space, and thus better fabrication tolerance, compared to those using first-order elements.

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Qixiang Cheng (M'18) received the B.S degree from the Huazhong University of Science and Technology, Wuhan, China, in 2010, and the Ph.D. degree from the University of Cambridge, Cambridge, U.K., in 2014.

In March 2015, he joined Shannon Laboratory, Huawei, China, as a research engineer studying future optical computing systems. He is currently a Research Scientist with Lightwave Research Laboratory, Columbia University, New York, NY, USA. His research interests include design, simulation, and characterization of large-scale optical integrated devices for data center and optical computing applications.

Meisam Bahadori received the B.Sc. degree in electrical engineering (Hons.), and the M.Sc. degree in electrical engineering, from the Sharif University of Technology, Tehran, Iran, and the Ph.D. degree in electrical engineering from Columbia University, New York, NY, USA, in 2011, 2013, and 2018, respectively.

From fall 2011 to spring 2014, he was a Research Assistant with Integrated Photonics Laboratory, Sharif University of Technology. In 2014, he joined the Lightwave Research Laboratory, Columbia University. His research interests include silicon photonic devices, thin-film Lithium Niobate photonics, and nano-photonics.

Yu-Han Hung received the M.S. and Ph.D. degrees from National Cheng Kung University, Tainan, Taiwan, in 2012 and 2016, respectively, both in nonlinear dynamics of semiconductor lasers and their applications. In June 2018, he was a Postdoctoral Researcher. He is currently a Postdoctoral Research Scientist in Columbia University, New York, NY, USA. His research interests include design/testing of photonic circuit integrations for data centers and test-bed design for high-performance computing architecture.

Yishen Huang received the B.Sc. degee in engineering physics from Queen's University, Kingston, ON, Canada, and the M.S. degree in electrical engineering from Columbia University, New York, NY, USA, where he is currently working toward the Ph.D. degree in the Lightwave Research Laboratory. His research interests include large-scale silicon photonic switch fabrics and high-performance silicon photonic modulators, with specific focus on novel structures and control schemes to enable energy efficient optical link designs.

Nathan Abrams received the B.S. degree in electrical engineering from Columbia University, New York, NY, USA, in 2014, and the B.A. degree in natural mathematics and sciences from Whitman College, Walla Walla, WA, USA, in 2014. He is currently working toward the M.S. and Ph.D. degrees at Columbia University. His current research focuses on photonic devices.

Keren Bergman (S'87–M'93–SM'07–F'09) received the B.S. degree from Bucknell University, Lewisburg, PA, USA, in 1988, and the M.S. and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1991 and 1994, respectively, all in electrical engineering. She is currently a Charles Batchelor Professor with Columbia University, New York, NY, USA, where she also directs the Lightwave Research Laboratory. She leads multiple research programs on optical interconnection networks for advanced computing systems, data centers, optical packet switched routers, and chip multiprocessor nanophotonic networks-on-chip. She is a Fellow of OSA.