Open-Access 3-μm SOI Waveguide Platform for Dense Photonic Integrated Circuits

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***Abstract*—This paper gives an overview of the 3-μm silicon-on-insulator (SOI) platform that is openly available from VTT and suitable for the realization of photonic integrated circuits (PICs) for near and mid-infrared applications. Specific benefits of this thick-SOI PIC platform include low optical losses ($\sim$0.1 dB/cm), ultra-dense integration (μm-scale bends), small polarization dependency (down-to-zero birefringence), and ability to tolerate relatively high optical powers ($>$1 W). Fabrication technology is based on an i-line stepper and 150-mm wafer size. Open access to the waveguide platform is supported by design kits, wafer-level testing, multi-project wafer runs, dedicated R&D runs, and small-to-medium volume manufacturing.**

***Index Terms*—Silicon photonics, silicon-on-insulator, photonic integrated circuits, foundries.**

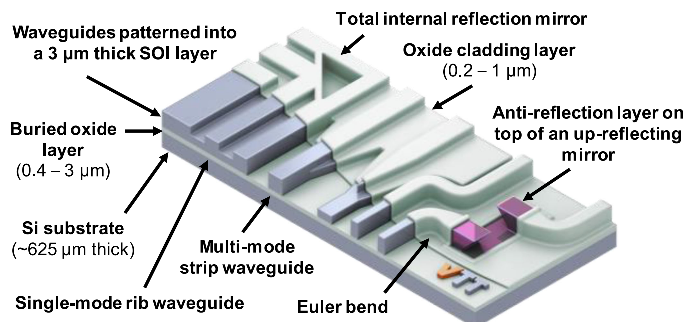

Fig. 1. Schematic illustration of the 3 μm SOI platform.

I. Introduction

SILICON photonics (SiPh) represents a scalable path to the deployment of photonic integrated circuits (PICs) [1]. It basically copies the proven success of silicon microelectronics into photonics. The fundamental idea is to integrate a large number of photonic functions in a small footprint on the surface of a silicon chip. Silicon wafer processing foundries play a key role in the success of this research, development and innovation path as they develop and offer a generic technology platform for multiple applications, markets and end users. Research and manufacturing in SiPh can benefit from the maturity and infrastructure of silicon microelectronics, which has led to the extensive use of modern microelectronics fabrication methods and tools [2].

However, PICs are not identical to electronic ICs and the latest nano/microelectronics technology is not always ideal for PICs. Photons and electrons have some clear differences in terms of wavelength and polarization, for example. Reducing the physical size of optical waveguides into submicron dimensions makes light propagation very sensitive to not only those dimensions, but also to the wavelength, polarization and intensity of the light. The discrepancy between the latest IC technology nodes and the functional requirements for PICs becomes apparent when trying to couple light from submicron Si waveguides to standard single-mode fibers (SSMFs) that form the foundation of modern communication networks. Therefore, it is useful to also take a look at the possibilities of micron-size Si waveguides and related microfabrication technologies in realizing dense and low-loss PICs.

In this paper we present VTT's foundry-enabled PIC platform that is based on 3 μm thick silicon-on-insulator (SOI) waveguides (Fig. 1), as opposed to the mainstream use of submicron-size waveguides (nanowires) in SiPh development. It has open access via multi-project wafer (MPW) runs, dedicated process runs, prototyping and small-to-medium volume production services. This platform is also known as thick-SOI platform and in the following sections, we present an overview of this technology, as well as some latest results and our plans in developing the platform further. The main benefits of this PIC platform are low losses, dense integration, polarization independent operation, wide wavelength range, ability to tolerate high optical powers and smooth transition from R&D and prototyping to volume production.

II. Fundamental Properties of Thick SOI Waveguides

The foundation for the 3 μm SOI platform is the combination of rib and strip type waveguides, and the ability to couple light adiabatically between them without exciting higher order modes (Fig. 2) [3]. This allows to make effectively single-mode (SM) PICs even if the strip waveguides are strongly multi-moded. The

Manuscript received December 1, 2018; revised March 8, 2019; accepted March 14, 2019. Date of publication April 1, 2019; date of current version June 24, 2019. This work was supported in part by RAPSI, funded by Business Finland under Grant 55388, in part by OPEC, funded by Tekes under Grant 2814/31/2015 and in part by RAPIDO, PASSION, MIREGAS, PIXAPP and ACTPHAST, funded by European Commission under Grants 619806, 780326, 644192, 731954, and 619205, respectively. The work is also part of the Academy of Finland Flagship Programme, Photonics Research and Innovation (PREIN), decision 320168. *(Corresponding author: Timo Aalto.)*

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Digital Object Identifier 10.1109/JSTQE.2019.2908551

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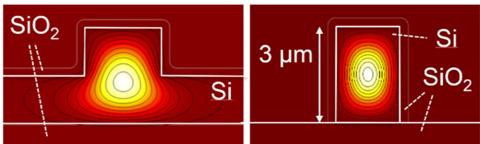


Fig. 2. Simulated intensity distributions of the fundamental modes in a SM rib waveguide (left) and a strip waveguide (right). Sometimes a thin Si pedestal is left around the strip waveguides (not shown here). Field distributions are almost the same for TE and TM polarizations, and from 1.2 to 2 μm wavelength.

rib waveguides offer single-moded operation over an ultra-wide wavelength range (e.g., 1.2–4 μm) since the SM condition is not dependent on wavelength or exact waveguide dimensions, as long as the relative waveguide dimensions (height, width, slab thickness) are well-controlled [4]. Micron-scale Si waveguides are, therefore, particularly well-suited for spectroscopy and extensive wavelength division multiplexing over multiple wavelength bands, as well as operation from near to mid infrared.

The optical mode fields in 3 μm SOI waveguides are almost completely confined inside the Si core. This leads to small propagation losses (~0.1 dB/cm for 3 μm wide rib and ~0.15 dB/cm for 2 μm wide strip waveguides at 1550 nm wavelength), small polarization dependency (down to zero birefringence) and small absorption from the oxide cladding in mid-infrared applications. The large cross-section area of the waveguides allows to propagate higher optical powers (>1 W) compared to submicron SOI waveguides (<100 mW) since nonlinear absorption depends on light intensity inside the waveguides. In rib waveguides, the SM operation is based on the radiation of higher order modes into the surrounding Si slab, which leads to large bending radii. Strip waveguides, on the other hand, enable extremely dense integration by completely avoiding such horizontal radiation. With the combination of rib and strip waveguides, it has been possible to create a library of various passive and active building blocks. Some of those are described in the following Chapters.

III. Monolithic Building Blocks

A. Bends, Mirrors and Spirals

The footprint of circuits in different integrated optics platforms scales roughly with the square of the minimum bending radius. In turn, the minimum bending radius and the mode size scale inversely with the index contrast, meaning that small footprint requires small high index contrast waveguides. All this reasoning is based on a hidden but key assumption: the single-mode condition of the bent waveguide. This is a very sensible and reasonable assumption, because modes couple to each other in bends, therefore spoiling the SM operation of the whole circuit. In the thick-SOI platform, this one-to-one relation between the size of waveguides and bends was successfully broken. It was first explored, if small bends in high index contrast multimode waveguides with large cross-sections could be used without spoiling the SM operation of the PICs. This led to a major breakthrough, that is the Euler bend [5]. Even though this shape had been previously used to minimize transition losses between single-mode straight and bent sections, for the first time, the

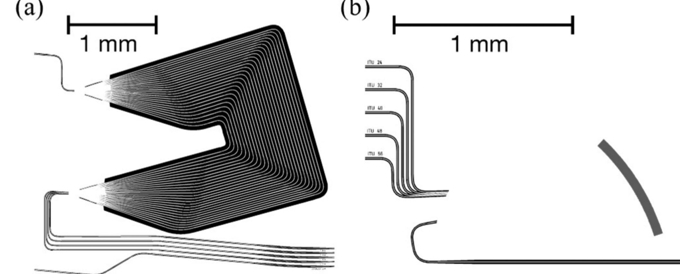


Fig. 3. Layouts of an (a) polarization insensitive 1 × 4 AWG and an 1 × 4 echelle grating. Note the different scales. The device footprints are not directly comparable as the size is much dependent on the wavelength spacing of the outputs.

concept was applied to multimode waveguides, and led to the demonstration of effective single-mode operation in low-loss bends with effective radii as small as 1.3 μm. Another very effective approach to bend light in micron-scale waveguides is to use mirrors based on total internal reflection (TIR) [6]. With elliptically curved mirror facets, the losses of TIR mirrors were reduced down to 0.1 dB/90° for both polarizations [7]. Still, when it comes to very long spirals with several hundreds of bends, Euler bends are the preferred choice. With them, up to 1.5 m long spirals have been demonstrated in about 4 mm^2 footprint [8] and no significant polarization conversion when propagation losses are below 10 dB.

Spiral waveguides in the platform have been demonstrated to have a unique combination of linear and nonlinear properties [9], which made possible instantaneous frequency measurements [10], otherwise impossible with submicron silicon waveguides.

The unique combination of long, low-loss and compact delay lines and compact echelle gratings recently enabled also novel buffering and routing architectures [11], [12]. Mach-Zehnder interferometers (MZIs) with compact and low-loss spirals have been used to demonstrate also differential phase-shift keying (DPSK) demodulation [13].

B. Echelle Gratings and AWGs

The most used component for doing wavelength division multiplexing has been the arrayed waveguide grating (AWG) [14], [15]. The device is straight-forward to manufacture using standard passive waveguides, and unlike cascaded Mach-Zehnder multiplexers, can achieve high channel counts with low insertion loss and low cross-talk [16]. An example of an 1 × 4 AWG on 3 μm SOI is shown in Fig. 3(a) and the corresponding measured spectra in Fig. 4. The measured average channel insertion loss was 3.5 dB and the cross-talk −25 dB. As shown, polarization independent components in the 3 μm SOI platform can be designed simply by tuning the waveguide widths in the array section. Also, the size of the devices is compact as the array section uses multi-mode strip waveguides with the Euler bends.

An alternative component for wavelength multiplexing is the echelle grating, shown in Fig. 3(b). The fundamental operating principle is the same as in AWG but, depending on the

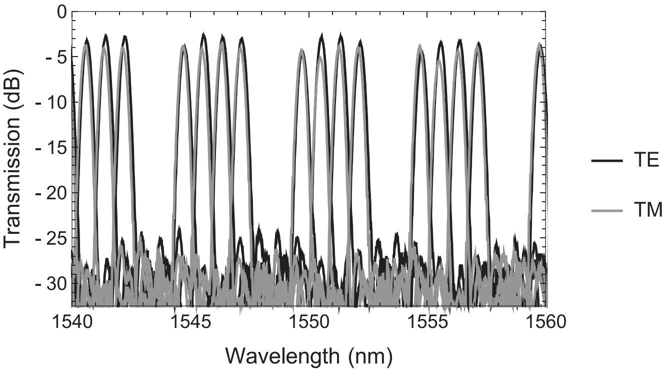


Fig. 4. Measured transmission spectra of the 1 × 4 AWG depicted in Fig. 4(a). Low polarization dependency is achieved by adjusting the waveguide width in the array section for a near-zero birefringent cross-section.

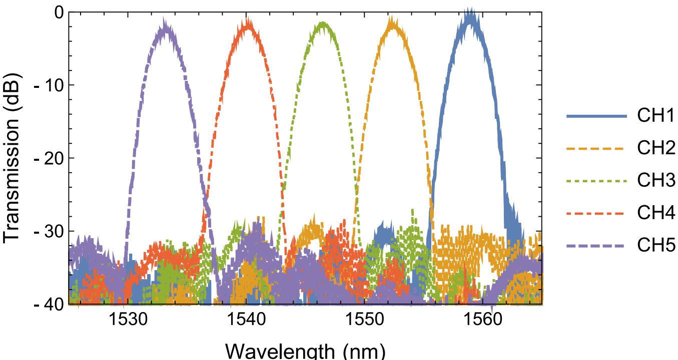


Fig. 5. Measured transmission spectra of the 1 × 5 echelle grating depicted in Fig. 3(a).

configuration and the required channel spacing, an echelle can achieve still lower losses and lower cross-talk in a much smaller footprint, and is therefore an attractive alternative [17]. The performance of an echelle is, however, greatly influenced by the quality of the back-reflecting facets of the grating and these have been traditionally difficult to realize in integrated optics. Both the facet verticality and the etch quality affect the losses and the crosstalk, and therefore need to be controlled. A separate silicon through-etch step has been used in the 3 μm SOI processing to create the echelle facets. The same etch step has been used to create the edge-coupling waveguide facets where the etch quality is also important. To enhance the back-reflection, the grating has been coated with aluminum, leaving a thin silicon dioxide layer between the silicon and the metal. The measured transmission spectra of the echelle in Fig. 3(b) are given in Fig. 5. The result shows an insertion loss of 1–2 dB and cross-talk of −28 dB.

C. MMI-Based Filters and Multiplexers

Interferometric filters can be also synthesized by suitable combinations of simple splitters and delay lines [18], [19]. Compact power splitters are actually a challenge on a micron-scale silicon platform. Directional couplers based on rib waveguides are several millimeters long, no matter the etch depth or the gap, because of the inherent low index contrast of the rib waveguides, limiting the difference of the effective indices of the two supermodes. On the other hand, if strip waveguides are used, tight light confinement prevents any coupling to adjacent waveguides. Therefore, the only viable choice is using multimode interference (MMI) splitters, which are typically in the 100 μm scale when single polarization operation is acceptable, and must be scaled up to about 1 mm when polarization insensitive operation is required [20]. Ring resonators with MMI splitters have been demonstrated achieving quality factors up to 2×10^4, finesse up to 16 [21] and free spectral ranges (FSR) in the order of some hundreds of gigahertz, i.e., a few nanometers in the C-band. Very simple MMI resonators have also been demonstrated for the first time both based on metal mirrors and MMI mirrors, [22] showing comparable performances.

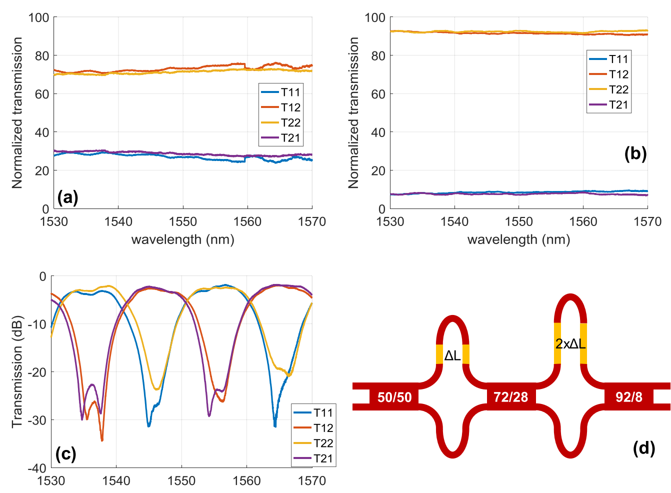


Fig. 6. Broadband response of (a) 72:28 and (b) 92:8 tapered MMIs, and spectral response (c) of the second-order MMI sketched in (d).

Lattice filters based on MZIs have been demonstrated [23] with losses lower than 0.2 dB per MZI. Higher order MZIs have been also designed and fabricated that ensure flat-top response [24], and even better performance was obtained using ring-loaded MZIs [21]. The arbitrary splitting ratios required in most filters have been achieved using double-MMIs, either with tapered [25] or bent [24] connecting waveguides. Recently, also a different approach has been used, that is tapered MMIs [26], which led to very broadband operation (see Fig. 6) and superior robustness to fabrication errors.

In general, very high tolerances of the devices to fabrication errors have been observed, from chip to chip and even from wafer to wafer [21], [23]. It has been verified that even linewidth departures up to 200 nm from the nominal values, affects only the overall losses but not the designed type of spectral response.

D. Thermo-Optic and Electro-Optic Devices

The standard process includes only one level of implantation for both types p and n, and with relatively high doses. We use p-type doping to create relatively short (50 to 100 μm) resistors besides the waveguides (see Fig. 7), e.g., for thermo-optic

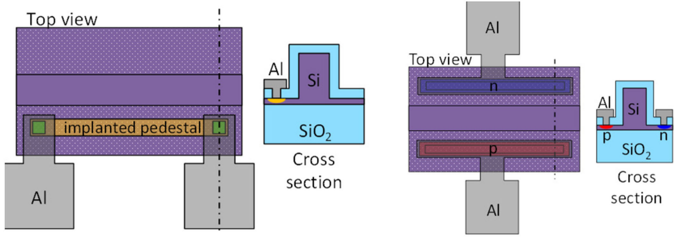


Fig. 7. Two types of phase shifter: the thermo-optic phase shifter with implanted heater and the PIN junction for carrier injection.

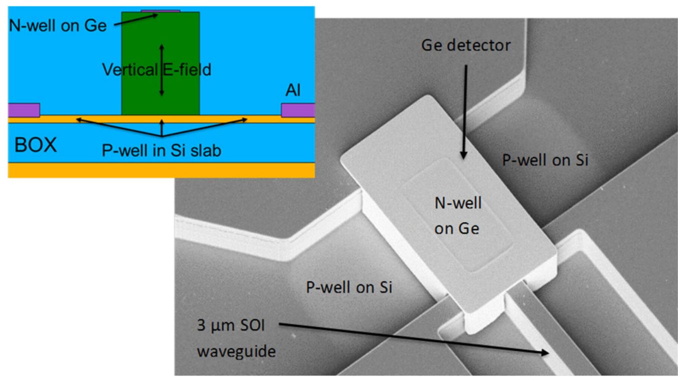


Fig. 8. Schematic illustration and SEM picture of a vertical Ge PIN detector. No visible defects can be seen after the CMP and dry etch. SEM picture was taken prior to metallization.

switches. Lowest power consumption demonstrated so far is about 25 mW. Simulations show that, by selectively removing the Si substrate underneath the heater, it should be possible to suppress the power consumption close to 1 mW. Cross-talk levels are lower than −25 dB over a broad wavelength range (>50 nm) and can be lower than −40 dB in a narrow band (about 5 nm). Excess loss is below 0.5 dB. Typical time response of the switches is 30 μs. When higher speed is required, advanced modulation methods [27] can be exploited, or phase shifters based on carrier injection. In this latter option, a silicon pedestal is implanted with p-type on one side and n-type on the other side of a waveguide, and then carriers are injected through the resulting PIN junction. This way, switching speeds up to 2.5 MHz have been demonstrated, with power consumption smaller than 5 mW. The only drawback of this approach is the losses induced by the injected carriers. Indeed, long enough PIN junctions can be effectively used as variable optical attenuators [28]. Even faster modulation is possible with the Franz-Keldysh effect in SiGe alloys. This has been demonstrated to ensure fast amplitude modulation also in micron-scale waveguides [29], [30].

E. Ge Photodiodes

Ge-based monolithic waveguide PIN photodetectors (PD) have been developed on 3 μm SOI. Also Ge avalanche photodetectors (APD) have been developed for bi-directional optical sub-assemblies (BOSA) for optical transceivers. The aim has been to develop efficient detectors in terms of high responsivity and low power consumption (monitor PD) and high bandwidth (receiver PD). One of the advantages of the 3 μm SOI platform is that it enables efficient butt coupling of detectors to optical waveguides. In the telecommunication wavelength range this enables compact devices with small junction capacitance, as the absorption length is typically less than 10 μm. PIN detectors have been fabricated in both lateral and vertical geometry. The lateral detector geometry requires Ge deposition before the waveguide patterning but it allows fabricating less than 1 μm wide (intrinsic) I-region, which enables small transit time. This kind of detector can reach 35 GHz 3-dB bandwidth, if it can maintain the high E-field needed for the maximum carrier drift speed in Ge [31], [32]. Initial results at VTT have confirmed this, and reached up to 40 GHz 3-dB bandwidth. The vertical detector is easier to fabricate because Ge is deposited after the waveguide patterning. In this design, the maximum bandwidth is compromised, since the I-region is almost 3 μm wide as it is defined by the waveguide thickness.

The vertical detector geometry is shown in Fig. 8. Both detector geometries utilize selective reduced pressure chemical vapor deposition (RPCVD) Ge epitaxy, which means that the Ge is grown only in the etched cavities. After Ge epitaxy chemical mechanical polishing (CMP) is applied to planarize the surface. The Ge-first approach (lateral geometry) allows self-aligned butt coupling of the I-region with the silicon waveguide and patterning of <1 μm wide detector (limited by the lithographic resolution). As the optical axis of the waveguide is in the middle of the detector, only small amount of light is absorbed in the P- and N-regions, which reduces the amount of slow diffusion current. After the detector patterning, the Ge slab and the detector sidewalls are implanted. Ti/Al contacts are made directly on the Ge slab. In the vertical geometry, the Ge is deposited after the waveguide patterning and the p-contact is made on the Si slab. This Ge-last approach allows higher thermal budget in the previous process steps, since the n-contact is implanted late in the process, and fast N-type dopant diffusion in Ge [33] is not a limiting factor. In the vertical APD, the Si multiplication and charge areas are placed laterally in the Si slab and the Ge absorption layer is epitaxially grown on the charge layer.

The measured responsivity of a 1.5 μm wide lateral PIN is shown in Fig. 9. Responsivity is about 0.9 A/W and the dark current for this device is about 1 μA at −1 V reverse bias. For the APD, a maximum responsivity of 19 A/W at −44 V reverse bias was obtained. The punch-through voltage was about −10 V. The APD capacitance was about 35 fF according to the S11 measurements at −20 V. The 3 dB bandwidth was measured to be about 0.7 GHz.

IV. Up-Reflecting Mirrors for Wafer-Level Testing (WLT) and Vertical I/O Coupling

With all the useful functionalities that a photonic chip can provide, it is also important to look into the light coupling efficiency in and out of the chip. For these purposes, cleaved or polished end facets, gratings couplers, and metallized up-reflecting mirrors (Fig. 1) have been in use for some time now. Cleaved or

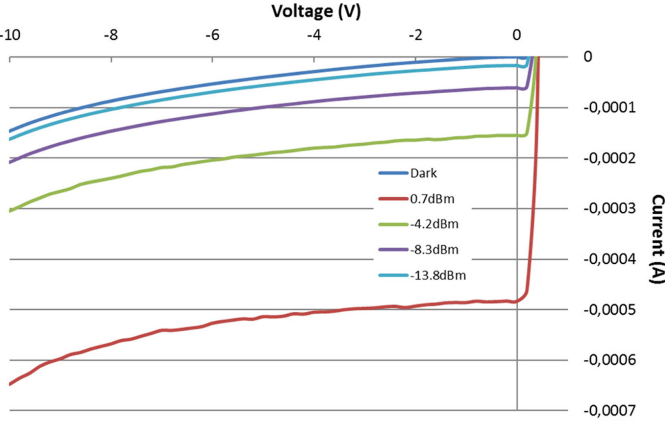


Fig. 9. Lateral PIN detector responsivity measured at 1510 nm. Good response with low reverse bias is seen.

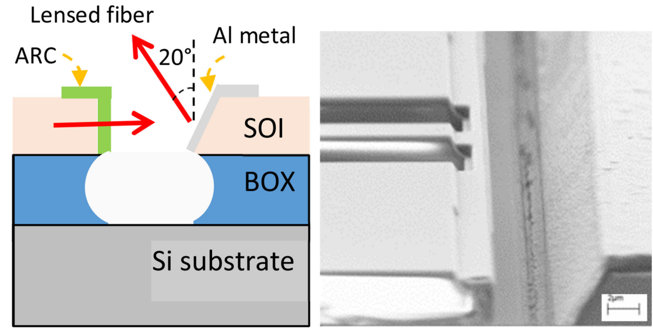


Fig. 10. Schematic (left) and SEM (right) image showing a fabricated up-reflecting 54.7° external mirror on 3 μm SOI.

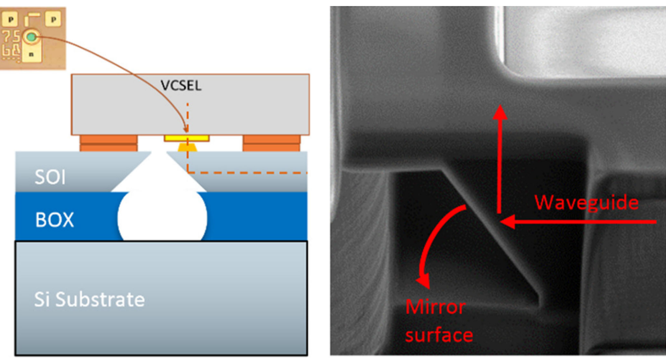


Fig. 11. Schematic and FIB cross-section image showing a fabricated up-reflecting 45° TIR mirror on 3 μm SOI. Also VCSEL integration is shown.

polished end facets are the easiest to fabricate, but they suffer from many disadvantages such as their availability only at the edges of the chip, and always at the end of the fabrication process cycle with no possibility for wafer-level anti-reflection (AR) coating or wafer level testing (WLT). While they can be useful in hybrid integration of chips from multiple fab platforms in a horizontal end-fire coupling architecture, they cannot be used for chip-on-chip integration, and it is non-trivial to integrate individual light sources, detectors or other components at these sites directly. Grating couplers, on the other hand, can be placed anywhere on the chip and provide the possibility of WLT. However, they have limited bandwidth (∼40 nm), and traditional designs usually have low coupling efficiencies (∼−4 dB) into fiber. With linear grating apodization designs, low coupling efficiencies (−2.7 dB) have been demonstrated [34], [35], and the record value reported stands at −0.62 dB achieved using an Al back-reflector in a 250 nm SOI wafer [36]. In addition, they need very high-resolution lithography tools (below 20 nm), the designs can get very complex for higher coupling efficiencies or polarization insensitive applications, and are very sensitive to fabrication tolerances. In comparison, metal mirrors are well recognized for their light steering behavior, and are quite preferred in applications requiring broadband functionality, wavelength and polarization insensitivity. The standard wet etch of (100) Si yields 54.7° tilted mirror surfaces corresponding to the 111 planes of Si, which have been used as external mirrors for coupling light in and out of the chip or wafer on the VTT 3 μm SOI platform. This is shown in Fig. 10, and reasonably good performance with coupling loss of about 1.8 dB has been demonstrated when the mirror surface is coated with Al. By placing them at strategic locations on the chip or wafer, they allow for WLT possibility, and for testing devices even in the middle of fabrication runs. This, in turn, has significant commercial value when moving towards early error detection, automation, volume production, and wafer level packaging.

While the metal mirrors have numerous advantages mentioned above, they are not ideal for chip-on-chip optical integration, or for component integration on the chip such as vertical-cavity surface-emitting lasers (VCSELs) and detectors. This is due to their non-orthogonal coupling and the beam divergence between the waveguide facet and the mirror surface. For most applications, a 45° mirror would be ideal, and with a TIR mirror it is possible to obtain the highest possible reflection coefficient at any wavelength, and independent of fabrication tolerances. Moreover, they can perform all the functionalities that are offered by the 54.7° mirror. Although the standard Si wet etching produces 54.7° angles, additional surfactant can change the etch chemistry to produce 45° mirrors. To realize these on the 3 um SOI technology platform, the SOI layer was first dry-etched through to reach the BOX layer. The top and side-walls were then passivated and the BOX layer was over-etched to expose the bottom corner of the SOI layer. This was followed by a Si wet etch step that resulted in the final mirror surface (Fig. 11). The schematic in Fig. 11 shows the idea of integrating VCSELs directly on top of a chip with the 45° TIR mirrors.

The 45° vertical coupling TIR mirrors have been integrated with waveguides, and the coupling losses to/from lensed fibers have been estimated over the 1520–1580 nm range. As shown in Fig. 12 below, the total coupling loss for the reference waveguides with polished facets (facet input and facet output) is in the range of 2.0–2.8 dB (so 1.0–1.4 dB per facet, including some reflections due to imperfect AR coating), while for the mirror integrated waveguides (facet input and mirror output) these are in the 1.1–1.5 dB range, for both polarizations (excluding a few outliers which could be due to damaged waveguides). This clearly

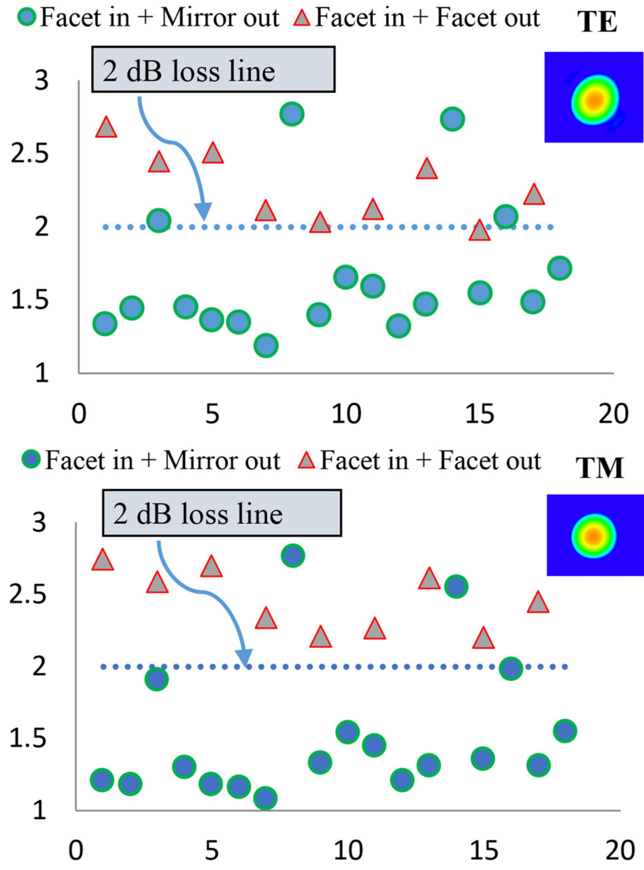
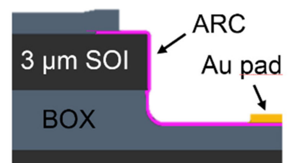


Fig. 12. Insertion losses of different test waveguides (numbered on the x-axis) with and without the up-reflecting mirrors. The mirrors have clearly lower losses than the polished waveguide facets at both polarizations.



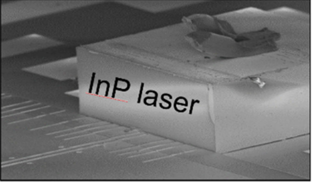


Fig. 13. Structure of a flip-chip mount (left). Hybrid integrated InP laser on a Thick-SOI chip (right).

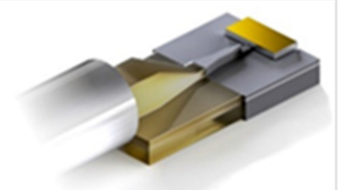


Fig. 14. Schematic view (left) of a silicon interposer between an optical fiber and 3 μm SOI chip. Also a flip-chip integrated laser chip is included here. Pigtailed chip prototype (right) with 3 μm SOI PIC, 12 μm SOI interposer and a SSMF array.

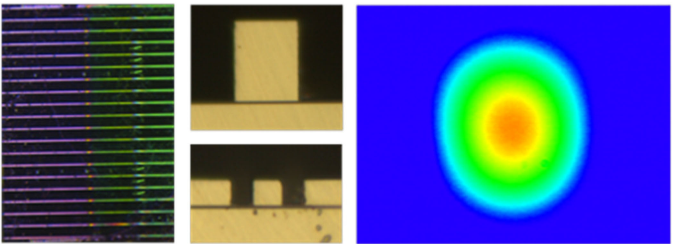


Fig. 15. A 12 μm interposer with an array of polished waveguides (left). Waveguide spacing is 250 μm and the length of the interposer 3.8 mm. Waveguide profile changes from 12 μm by 9.5 μm (top) to 3 μm by 3 μm (bottom). Measured output mode field (right) confirms the single mode operation of the waveguide taper.

indicates that the mirror to fiber coupling loss must be below 0.5 dB over the entire C-band, and for both polarizations.

V. Horizontal I/O Coupling and PIC Packaging

Horizontal end-fire coupling through an etched waveguide facet can be used for coupling light from/to optical fibers, edge-emitting lasers, amplifiers and modulators. Single layer of Si_3N_4 or TiO_2, double layer SiO_2/Si_3N_4 or TiO_2/Al_2O_3 nanolaminate is used as an anti-reflection coating. Facet reflectivity can be reduced to $<0.5\%$ or $<0.1\%$ with single or double layer ARC, respectively, either on 1.3 or 1.55 μm wavelength band, by tuning the thickness of the AR coating. Currently developed broadband multilayer ARC solutions target $<0.1\%$ reflectivity in a full wavelength range from 1.2 to 1.7 μm.

Hybrid integration of light sources and high-speed modulators has been realized on the 3 μm SOI platform using primarily Au-Au thermo compression bonding [37]. One key advantage of this concept is excellent thermal contact. An illustration of the flip-chip mount and some examples of light sources and modulators integrated on the 3 μm SOI platform are shown in Figs. 13 and 17.

Lensed fibers with 2.5 μm spot size can be used to couple light to 3 μm waveguides, especially when characterizing the chips. The coupling loss and the internal loss of the lensed fiber together are approx. 1.5 dB and the finite working distance avoids any physical contact with the chip. However, lensed fibers are not practical for chip packaging where permanent fiber pigtail arrays need to be attached to the chip with good alignment accuracy. The coupling loss between a horizontally tapered 3 μm SOI waveguide (width 11 μm) and a standard SM fiber (SSMF) is approx. 5 dB, which makes this direct coupling approach too lossy for most applications. The coupling loss between the SSMF and an untapered 3 μm waveguide is even worse, approx. 7 dB.

For packaging purposes, a special optical interposer chip has been developed on 12 μm thick SOI. The 12 μm thick waveguide with the same waveguide width has a good mode matching with SSMF. Adiabatic tapering of the 12 μm waveguide both vertically and horizontally to 3 μm size produces a spot-size converter (SSC) structure that enables low loss fiber coupling to a 3 μm SOI waveguide. Fig. 14 shows an example of such optical interposer and Fig. 15 shows an actual interposer chip realized in 12 μm SOI. Here, the input waveguide size at the SM fiber end of the interposer is 12 μm by 9.5 μm. Horizontal tapering has been realized using tapering waveguide structure in the optical

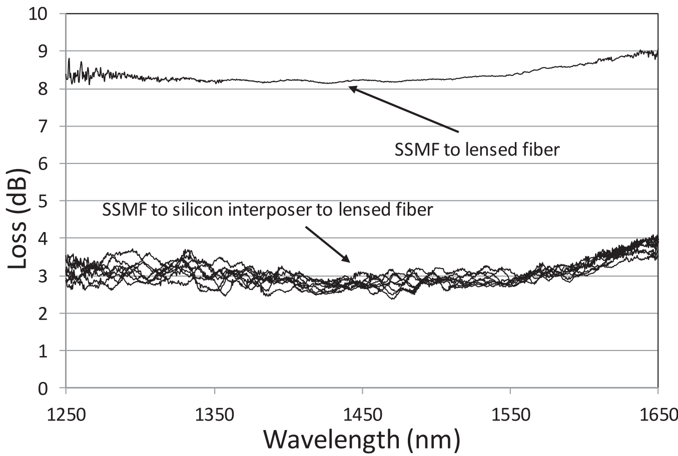


Fig. 16. Measured coupling loss from a standard SSMF to the lensed fiber (2.5 μm diameter) through a polished silicon interposer. Measured spectra for eight adjacent channels show repeatable operation. Coupling directly from an SSMF to lensed fiber has significantly higher coupling loss. Losses related to the lensed fiber are still included in the measured loss values.

lithography mask. Vertical tapering has been realized by polishing the chip surface in an angle so that the other waveguide end remains in 12 μm thickness but the thickness in the other end is reduced to 3 μm. Tapering angle has been kept small (0.28°) in order to ensure adiabatic tapering. After the taper has been polished on chip-level, the chip facet is polished and a TiO_2/Al_2O_3 nanolaminate AR coating is applied on chip level using atomic layer deposition (ALD).

Insertion loss measurement of the fabricated interposers has been made by coupling unpolarized light from a SSMF to the 12 μm waveguide and using a lensed fiber to collect the light at the 3 μm waveguide end. This effectively corresponds to coupling from a SSMF to a 3 μm Si waveguide and simultaneously allows to characterize the insertion loss of the waveguide interposer without permanently attached fiber pigtails. Measurements show that with the silicon interposer, the coupling between a SSMF and a lensed fiber can be improved by 5.5 dB in a very broad wavelength range compared to the situation with no silicon interposer in between the fibers (Fig. 16). The same loss reduction can be achieved also when silicon interposer is used in coupling from SSMF to 3 μm SOI waveguide. Fig. 16 shows also that adjacent channels are working in a repeatable way. It is noteworthy, that the losses of the lensed fiber are still included in the measured loss value. Also the loss curve shape is due to the wavelength dependence of the lensed fiber operation. Measured coupling loss is comparable or even lower to the corresponding coupling loss values reported recently for SM fiber coupling to submicron SOI waveguides [38].

Figure 14 shows a pigtailed chip prototype with 3 μm SOI PIC, 12 μm SOI interposer and SSMF glued together on a packaging substrate. In addition to improving the 12 μm SOI interposer fabrication process and performance we are currently also developing our wafer level packaging (WLP) capabilities.

VI. Faraday Rotation in Thick SOI Waveguides

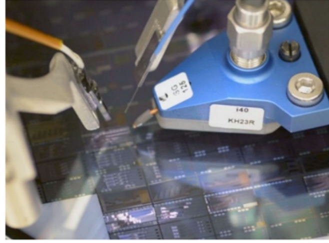
A unique opportunity for the micron-scale silicon platform is the exploitation of Faraday rotation of silicon itself. In fact, the Verdet constant of silicon is only two orders of magnitude smaller compared to iron garnets, whereas propagation losses are much smaller. In practice, this means that, with a magnetic field of 0.5 T (that is achievable with a standard neodymium magnet), 45° Faraday rotation would require a 6 cm long zero-birefringent silicon waveguide, In practice, the birefringence should be small enough compared to the strength of Faraday rotation. In collaboration with the Hamburg University of Technology, it has been recently proposed and demonstrated how to achieve the rotation in a compact spiral waveguide that has equivalent length to a straight waveguide aligned with the magnetic field, even if the waveguide direction varies in the spiral [39]. The work is still in progress, to show higher isolation levels and fully integrated isolators and circulators by adding polarization splitters and reciprocal rotators. This would represent a major breakthrough, especially when combined with hybrid integration of lasers.

VII. Access to Technology and Design Kits

The development of the thick-SOI waveguide technology was started at VTT as early as 1997, and it has included various R&D activities with SOI thicknesses ranging from 1 to 12 μm. Low-cost access to the 3 μm SOI waveguide platform was launched via multi-project wafer (MPW) runs under ePIXfab with the support of the EU project ESSenTIAL. An important step in opening the access to this technology was the preparation of a process design kit (PDK) that allows external users to make their own designs and to participate MPW runs without the need to have their own fabrication facilities. Presently, the PDKs are available in Synopsys and IPKISS software. Two MPW process modules, namely passive module and active module, have been offered in 2014–2018. With the passive module, basic waveguide structures can be achieved, and optical data processing functionalities like multiplexing and filtering can be realized. More advanced functionalities such as active tuning and hybrid integration are possible with the additional active module that includes p and n type implantation and Al metallization. Standard chip size in MPW runs is 5 $\times$ 10 mm, with deep-etched chip facets to support the end-fire coupling of fibers and fiber arrays to the waveguide facets.

Most of the results shown in this paper are based on chips fabricated in MPW runs, while some of the results, like Ge photodiodes and up-reflecting mirrors, have been obtained from dedicated R&D runs. One goal of the dedicated runs is to develop new building blocks for the future MPW runs. Both Ge photodiodes and up-reflecting mirrors are planned to be included in MPW runs at the latest in 2020.

For both MPW runs and dedicated runs, major fabrication steps in wafer processing include Si waveguide etching, waveguide cladding deposition, AR coating on waveguide facets, ion implantations, metallization and patterning of metal layers. The repeatability and yield of the process steps are being continuously monitored and developed. All the individual processing steps and the whole process integration have been developed in the Micronova clean room facility in Espoo, Finland (http://www.micronova.fi). It is jointly used by VTT (https://www.vtt.fi/siliconphotonics), Aalto university, a number of industrial companies and VTT Memsfab Ltd.



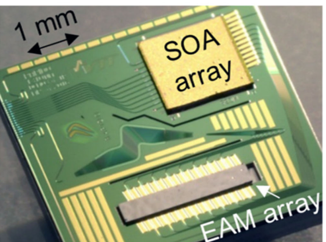


Fig. 17. Simultaneous optical and electrical testing of a 3 μm SOI wafer (left). Diced 3 μm SOI chip with etched and anti-reflection (AR) coated input/output (I/O) facets, as well as semiconductor optical amplifier (SOA) and electro-absorption modulator (EAM) arrays hybrid-integrated on top (right).

(www.vttmemsfab.fi) that offers contract manufacturing services for the technologies developed in Micronova, including Si photonics. Furthermore, Rockley Photonics is commercializing the versatility of the thick-SOI platform for large volume applications, including sensing (https://rockleyphotonics.com/rockley-targets-high-volume-sensing-and-imaging-markets) and high-data-density in-package optics for datacenter communications [25].

One important aspect in ramping up both R&D and manufacturing activities is fast and automated testing. Figure 17 shows a 3 μm SOI wafer with up-reflecting metal mirrors being tested with an automated WLT setup. Testing is done automatically, and simultaneously with electrical and optical signals. Hence, designs and chips can be characterized at the wafer level, and at multiple points during the fab cycle. Another important aspect is assembly and packaging, which was discussed in Section V. Figure 17 shows a 3 μm SOI chip that was fabricated in an MPW run and later equipped with hybrid integrated amplifier and modulator arrays.

VIII. Conclusion and Future Work

An open-access PIC platform on 3 μm SOI is a versatile tool for doing research, prototyping and small-to-medium volume production in silicon photonics, or photonics integration in general. This technology is very general and can be used in various application fields from communication to sensing. The main advantages of thick-SOI technology are low optical losses, ultra-dense integration, small polarization dependency and the ability to tolerate relatively high optical powers. Several building blocks and functionalities are already available via MPW runs, while new ones, like fast modulators, fast photodiodes, athermal multiplexers, on-chip isolators and standard packaging concepts are being developed to include them as mature MPW building blocks in the future.

Acknowledgment

We would like to thank G. Delrosso, S. Ylinen, B. Wälchli, A. Hokkanen, and K. Grigoras for their contributions in developing the mirror etching process, the WLT capability and the chip-level testing, and also would like to thank M. Karppinen, A. Sitomaniemi, N. Heinilehto, J. Ollila, and T. Haatainen for their contributions in developing the hybrid integration and packaging technologies.

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