Monolithically Integrated CMOS-Compatible III–V on Silicon Lasers

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***Abstract*—CMOS-compatible III–V lasers integrated on silicon are a crucial step to reduce power consumption and cost for next-generation optical transceivers. Here, we demonstrate a concept to co-integrate III-V lasers into a CMOS Silicon Photonics platform, in which lasers, photonics, and electronic circuitry share the same back end of line. Based on a bonded III–V epitaxial layer stack, ultra-thin laser devices, optically pumped lasing and coupling to silicon are demonstrated. Furthermore, we present all building blocks for electrically pumped laser devices.**

***Index Terms*—CMOS, III-V, Laser, Silicon Photonics.**

I. Introduction

DATACENTERS represent the backbone of modern, data-rich applications such as cloud computing, analytics and streaming video [1]. Their performance is based on interconnected servers and thus the network of a datacenter is crucial for its operation. Increasing data traffic [2] forecasts demand for high-throughput and low-latency networks. Cost-efficient optical interconnects are the technology of choice that provide the required bandwidth, distance, power efficiency and density [3], [4].

In contrast to electrical links, for which the signal is also the carrier, in optical communication the signal is modulated on a carrier operating in the 200 to 300 THz range. This gives rise to large bandwidth, low loss and long-distance links, according to the physics and materials properties at optical frequencies. However, to transmit and receive optical signals, more components and assembly steps are required as compared to an electrical link. A typical optical transceiver (transmitter and receiver) contains at least the following three building blocks that need to be assembled; active optical devices (laser and photodetector), an optical modulator and electrical circuits. Assembly of these building blocks represent a substantial fraction of the total transceiver cost [5], [6]. Hence, a monolithic integration of these components is a worthwhile route to explore for reducing cost. Furthermore, tight integration of these building blocks will have a positive impact on the functionality, performance and density [7]. Already today, the CMOS-compatible Silicon Photonics platform is an integration scheme in which all building blocks except the laser can be fabricated on the same chip [8]. One path to integrate lasers on Silicon Photonics is the heterogeneous integration approach of III-V on silicon [9]. A well-explored concept to integrate large areas of III-V on silicon is the molecular wafer bonding technique [10]. This has enabled the realization of on-chip lasers [11], [12], photodetectors [13], [14] and modulators [15], [16]. To reduce the cost of such devices further, it is desirable to use standard chip assembly techniques that preserve the cost advantages of CMOS chips throughout the packaging. Silicon chips that comprise a standard CMOS back end of line (BEOL) are a prerequisite for applying standard assembly techniques. Furthermore, the BEOL interconnectivity stack is mandatory for co-integrating the III-V devices with CMOS or Bi-CMOS circuitry, such as drivers and amplifiers. This creates advanced capabilities such as directly modulated lasers monolithically integrated with passive Silicon Photonics structures and the electrical circuitry. The following analysis shows the potential power-efficiency advantage of such an approach.

Coupling an external laser to the Silicon Photonics chip through a grating coupler introduces an optical loss of typically -3 dB [5]. Consequently, an on-chip laser can be operated at half the optical power of an external one, substantially reducing its electrical input power. Furthermore, the insertion loss of a silicon optical modulator is roughly -3 dB [17]. Therefore, in some cases in which power consumption is of paramount importance, directly modulated lasers instead of continuous-wave (CW) lasers can make modulators unnecessary. Consequently, a directly-modulated on-chip laser can be operated at half the optical power of an on-chip CW laser which uses an additional modulator. This reduces again the electrical

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TABLE I
POWER CONSUMPTION OF SI-PHOTONICS TRANSCEIVER

Electrical power consumption	Current Silicon Photonics	Silicon Photonics with on-chip laser	Silicon Photonics with directly-modulated on-chip laser
Laser	200 mW	100 mW	50 mW
Driver	100 mW	100 mW	100 mW
Amplifier	100 mW	100 mW	100 mW
Total link @ 25 Gbps	400 mW	300 mW	250 mW

input power of the laser by 50%. Furthermore, we assume that the driver of a laser consumes the same amount of power as the driver of a modulator. Table I summarizes these estimated calculations, assuming a power consumption of 4 mW/Gbps for both the driving circuit and the transimpedance amplifier in the receiver [18]. Additionally, we estimate a wall-plug efficiency of 10% for the laser and a required optical launch power of 20 mW. This estimation clearly shows the strong potential of integrated lasers for reducing the power consumption of optical transceivers.

However, most integrated laser devices shown so far make use of a several micrometer-thick III-V layer stack, which hinders their integration into a common CMOS BEOL. To overcome this drawback, we integrate an ultra-thin III-V epitaxial layer stack between the front end of line (FEOL) and BEOL of a CMOS Silicon Photonics chip. The integration scheme presented here reduces assembly and signal routing complexity. Furthermore, the possible combination of CMOS electronics with passive and active optical building blocks on a single chip brings new and important opportunities for system-level integration of optical interconnects such as a tight and dense co-packaging with the processor or switch-chip. Both, the reduction of cost and power consumption are seen key for future high-speed and high-volume integrated optical technologies.

II. CONCEPT AND DESIGN

The III-V gain layer for the laser devices presented in this work is integrated between the FEOL and BEOL of a CMOS chip, within the first interlayer dielectric ILD0' as shown schematically in Fig. 1(a). The laser consists of two vertically separated waveguides as shown in Fig. 1(b) together with the simulated intensity field. The passive silicon waveguide is positioned at the bottom and the active III-V layer stack on top. The silicon waveguide has a thickness of 220 nm, the III-V layer stack is thinner than 300 nm. The latter is a requirement for obtaining compatibility with the BEOL dimensions of modern CMOS processes. The silicon waveguide and the III-V layer are separated by 300 nm of silicon dioxide. While the III-V layer stack provides optical gain, the laser cavity is formed by means of fully-etched Bragg mirrors in the silicon waveguide with 7 periods on one side and 3 periods on the other side of the gain section. The mirror reflectivities of 99 % and 92 %, together with their stop-band width of 400 nm were calculated with the FDTD method [19], using an open source software package [20].

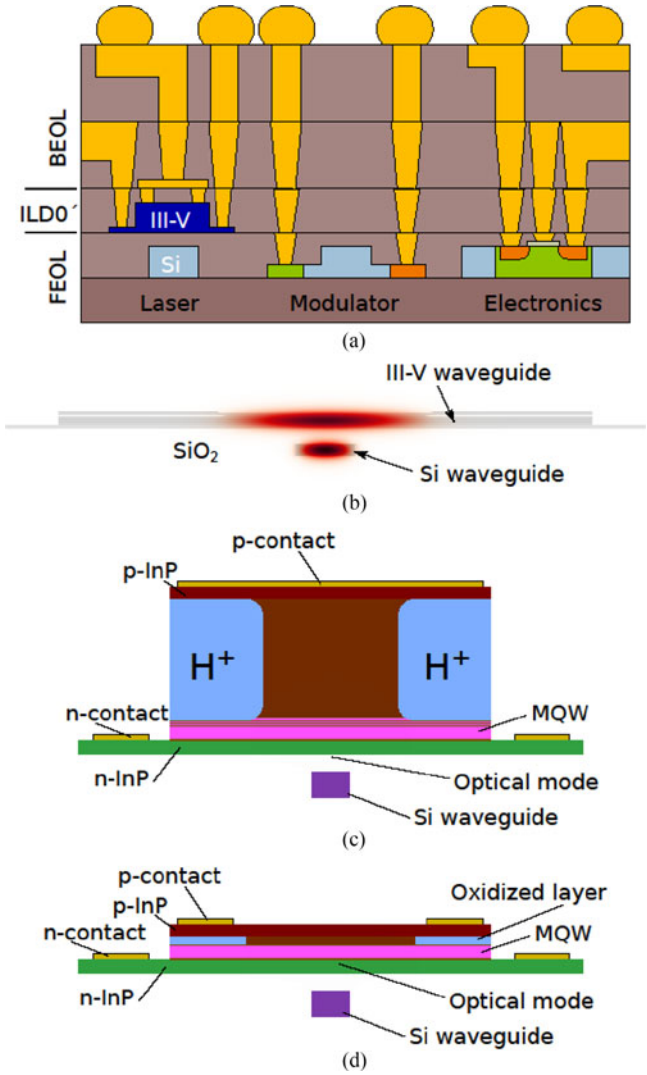

Fig. 1. (a) Schematic cross-section of the CMOS Silicon Photonics layer stack, showing the III-V gain layer, integrated between FEOL and BEOL. (b) Simulated intensity field of the fundamental mode of the laser device. (c) Schematic cross-section of conventional heterogeneously integrated III-V laser with a μm-thick epitaxial layer stack and hydrogen implantation. (d) Schematic cross-section of our laser concept, based on a thin III-V epitaxial layer stack and selective lateral oxidation.

To couple the III-V gain section to the silicon cavity, low-loss mode conversion between the two waveguides is necessary. To facilitate this, the effective refractive index of the silicon waveguide was designed to be higher than the mode index of the III-V waveguide. This is achieved by selecting an optimized vertical spacing together with a matched III-V layer stack thickness. In this configuration, the mode is highly confined in the silicon waveguide for wide waveguide designs. Upon reducing the silicon waveguide width, its effective refractive index drops below that of the III-V waveguide at some point and the mode is thereby transferred to the latter as shown in Fig. 2(a). To make this transition as loss-less and as short as possible, the silicon taper was designed in a non-linear fashion by means of the adiabaticity criterion [21], [22]. The resulting taper geometry is shown in Fig. 2(b). Having the mode transition fully controlled

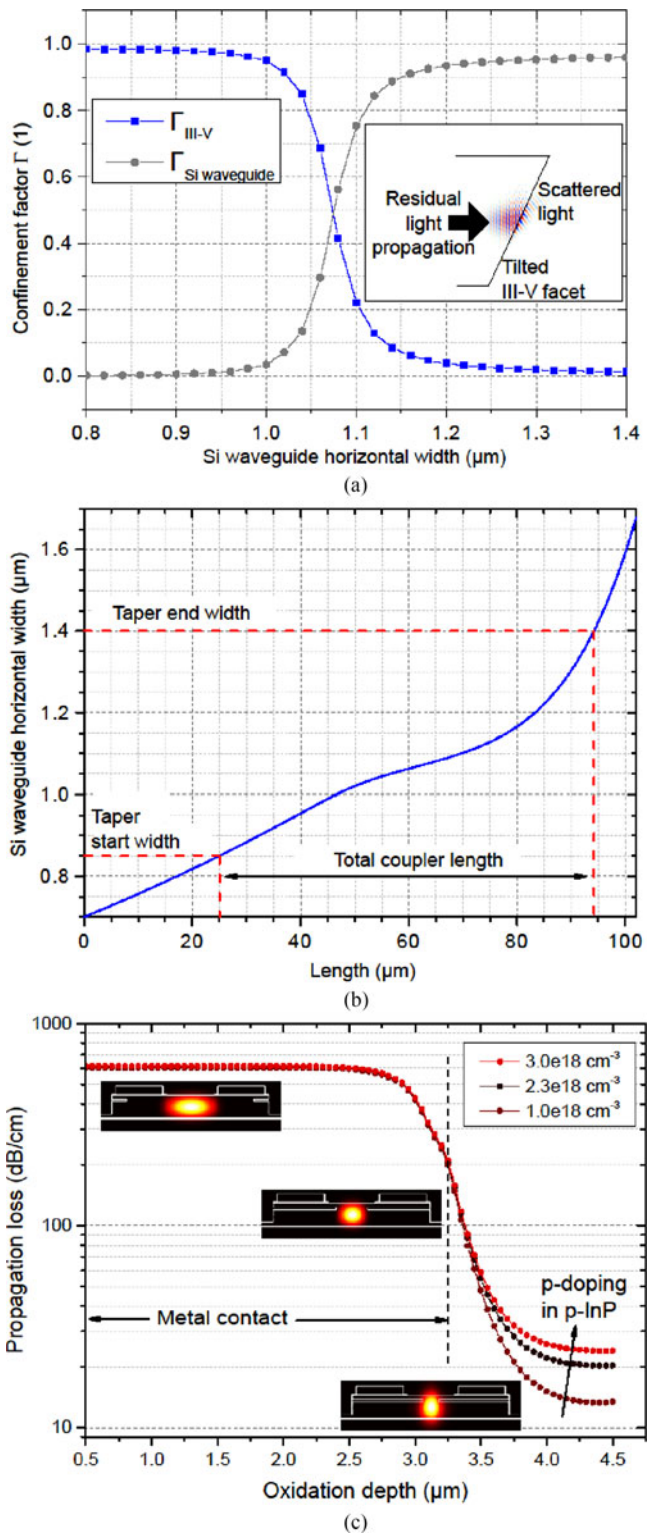

Fig. 2. (a) Confinement factor of the fundamental mode relative to the III-V layer stack (blue squares) and the silicon waveguide (gray circles). Inset: top-view schematic with simulated electric field of the residual light, scattered by the tilted III-V end-facet. (b) Nonlinear taper geometry for the silicon waveguide, resulting from an adiabatic design criterion. (c) Calculated propagation loss in the III-V waveguide vs. oxidation depth for three different p-doping levels. Insets: simulated electrical mode field cross-section, overlaid with the structure at three different oxidation depths. The metal contacts are visible on top of the III-V waveguide.

by the silicon waveguide width overcomes the necessity for a precise taper in the III-V waveguide. A down-tapering of the III-V waveguide relies on a very sharp tip, as a coarse waveguide end is associated with back-reflections which can form an additional cavity [23]. Our mode transformer reduces the mode overlap with the III-V stack down to 2 %. This residual light is scattered away at the end of the III-V waveguide using a tilted facet [inset of Fig. 2(a)].

The p-type contact of state-of-the-art laser devices is placed on top of the III-V waveguide and the n-type contact is made from two contact stripes on the lowermost layer of the III-V stack, as shown in Fig. 1(c). Contrary to previously demonstrated III-V on silicon laser integration schemes [12], our III-V epitaxial layer stack is very thin and does not contain a micrometer thick InP layer on top of the device, as shown schematically in Fig. 1(d). A careful placement of the p-type contact at the edges of the III-V waveguide is required to reduce the overlap between the optical mode and the contacts, to prevent absorption losses. Although III-V lasers below 1 μm thickness have been demonstrated [24], [25], they have never been coupled to Silicon Photonics so far.

To avoid the majority of carrier recombination taking place at the edge of our III-V waveguide, current confinement is essential. Hydrogen implantation, as shown in Fig. 1(c), used for μm-thick layer stacks is not feasible for our thin stack. Instead we use a laterally oxidized layer to generate an electrically isolating area on the sides of the III-V waveguide. This is shown schematically in Fig. 1(d). To demonstrate the importance of this oxidized layer, we performed mode simulations on the cross-section of the III-V waveguide with the commercially available software package OptoDesigner from Phoenix Software. Fig. 2(c) shows the calculated propagation loss of the fundamental mode versus oxidation depth. To a large extend this loss originates from the overlap with the metal contact and can be reduced by an order of magnitude through a several microns deep oxidation. The insets in Fig. 2(c) show the cross-sections of the simulated electrical mode fields with the overlaid III-V waveguide structure for three different oxidation depths. The increasing optical confinement with larger oxidation depths is clearly visible. In addition to this optical confinement, the laterally oxidized layer forms a current confinement, such that the recombination of charge carriers take place in the center of the III-V waveguide where the optical mode is located. The positive effect of such a current confinement on the efficiency of a laser is well known from oxide-confined vertical-cavity surface emitting lasers (VCSEL) [26].

A fundamental challenge of the thin III-V waveguide is the overlap between the optical mode and the p-doped InP layer as free carrier absorption increases with higher doping levels. A high p-doping is desired to decrease electrical resistance for the holes that are injected from the top contacts and need to travel several microns laterally before reaching the quantum wells in the non-oxidized region.

The right end of the curves in Fig. 2(c) shows the minimum achievable propagation loss in our structure for three different p-doping levels. This loss originates only from the

free carrier absorption in the p-doped InP layer, optical gain from the quantum wells was not considered for this calculation. Thus, a propagation loss of around 20 dB/cm is inherent in our structure.

III. Fabrication

The Silicon Photonics waveguides were fabricated in the 220 nm thick top silicon layer of a 4" SOI wafer with a 2 μm buried oxide (BOX) below. Electron beam lithography and inductively-coupled plasma – reactive ion etching with HBr were used for this purpose. A SiO_2 cladding layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) and planarized by chemical-mechanical polishing (CMP) to a thickness of 300 nm above the waveguides. The surface roughness after CMP was measured with an atomic-force microscope (AFM) on a $5 \times 5\ \mu m^2$ area and is less than 0.5 nm rms. This value is critical to achieve high-yield molecular wafer bonding [10].

The III-V epitaxial layer stack comprises an InAlGaAs multiple quantum-well (MQW) section (a cross-section is shown in Fig. 3(a), inset), sandwiched between cladding layers of different composition and doped InP contact layers. It was grown by metal-organic chemical vapor deposition (MOCVD) on a 2" semi-insulating InP substrate. The composition and thickness of the MQW were tuned to achieve a room-temperature photoluminescence (PL) peak centered at 1300 nm, as shown in Fig. 3(a). A thin alumina layer was deposited by atomic layer deposition (ALD) on both wafers to promote adhesion for bonding. After thermal annealing of the bonded wafers, the InP substrate was removed by wet chemical etching, leaving only the epitaxial layer stack with a thickness of less than 300 nm on the Silicon Photonics wafer. A photograph of the bonded epitaxial layer stack is shown in Fig. 3(b).

To structure the III-V layer stack, we developed a Cl_2-based dry etch process by means of ICP-RIE. This was necessary to achieve very smooth sidewalls and etched surfaces. The commonly used $BCl_3/Cl_2/CH_4/H_2$ etch chemistry resulted in very rough surfaces on our bonded material [27]. Fig. 3(c) shows a cross-section SEM image of an etched layer stack, for which a sidewall angle of 65° and nearly no trenching is observed.

The metal stacks of electrical contacts on InP are critical for CMOS-compatibility and gold, as usually applied for laser contacts is not an option. The properties of various CMOS-compatible metal stacks were therefore studied using transfer length method (TLM) structures [27], [28]. After passivating and capping the semiconductor, via-openings were etched through the capping and metal was deposited by sputtering. The metal was then patterned by dry etching and finally annealed under forming gas atmosphere. Ohmic behavior for n-type contacts on InP:Sn ($5 \cdot 10^{18}\ cm^{-3}$) was obtained with a Ni/Si stack, resulting in a specific contact resistivity ρ_c of $0.6 - 1.6 \cdot 10^{-7}\ \Omega \cdot cm^2$. Ohmic contacts on p-type InP:Zn ($2 \cdot 10^{18}\ cm^{-3}$) require an additional p-$In_{0.53}Ga_{0.47}As$ cap layer. A Mo/W metal stack yielded best results with ρ_c of $1 \cdot 10^{-5}\ \Omega \cdot cm^2$. The same metal stack can also be used on n-type InP to achieve low-resistive Ohmic contacts, which simplifies the metallization process considerably.

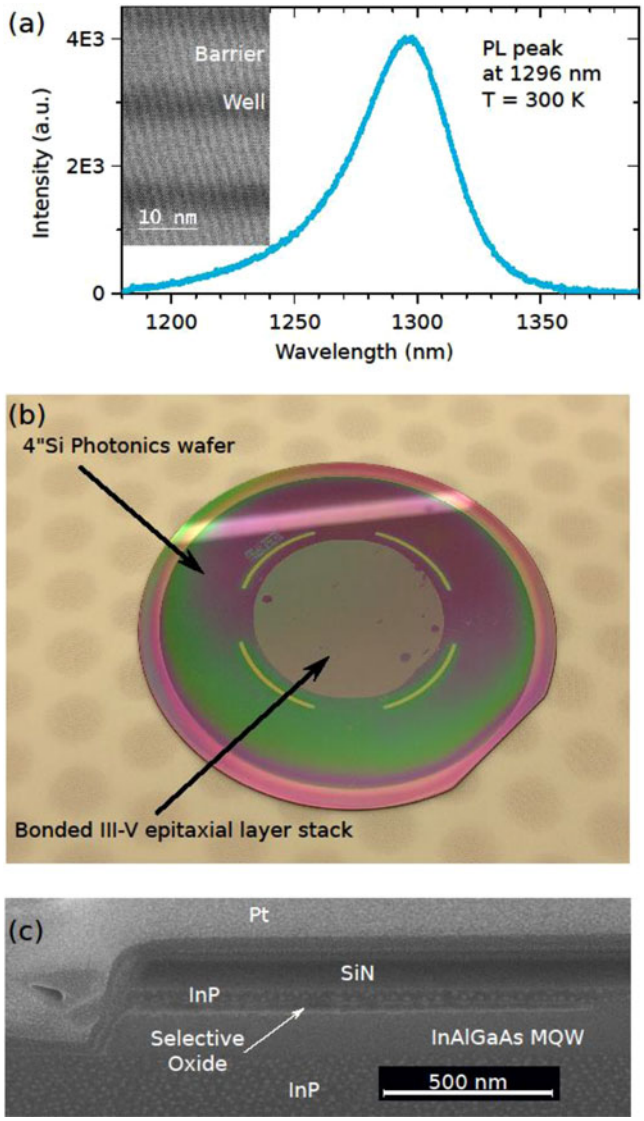

Fig. 3. (a) Room temperature PL measurement of the III-V epitaxial layer stack. Inset: scanning transmission electron microscopy (STEM) image of MQW section with atomically flat interfaces. (b) Photograph of bonded epitaxial layer stack on Silicon Photonics wafer. (c) Cross-sectional scanning electron microscopy (SEM) picture of an etched III-V layer stack with selective lateral oxidation (only one single layer is oxidized).

The above-mentioned p-InGaAs cap layer, required for the Ohmic contacts on p-type InP, absorbs light at 1300 nm due to its band gap. It was therefore removed by selective wet chemical etching everywhere except below the metal contacts. Two p-contacts were placed on the III-V layer stack at the edge of the III-V waveguide, as shown in Fig. 1(d) to ensure a minimum overlap with the optical mode. To establish lateral mode – and current confinement we performed lateral oxidation of a 30 nm thick $In_{0.52}Al_{0.48}As$ layer via water vapor annealing at 500°C for 1 hour as shown in Fig. 3(c). As our lasers are integrated before processing the BEOL, only the underlying (Bi-)CMOS performance could be affected by this process step. However, stable FET performance has been demonstrated with this thermal budget [29] and thus CMOS

compatibility is ensured throughout this process. The devices were finally capped with 800 nm of PECVD-deposited SiO_2, vias were etched down to the contact metals and a second metal layer was deposited by sputtering and patterned by dry etching.

IV. Experimental Results

A. Optically-Pumped Lasers

To investigate our general laser design concept, we first characterized our devices by optical pumping. The devices that were characterized by optical pumping did neither feature the lateral oxidation, nor the p-InGaAs cap layer on top of the p-type InP as this is only necessary to form Ohmic contacts. We used a fiber-coupled pump laser with a wavelength of 980 nm, which we injected into a custom-made beam-shaping optics to generate a homogeneous line profile on the sample. A line width of 20 μm and length of 600 μm were measured with a beam profiler on the sample plane. The pump laser was operated in pulsed mode with a pulse duration of 100 ns, a repetition rate of 2 μs and a maximum peak optical power of 400 mW on the sample. The wavelength of the pump laser was chosen such that both the barriers of the MQW section and the cladding layers absorb the radiation well. However, the short interaction length of our thin epitaxial layer stack makes efficient optical pumping challenging.

To detect the light from our devices, the chips were diced and the emitted light was collected from the silicon waveguide via butt-coupling into a lensed single-mode fiber. An average chip to fiber coupling loss of -15 dB was subtracted from the power measurements. To normalize the peak pump power, we multiplied the active area of the device by the power density of the pump laser profile. Fig. 4(a) shows the laser output power versus pump power of two different devices. A clear threshold is observed at a power density of 1.7 kW cm^{-2}.

The device with a lower mirror reflectivity shows a slightly higher threshold current and an increased slope efficiency as expected. An output spectrum was acquired with an optical spectrum analyzer with a resolution bandwidth of 80 pm and is shown in Fig. 4(b). As expected for a Fabry-Pérot-like cavity defined by two DBR mirrors, several longitudinal modes are observed and the extracted free spectral range (FSR) of 231 pm agrees with the calculated FSR of the cavity. To prove the optical coupling between the III-V and silicon waveguide and to rule out that the cavity is formed accidentally by the III-V facets, laser spectra of ring lasers were measured (not shown). The cavity of such lasers is formed by a large ring in the silicon waveguide in contrast to fully etched mirrors of the previously mentioned devices. The FSR of this ring cavity is therefore clearly different from the FSR of the cavity that is possibly formed by the III-V facets. The measured FSR of such laser spectra clearly scales with the ring dimension (not shown), proving that the cavity is formed in the silicon and confirming therefore the optical coupling concept between the waveguides.

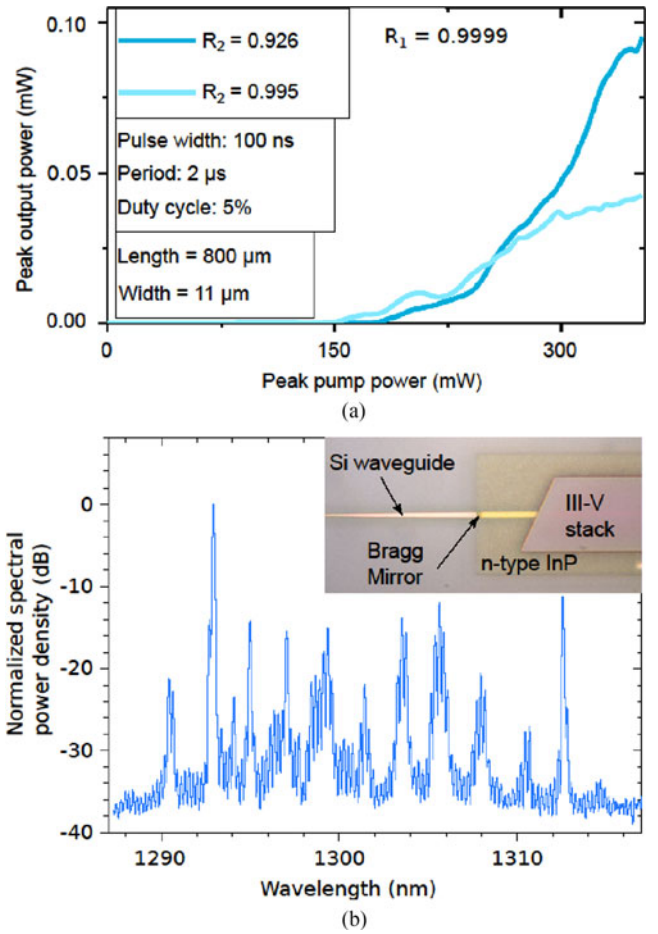

Fig. 4. (a) Room temperature light-in – light-out (L-L) curve of two optically pumped lasers showing output power dependence of mirror reflectivity R_2. (b) Room temperature optical spectrum of optically pumped laser device. Inset: Top-view photograph of laser device.

B. Current Injection Properties

To study the electrical current injection properties of our III-V layer stack, we fabricated light emitting diodes (LED). For this purpose, the exact same epitaxial layer stack was grown upside-down on an InP wafer and the LED were fabricated directly on this wafer by using the same processes as used for fabricating the laser devices. Rectangular devices with a width of 16.5 μm and length of 50 μm were fabricated and metallized with two metal levels. The devices were contacted with electrical probes and biased in forward direction. The optical emission of the device was captured with an IR-camera from the top (Fig. 5, inset). Due to the metallization scheme that covers the top of the device, the light is mainly emitted to the bottom and reflected back from the sample holder. Therefore, the illuminated circle is much bigger than the actual device. Fig. 5 shows a typical V-I curve for which the current axis was normalized to current density by multiplying the pump current with the area of the pumped device. The diode's turn-on voltage is around 1 V, which is similar to the band gap of our quantum well material ($\sim$0.95 eV), confirming Ohmic behavior at both n-type and p-type contacts. Furthermore, rate equation modelling of our laser structure allows us to estimate the threshold current density

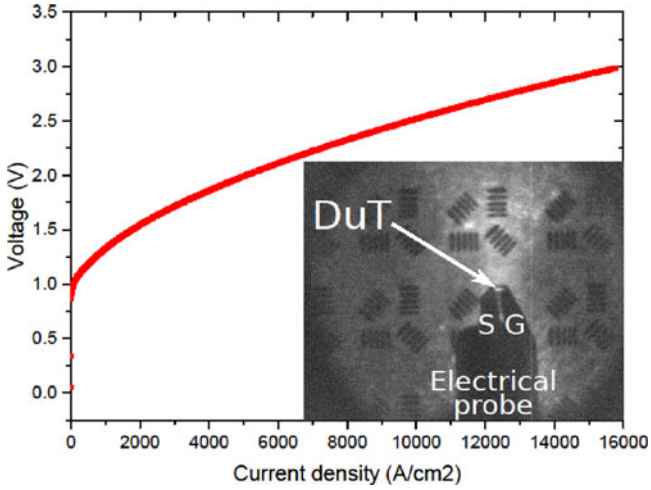

Fig. 5. V-I curve of LED device. Inset: photograph of biased LED device, taken with infrared camera.

of approximately 10 kA/cm^2, which is lower than the maximum current density measured for the LED. This shows that our III-V epitaxial layer stack, together with our CMOS-compatible Ohmic contacts enable efficient electrical carrier injection.

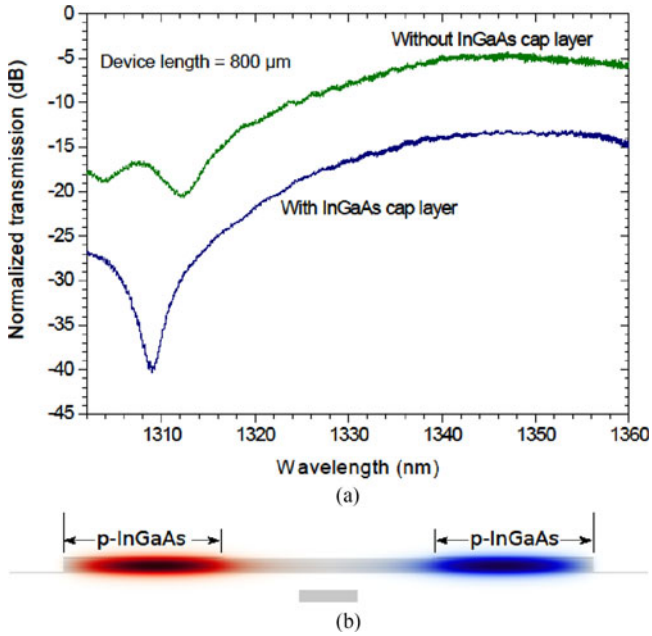

Fig. 6. (a) Normalized transmission loss measurement of laser devices with and without InGaAs cap layer. (b) Simulated electrical field of laser device with p-InGaAs layer stripes without lateral oxidation.

C. Towards Electrically-Pumped Lasers

To fabricate electrically-pumped lasers, the electrical injection scheme that was shown above was applied on laser devices, similar to the ones previously characterized. The main difference to the optically-pumped laser devices is the additional p-InGaAs layer, that is necessary to form p-type Ohmic contacts. To investigate the influence of the p-InGaAs cap layer on the laser performance and thus to uncover possible challenges on the way to electrically pumped lasers, we fabricated laser devices with a 15 nm thick p-InGaAs cap layer and studied the transmission losses of the devices at a wavelength of 1360 nm. At this wavelength the III-V layer stack is transparent and the devices can be measured without any pumping. To measure the transmission loss of a device we injected a tunable laser with a CW power of 5 mW from a cleaved single-mode fiber into a focusing grating coupler that was fabricated in the silicon waveguide layer. The grating couplers were designed for a center wavelength of 1300 nm under an angle of 15° to normal incidence and the grating trenches were patterned using a 70 nm deep partial etch process. The light was coupled from the silicon waveguide to the III-V and back and collected through a second grating coupler with another cleaved single-mode fiber. The transmitted power was normalized to the spectral transmission of a straight waveguide of the same length. This removes both, the wavelength dependence and the coupling loss of the grating couplers.

To study the influence of the p-InGaAs cap layer, we compared the transmission loss of devices with and without cap layer [see Fig. 6(a)] as well as devices for which the cap layer was removed everywhere except at the places of the two contact metals.

Devices with cap layer show a device length dependent loss of around −170 dB/cm which is associated with the modal overlap with the absorbing p-InGaAs layer. After removing this layer by means of selective wet chemical etching, only a length-independent loss is observed. This constant loss of −6 dB is associated with the two silicon to III-V couplers of every device. For devices where the p-InGaAs layer was only removed in the center of the III-V waveguide (4 μm wide) and left untouched at the sides of the III-V waveguide (3.5 μm wide), the transmission loss is again device-length-dependent with around −100 dB/cm and shows an additional constant loss. Mode simulations of this cross-section show that the large refractive index of the p-InGaAs has a strong influence on the optical mode. As shown in Fig. 6(b), the p-InGaAs stripes pin the mode on the edges of the III-V waveguide. Therefore, the mode overlaps with the absorbing p-InGaAs which explains the length-dependent loss.

In addition, the mode shape changes compared to the fundamental mode of the un-capped III-V waveguide. The III-V to silicon coupler is designed for the fundamental mode and transforms the mode of this device less efficient to the silicon waveguide, which explains the additional constant loss.

This analysis demonstrates the importance of lateral optical confinement to prevent the mode from leaking to the p-InGaAs stripes at the III-V waveguide edges. This confinement is provided by the laterally oxidized layers. In addition to this optical confinement, the laterally oxidized layers provide the previously discussed current confinement that is essential for efficient electrical pumping.

Without having the lateral oxidation process integrated into our fabrication process yet, the above discussed laser devices have a clearly higher optical loss, compared to their optical gain.

Therefore, room-temperature lasing is not achievable. However, the optical gain can be increased by reducing the device temperature. We therefore mounted our chip in a He-flow

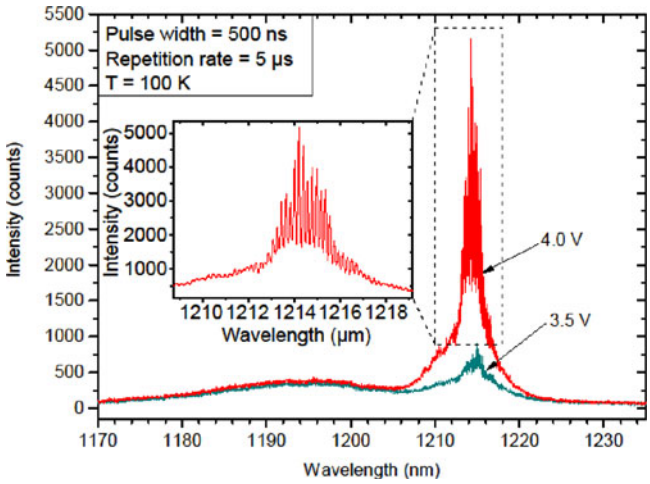

Fig. 7. Optical spectra of electrically pumped laser devices at 100 K at different bias voltages. Inset: Zoom-in on the indicated area of the spectrum.

cryostat and cooled it down to a temperature of 100 K. The light emitted from the grating couplers in the silicon waveguide was collected with a microscope objective (numerical aperture = 0.3) and detected with a spectrometer (grating: 830 lines/mm, blaze: 1.2 μm, liquid N_2 cooled InGaAs detector). We characterized a laser device similar to the one used for the optical pumping experiments as previously described. The device was electrically contacted and operated in pulsed mode. Fig. 7 shows two optical spectra from the same device at different bias voltages. For bias voltages lower than 3 V, only an electroluminescence (EL) peak, centered at around 1195 nm is observed. This peak can be seen in Fig. 7. The shift from the room temperature PL peak at 1300 nm can be explained by the change in temperature. When increasing the bias voltage to above 3 V, peaks located at a wavelength of around 1214 nm, 10 dB above the EL spectrum obtained at low bias, are observed (shown in detail in the inset of Fig. 7). This experiment shows that by increasing the gain or by accordingly reducing the optical loss in our devices we have a clear path towards electrically pumped lasing at room-temperature.

V. Conclusion

We have shown a concept to integrate a 300 nm thin III-V layer stack for laser devices in CMOS Silicon Photonics chips, in which (Bi)CMOS, Silicon Photonics and lasers would share the same BEOL. Adiabatic optical couplers for low-loss mode transformation between III-V and silicon waveguides have been designed. Epitaxial layer stack optimization and bonding thereof on Silicon Photonics wafer have been shown. Furthermore, optimized dry etching of the III-V layer stack, CMOS-compatible Ohmic contacts on InP and current confinement via lateral oxidation were presented. Optically-pumped lasers with feedback in silicon were demonstrated and the feasibility of an electrical injection scheme was shown on LED with a current density of 16 kA/cm^2. Finally, lateral mode confinement by selective oxidation has been shown to be crucial for reducing optical losses of electrically contacted laser devices. Strong peaks, 10 dB above the broad electroluminescence signal have been observed on electrically pumped laser devices at 100 K. Further work will focus on integrating the lateral oxidation process into the fabrication flow of our devices to show electrically-pumped lasing at room-temperature.

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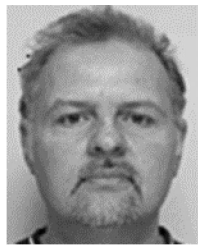

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