





High-Performance Back-Illuminated Three-Dimensional Stacked Single-Photon Avalanche Diode Implemented in 45-nm CMOS Technology

Myung-Jae Lee , *Member, IEEE*, Augusto Ronchini Ximenes, *Student Member, IEEE*, Preethi Padmanabhan , *Student Member, IEEE*, Tzu-Jui Wang, Kuo-Chin Huang, Yuichiro Yamashita , *Member, IEEE*, Dun-Nian Yang, and Edoardo Charbon , *Fellow, IEEE*

Abstract—We present a high-performance back-illuminated three-dimensional stacked single-photon avalanche diode (SPAD), which is implemented in 45-nm CMOS technology for the first time. The SPAD is based on a P⁺/Deep N-well junction with a circular shape, for which N-well is intentionally excluded to achieve a wide depletion region, thus enabling lower tunneling noise and better timing jitter as well as a higher photon detection efficiency and a wider spectrum. In order to prevent premature edge breakdown, a P-type guard ring is formed at the edge of the junction, and it is optimized to achieve a wider photon-sensitive area. In addition, metal-1 is used as a light reflector to improve the detection efficiency further in backside illumination. With the optimized 3-D stacked 45-nm CMOS technology for back-illuminated image sensors, the proposed SPAD achieves a dark count rate of 55.4 cps/ μm^2 and a photon detection probability of 31.8% at 600 nm and over 5% in the 420–920 nm wavelength range. The jitter is 107.7 ps full width at half-maximum with negligible exponential diffusion tail at 2.5 V excess bias voltage at room temperature. To the best of our knowledge, these are the best results ever reported for any back-illuminated 3-D stacked SPAD technologies.

Index Terms—Avalanche photodiode (APD), CMOS image sensor, detector, Geiger-mode avalanche photodiode (G-APD), image sensor, integrated optics device, integrated photonics, light detection and ranging (LiDAR), low light level, optical sensor, photodiode, photomultiplier, photon counting, photon timing, semiconductor, sensor, silicon, single-photon avalanche diode (SPAD), single-photon imaging, standard CMOS technology, three-dimensional fabrication, three-dimensional vision.

Manuscript received February 1, 2018; revised March 20, 2018 and March 28, 2018; accepted March 29, 2018. Date of publication April 16, 2018; date of current version May 15, 2018. This work was supported in part by the grant of the Swiss National Science Foundation. (*Corresponding author: Myung-Jae Lee.*)

M.-J. Lee, P. Padmanabhan, and E. Charbon are with the Institute of Microengineering, École Polytechnique Fédérale de Lausanne, Neuchâtel 2002, Switzerland (e-mail: fodlmj@gmail.com; preethi.padmanabhan@epfl.ch; edoardo.charbon@epfl.ch).

A. R. Ximenes is with the Department of Quantum Engineering, Delft University of Technology, Delft 2628, The Netherlands (e-mail: A.R.Ximenes@tudelft.nl).

T.-J. Wang, K.-C. Huang, Y. Yamashita, and D.-N. Yang are with the Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan (e-mail: tjwang@tsmc.com; huangkca@tsmc.com; yuichiro@tsmc.com; dnyaung@tsmc.com).

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Digital Object Identifier 10.1109/JSTQE.2018.2827669

I. INTRODUCTION

SINGLE-PHOTON avalanche diodes (SPADs) in standard CMOS technology have been receiving great attention from both the scientific and industrial communities since they provide high cost-effectiveness, mass-production capability, and easiness of integration. Consequently, SPADs can play an important role in various applications, especially LiDAR in advanced driver-assistance systems (ADAS), autonomous vehicles, service drones, robots, machine vision, gesture recognition, etc. Another important class of applications include biomedical imaging and diagnostic techniques, such as positron emission tomography (PET), single-photon emission computed tomography (SPECT), fluorescence-lifetime imaging microscopy (FLIM), super-resolution microscopy, near-infrared optical tomography (NIROT), Raman spectroscopy, etc. [1]–[4]. One critical limitation of monolithic SPAD systems is the relatively low fill factor, due to pixel circuits for quenching and recharge circuits. This problem is exacerbated whenever advanced *in situ* functionality is required, such as counting, timestamping, processing, compression, memory, etc.

In order to increase fill factor, CMOS process shrinking is very helpful; for this reason, researchers have proposed SPADs implemented in smaller and smaller technology nodes. An example of this trend is shown in Fig. 1, where the fill factor is just 1% in a 0.8 μm CMOS technology node but it is improved to 35% in a 65 nm CMOS process. In addition, process shrinking provides certain advantages in higher resolution and low power consumption as well as more cost-effective production. In general, however, it has negative effects on other SPAD performance due to higher doping concentrations resulting in a narrower depletion region. As a result, high tunneling-based dark count rate (DCR) and lower photon detection probability (PDP) are generally measured.

Recently, three-dimensional (3D) stacked technology has received a great deal of attention, since it can dramatically improve fill factor while enabling increased functionality, better timing, lower power, and higher uniformity in all these performance measures. In a 3D-stacked approach, SPADs are implemented in the top-tier chip, and all the circuits for data processing, com-

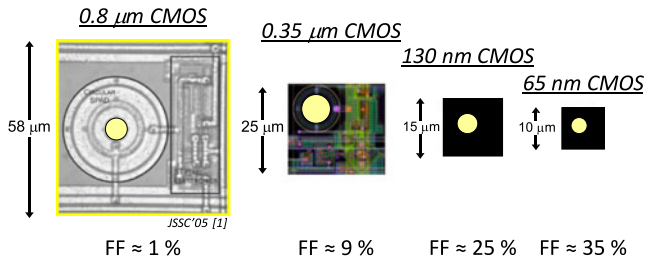


Fig. 1. Examples of SPAD's fill factor increases according to the technology node shrinking. The yellow circles represent the SPADs' active areas.

pression, and communication are placed on the bottom-tier chip, which is generally fabricated in a more advanced CMOS technology. In addition, the 3D-stacked architecture provides the freedom to optimize both processes individually, and therefore DCR and PDP can be improved simultaneously by using a better technology for SPADs, whereas doping levels and profiles are properly optimized. At the same time, a more advanced technology node may be used in the bottom tier, thus enabling advanced functionality, such as pixel-level digital memory and/or histogram processing. Furthermore, a 3D-stacked technology enables smaller pitch, thus achieving multi-megapixel SPADs is becoming feasible.

To date, there have been a few attempts to build 3D-stacked SPADs. The first successful attempt involving standard CMOS technology was implemented in 130 nm, whereas the SPAD was back-illuminated and the top- and bottom-tier chips were bound using wafer-to-wafer bonding [5], [6]. As shown in Fig. 2(a) and (c), the PDP performance obtained from these attempts was limited in wavelength mostly due to thick silicon substrate (about 4–5 μm). More recently, another back-illuminated 3D-stacked SPAD was reported in 65 nm CMOS image sensor (CIS) technology shown in Fig. 2(b) [7]; it achieves higher PDP and a wider sensitivity spectrum thanks to improved backside thinning and a deeper junction, which is thus closer to the surface. However, all of these solutions still suffer from reduced PDP in the visible range, and virtually zero sensitivity below 450 nm. In addition, median DCR is generally over 250 $\text{cps}/\mu\text{m}^2$ even with moderate excess bias voltage.

In this paper, we introduce the world's first back-illuminated SPAD fabricated in 45 nm CIS technology. The SPAD is 3D-stacked with a 65 nm standard CMOS technology, whereas preliminary test results of this technology were presented in [8]. This paper presents a full characterization of the technology with an extensive discussion of the results. The proposed SPAD has several advantages over existing designs. The fill factor is optimized thanks to a metal-free substrate, moreover PDP is enhanced at shorter wavelengths thanks to an ultra-thin substrate minimizing carrier recombination on the surface in backside illumination. In addition, a DCR of 55.4 $\text{cps}/\mu\text{m}^2$ and a jitter of 107 ps full width at half maximum (FWHM) at 2.5 V excess bias voltage are achieved, the lowest ever reported in a back-illuminated 3D-stacked CMOS technology. This performance was reached through optimized 3D-stacking, with a tight control of damage, improved doping profiles, and an especially designed optical stack [9]–[11]. This performance was achieved through careful analysis of the devices via extensive TCAD

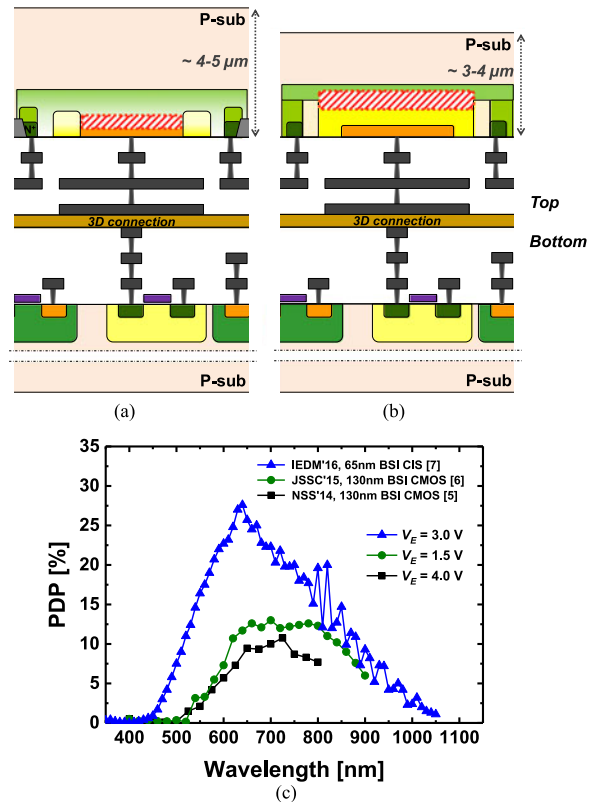


Fig. 2. Simplified cross sections of the back-illuminated 3D-integrated SPADs: (a) NSS'14 [5] and JSSC'15 [6], (b) IEDM'16 [7]. (c) PDP comparison of the SPADs.

simulations. To demonstrate the SPAD performance, we designed a complete imaging system in the bottom tier, while the availability of even more advanced nodes will increase functionality further in the future, resulting in densification of in-pixel operations. The suitability of the approach has been demonstrated through an array of identical pixels. Each pixel comprises a SPAD, quenching and recharge, as well as time-resolved circuitry for single-photon timestamping. The SPAD performance is uniform across the array, whereas breakdown voltage and PDP variability are kept to a minimum. Thanks to low dead time, afterpulsing, and crosstalk, image sensors based on this technology, are suitable for a wide range of exposures, involving photon-flooded to photon-starved modalities.

This paper is organized as follows. The overall device structure and technology are outlined in Section II, and Section III explains TCAD simulations to optimize the SPAD structure and presents the characterization results including dark current, breakdown voltage, fill factor, DCR, PDP, jitter, and afterpulsing. In Section IV, the state-of-the-art comparisons are presented with discussions, highlighting the achieved performance with the proposed back-illuminated 3D-stacked SPAD. Section V concludes this paper.

II. BACK-ILLUMINATED 3D-STACKED SPAD

Fig. 3 shows a cross section of the proposed back-illuminated 3D-stacked SPAD, where an advanced 45 nm CIS technology, featuring the back-illuminated SPAD, is stacked on top of a 65 nm standard CMOS technology. Two wafers are face-to-face

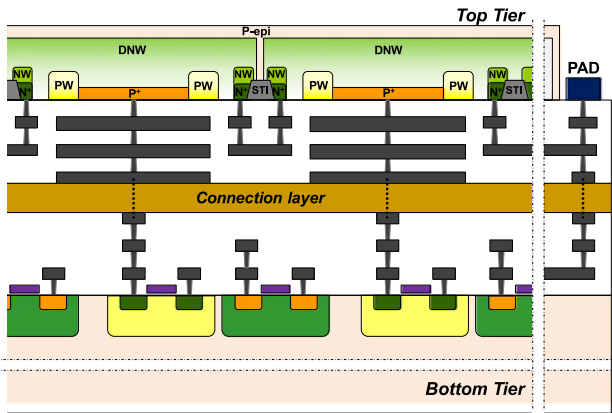


Fig. 3. Cross section of the proposed back-illuminated 3D-integrated SPAD.

stacked, and therefore the substrate of the top wafer can be thinned down to only a few micrometers. The SPAD is based on the P⁺/Deep N-well (DNW) junction, where the N-well is intentionally excluded in order to achieve wider depletion region, thus resulting in lower tunneling noise and better jitter performance as well as higher detection efficiency with wider spectrum, and P-well (PW) guard ring (GR) is implemented to prevent premature edge breakdown, enabling higher electric fields at the active region, as shown in Fig. 3. The SPAD is designed and realized in a round shape with an active-area diameter of 12.5 μm , 2 μm GR, and 1 μm distance between GR and cathode. The conservative design parameters were chosen in this first attempt to obtain the first functional back-illuminated SPAD in 45 nm, rather than maximizing fill factor. Based on the achieved results, a parameter optimization can be performed in order to achieve fill factor higher than 70% in future generations. Metal-1 *in primis*, and other metals, are designed to cover all the SPAD active region and to reflect lower energy photons back to the active region, so as to enhance PDP at longer wavelengths.

In order to take the full advantages of the back-illuminated 3D-stacked approach, the dedicated technology development and optimization are also crucial. The top-tier wafer is thinned down to the target thickness, less than 3 μm , which is a very challenging task for 300 mm bulk silicon wafer based technology. The process includes chemical and mechanical etching, whereas epi-wafer quality and thin-down flow have been optimized, with a final thickness tolerance of less than 3% [9]. In addition, the defects induced by etching, which can degrade and even suppress SPAD operation, have been reduced by more than 10 times with this optimization process. In addition, the direct 3D connection technology enables smaller pitch and consequently better 3D connection quality [10], and the impact of the 3D connections have been significantly minimized with further process improvement [11].

Fig. 4 shows a schematic diagram of the 3D-stacked SPAD pixel. A passive quenching and recharge circuit was implemented on the bottom tier, featuring a local 1-bit memory for optical and electrical masking and dual-mode operation: Pulse and State. In Pulse mode, upon avalanche detection, a signal pulse is generated with fix width. After the dead time, the SPAD is available for a new detection. In State mode, upon

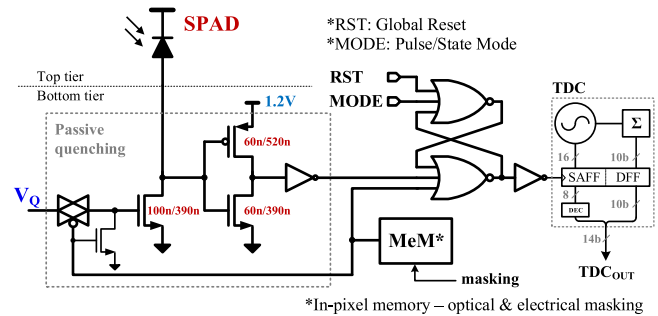


Fig. 4. Schematic diagram of the back-illuminated 3D-stacked SPAD sensor.

avalanche detection, the state of the pixel is held until the next global reset is issued.

III. SIMULATION AND CHARACTERIZATION RESULTS

A. TCAD Optimization

TCAD simulation is very useful to check and analyze SPAD characteristics in terms of doping profile, dark current, avalanche breakdown voltage, and electric-field profile, which provide helpful guidelines for the device design, in advance of its fabrication [12]–[14]. In addition, it is an appropriate method to compare different SPAD structures and identify expected results. Fig. 5 shows SPADs based on different junctions, P⁺/N-well and P⁺/DNW, along with the relative doping profile, electric field, and current-voltage characteristics, obtained by TCAD simulations for each device. In deep submicron CMOS technology, SPADs suffer from tunneling noise due to higher doping concentrations, and the higher tunneling becomes critical for Geiger-mode operation especially in ultra-deep submicron CMOS technology, below 90 nm. As mentioned earlier, we intentionally removed the N-well layer at the junction in the proposed SPAD, so as to achieve a large depletion region of about 1 μm . Note that the DNW layer is characterized by retrograde doping, as shown in the relative doping profile of Fig. 5(b), which supports a thicker multiplication region and wider PDP as well as lower DCR. In general, a SPAD implemented in technology nodes below 90 nm in standard CMOS technology shows large DCR due to tunneling caused by increased doping concentrations resulting in a narrower depletion region, and therefore achieving a large depletion region is extremely important in this kind of advanced CMOS technology node. Although we consider the use of a better N-well for photodiodes provided by the CIS technology as shown in Fig. 5(a), its breakdown voltage is lower and the depletion width is smaller than those of the P⁺/DNW junction as shown in Fig. 5(b). In addition, from the TCAD current-voltage analysis, we can check that the P⁺/N-well junction can have larger dark currents compared to the P⁺/DNW junction. In order to prevent premature edge breakdown, PW GR is implemented at the edge of the junction, and it is optimized to achieve larger photon sensitive area. The wider depletion region based on the DNW-based junction results in higher breakdown voltage, which enables higher electric fields at the PW GR region with the retrograde DNW. The electric-field profile of Fig. 5(b) clearly shows that the

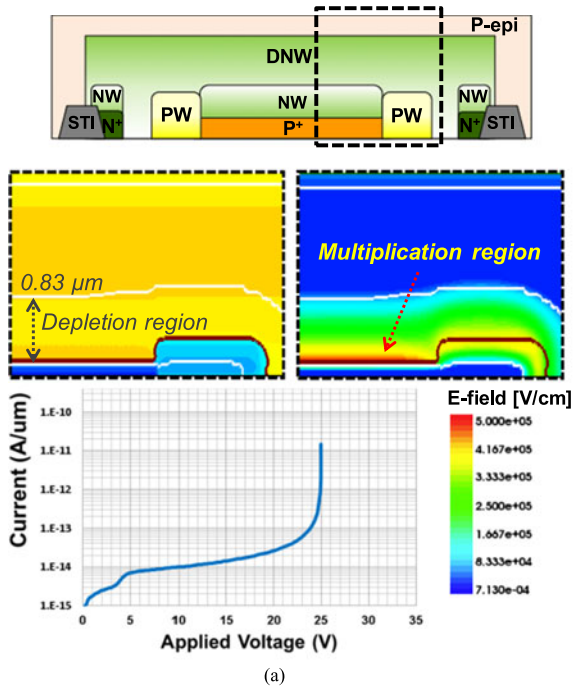


Fig. 5. TCAD simulation results for back-illuminated SPADs based on (a) P⁺/NW junction and (b) P⁺/DNW junction: device structures, relative doping profiles and electric-field profiles at around each breakdown voltage, and current-voltage characteristics.

multiplication region, represented by yellow, is extended below the GR region, because the PW GR doping profile is carefully selected for the retrograde DNW-based junction to have the similar level of electric fields to the main junction.

B. Measurement Results

Fig. 6(a) shows a micrograph of the fabricated SPADs based on the P⁺/DNW junction with PW GR, and Fig. 6(b) a

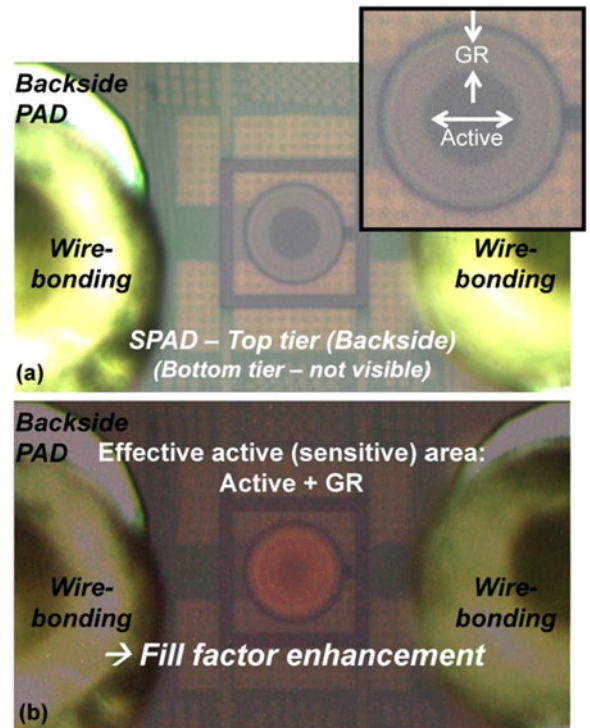


Fig. 6. (a) Micrograph of the back-illuminated 3D-integrated SPAD. The inset shows magnified micrograph indicating active and GR areas. (b) Micrograph with the operating SPAD to check light emission area and effective fill factor.

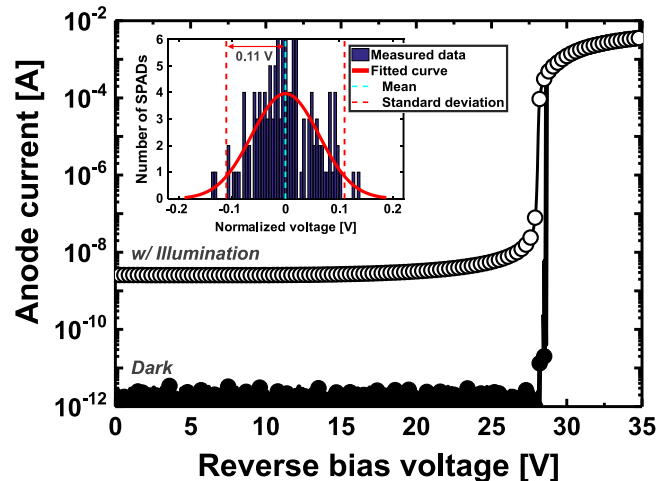


Fig. 7. Current-voltage characteristics under dark conditions at room temperature. The inset shows the breakdown voltage distribution of the SPAD at room temperature.

micrograph at above its avalanche breakdown voltage. Since light emission can be observed in silicon with the avalanche multiplication process despite its indirect bandgap [13]–[15], effective active area where the avalanche multiplication process occurs can be checked and consequently the effective fill factor. The image clearly shows that also the GR area exhibits emission, thus contributing to higher fill factor up to 60.5%.

The SPAD shows very low dark current, in the pA range, and a breakdown voltage of about 28.5 V, as depicted in Fig. 7, matching very well with the TCAD simulation result. The inset

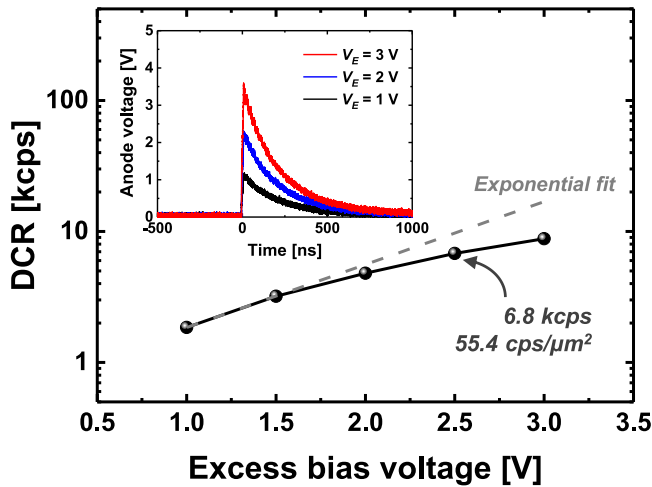


Fig. 8. DCR as a function of the excess bias voltage at room temperature. The inset shows the output pulses of the SPAD as a function of time at different excess bias voltages at room temperature.

of Fig. 7 shows the breakdown voltage distribution obtained by 128 SPADs, showing a standard deviation of 0.11 V.

The inset of Fig. 8 shows the time-dependent outputs of the SPAD at different excess bias voltages. The SPAD output pulses show the exponential behavior because of the RC recharge. Due to the fact that these results are obtained from a standalone SPAD without an integrated quenching circuitry, the C becomes very high because of the parasitic capacitance from the output PAD, external components, and setup. The parasitic capacitance is estimated to be tens of pF, which is three orders of magnitude larger than the expected SPAD junction capacitance that will dominate in a fully integrated implementation. Fig. 8 shows DCR as a function of the excess bias voltage varying over less than one order of magnitude. The DCR at the nominal operating condition, an excess bias voltage of 2.5 V, is $55.4 \text{ cps}/\mu\text{m}^2$. The achievement is due to the defect-minimized technology and also the DNW-based junction having large depletion region. The DCR shows a sub-exponential dependence on the excess bias voltage, which indicates a smaller tunneling contribution to DCR at higher excess bias voltages. A test SPAD structure based on the P^+/N -well junction is also fabricated for comparison purposes, and it shows about 40 times higher DCR than the proposed SPAD's DCR while it also shows very low dark current similar to the proposed one (Fig. 7), which implies that the P^+/N -well junction SPAD suffers from high tunneling noise as analyzed and expected from the TCAD simulations. A cumulative DCR distribution with 128 SPADs is shown in Fig. 9. The plot shows a really small population of noisy SPADs, about 4% of the population.

In order to investigate temperature-dependent characteristics of the SPAD and identify the main contributor to its DCR further, its breakdown voltage and DCR were measured at various temperatures from -60°C to 60°C as shown in Fig. 10 and 11(a). Although it is preferred to use one identical sample for all characterization, these temperature-dependent measurements were performed separately as additional tests using a different sample, resulting in a little difference in DCR at room temperature

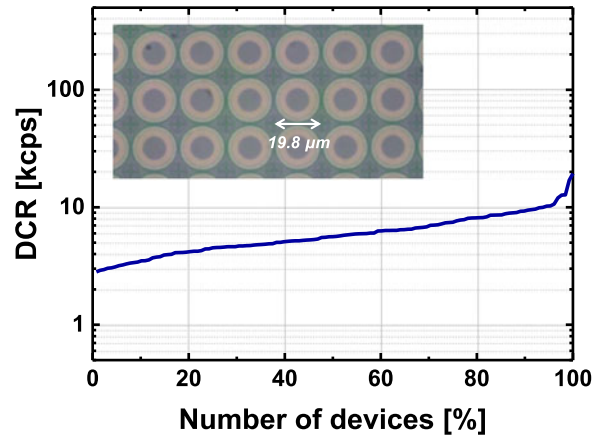


Fig. 9. Cumulative DCR distribution obtained from 128 SPADs. The inset shows a micrograph of the back-illuminated 3D-integrated SPAD arrays used for the DCR distribution test.

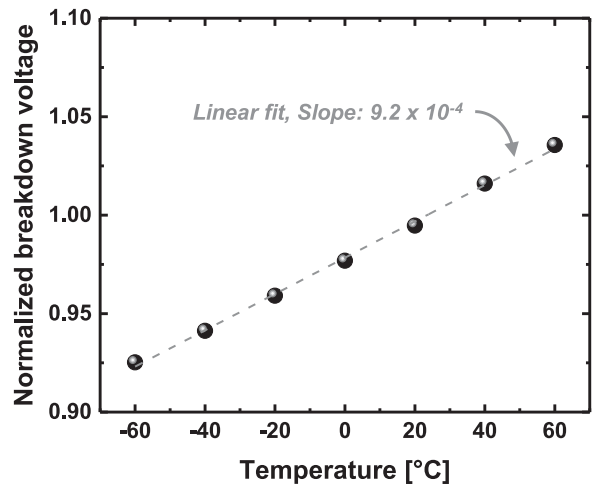
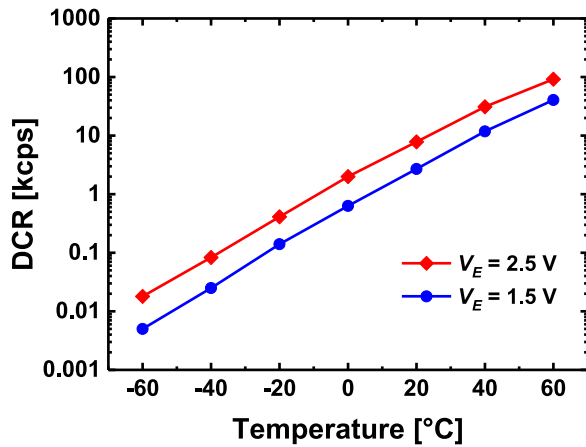
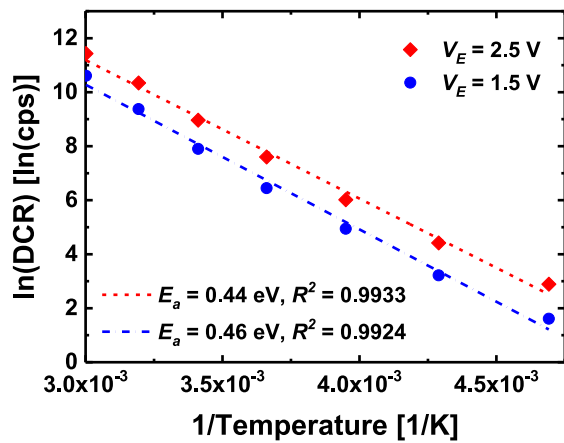


Fig. 10. Avalanche breakdown voltage as a function of temperature. The values are normalized to the room-temperature value.

between Fig. 8 and Fig. 11(a). Fig. 10 shows a typical breakdown voltage versus temperature characteristic: the breakdown voltage increases with increasing temperature because higher energy is required for avalanche at higher temperature due to increased optical phonon scattering. In other words, higher voltage is needed for avalanche breakdown at higher temperature since the ionization rate becomes smaller. The rate of increase of the breakdown voltage with temperature is about 0.092%. In case a SPAD sensor suffers from high temperature variation in an application, two approaches can be considered: (i) using a cooling system to maintain a stable temperature and (ii) using a feedback loop to compensate for breakdown voltage variations [16]. Fig. 11(a) shows that DCR of the SPAD is highly dependent on temperature, implying that the major contributor to the DCR is not tunneling but trap-assisted thermal generation and the DCR performance can be greatly improved with cooling. Fig. 11(b) shows the Arrhenius plot of the DCR, with which the activation energy, E_a , for each excess bias voltage is calculated. The activation energies, $E_a = 0.44 \text{ eV}$ and 0.46 eV , correspond to single-level traps caused by the phosphorus ion implantation [17], [18], which indicates that the main contributor to the DCR



(a)



(b)

Fig. 11. (a) DCR versus temperature and (b) Arrhenius plot of the DCR at the excess bias voltages of 1.5 V and 2.5 V.

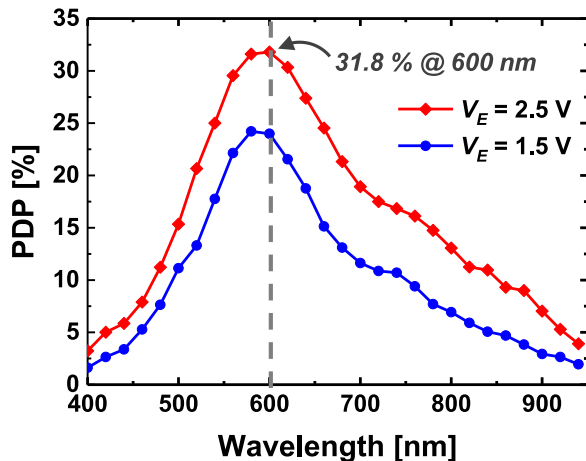
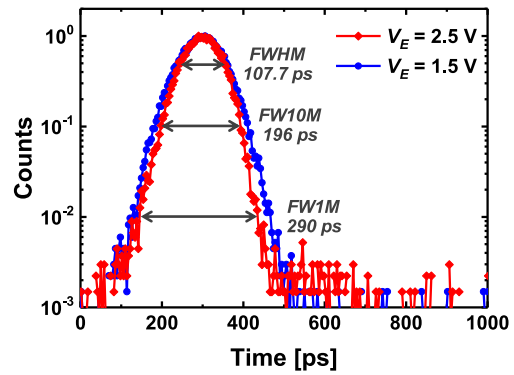


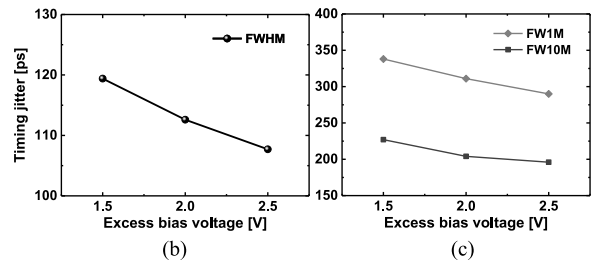
Fig. 12. PDP at the excess bias voltages of 1.5 V and 2.5 V.

is Shockley-Read-Hall (SRH) thermal generation, also known as trap-assisted thermal generation, and further DCR improvement is achievable with better treatment to remove the traps during the phosphorus ion implantation process.

The SPAD has a maximum PDP of 31.8% at 600 nm at the excess bias voltage of 2.5 V, as shown in Fig. 12, in contrast



(a)



(b)

(c)

Fig. 13. (a) Timing jitter measurement results at the excess bias voltages of 1.5 V and 2.5 V when using a 637 nm laser. (b) FWHM and (c) FW10M and FW1M as a function of the excess bias voltage.

to a typical PDP peak at around 500 nm in frontside illumination. The SPAD achieves higher PDP at longer wavelengths, when compared to CMOS SPADs in frontside illumination [19]. Thanks to the large depletion region and the ultra-thin substrate, the sensitivity in the 400–600 nm range is enhanced, reaching a more balanced sensitivity over the visible range and opening up more applications for which this range is of interest. With the metal-1 light reflector, the PDP is further improved at long wavelengths, above 700 nm.

The timing jitter is characterized using time-correlated single-photon counting (TCSPC). A 637 nm solid-state laser source (A.L.S. GmbH, Germany) with a pulse width of 35 ps and a repetition rate of 40 MHz is used to illuminate the SPAD; the time interval between the laser output trigger and the leading edge of the SPAD pulse is measured using a high-performance oscilloscope (Teledyne LeCroy WavePro 760Zi-A, United States) operating as a TDC. Neutral density filters are used to reduce the SPAD firing rate, so as to prevent pile-up, and a histogram is obtained from the time interval measurements repeated over very large number of times. The normalized histograms are shown in Fig. 13(a), while (b) and (c) show the evolution of jitter as a function of excess bias. At an excess bias voltage of 2.5 V, a jitter of 107.7 ps FWHM is achieved; this includes the contributions from the laser jitter of 37 ps FWHM. It's also notable that the SPAD achieves very good full width at 10% of maximum (FW10M) and full width at 1% of maximum (FW1M), since the diffusion tail becomes very small with the large depletion region. This feature can be very useful in some applications like quantum number generation and quantum communications.

The afterpulsing probability was measured to be 1.5% and 2.2% at 1.5 V and 2.5 V of excess bias, respectively, with a

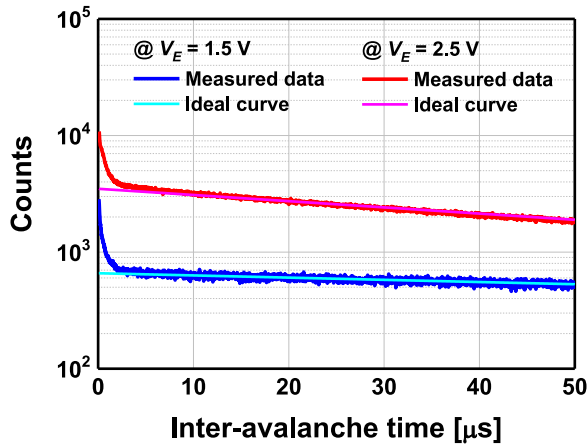


Fig. 14. Afterpulsing probability: inter-arrival time histogram measured at the excess bias voltages of 1.5 V and 2.5 V at room temperature along with a fitted exponential curve.

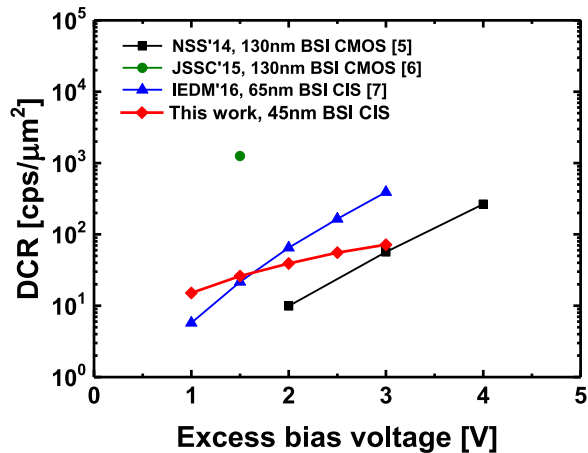


Fig. 15. DCR comparison of the state-of-the-art back-illuminated SPADs in 3D-stacked CMOS technologies.

100 ns dead time as shown in Fig. 14. As described with Fig. 8, these values are significantly overestimated with huge parasitic capacitance due to the lack of integrated quenching and recharge circuits for this characterization. Therefore, we can assume that the afterpulsing is negligible in a SPAD sensor array at comparable dead times.

IV. STATE-OF-THE-ART COMPARISONS AND DISCUSSIONS

Figs. 15–18 show comparisons of the proposed SPAD with the state-of-the-art back-illuminated SPADs fabricated in 3D-stacked CMOS technologies. The comparison parameters are normalized DCR, PDP, and jitter. In an advanced CMOS technology, SPADs suffer from high tunneling noise due to narrow depletion widths caused by high doping concentrations. Therefore, the DCR of other SPADs is highly dependent on the excess bias voltage, and in addition, their exponential dependence also indicates their DCRs are dominated by tunneling, as can be seen in Fig. 15. The proposed SPAD, however, can effectively reduce the contribution of the tunneling assisted DCR thanks to the large depletion region, thus achieving a modest upward sloping curve and the lowest DCR at the operating condition.

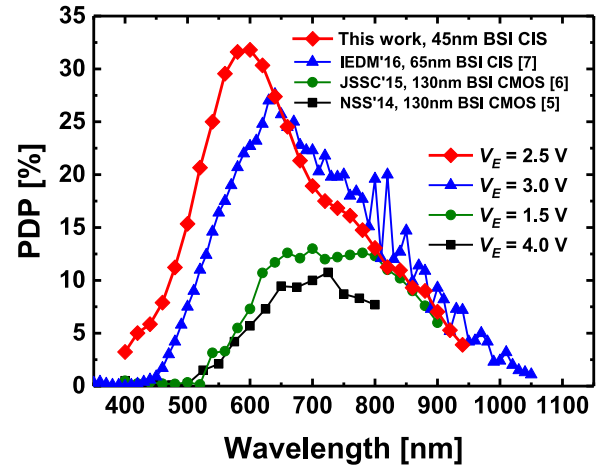


Fig. 16. PDP comparison of the state-of-the-art back-illuminated SPADs in 3D-stacked CMOS technologies.

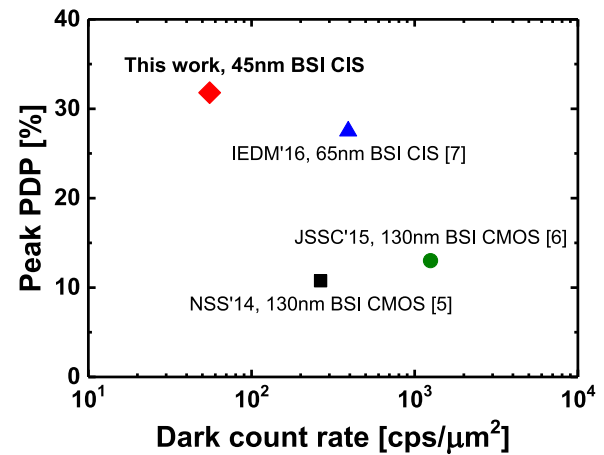


Fig. 17. Performance comparison of the state-of-the-art back-illuminated SPADs in 3D-stacked CMOS technologies: peak PDP versus area-normalized DCR.

Fig. 16 shows a PDP comparison. The SPADs based on 130 nm CMOS technology show lower PDP peaking at around 700 nm, which corresponds to the light penetration depth of about 5 μm and indicates that the quality of the backside thinning process was insufficient. The SPAD fabricated in 65 nm CIS technology shows a maximum PDP at 640 nm with almost zero PDP at 350–450 nm, which implies that the backside thinning was improved, but it was not sufficiently shallow. Compared to other back-illuminated 3D-stacked CMOS SPADs, the proposed SPAD achieves the best maximum PDP and a wider sensitivity spectrum, along with relatively high violet and blue sensitivities thanks to a more aggressive backside thinning and an optimized SPAD design, including the metal-1 light reflector.

The state-of-the-art comparison of SPADs in terms of peak PDP and area-normalized DCR is depicted in Fig. 17. As can be seen from the figure, the proposed SPAD achieves superior DCR and PDP simultaneously among all back-illuminated 3D-stacked CMOS SPADs. In addition, as shown in Fig. 18, it also exhibits better jitter performance, which is very useful in many applications using the time-of-arrival technique. Table I summarizes the performance measures of the proposed device

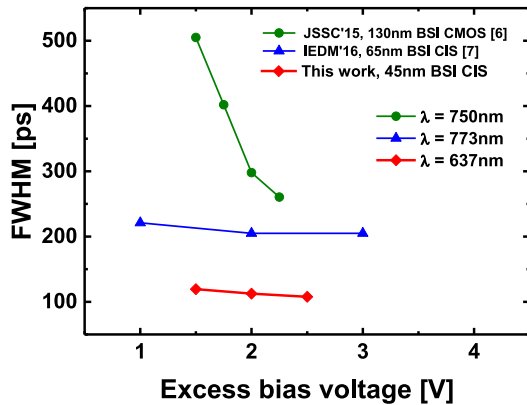


Fig. 18. Jitter comparison of the state-of-the-art back-illuminated SPADs in 3D-stacked CMOS technologies.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH BACK-ILLUMINATED SPADs IN 3D-STACKED CMOS TECHNOLOGY

	[5]	[6]	[7]	This work
Top tier	130 nm CMOS	130 nm CMOS	65 nm CIS	45 nm CIS
Bottom tier	130 nm CMOS	130 nm CMOS	40 nm CMOS	65 nm CMOS
Junction GR	P ⁺ /NW PW GR	NLDD/PW NW GR	PW/DNW Virtual GR	P ⁺ /DNW PW GR
Shape	Round	Round	Round	Round
Active area	28.3 μm^2	28 μm^2	27.6 μm^2	122.7 μm^2
V_B	12.3 V	16.5 V	12.0 V	28.5 V
V_E	4 V	1.5 V	3 V	2.5 V
Fill factor	n.a.	23.3%	45%	up to 60.5%
DCR (cps/ μm^2)	7.5 kcps (265.3)	35 kcps (1250)	10.8 kcps (391.4)	6.8 kcps (55.4)
PDP peak	11% (@725 nm)	13% (@700 nm)	27.5% (@640 nm)	31.8% (@600 nm)
PDP @450 nm	0.3%	0.3%	0.9%	6.9%
PDP @850 nm	n.a.	9.6%	14.7%	10.1%
Jitter (FWHM)	n.a.	505 ps (@750 nm)	205 ps (@773 nm)	107.7 ps (@637 nm)
Jitter (FW10M)	n.a.	~840 ps (@750 nm)	n.a.	196 ps (@637 nm)
Jitter (FW1M)	n.a.	~1360 ps (@750 nm)	n.a.	290 ps (@637 nm)

and also reports a performance comparison with the state-of-the-art back-illuminated 3D-stacked CMOS SPADs.

V. CONCLUSION

We demonstrate and fully characterize the world's first back-illuminated 3D-stacked SPAD in 45 nm CIS technology. The detector enables significant benefits beyond the state-of-the-art. A P⁺/DNW junction enabling wider depletion is used, along with an optimized guard ring structure and metal-1 light reflector, so

as to facilitate lower DCR, higher and wider PDP, better jitter, and higher fill factor. The SPAD, that was optimized *a priori* using extensive TCAD simulations, has a DCR of 55.4 cps/ μm^2 , a maximum PDP of 31.8% at 600 nm wavelength with significant blue and NIR sensitivity, and a timing jitter of 107.7 ps FWHM and 290 ps FW1M at room temperature and 2.5 V excess bias voltage. To the best of our knowledge, the proposed SPAD exhibits the best performance among all back-illuminated 3D-stacked CMOS SPADs, to date. In the near future, large arrays of this SPAD will be implemented for a number of applications requiring low noise, high efficiency, and high timing resolution.

ACKNOWLEDGMENT

The authors would like to thank Z.-Y. Chang for his assistance in wire bonding and also E. Venialgo and I. M. Antolovic for providing feedback and comments.

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Myung-Jae Lee (S'08–M'13) received the B.S., M.S., and Ph.D. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2006, 2008, and 2013, respectively. His doctoral dissertation concerned silicon avalanche photodetectors fabricated with standard CMOS/BiCMOS technology. From 2013 to 2017, he was a Postdoctoral Researcher with the faculty of electrical engineering, Delft University of Technology, Delft, The Netherlands, where he worked on single-photon image sensors and applications based

on single-photon avalanche diodes. In 2017, he was with the School of Engineering, École Polytechnique Fédérale de Lausanne, Neuchâtel, Switzerland, as a Scientist, working on advanced single-photon image sensors and applications as well as coordinating and managing several research projects. His research interests include single-photon avalanche diodes, LiDAR sensors and applications, biosensors and applications, quantum applications, image sensors, CMOS- and BiCMOS-compatible photodetectors and receivers, avalanche photodetectors, silicon photonics, and optical interconnects.



Augusto Ronchini Ximenes (S'10) was born in Brazil, in 1983. He received the B.S. and M.S. degrees from State University of Campinas, Campinas, Brazil, in 2008 and 2011, respectively. Since 2012, he has been working toward the Ph.D. degree at Delft University of Technology, Delft, The Netherlands. In 2008, he spent nine months with McMaster University, Hamilton, ON, Canada, as undergrad exchange student, working on postprocessing APS image sensors. In 2009, he spent six months with Technical University of Denmark (DTU), as a Master's exchange student, working on RF circuit design. Between 2010 and 2012, he worked as RF circuit designer at Center for Information Technology Renato Archer (CTI), Campinas, Brazil. Between September and December of 2015, Augusto was an intern with Xilinx, Dublin, Ireland, working on high-performance ADPLLs using FinFet technology. His main research interests include mixed-signal circuit design, digital frequency synthesizers and time-of-flight depth sensors.



Preethi Padmanabhan (S'17) received the B.E. degree in electronics and instrumentation engineering from Anna University, Chennai, India, in May 2014 and the M.Sc. (*cum laude* and Hons.) degree in electrical engineering from Delft University of Technology, Delft, The Netherlands, in August 2016. Since November 2016, she has been working toward the Ph.D. degree in microsystems and microelectronics at Advanced Quantum Architecture Laboratory, École Polytechnique Fédérale De Lausanne, Lausanne, Switzerland. During her Master's study, in

the summer of 2015, she worked as an analog circuit designer in Advanced Detector Arrays, Systems, and Nanoscience Group with NASA's Jet Propulsion Laboratory (JPL), Pasadena, CA, USA, where she implemented a CMOS readout circuit for UV avalanche photodiodes. The results from this work also led to a Best Poster Award at the International Image Sensors Workshop in May 2017, Hiroshima, Japan. Her current research interests include analog and digital circuit design for SPAD-based TOF image sensors in LiDAR applications.

Tzu-Jui Wang received the Ph.D. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2008. Since 2009, he was with the CMOS Image Sensor group for pixel device development, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan.

Kuo-Chin Huang received the Master's degree from the Department of Electrical Engineering, National Chiao Tung University, Hsinchu, Taiwan. Since 2011, he has been a CMOS Image Sensor engineer, Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan. He is currently working on CIS related characterizations, image quality analysis, and device developments.



coauthored more than 100 granted patents. He is a Member of ITE.

Yuichiro Yamashita (M'xx) received the B.S. and M.S. degrees in electrical engineering from Tohoku University, Sendai, Japan, in 1995 and 1997, respectively, and the Engineering degree from Stanford University in 2003. He was with Canon Inc., Japan, in 1997, where he engaged in the R&D of the CIS pixel devices and readout circuits and the design of the CIS products. Since 2012, he has worked in TSMC, Taiwan, Hsinchu, where he has been responsible for simulation, characterization and exploratory researches of sensing devices. He has authored and



and a Member of the technical program committee of IISW since 2015. He has authored and coauthored more than 250 patents and 45 papers. He is currently the Director of CMOS Image Sensor Divisions in TSMC R&D.

Dun-Nian Yang received the M.S. and Ph.D. degrees from the Institute of Microelectronics, National Cheng Kung University, Tainan, Taiwan, in 1994 and 2000, respectively. He was with the Taiwan Semiconductor Manufacturing Company (TSMC) in 1995 and dedicated in process integration and SRAM development. From 1999, he led CMOS Image Sensor RD team in 0.25–0.11 μm FSI development, 0.11 μm /N65 BSI, and stack technology initiation. He was a Subcommittee Member of "Display, Sensor and MEMS" session of IEDM from 2012 to 2014,



where he was the Architect of the company's initiative on information hiding for intellectual property protection. In 2000, he was with Canesta Inc., as the Chief Architect, where he led the development of wireless three-dimensional (3-D) CMOS image sensors. Since 2002, he has been a member of the faculty of École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, where is a full Professor since 2015. From 2008 to 2016, he was a full Professor and the Chair of VLSI design at Delft University of Technology. He has been the driving force behind the creation of deep-submicron CMOS SPAD technology, which is mass-produced since 2015 and is present in telemeters, proximity sensors, and medical diagnostics tools. His interests span from 3-D vision, FLIM, FCS, NIROT to super-resolution microscopy, time-resolved Raman spectroscopy, and cryo-CMOS circuits and systems for quantum computing. He has authored or coauthored more than 300 papers and two books, and he holds 20 patents. He is a distinguished Visiting Scholar with the W. M. Keck Institute for Space at Caltech, a fellow of the Kavli Institute of Nanoscience Delft, a distinguished Lecturer of the IEEE Photonics Society.

Edoardo Charbon (SM'00–F'17) received the Diploma degree from ETH Zurich, Zürich, Switzerland, the M.S. degree from the University of California at San Diego, San Diego, CA, USA, and the Ph.D. degree from the University of California at Berkeley, Berkeley, CA, USA, in 1988, 1991, and 1995, respectively, all in electrical engineering and EECS. He has consulted with numerous organizations, including Bosch, X-Fab, Texas Instruments, Maxim, Sony, Agilent, and the Carlyle Group. He was with Cadence Design Systems from 1995 to 2000,