Single-Photon Avalanche Diodes in a 0.16 μm BCD Technology With Sharp Timing Response and Red-Enhanced Sensitivity

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***Abstract*—CMOS single-photon avalanche diodes (SPADs) have recently become an emerging imaging technology for applications requiring high sensitivity and high frame-rate in the visible and near-infrared range. However, a higher photon detection efficiency (PDE), particularly in the 700–950 nm range, is highly desirable for many growing markets, such as eye-safe three-dimensional imaging (LIDAR). In this paper, we report the design and characterization of SPADs fabricated in a 0.16 μm BCD (Bipolar-CMOS-DMOS) technology. The overall detection performance is among the best reported in the literature: 1) PDE of 60% at 500 nm wavelength and still 12% at 800 nm; 2) very low dark count rate of $<$ 0.2 cps/μm^2 (in counts per second per unit area); 3) $<$ 1% afterpulsing probability with 50 ns dead-time; and 4) temporal response with 30 ps full width at half-maximum and less than 50 ps diffusion tail time constant.**

***Index Terms*—Photon counting, photon timing, single-photon avalanche diodes (SPADs), time-correlated single-photon counting (TCSPC), LIDAR, three-dimensional (3-D) ranging, FLIM.**

I. Introduction

SILICON Single-Photon Avalanche Diodes (SPADs) fabricated with custom epitaxial technologies [1], [2] provide best-in-class performance in terms of photon detection efficiency (PDE), dark-count rate (DCR) and timing response. However, custom fabrication technologies are expensive and, owing to their inherently limited system integrability, are best suited for small (up to hundreds of pixels [3]) SPAD arrays. As a consequence, the increasing demand for large SPAD arrays in many applications, such as fluorescence lifetime imaging microscopy (FLIM) [4]–[9] and 3-D ranging and imaging (LIDAR) [10]–[16], has driven the research toward the fabrication of SPADs in conventional CMOS processes, aiming at producing reliable single-chip detection systems at low cost and with high reproducibility.

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The breakthrough occurred in early 2000's, when SPADs were successfully demonstrated using a high-voltage 0.8-μm CMOS technology [17], [18]. This paved the way for the fabrication of large ($>10^4$ pixels [19]–[21]) SPAD imagers. However, the trend toward deep-submicron (DSM) CMOS technologies to attain either higher system integration, higher spatial resolution or higher fill factor (i.e., the active-to-total area ratio of a single pixel) is hindered [22]. A major concern with DSM technologies is that MOSFET scaling leads to higher doping levels and curtailed annealing steps, which in turn give rise to thinner depletion layers and higher defects concentration [3]. An attracting alternative to enhance the device performance is given by smart power technologies, such as BCD (Bipolar-CMOS-DMOS), since technological features required by high-voltage devices are also favorable to high-performance SPADs [1], [22]. Furthermore, smart power technologies are based on the concept of modularity [23], [24], i.e., additional implants for optional devices can be added to a basic process flow-chart.

In this paper, we present the design criteria and the experimental characterization of the SPADs we developed in the 0.16-μm STMicroelectronics' BCD8sP technology [25]. These BCD SPADs show enhanced PDE in the near-infrared (NIR) compared to standard CMOS SPADs, coupled with state-of-the-art DCRs and timing response, and maintains full compatibility with Bipolar, CMOS and DMOS on-chip circuitry, thus being suitable for SPAD imaging arrays.

II. Device Description

A constraint in SPAD arrays is the need to isolate SPAD detectors from CMOS circuitry and to limit the collection of minority carriers from the neutral volume below their space charge region. This is usually achieved by enclosing the SPAD in an n-well diffused through the p-type substrate and reverse-biasing the resulting (cathode-substrate) p-n junction. A low-doped ($<10^{17}$ cm^{-3}) and deep n-type well is fundamental to achieve good photon-counting performance, i.e., high PDE and low DCR. The reason being that a wide space charge region (1–2 μm) increases the quantum efficiency, reduces field-enhanced carrier generation [26] and avoids band-to-band tunneling [27].

For reducing the diffusion tail, the n-well neutral region underneath the space charge should be thin and lightly doped [28].

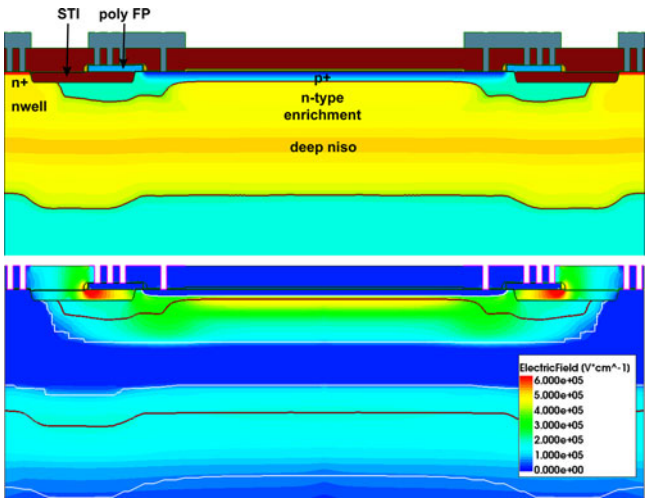

Fig. 1. Cross section of a 'shallow' BCD SPAD from wafer A with simulated net doping concentration (top) and electric field distribution at 5 V excess bias (bottom).

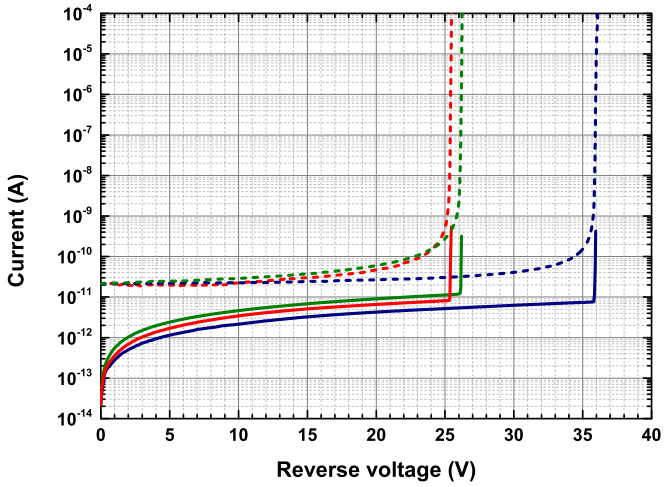

Fig. 2. Typical dark and illuminated I-V characteristics of 30-μm BCD SPADs from wafer A, B and C at 300 K. The absence of any dark current multiplication up to breakdown suggests that perimeter leakage dominates the dark current.

On the other hand, as demonstrated in [29], for achieving a narrow timing response full-width at half maximum (FWHM) the n-well doping should be high enough to guarantee a low resistivity path to the side cathode contact.

In order to attain low doping concentration within the space charge region coupled with a thin ($\sim$1 μm) and low-resistivity ($<$ 0.1 Ω·cm) buried layer, we designed a retrograde custom implant, referred in the following as *deep n-iso*. The SPAD junction is enclosed in a pocket delimited underneath by the deep n-iso and laterally by a heavily doped BCD8sP n-well, which overlaps the deep n-iso and provides a low resistance path to the side cathode contact. We sized such a double n-type well pocket to guarantee 50 V isolation toward the substrate.

A. 'Shallow' SPADs

Fig. 1 shows the simulated cross-section of a p^+/n junction BCD SPAD. In this 'virtual' guard ring structure, a dedicated Phosphorus implant, referred in the following as *enrichment*, is employed to define the avalanche region. Indeed, a fully depleted p-type guard ring is formed implicitly, owing to the residual epitaxial layer doping. The p^+ anode and active masks extend laterally 1–2 μm beyond the enrichment mask, thus leaving a gap between the shallow trench isolation (STI) and the avalanche region edge. Being two order of magnitude higher than the mean free path of carriers, the gap prevents the interface states at the SiO_2–silicon boundary from affecting DCR and afterpulsing [30]. The resulting annular space is used as the silicidized anode ohmic contact, while a salicide (self-aligned silicide) blocking mask prevents salicidation in the SPAD avalanche region and forms a pinhole shielding the guard ring from light. Finally, a polysilicon field-plate, kept at the same anode potential, avoids edge breakdown.

Through the custom tailoring of the enrichment doping profile, a suitable shaping of the electric field in the space charge region can be achieved. However, a few iterations may be needed to identify the best electric field distribution to attain the desired trade-off between device properties. In this work we present two designs, a first one (wafer A) with a breakdown voltage of 35.8 V at room temperature (see Fig. 2) and a second split lot (wafer B) with a 25.4 V breakdown, as a result of the higher dose and lower energy of the enrichment implant. According to simulations, performed with the Synopsys Sentaurus TCAD suite [31], [32] and STMicroelectronics process calibration data, for a given excess bias voltage (i.e., the voltage above breakdown) the electric field distribution has a ($\sim$10%) lower and broader peak in wafer A, while the space charge width differs by less than 100 nm, since the deep n-iso stops the electric field.

B. 'Deep' SPADs

An intrinsic limitation of CMOS SPADs, which are typically one-sided p+/n junctions, arises from the fact that NIR photons are primarily absorbed in the n-type side of the depletion layer. Therefore, avalanches are primarily initiated by holes [1], which have a lower avalanche triggering probability compared to electrons in Silicon [33].

A promising solution is to implant high energy Boron ions instead of low energy Phosphorus ones into the enrichment mask opening, as shown in Fig. 3, thus creating a 'deep' p/n+ junction. This way, the avalanche is primarily initiated by minority electrons moving toward the buried multiplication region, leading to a higher PDE [34].

For the split lot C, we sized a Boron enrichment implant for achieving nearly the same electric field peak and depletion layer width as in wafer B, thus making relative performance comparison straightforward.

III. Photon Detection Efficiency

For measuring the PDE, i.e., the probability of detecting an incoming photon, we monitored the light from a broadband and stable Quartz Tungsten Halogen (QTH) lamp, attenuated by means of optical neutral density filters and passed through a monochromator, by means of a large-diameter ($>$1 cm)

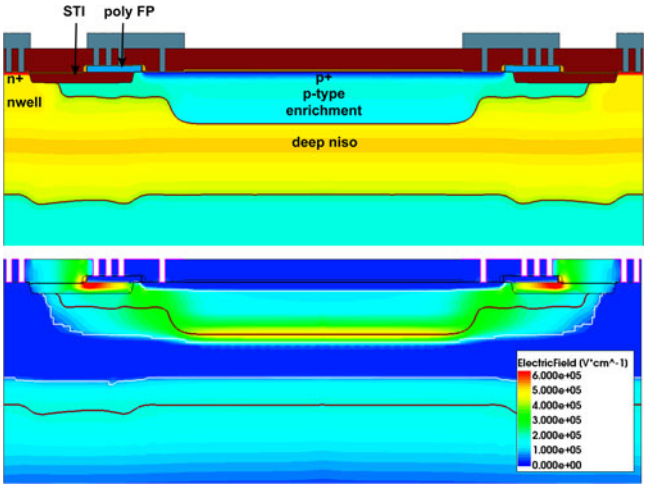

Fig. 3. TCAD process (top) and device (bottom) simulation of a "deep" BCD SPAD (wafer C) at 5 V excess bias.

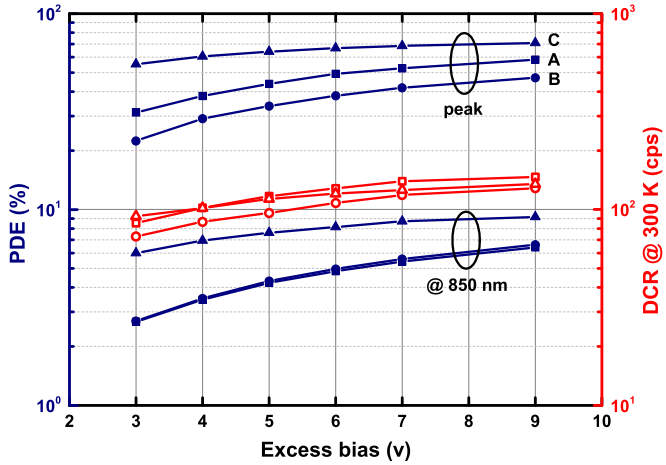

Fig. 5. PDE and DCR as a function of the excess bias for 'shallow' (wafers A and B) and 'deep' (wafer C) BCD SPADs of 30 μm-diameter.

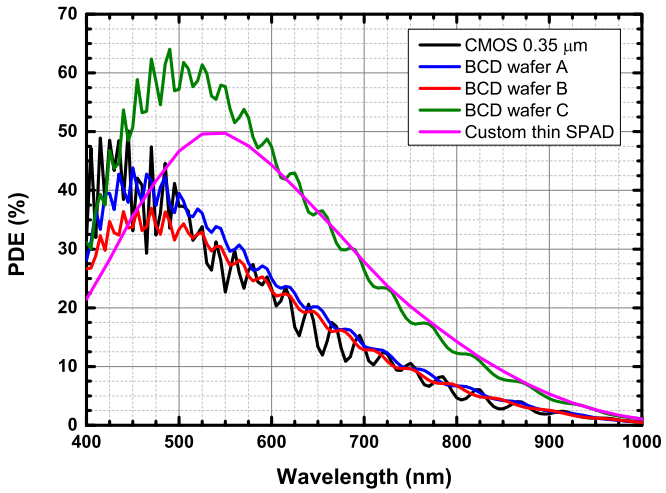

Fig. 4. PDE versus wavelength (at 5 nm steps) of 30 μm-diameter BCD SPAD devices, operated at 5 V excess bias, compared to a 0.35 μm CMOS SPAD [35] and of a custom Silicon SPAD [36], in the same setup.

calibrated photodiode. The light from the monochromator is fed to an integrating sphere to obtain a spatially uniform photon flux over the SPAD. The PDE is calculated as the rate of net photon detections (i.e., after subtracting the DCR), divided by the photon arrival rate through the SPAD avalanche region, i.e., the area defined by the enrichment implant.

Fig. 4 shows the PDE as a function of wavelength of all the split lots described so far. All detectors were held at room temperature (300 K) and biased 5 V above their breakdown voltage. The PDE of the state-of-the-art 0.35 μm CMOS SPAD of Ref. [35] and the Silicon SPAD of [36], fabricated using a fully custom planar technology, have been measured with the same setup and are reported in Fig. 4 as benchmarks.

Shallow SPADs from wafers A and B reach PDE values that are comparable to the device of [35] in the 500–1000 nm range, but lower than those achievable with a fully custom SPAD. The PDE peaks are 36% and 43% at 450 nm and the PDE is 7% at 800 nm. The interference ringing, due to the multiple dielectric interfaces in the back end of line (BEoL), is significantly lower than that of [35], thanks to the passivation that was selectively thinned over the SPADs avalanche region.

As expected, deep SPADs (wafer C) outperform the shallow ones (wafers A and B), owing to the higher avalanche triggering probability of electrons with respect to holes. The PDE peak shifts from 450 nm to 490 nm and is above 60%. The PDE is very good in the NIR, being approximately 12% at 800 nm, 8% at 850 nm and still 4% at 900 nm, and even better than custom SPADs in the 400–600 nm range. The reason being that most high-energy photons are absorbed in the upper neutral region of custom SPADs, and photo-generated holes (collected by diffusion) trigger the avalanche [34]. On the other hand, in wafer C SPADs the avalanche is primarily triggered by electrons regardless of the wavelength, leading to a higher PDE at short wavelengths.

Fig. 5 shows the PDE and DCR (see Section IV) dependence on excess bias of 30 μm-diameter SPADs at 300 K. At 9 V excess bias the PDE of the deep SPAD is 71% at 490 nm wavelength and 9% at 850 nm.

An important issue in SPAD fabrication is the electric field uniformity that leads to uniform PDE and jitter. In order to assess such uniformities, we focused an 850-nm laser into a small spot ($\sim$5 μm-diameter), we performed an x-y scan at 1 μm steps across the detector, and measured the avalanches ignition rate at each position. After checking the laser power stability, we obtained the relative PDE maps shown in Fig. 6. The PDE is quite uniform over the sensitive area and it correctly drops outside its edges, with no detectable premature edge breakdown. The FWHM of the PDE map is 29, 30 and 31 μm for wafer A, B and C, respectively. The normalized PDE drops from 0.9 to 0.1 over a length of 6 and 7 and 3 μm for wafer A, B and C respectively. The reason of the sharper drop of the deep SPAD is twofold: i) the avalanche triggering probability of electrons increases faster with the electric field and is closer to saturation at 5 V excess bias (see Fig. 5); ii) the polysilicon field plate that avoids edge breakdown smooths the electric field transitions of shallow SPADs.

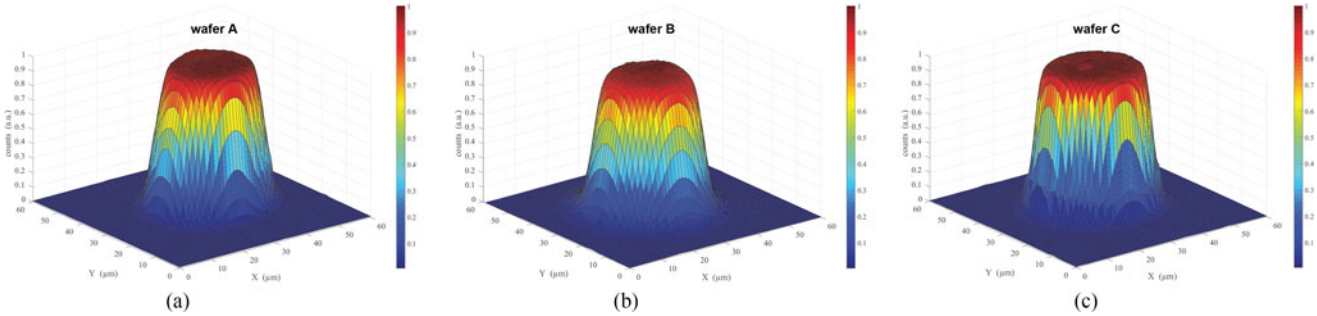

Fig. 6. Normalized PDE maps of a 30 μm SPAD from wafers A, B and C operated at 5 V excess bias, measured by scanning a light spot (850 nm wavelength, ~5 μm-diameter) across the detector with 1 μm steps. The measured FWHM is 29, 30 and 31 μm for wafer A, B and C, respectively.

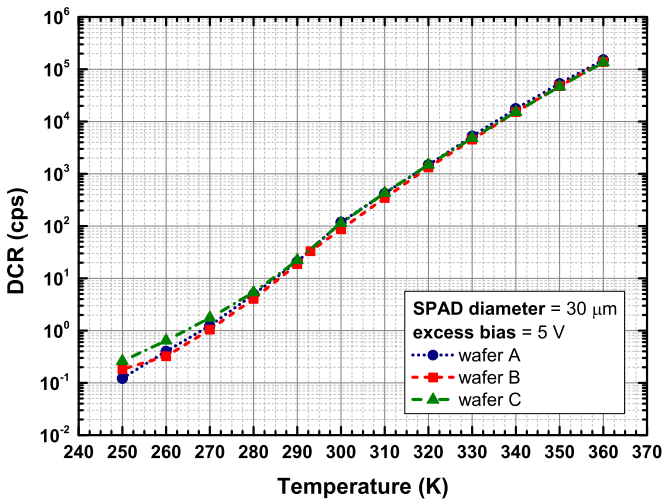

Fig. 7. Temperature dependence of DCR for 30 μm-diameter SPADs operated at 5 V excess bias.

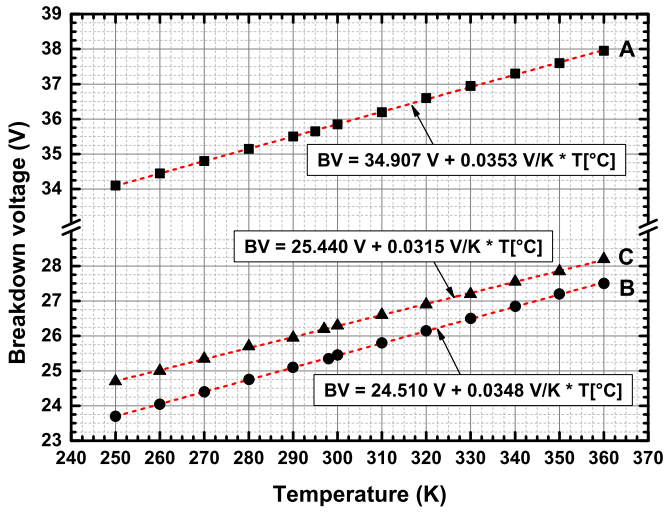

Fig. 8. Breakdown voltage vs. temperature: experimental data and linear fitting for 'shallow' (wafers A and B) and 'deep' (wafer C) SPADs.

IV. Dark Count Rate

The generation of carriers within the space charge region, due to either Shockley-Read-Hall processes [26] or trap-assisted tunneling (TAT) [27], gives rise to the DCR, i.e., the average avalanche ignition rate in the absence of illumination, whose Poissonian fluctuations represents the primary noise source of SPADs. The electric field distribution of all the split lots was designed to reduce the weight of the tunneling contribution. As shown in Fig. 5, the DCR dependence on the excess bias tracks the increase and saturation of the avalanche triggering probability (as the PDE does) up to $V_{EX} = 9$ V, demonstrating that field-assisted carrier generation mechanisms are negligible at 300 K for all detectors.

Fig. 7 shows the temperature dependence of DCR of 30 μm-diameter SPADs. All SPADs were operated by a monolithically integrated quenching circuit having the same topology described in [37]. Measurements were performed at a constant excess bias voltage 5 V adjusting the cathode bias for compensating the breakdown drift over temperature (see Fig. 8). In order to rule out afterpulsing (see Section V) a dead-time of approximately 0.25 μs was enforced by the active quenching circuit after each avalanche ignition.

For all the wafers, the DCR increases from 1 to 10^5 cps over the temperature range from 0 to 90 °C. The DCR is almost the same among the three wafers, as a direct consequence of the BCD8sP high reproducibility. The deep SPAD (wafer C) exhibits a change in the slope of the curve at about 0 °C. Conversely, tunneling generation is negligible for the shallow SPAD from wafer A and is barely visible at –20 °C for the shallow SPAD from wafer B.

Fig. 9 shows the DCR at room temperature vs. SPAD diameter at 3 V, 4 V and 5 V excess bias, respectively; SPAD samples are from wafer A. The linear dependence of DCR with the SPAD area (i.e., the quadratic dependence on diameter) is a clear signature that interface states at STI SiO_2–silicon boundary do not significantly affect the DCR [30].

V. Afterpulsing

During an avalanche, few carriers may get trapped by deep levels and released with a statistical delay, eventually igniting a correlated 'afterpulse' when the SPAD is re-armed. Since each afterpulse is correlated to the avalanche ignition that populated the deep levels, afterpulses have a strong correlation to the signal as well, thus causing non-linear distortion in photon-counting

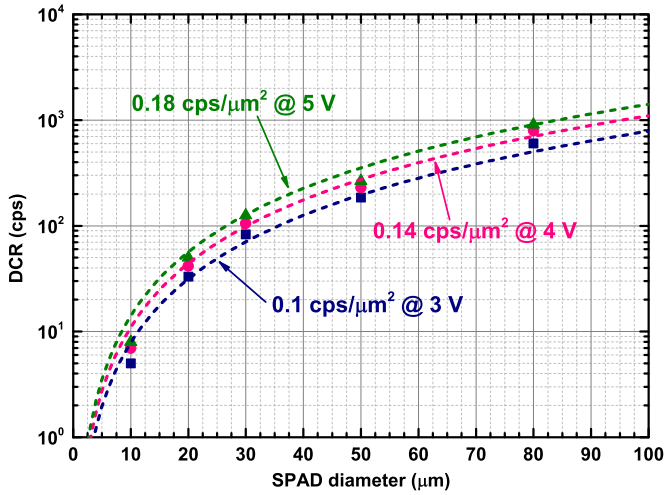

Fig. 9. Room temperature DCR vs. SPAD diameter at different excess bias, for wafer A, together with a quadratic fitting. The DCR per unit area is 0.1 cps/μm^2 at V_{EX} = 3 V, 0.14 cps/μm^2 at 4 V and 0.18 cps/μm^2 at 5 V.

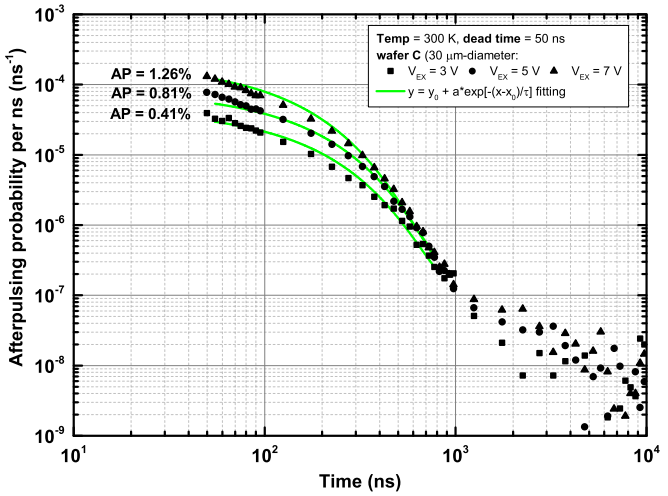

Fig. 11. Afterpulsing probability density for 30 μm-diameter SPADs from wafers C, operated by an integrated active quenching circuit (AQC) with 50 ns hold-off at 3, 5 and 7 V of excess bias.

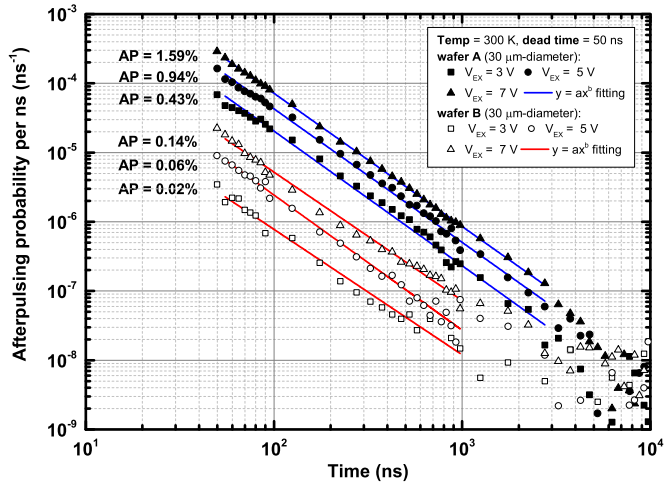

Fig. 10. Afterpulsing probability density for 30 μm-diameter SPADs from wafers A and B, operated by an integrated active quencing circuit (AQC) with 50 ns hold-off at 3, 5 and 7 V of excess bias.

measurements. As a result, the afterpulsing probability has to be kept small, down to 1% or even lower, by enforcing a sufficiently long dead-time to allow nearly all trapped carriers to be emitted and swept from the multiplication region.

Figs. 10 and 11 show the afterpulsing probability density measured at room temperature on 30 μm-diameter SPADs by using the time-correlated carrier counting (TCCC) technique [38]. Such a technique requires to measure the time intervals between two successive avalanche ignitions and to collect a histogram of a statistically significant number of repetitions (about 10^7 events in our measurements). The content of each histogram cell is normalized to the total number of repetitions and then is divided by the time-bin width in order to result in the probability distribution that describes the time between consecutive avalanche ignitions. Eventually, the afterpulsing probability density is obtained by subtracting the exponential decay due to the intrinsic DCR (measured at very long time-delays) from the distribution.

For the shallow SPADs shown in Fig. 10, the afterpulsing probability density decay is fitted quite well by a power-law temporal dependence, as recently proposed in [39] for InGaAs/InP SPADs. This is a clear signature that there is a broad and dense spectrum of trap levels, contrary to the common belief that just a few defect families are dominant. Conversely, measurements on wafer C with deep multiplication region shown in Fig. 11 clearly exhibit a dominant exponential decay. We believe that defect types and concentrations are similar in all processed wafers. However, in deep SPADs, traps capturing electrons (and not holes) are those primarily effective in triggering afterpulses. We can conclude that there is a dominant donor trap and many acceptor traps with close energies.

Figs. 10 and 11 also report the total afterpulsing probability, i.e., the integral of each afterpulsing probability density curve. As can be seen, at room temperature and with 50 ns dead-time, the afterpulsing probability is approximately 1% for 30 μm-diameter SPADs from wafer A and C, and below 0.1% for wafer B SPADs, probably due to the higher electric field. These excellent results (see also Table I) are due to both the high cleanness of the BCD8sP STMicroelectronics foundry and the fast avalanche quenching performed by the monolithically integrated quenching circuit.

VI. Timing Jitter

In time-correlated single-photon counting (TCSPC) measurements, e.g., in FLIM and time-of-flight LiDAR, each photon is timed with respect to an exciting laser pulse. Hence, another important SPAD performance metric is the uncertainty in the identification of the photon arrival time, i.e., its timing jitter.

Fig. 12 shows, on a log scale and after amplitude normalization, the pulse of a gain-switching laser at 850 nm, which uniformly illuminates the entire SPAD area, acquired with the BCD SPADs described so far and a standard TCSPC setup. The laser has been attenuated so that the mean number of photons per pulse reaching the avalanche region is lower than 0.05.

TABLE I
PERFORMANCE COMPARISON

	Technology (nm)	Diameter (μm)	V_{EX}/V_{BD} (V)	Peak PDE (%) @λ (nm)	PDE (%) @850 nm	DCR/unit area (cps/ μm^2)	AP (%)	Jitter (ps)	Diffusion tail (ps)
Ghioni [1]	custom thin	50-200	5-10/30-35	52-68 @ 550	12-15	0.4-1.6[a]	2[b]	35[c]	280-110[c]
Gulinatti [2]	custom RE	50	20/45-55	58 @ 650	28	0.3[d]	N/A	93[c]	~400[c]
Villa [35]	350	10-500	2-6/25	37-53 @ 450	2-4.5	0.05[a]	~ 1[e]	~ 90[f]	N/A[f]
Leitner [45]	180	10	1-3.3/21	35-47 @ 450	N/A[g]	0.3-1.8[a]	N/A	N/A	N/A
Veerappan [44]	180	12	2-10/23.5	24-48 @ 480	3-8	0.16-176[a]	0.03-0.3[h]	112-88[i]	~170[i]
Veerappan [46]	180	12	1-4/14	23-47 @ 480	4-7	0.28-16[d]	0.2[j]	161-141[i]	~430[i]
Veerappan [47]	180	12	1-12/25	18-47@ 520	2-8	0.2-6[d]	7.2[k]	139-101[i]	N/A
Xu [48]	150	10	2-5/19	24-32 @ 450	2-3.5	0.1-1	1-13[l]	42[m]	~430[m]
Lee [49]	140 (SOI)	12	0.5-3/11	10-25 @ 500	2.5-7	0.9-260	1.7[n]	65[o]	N/A
Richardson [50]	130	8	0.6-1.4/14	18-28 @ 500	3-5	0.24-0.6[a]	0.02[p]	~200[q]	N/A
Richardson [51]	130	8	0.2-1.2/12-18	18-33 @ 450	2-5	0.4-0.8	0.02[r]	237-184[s]	N/A[s]
Niclass [52]	130	10	1-3.5/10	34-41 @ 450	3	120-1300[d]	N/A	144[i]	N/A[i]
Gersbach [53]	130	4.3	1-2/9	18-30 @ 480	3.5-5	1.5-11.5	<1[t]	125[i]	~720[i]
Charbon [54]	65	8	0.05-0.4/9	2-5.5 @ 420	0.2-0.4	340-15.6k[a]	<1[u]	235[i]	N/A
this work (A)	160	10-80	3-9/36	31-58 @ 450	2.5-6.5	0.12-0.2[v]	0.43-1.59[w]	39-28[c]	93[x]
this work (B)	160	10-80	3-9/25	22-47 @ 450	2.5-6.5	0.1-0.18[v]	0.02-0.14[w]	36-28[c]	107[x]
this work (C)	160	10-80	3-9/26	55-71 @ 490	6-9	0.13-0.19[v]	0.41-1.26[w]	41-28[c]	48[x]

[a]At 20°C. [b]200 μm-diameter, at 25°C, 80 ns dead time, V_{EX} = 5 V. [c]820 nm wavelength [d]At 25°C. [e]30 μm-diameter, at 25°C, 40 ns dead time, V_{EX} = 5 V, integrated AQC. [f]A time resolution of 28-37 ps FWHM and a diffusion tail of 160-340 ps were demonstrated in Ref. [42] using the substrate bias as a trade-off parameter between jitter and diffusion tail. [g]PDE = 10-13% at 800 nm. [h]300 ns dead time, V_{EX} = 2-10 V. [i]637 nm wavelength. [j]300 ns dead time, V_{EX} = 4 V. [k]300 ns dead time, V_{EX} = 11 V. [l]50 ns dead time, V_{EX} = 1.5-5 V. [m]831 nm wavelength. [n]200 ns dead time, V_{EX} = 2 V. [o]405 nm wavelength. [p]200 ns dead time, V_{EX} = 2 V. [q] 815 nm wavelength. [r]50 ns dead time. [s]470 nm wavelength. [t]180 ns dead time. [u]5 μs dead time. [v]At 300 K. [w]30 μm-diameter, at 300 K, 50 ns dead time. [x]850 nm wavelength.

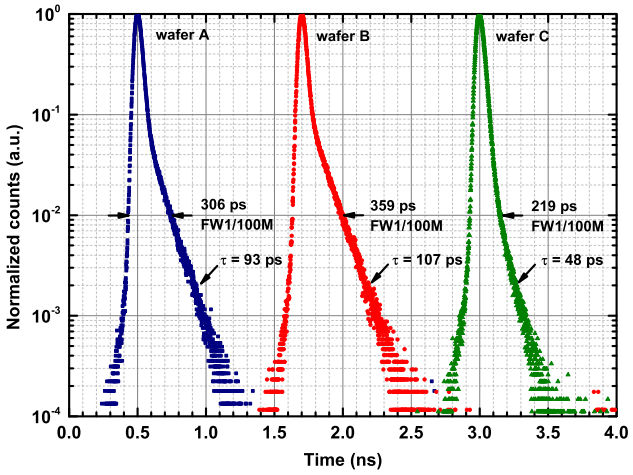

Fig. 12. Timing response of 30 μm SPADs belonging to wafer A, B, and C to a narrow (~50 ps) laser pulse at 850 nm. The excess bias voltage is 5 V. All curves show a narrow peak with less than 60 ps FWHM and a very clean and short exponential diffusion tail. Note that the Full-Widths at 1/100 of the Maximum (and not the FWHM) are reported in the plots.

Pile-up corrections to the acquired histogram are not required, since the probability of having more than one photon per pulse is negligible. The SPADs are operated at room temperature by using a monolithically integrated AQC. The timing signals are generated at the cathode by employing the current pickup network described in [40], [41] (with ~500 ps differentiating time constant) that feeds a fast comparator. With a threshold voltage of 5 mV, the avalanche is sensed at approximately 100 μA, when it is still confined within a small area around the seed point, in order to avoid degradation of the photon-timing performances due to the statistical phenomena involved in the avalanche lateral spread [29]. The Full-Width at Half Maximum (FWHM) of the responses of the three SPADs is always about 60 ps, limited by the intrinsic laser pulse width.

The so-called 'diffusion tail', which is due to minority carriers photogenerated in the deep n-iso neutral region and diffusing toward the space charge is minimized, appearing more than one decade below the peak and being purely exponential (see Fig. 12). The lifetime fit parameters are just 93 ps and 107 ps for wafer A and B, respectively, and 48 ps for wafer C, with a standard error of about 1 ps. These extremely sharp timing responses lead to less than 400 ps FW1/100M (at 1/100 from the peak), and less than 1 ns even down four decades (FW1/10,000M) from the peak, thus being attractive for applications requiring high-resolution measurements of fast optical signals with wide dynamic range.

In order to ascertain the intrinsic FWHM timing jitter, we characterized the BCD SPAD responses to a narrower (FWHM ~15 ps) 820 nm pulsed laser (*Antel MPL-820 laser module*). Fig. 13 shows the measurements. Thanks to the very short diffusion tails, very weak features on the laser pulse waveform can be observed, such as the residual optical oscillation after the main peak, which is likely due to a ringing in the fast driving current pulse. The measured FWHM timing resolution is approximately 30 ps. Fig. 14 shows the peak FWHM dependence on excess bias voltage. The higher the excess bias voltage, the narrower is the measured FWHM, because of the faster avalanche current build-up. By quadratically subtracting the laser pulse FWHM, the actual time resolution of the BCD SPADs is better than 24 ps FWHM at V_{EX} = 7 V for all detectors.

These outstanding results have been achieved thanks to the tailored electric field in the avalanche region and to the deep n-iso implant. Specifically, the low resistivity path towards the

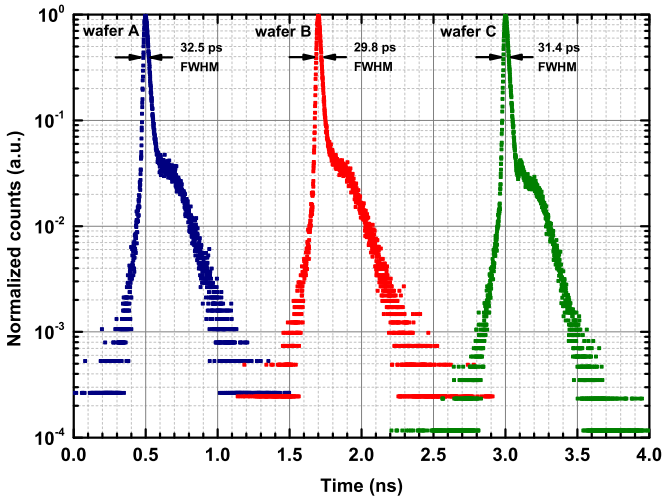

Fig. 13. Timing response to a very narrow (~15 ps) laser pulse at 820 nm. The excess bias voltage is 5 V.

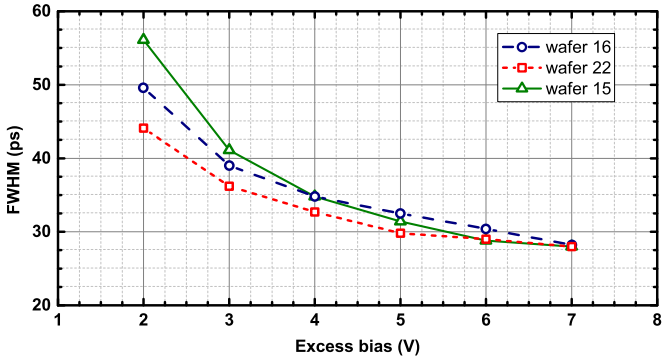

Fig. 14. Measured timing jitter as a function of excess bias. The laser pulse (~15 ps FWHM) has not been quadratically subtracted.

side ohmic cathode established by the deep n-iso high doping relaxes the well-known trade-off between time resolution FWHM and diffusion tail time constant of CMOS SPADs [35], [42].

The achieved state-of-the-art performance enables applications requiring single-photon detection of extremely fast and sharp visible and NIR optical signals, with wide dynamics. For example, to detect transparent objects just behind strongly reflecting targets in 3D time-of-flight LIDAR systems (e.g., a second opaque object with a factor 10 000 in reflectivity just 1 ns, i.e., 15 cm, beyond a first highly reflecting object); in time-resolved near-infrared spectroscopy (NIRS) for the study of the functional activation of human cerebral cortex, even with non-contact optical sensing [43].

VII. State-of-the-Art Comparison

Table I compares the performance of the BCD SPADs presented in this work with other state-of-the-art devices suitable for arrays (i.e., isolated from the chip substrate [44]) fabricated in either custom or CMOS technologies.

Among CMOS SPADs, those developed in 0.35-μm [35] and 0.18-μm technologies [44]–[47] resulted in higher PDE, since the higher doping level of 150–130 nm technologies limits the PDE peak to about 30%. Veerappan *et al.* [44] attained the best PDE spectral response: peak PDE of 47.6% at 480 nm and >40% from 440 to 620 nm at 10 V excess bias. However, the authors claim that the integration of circuitry for reliable operation at 10 V excess bias is not straightforward. The PDE drops considerably at 4 V excess bias, but the overall spectral response remains among the best CMOS SPADs reported in the literature. In [46], the same authors attained at 4 V excess bias nearly the same PDE spectral response they reported in [44] at 10 V. Specifically, they designed a narrower depletion region and a relatively wider neutral region, from which holes are collected by diffusion. The drawback of this approach is a relatively slow diffusion tail (~400 ps lifetime) in the timing response.

To the best of our knowledge the performance achieved by the wafer C SPAD presented in this work is superior to any other substrate isolated CMOS SPAD reported in the literature. At 5 V excess bias the peak PDE is 60% at 490 nm. It is worth noting that the PDE spectral response of our 'deep' SPAD and the state-of-the-art device of [46] become nearly identical in the 650–850 nm wavelength range. However, the BCD deep SPAD is a better candidate for photon timing application at red and NIR wavelengths, owing to its much faster diffusion tail (<50 ps lifetime).

Table I also shows that the achieved DCR per unit area (<0.2 Hz/μm^2) is better than most CMOS SPADs. Only the 0.35-μm low-noise SPAD reported in [35] attains better noise performance (0.05 Hz/μm^2). As shown in Fig. 5, the excess bias voltages can be increased up to 9 V with little impact on DCR. Conversely, for most CMOS SPADs in Table I, the DCR exhibits a strong dependence on the excess bias voltage.

It is harder to make a fair afterpulsing comparison between different SPAD designs and CMOS technologies. The reason being that each research group performed measurements in different experimental conditions (e.g., SPAD diameter, excess bias, dead time, quenching circuit, etc.).

Finally, to the best of our knowledge, the achieved timing response is the new state-of-the-art among CMOS [42] and custom SPADs [1] so far reported in the literature.

VIII. Conclusion

We have reported the design criteria and experimental characterization of the first SPADs ever fabricated in a BCD technology, which exploit the high modularity of the STMicroelectronics BCD8sP process to achieve enhanced PDE, low DCR and state-of-the-art timing resolution. To the best of the author's knowledge the overall detection performance surpasses the very best CMOS SPADs with substrate isolation. We are currently fabricating a 32 × 32 time-resolved SPAD imager to fully characterize the performance uniformity over a statistically significant number of BCD SPADs as in [55], [56].

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