Heterogeneous CMOS Photonics Based on SiGe/Ge and III–V Semiconductors Integrated on Si Platform

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***Abstract*—The heterogeneous integration of SiGe, Ge, and III–V semiconductors on Si provides many opportunities to develop high-performance photonic integrated circuits through complementary metal oxide semiconductor (CMOS) processes. We found that strained SiGe possesses greater free-carrier effects than Si, contributing to the improved modulation efficiency of Si-based optical modulators. In addition to low-dark-current Ge photodetectors (PDs) with GeO_2 passivation, we investigated Ge CMOS photonics platform for midinfrared wavelengths. We demonstrated Ge passive waveguides and carrier-injection variable optical attenuators (VOAs) on a Ge-on-insulator wafer. We also investigated III–V CMOS photonics platform on a III–V-on-insulator (III–V-OI) wafer. The strong optical confinement in the III–V-OI structure enabled the realization of ultrasmall III–V passive waveguides similarly to those in Si photonics. Carrier-injection InGaAsP optical switches and VOAs as well as InGaAs waveguide PDs were also demonstrated on III–V-OI wafers. We discuss the opportunities and challenges of heterogeneous CMOS photonics technologies to develop high-performance electronic–photonic integrated circuits for near-infrared and midinfrared applications.**

***Index Terms*—Si photonics, CMOS photonics, electronic–photonic integrated circuits, heterogeneous integration.**

I. Introduction

SILICON photonics provides a versatile platform for photonic integrated circuits (PICs) because the strong optical confinement in a Si waveguide on a Si-on-insulator (SOI) wafer offers a new path for developing ultra-small photonic components through complementary metal oxide semiconductor (CMOS)-compatible processes. As a result, the intense development of passive and active photonic components on SOI wafers has been taking place.

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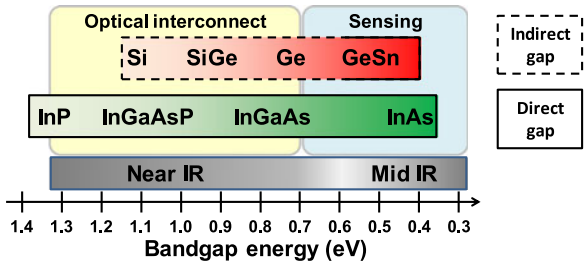

Fig. 1. Bandgap energies of group IV and III-V compound semiconductors covering near-infrared and mid-infrared wavelengths for optical interconnect and sensing applications.

Since Si is an indirect-bandgap semiconductor and transparent to near-infrared wavelengths, the heterogeneous integration of group IV and III-V semiconductors on Si is a common way to extend the functionalities of Si photonics platform. Fig. 1 shows the bandgap energies of SiGe, GeSn, and InGaAsP compounds. The monolithic integration of narrow-bandgap Ge or SiGe on Si is one of the standard ways to build photodetectors (PDs) for near infrared wavelengths on Si photonics platform [1]. Moreover, GeSn is expected to extend the available wavelength range for PDs and laser diodes (LDs) to mid-infrared wavelengths [2]. Direct-bandgap InP-based III-V compounds are more suitable for the monolithic integration of LDs on the Si photonics platform. The wafer bonding of III-V layers on Si enables III-V/Si hybrid LDs, which are currently the most promising way to integrate light sources on the Si photonics platform [3], [4]. Recently III-V lasers directly grown on Si have emerged as monolithically integrated light sources [5], [6]. Photonics devices operating at mid-infrared wavelengths are available when we use InAs-related compounds. Note that Ge and III-V semiconductors are also attractive for electronics because of their high hole and electron mobilities [7], [8]. Ge/III-V CMOS transistors [9] have been intensively developed to replace current Si CMOS transistors. Thus, the heterogeneous integration of group IV and III-V semiconductors on Si provides numerous opportunities for developing high-performance electronic-photonic integrated circuits (EPICs) operating at near-infrared and mid-infrared wavelengths for optical interconnect and sensing applications.

In this paper, we discuss CMOS photonics technologies based on the heterogeneous integration of SiGe, Ge, and III-V semiconductors on Si, which enable high-performance EPICs

through CMOS-compatible processes. We present strained SiGe technologies for high-performance optical modulators. Then, we discuss low-dark-current Ge PDs with GeO_2 passivation. Ge CMOS photonics platform for mid-infrared wavelengths is also introduced. We also present III-V CMOS photonics platform based on a III-V-on-insulator (III-V-OI) wafer, enabling III-V photonics on Si similarly to Si photonics.

II. Strained SiGe Optical Modulators

Since the emergence of a high-speed Si optical modulator with a modulation speed exceeding 1 GHz, Si optical modulators have developed rapidly. Since there is no electrical-field-induced electro-optic effect in Si, the free-carrier effects including the plasma dispersion effect and free-carrier absorption are the major practical phenomena used to modulate refractive index and absorption coefficient of Si [10]. According to the Drude model, the free-carrier-induced changes in the refractive index (Δn) and absorption $(\Delta\alpha)$ are expressed as

$$\Delta n = -\left(e^2\lambda^2/8\pi^2c^2\varepsilon_0 n\right)\left[\Delta N_e/m_{\mathrm{ce}}^* + \Delta N_h/m_{\mathrm{ch}}^*\right] \quad (1)$$

$$\Delta\alpha = -\left(e^3\lambda^2/4\pi^2c^3\varepsilon_0 n\right)\left[\Delta N_e\Big/ {m_{\mathrm{ce}}^*}^2\mu_e + \Delta N_h\Big/ {m_{\mathrm{ch}}^*}^2\mu_h\right] \quad (2)$$

where ΔN_{e} is the change in the free electron density, ΔN_{h} is the change in the free hole density, e is the elementary charge, λ is the wavelength, c is the speed of light in vacuum, ε_0 is the vacuum permittivity, n is the unperturbed refractive index, m_{ce}^* is the effective conductivity mass of electrons, m_{ch}^* is the effective conductivity mass of holes, μ_{e} is the electron mobility, and μ_{h} is the hole mobility. When the number of free carriers is modulated by depletion, accumulation, or injection, we can achieve phase and intensity modulation [11]. To achieve the balance between modulation efficiency and modulation bandwidth, carrier depletion through a PN junction is a practical method. However, the modulation efficiency $V_\pi L$ in depletion-based Si optical modulators typically ranges from 1 to 4 Vcm, which is insufficient for low-power operation or large-scale integration. Thus, it is essential to enhance the free-carrier effects themselves for high-performance Si-based optical modulators.

To improve the performance of Si-based optical modulators, we have proposed the introduction of strained SiGe into the Si waveguide [12]. When SiGe is grown on Si, a biaxial compressive strain is applied to SiGe, resulting in a reduction in the effective hole mass in SiGe. As is expected from (1) and (2), the free-carrier effects are enhanced when the effective masses decrease. Fig. 2 shows the enhancement factors of the changes in the refractive index and absorption due to holes in SiGe. The hole effective mass has been numerically analyzed by the $k \cdot p$ method. As shown in Fig. 2, it was predicted that the enhancement factor of the plasma dispersion effect will exceed a factor of three when the Ge mole fraction is greater than 0.5. Because the hole effective mass is more sensitive to compressive strain, the strain effect on the enhanced plasma dispersion effect is dominant as compared with the impact of increasing the Ge content. Since the electron effective mass is not changed so much by compressive strain, the enhancement of the electron-induced plasma dispersion effect is negligible in SiGe, which should be taken into account to analyze SiGe optical modulators. The free-carrier absorption will also be enhanced by more than a factor of four. It is worth noting that the enhancement of the change in the absorption is expected to be 40% greater than that of the change in the refractive index because of the impact of the hole mobility in SiGe. In case of optical switch application, the increased absorption degrades on-state crosstalk by approximately 4 dB. In terms of the enhancement of the free-carrier effects, it is preferable to use SiGe with as high Ge content as possible. However, the bandgap energy in strained SiGe simultaneously decreases rapidly. Thus, for a given wavelength, there is a trade-off between the enhancement of the free-carrier effects and the insertion loss due to interband absorption. When a 1.55 μm wavelength is assumed, the optimal Ge contents for SiGe bulk and a quantum well (QW) are 0.3 and 0.5, respectively. When a mid-infrared wavelength is considered, the intervalence band absorption in SiGe might also be taken into account for more accurate calculation.

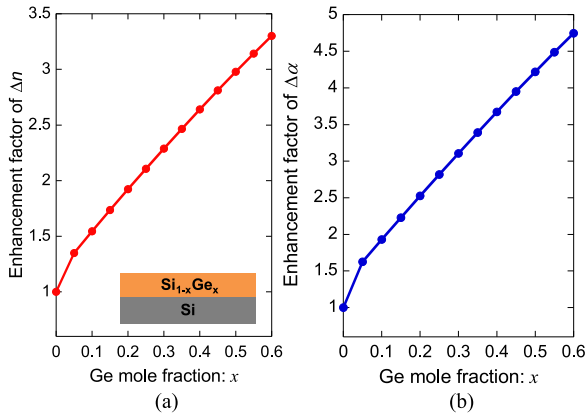

Fig. 2. Enhancements of changes in (a) refractive index and (b) absorption in SiGe grown on Si due to the hole-induced free-carrier effects [12].

A. Carrier-Injection SiGe Optical Modulator

To evaluate the effect of modulating the strain-induced hole effective mass on the free-carrier effects in SiGe, we have fabricated a carrier-injection SiGe optical modulator [13]. Fig. 3(a) is a schematic of the SiGe optical modulator. A strained SiGe layer is embedded in a Si rib waveguide formed on an SOI wafer. A lateral PIN junction is formed along the waveguide for carrier injection. Injected holes and electrons accumulate in the SiGe layer because of the band discontinuity between SiGe and Si, contributing to the effective modulation of the refractive index and absorption. The fabrication procedure is as follows. After thinning an SOI layer by thermal oxidation, a 30-nm-thick $Si_{0.77}Ge_{0.23}$ layer and a 75-nm-thick Si layer are grown by a standard chemical vapor deposition tool widely used in CMOS fabs. Since the SiGe thickness is below its critical thickness, the crystalline quality of the SiGe layer is high. A waveguide mesa is formed by dry etching with CF_4 gas. A lateral PIN junction is formed by the ion implantation of B and P. After depositing SiO_2 passivation layer, activation annealing is

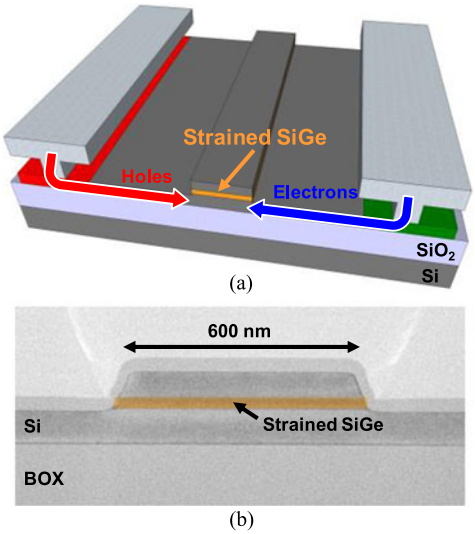

Fig. 3. (a) Schematic of carrier-injection SiGe optical modulator and (b) cross-sectional TEM image of the fabricated device [13].

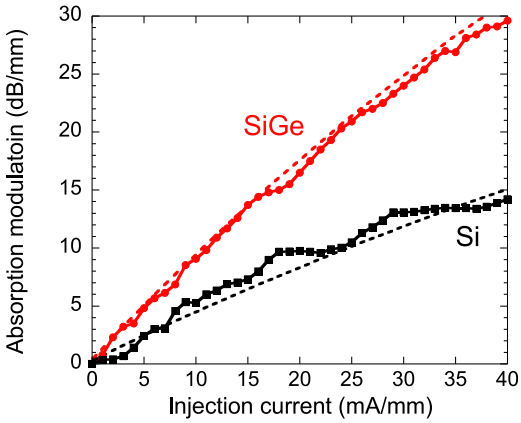

Fig. 4. Results of absorption modulation in SiGe and Si optical modulators as a function of injection current [13]. The dotted lines are simulation results.

carried out. Finally, Al electrodes are formed. Fig. 3(b) shows a cross-sectional transmission electron microscope (TEM) image of the fabricated device. The Si/SiGe/Si waveguide is formed on SiO_2 buried oxide (BOX) layer. The propagation loss of the Si/SiGe/Si waveguide is dependent on the Ge content in SiGe. When the Ge content is 28%, the propagation loss is approximately 0.54 dB/mm [14]. The optical confinement of the SiGe layer is estimated to be 19% by mode analysis. We have also fabricated Si optical modulator with the same dimensions as a reference.

First we examined the enhancement of the free-carrier absorption in SiGe by measuring the change in the transmission as the injection current increases. Fig. 4 shows the absorption modulation in the SiGe and Si optical modulators measured at a 1.55 μm wavelength. It can be clearly observed in Fig. 4 that the SiGe device exhibits greater absorption modulation than the Si device. The injection current required for a given absorption modulation in the SiGe device is approximately half of that in the Si device. The dotted lines in Fig. 4 show simulation results.

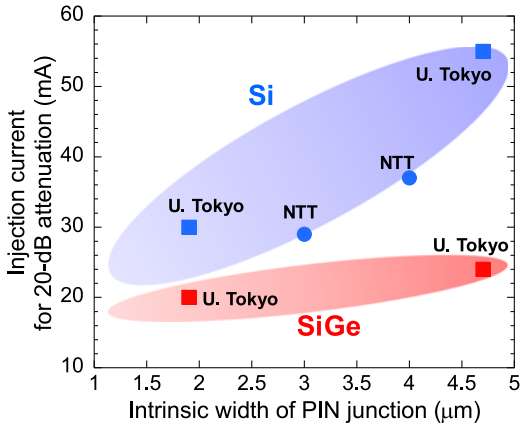

Fig. 5. Benchmark injection current for 20-dB attenuation among 1-mm-long carrier-injection SiGe and Si optical modulators [15].

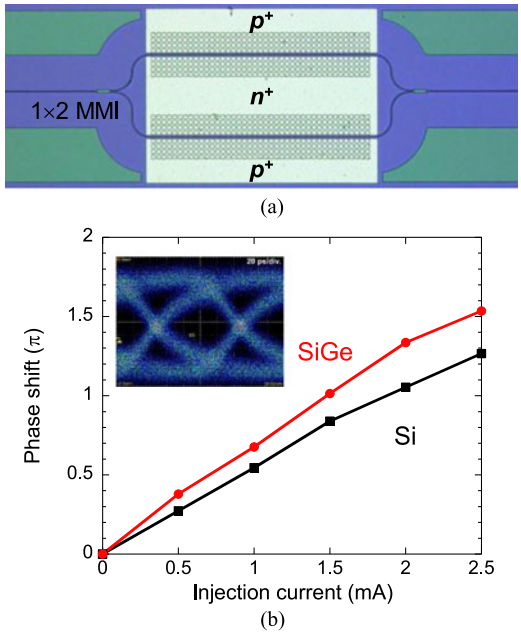

Fig. 6. (a) Plan-view photograph of SiGe asymmetric Mach-Zehnder interferometer optical modulator and (b) phase shift in SiGe and Si devices as a function of injection current [16].

We have obtained a good agreement between our prediction and experimental results. Thus, we have successfully demonstrated the enhanced free-carrier absorption in strained SiGe as theoretically predicted.

Fig. 5 shows the benchmark injection current for 20 dB attenuation for 1-mm-long carrier-injection SiGe and Si optical modulators [15]. When the intrinsic width of the lateral PIN junction decreases, the injection current for 20 dB attenuation decreases owing to improved carrier-injection efficiency. By minimizing the intrinsic width of the PIN junction, we achieved an injection current as low as 20 mA in the SiGe optical modulator.

A SiGe asymmetric Mach-Zehnder interferometer optical modulator has also been fabricated to evaluate the plasma dispersion effect in SiGe [16]. Fig. 6(a) shows a top view of the fabricated SiGe device. The measured phase shifts in the SiGe and Si devices are shown in Fig. 6(b). We found that the SiGe

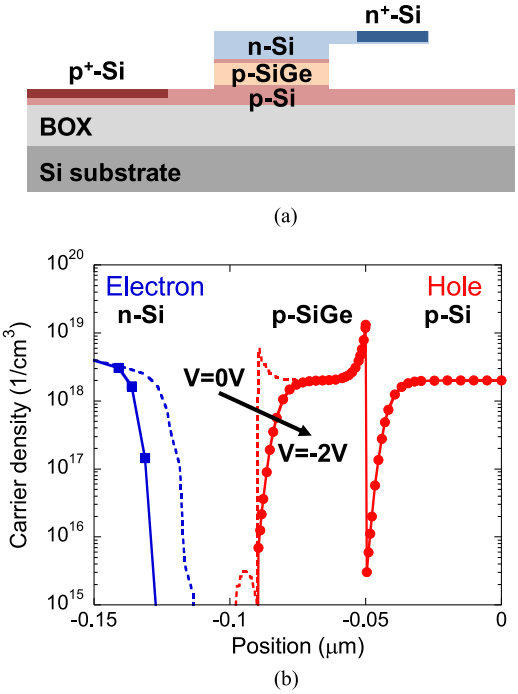

Fig. 7. (a) Cross-sectional schematic of carrier-depletion SiGe optical modulator and (b) electron and hole distributions at reverse bias voltages of 0 V and −2 V [18].

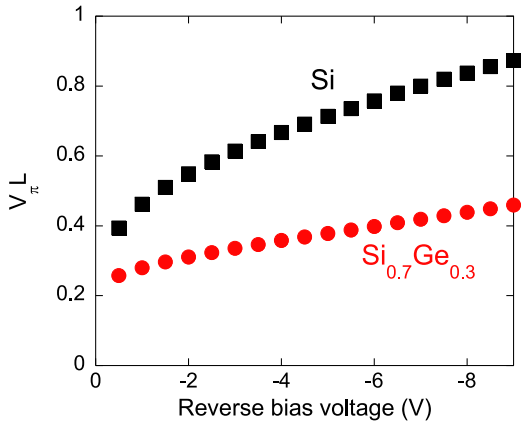

Fig. 8. $V_\pi L$ for carrier-depletion Si and SiGe optical modulators as a function of reverse bias voltage. The Ge content and doping concentration of the SiGe layer are 0.3 and 2×10^{18} cm^{-3}, respectively [18].

device exhibits a greater phase shift than the Si device, evidencing the enhanced plasma dispersion effect in strained SiGe. Modulation at 10 Gbps was also confirmed by using a pre-emphasis driving scheme.

To further improve the modulation efficiency of SiGe optical modulators, we should suppress the out-diffusion of Ge atoms from the SiGe layer into the top and bottom Si layers during high-temperature annealing. In general, high-temperature annealing is required to activate implanted dopants. We also performed high-temperature annealing after SiO_2 passivation to annihilate surface defects on Si surfaces, which is important especially for carrier-injection devices to achieve high injection efficiency. Consequently, the initial Ge content in the as-grown SiGe layer was reduced from 23% to approximately 10%, degrading the modulation efficiency [13]. To avoid high-temperature activation annealing, short-time annealing such as flash lamp annealing or laser annealing can be introduced. We also found that passivation with Al_2O_3 deposited by atomic layer deposition (ALD) at 200 °C is comparable to passivation with thermally grown SiO_2 [17]. We expect that the operation current for a π phase shift can be reduced to approximately 0.6 mA by introducing short-time annealing and Al_2O_3 passivation. The modulation efficiency is also expected to be enhanced if we can use a thicker SiGe layer or fully SiGe rib waveguide.

B. Carrier-Depletion SiGe Optical Modulator

We investigated a carrier-depletion SiGe optical modulator [18]. To deplete a SiGe layer effectively by applying a reverse bias to a PN junction, a vertical PN junction in a waveguide mesa is effective as shown in Fig. 7(a). We designed an n-Si/p-Si/p-SiGe/p-Si PN junction so that the p-SiGe layer starts to be depleted when a reverse bias voltage is applied. Fig. 7(b) shows the electron and hole distributions in the waveguide mesa along the vertical direction at bias voltages of 0 V and −2 V. As shown in Fig. 7(b), the 40-nm-thick p-$Si_{0.7}Ge_{0.3}$ was partially depleted by applying a reverse bias voltage. Fig. 8 shows the numerically calculated $V_\pi L$ for the $Si_{0.7}Ge_{0.3}$ and Si optical modulators. The doping concentration of the p-SiGe and p-Si layers was assumed to be 2×10^{18} cm^{-3}. We achieved $V_\pi L$ of 0.31 Vcm in the SiGe optical modulator at −2 V, which was 1.8 times higher than that in the Si device. Recently, a Si-based optical modulator with a selectively grown p-SiGe layer on the waveguide has been experimentally demonstrated [19].

C. Carrier-Accumulation SiGe Optical Modulator

Carrier accumulation using a MOS capacitor is the most efficient scheme for carrier modulation. In conjunction with equivalent oxide thickness (EOT) scaling for a MOS capacitor, we predicted $V_\pi L$ of 0.033 Vcm by using a $Si_{0.5}Ge_{0.5}$ QW [12].

One of the major obstacles to realizing a SiGe MOS optical modulator is the formation of a high-quality MOS interface between high-Ge-content SiGe and a gate dielectric. Since Ge atoms pile up at the SiGe interface during oxidation, the conventional thermal oxidation of SiGe is not effective. To resolve this issue, we investigated the plasma post-nitridation of an Al_2O_3/SiGe interface [20], [21]. Fig. 9 shows C-V curves of $Al_2O_3/Si_{0.75}Ge_{0.25}$ MOS capacitors, where the Al_2O_3 gate dielectric was deposited by ALD. When we applied no plasma after Al_2O_3 deposition, we observed significant frequency dispersion in the C-V curves around a bias voltage of 0 to 0.5 V, as shown in Fig. 9(a), indicating the existence of a huge number of interface traps. On the other hand, the large frequency dispersion can be suppressed by applying N_2 plasma to the SiGe surface through the Al_2O_3 layer. We found that a SiGe-ON interlayer is formed by plasma irradiation, which reduces the number of interface traps by a factor of ten. The interface trap density evaluated by the conductance method was less than 2×10^{12} cm^{-2}eV^{-1} even when the Ge content was as high as 0.5.

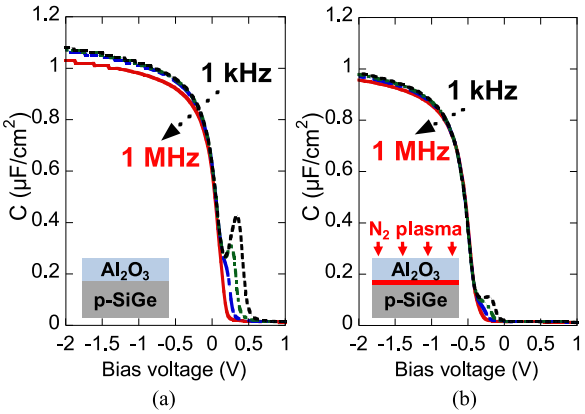

Fig. 9. C-V curves of Al_2O_3/SiGe MOS capacitors with (a) no plasma irradiation and (b) N_2 plasma irradiation [20].

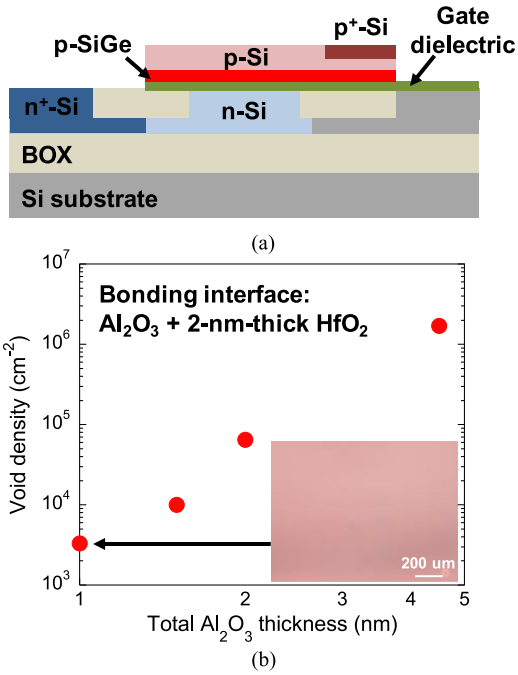

Fig. 10. (a) Schematic of SiGe MOS optical modulator fabricated by wafer bonding and (b) void density on the bonded wafer with an Al_2O_3/HfO_2 bonding interface after 700 °C annealing for 20 min as a function of total Al_2O_3 thickness. The inset is a microscopic image of the wafer surface after annealing [22].

The formation of a polycrystalline Si (poly-Si) gate electrode for the SiGe gate stack is another obstacle to realizing SiGe MOS optical modulators. Since the poly-Si mesa acts as both a gate electrode and a waveguide, high-temperature annealing to induce the crystallization of amorphous Si is required to obtain low resistivity and low propagation loss. However, such high-temperature annealing degrades the interfacial properties of the SiGe MOS capacitor. To avoid high-temperature annealing for crystallization, we have proposed formation of a MOS gate stack by wafer bonding [22]. Fig. 10(a) shows a schematic of our proposed SiGe MOS optical modulator. A p-SiGe/p-Si layer is bonded on a Si waveguide mesa with a gate dielectric to form a hybrid SiGe/Si MOS capacitor. Using this structure, we can avoid the formation of poly-Si to reduce the thermal budget. Thus, we can retain the original high-quality SiGe MOS interface even with a high-k gate dielectric such as Al_2O_3 or HfO_2, enabling EOT scaling. Moreover, a reduction in the propagation loss is expected by replacing poly-Si with crystalline Si. The phase modulation efficiency is almost same as shown in [12] despite the upside-down layer structures with each other.

To realize the proposed modulator structure in Fig. 10(a), void-free wafer bonding with a thin high-k dielectric bonding interface is essential. Generally speaking, a thin bonding interface causes void generation due to out-gassing from the bonding interface. We have used Al_2O_3 deposited by ALD as a bonding interface because we can achieve strong wafer bonding even without typical O_2 plasma irradiation [23]. However, we found that the ALD Al_2O_3 tends to generate voids after high-temperature annealing. To suppress void generation, we examined a high-k dielectric bonding interface consisting of ALD Al_2O_3 and HfO_2 [22]. Although strong wafer bonding cannot be obtained using HfO_2 itself, we found that the incorporation of HfO_2 in Al_2O_3 suppresses void generation. Fig. 10(b) shows the relationship between the void density on the bonded wafer and the total Al_2O_3 thickness in the case of a 2-nm-thick HfO_2 layer. The number of voids was counted after 700 °C annealing for 20 min. When the total Al_2O_3 thickness at the bonding interface was 5 nm, we observed a void density of more than 10^6 cm^{-2}. However, the void density linearly decreased as the Al_2O_3 thickness decreased. When the Al_2O_3 thickness was reduced to 1 nm, which was found to be the minimum thickness for which wafer bonding could be achieved, the void density was on the order of 10^3 cm^{-2}. As shown by the microscopic image of the wafer in the inset of Fig. 10(b), the 1-nm Al_2O_3/2-nm HfO_2 bonding interface enabled a nearly void-free surface even after 700 °C annealing. Using the Al_2O_3/HfO_2 bonding interface, we can fabricate the SiGe optical modulator shown in Fig. 10(a) with a low EOT. Note that this bonding method allows us to introduce various semiconductor layers on a Si waveguide. We have predicted that a III-V/Si hybrid MOS will be an ideal structure for phase modulation [24].

III. Ge Photonics

Since Ge has a direct bandgap of around 0.8 eV, Ge photonic devices including PDs [1], modulators [25], [26], and LDs [27] have been intensively investigated for optical interconnections at near-infrared wavelengths. Moreover, Ge is transparent in the entire mid-infrared range, making it suitable for PICs operating at mid-infrared wavelengths [28]. In addition to low-dark-current Ge PDs, we have developed a mid-infrared integrated photonics platform on a Ge-on-insulator (GeOI) wafer.

A. Low-Dark-Current Ge PDs

At the early stage of investigation of Ge PDs monolithically integrated on Si photonics platform, the large variability in the dark current was one of the technological issues. There are two major physical origins of dark current in Ge PDs as shown in Fig. 11. Since a commercially available SOI wafer basically has a p-type Si layer, an n^+-Ge layer is formed on the top of a Ge

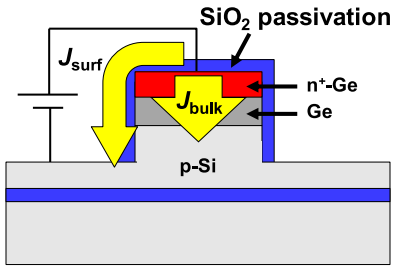

Fig. 11. Physical origins of dark current in a Ge PD: junction bulk leakage ($J_{\rm bulk}$) and surface leakage current ($J_{\rm surf}$).

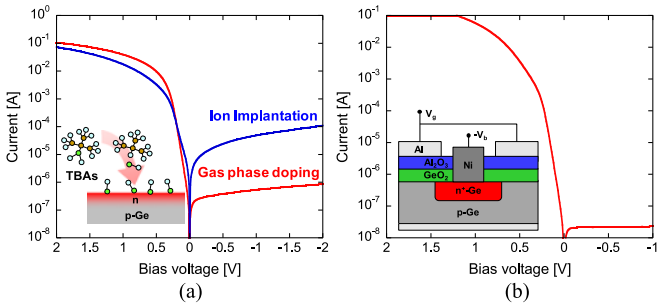

Fig. 12. (a) I-V curves of Ge PN junction formed by gas-phase doping and ion implantation. The inset is a schematic of gas-phase doping. (b) I-V curve of Ge PN junction with GeO_2 surface passivation and gas-phase-doped junction [30], [31].

mesa by ion implantation to fabricate a PIN junction. However, the rapid diffusion of implanted P or As atoms in Ge during activation annealing prevents the annihilation of crystal defects induced by ion implantation [29], which causes a significant junction bulk leakage current $(J_{\rm bulk})$. Surface passivation is also important for suppressing the surface leakage current $(J_{\rm surf})$. Conventional SiO_2 passivation is ineffective for Ge surfaces, resulting in a large surface leakage current.

To avoid the ion implantation of P or As into Ge, we have investigated gas-phase doping based on tertiary butyl arsine (TBAs) [30] as shown in the inset of Fig. 12(a). The gas-phase doping is carried out by injecting TBAs with H_2 carrier gas into a heated reactor. Since As atoms that decompose from TBAs diffuse into a Ge wafer, an n^+-Ge region can be formed with no crystal damage. Fig. 12(a) shows a comparison of the I-V curves of Ge PN junctions formed by gas-phase doping at 600 °C for 60 min and ion implantation [31]. From secondary ion mass spectroscopy (SIMS), the doping depth was found to be approximately 300 nm, indicating a significantly smaller diffusion constant than that of implanted As atoms. The implanted P atoms were activated at 600 °C for 10 s, which was found to be the optimal condition for minimizing the off-leakage current. The off-leakage current was two orders of magnitude smaller in the gas-phase-doped device than in the implanted device, which was attributed to the small junction bulk leakage current in the gas-phase-doped junction.

The impact of surface passivation on the dark current in Ge PDs was also investigated. Since we found that the high-temperature oxidation of Ge forms a high-quality GeO_2/Ge interface [32], a GeO_2-passivated Ge PD with a gas-phase-doped

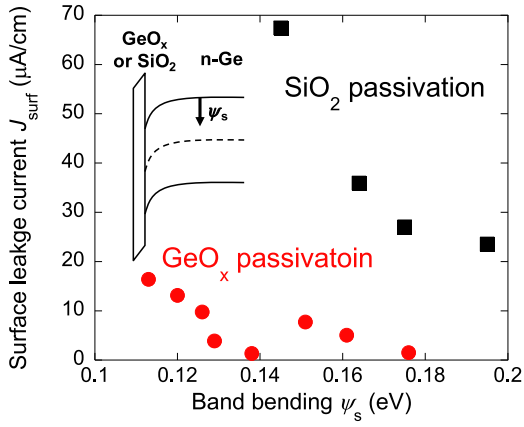

Fig. 13. Surface leakage current in Schottky junction formed on an n-Ge substrate with GeO_x passivation or SiO_2 passivation as a function of band bending at the Ge surface [33].

n^+/p junction was fabricated as shown in the inset of Fig. 12(b). In conjunction with gas-phase doping, the GeO_2-passivated Ge PD exhibited an extremely small leakage current density as shown in Fig. 12(b). By numerical fitting of the I-V curves for samples with various junction areas, $J_{\rm bulk}$ and $J_{\rm surf}$ were found to be 0.032 mA/cm^2 and 0.27 μA/cm, respectively, which are at least one order of magnitude lower than other previously reported values.

We also examined the impact of the surface potential of the Ge on the surface leakage current [33]. Fixed charges in a passivation layer modify the surface potential of a Ge, which changes the surface leakage, even with a low interface trap density on the Ge interface. Fig. 13 shows the surface leakage current in a Schottky junction formed on an n-Ge substrate with GeO_x passivation or SiO_2 passivation as a function of band bending at the Ge surface. Since Al_2O_3 and SiO_2 contain fixed charges, we can tune the band bending by changing the thicknesses of the Al_2O_3 and SiO_2 layers on the top of the sample. In this experiment, the GeO_x layer was formed by O_2 plasma irradiation through a thin Al_2O_3 capping layer [34], enabling excellent surface passivation comparable to that obtained by high-temperature oxidation. Since plasma oxidation performed at a low temperature generated Ge suboxides, the stoichiometry x of the GeO_x layer was below 2. As shown in Fig. 13, the GeO_x-passivated devices exhibited a lower surface leakage current than the SiO_2-passivated device because of the low interface trap density on the GeO_x-passivated surface. When the band bending was increased to promote accumulation on the Ge surface, the surface leakage tended to decrease regardless of the passivation layer, which was attributed to the suppression of the carrier generation process. Since the surface leakage current may dominate the dark current in a waveguide Ge PD, low-dark-current operation can be achieved by GeO_x passivation with an appropriate number of fixed charges in the capping layer.

B. Ge CMOS Photonics for Mid-Infrared Wavelengths

The transparency of Ge at mid-infrared wavelengths from 2 to 14 μm makes Ge an attractive material for mid-infrared

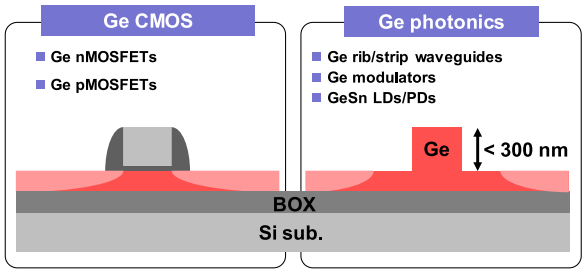

Fig. 14. Schematic of Ge CMOS photonics platform [35].

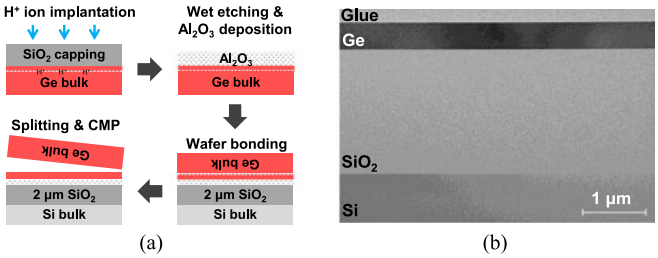

Fig. 15. (a) Fabrication procedure and (b) cross-sectional TEM image of wafer-bonded GeOI wafer [35], [36].

integrated photonics. To realize Ge-based PICs for the mid-infrared region, we have proposed the Ge CMOS photonics platform shown in Fig. 14 [35]. Similarly to the SOI wafer for Si photonics, a GeOI wafer enables Ge rib and slot waveguides, which are suitable for large-scale photonic integration owing to their strong optical confinement. We expect the monolithic integration of Ge-based optical modulators, GeSn LDs, and GeSn PDs with Ge passive waveguides. Moreover, Ge CMOS circuits can be co-integrated on a GeOI wafer, outperforming Si CMOS owing to the high electron and hole mobilities in Ge.

To demonstrate the Ge CMOS photonics platform, a high-quality GeOI wafer with a thick BOX layer is essential. Thus, we prepared a GeOI wafer by the direct wafer bonding of a Ge bulk wafer on SiO_2/Si wafer [36]. The fabrication procedure of the GeOI wafer is shown in Fig. 15(a). First hydrogen ions were implanted in the Ge bulk wafer to generate voids. After wafer bonding with an Al_2O_3 bonding interfacial layer, the Ge wafer was split by annealing. Finally, the planarization of the Ge surface was performed by chemical mechanical polishing (CMP). The cross-sectional TEM image of the GeOI wafer shown in Fig. 15(b) exhibits a uniform 400-nm-thick Ge layer on a 2000-nm-thick BOX layer. Additional annealing at 500 °C was carried out to improve the Ge film quality. We confirmed that the Hall mobility and residual carrier density in the Ge film after the annealing were close to those in the original Ge bulk wafer.

We confirmed the transmission of Ge rib waveguides fabricated on the GeOI wafer at a $2-\mu$m wavelength owing to the transparency of Ge [37]. We also measured the bend loss of the waveguide shown in the inset of Fig. 16. The strong optical confinement in the Ge waveguide on the GeOI wafer resulted in negligible bend loss even with a bend radius of 5 μm as shown in Fig. 16.

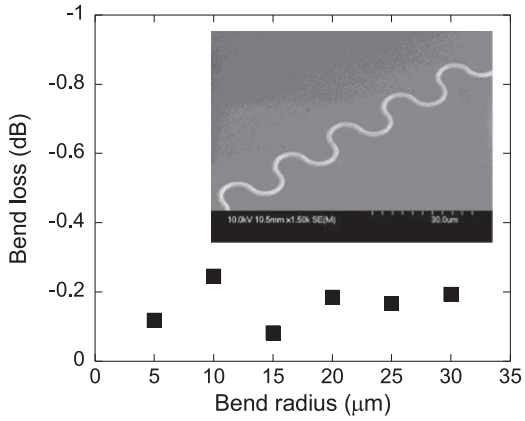

Fig. 16. Bend loss of Ge rib waveguide on GeOI wafer as a function of bend radius [37].

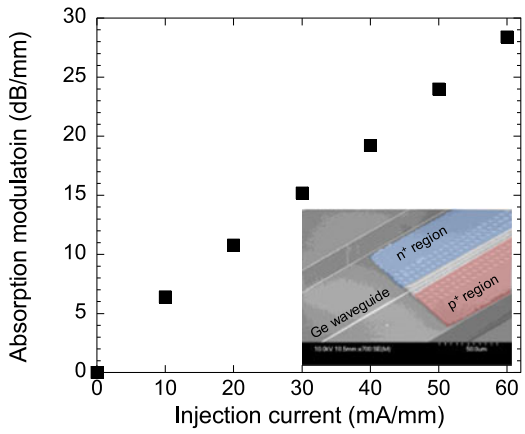

Fig. 17. Absorption modulation in carrier-injection Ge optical modulator based on free-carrier absorption [37].

Intensity modulation in the Ge waveguide at a $2-\mu$m wavelength was also investigated. It was predicted that Ge would exhibit more than 10 times greater free-carrier absorption than Si in the wavelength range of $2-3\,\mu$m [38]. Thus, we consider that a carrier-injection Ge optical modulator for mid-infrared wavelengths is promising. We examined the free-carrier absorption in the Ge waveguide by fabricating a lateral PIN junction along the waveguide as shown in the inset of Fig. 17 [37]. The PIN junction was formed by the ion implantation of B and P. As shown in Fig. 17, the modulation of absorption by carrier injection was successfully demonstrated.

Currently we use an SiO_2 BOX which prevent us from using a wavelength longer than 4 μm because of the SiO_2 absorption. To avoid the SiO_2 absorption, we may use a suspended Ge membrane by eliminating the SiO_2 BOX underneath the Ge waveguide.

IV. III-V CMOS Photonics

InP-based PICs fabricated on an InP wafer have mainly been developed for optical fiber communication because of their active/passive integration capability. However, the poor optical confinement due to the low index contrast in InP waveguides is obstacle to large-scale integration in contrast to Si photonics. To

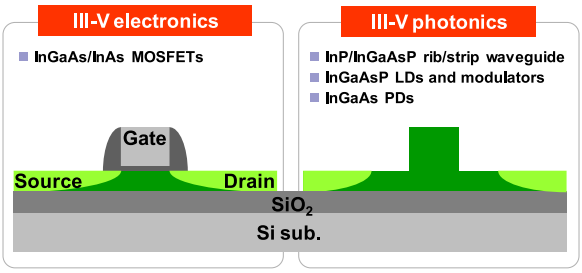

Fig. 18. Schematic of III-V CMOS photonics platform [39], [40].

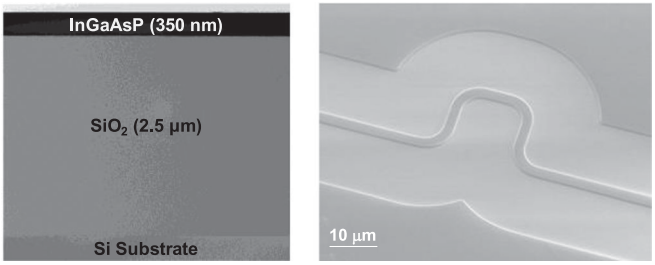

Fig. 19. (a) cross-sectional TEM image of III-V-OI wafer and (b) SEM image of InGaAsP rib waveguide on III-V-OI wafer [42], [44].

overcome this inherent drawback of the conventional InP PIC platform, we have proposed the III-V CMOS photonics platform shown in Fig. 18 [39], [40]. A III-V-OI wafer allows the fabrication of InP-based rib and strip waveguides with a large index contrast, enabling the large-scale integration of ultra-small active and passive components. Moreover, high-electron-mobility InGaAs or InAs MOS transistors, which outperform Si MOS transistors, can be monolithically integrated on the same III-V-OI wafer [41]. Hence, the III-V CMOS photonics offers a high-performance EPIC platform.

A. Preparation of CMOS-Compatible III-V-OI Wafer

To demonstrate various active and passive III-V photonic devices on the III-V CMOS photonics platform, a III-V-OI wafer, which can be processed by CMOS-compatible processes, is essential. For this purpose, the direct wafer bonding of an InP wafer and an SiO_2/Si wafer was performed [42]. First, we grew an InGaAsP layer with an InGaAs etch-stop layer on an InP wafer. After depositing a 2.5-nm-thick Al_2O_3 layer by ALD on the InP wafer and an SiO_2/Si wafer, the wafers were bonded to each other. The Al_2O_3 bonding interface provided us with strong bonding without O_2 plasma irradiation, resulting in low-damage bonding [43]. The Al_2O_3 layer simultaneously well passivated the InP surface. Finally, the InP substrate was removed selectively by wet etching. Fig. 19(a) is a cross-sectional TEM image of the III-V-OI wafer. A 350-nm-thick InGaAsP layer was bonded on a 2.5 $-$ μm-thick SiO_2 BOX layer. Using the III-V-OI wafer, passive waveguide components including sharp bends [42], arrayed waveguide gratings [42], and grating couplers [44] have been demonstrated as shown in Fig. 19(b).

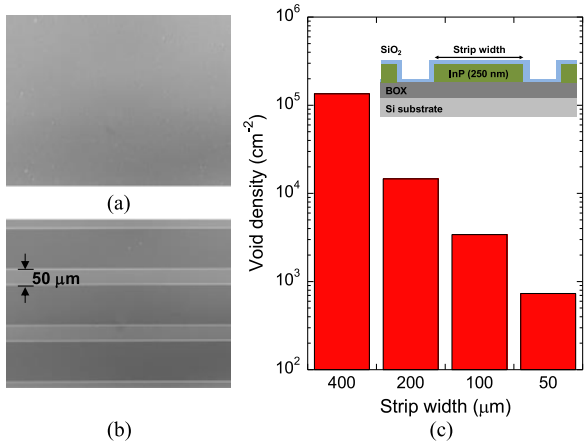

Fig. 20. Surface images of III-V-OI wafers with (a) no pattern and (b) 50-μm-wide stripes after 600 °C annealing. (c) Void density as a function of width of InP-OI strip.

To integrate active waveguide components on a III-V-OI wafer, which generally require a high thermal budget, the suppression of void generation on the wafer during high-temperature annealing is important. The thick SiO_2 BOX layer underneath the bonding interface contributes to absorption of the outgassed materials, helping us to suppress void generation. However, void generation may be affected by the amount of surface contaminants, making the BOX effect unstable. Sometimes we observed significant void generation on a III-V-OI wafer annealed at a temperature of more than 600 °C. On the III-V/Si hybrid platform, the outgassing via was examined with the aim of reducing the void generation from the bonded interface [45]. We also examined the impact of patterning a III-V-OI layer on void generation. We prepared a 250-nm-thick InP-OI wafer by wafer bonding. Then, the InP layer was patterned into strips with various widths as shown in the inset of Fig. 20(c). When an InP-OI wafer with no pattern was annealed at 600 °C, we observed many voids on the wafer, as shown in Fig. 20(a), and the void density counted from the plan-view photo of the sample was approximately 10^5 cm^{-2}. When an InP-OI wafer was patterned with 50 $-$ μm-wide strips, void generation was significantly suppressed as shown in Fig. 20(b). Fig. 20(c) shows the void density as a function of the strip width. As the strip width decreased, the void density was reduced to less than 10^3 cm^{-2}. Thus, a patterned III-V-OI wafer is effective for suppressing void generation. The impact of the generated gasses such as H_2 or H_2O on the III-V interface is not clear yet, which is important for future studies.

For the flexible placement of active and passive components on a III-V-OI wafer, quantum well intermixing (QWI) for a thin III-V layer containing multiple quantum wells (MQWs) was examined. To perform QWI on a III-V-OI wafer, the total thickness of the III-V layer should be less than a few hundred nm to avoid thermal-stress-induced degradation in the III-V layer. Thus, we grow an MQW layer with eight 6.5-nm-thick $In_{0.735}Ga_{0.265}As_{0.835}P_{0.165}$ quantum wells and seven 8-nm-thick $In_{0.735}Ga_{0.265}As_{0.513}P_{0.487}$ barriers sandwiched by 25-nm-thick barrier layers, and a 25-nm-thick InP top cladding

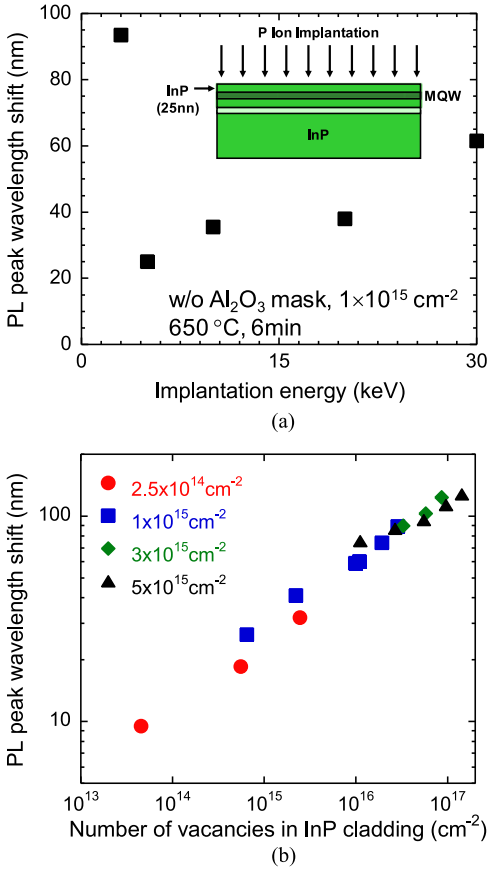

Fig. 21. (a) PL peak wavelength shift as a function of implantation energy and (b) PL peak shift as a function of number of vacancies generated in 25-nm-thick InP cladding.

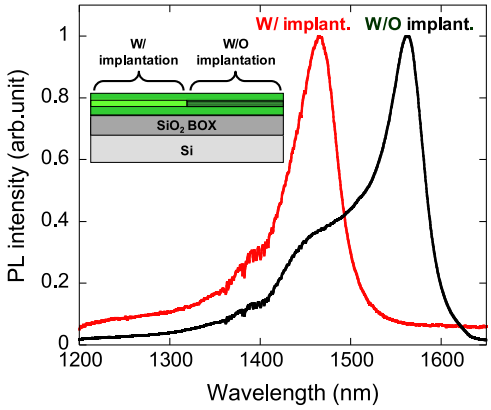

Fig. 22. PL spectra from the regions of a III-V-OI wafer with and without implantation.

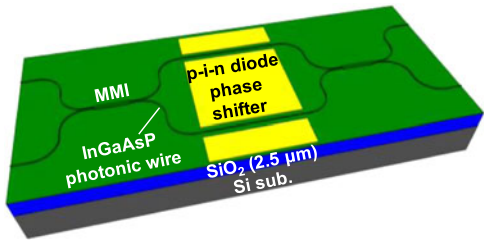

Fig. 23. Schematic of a 2 × 2 InGaAsP photonic-wire optical switch.

layer on an InP wafer by metal-organic vapor phase epitaxy (MOVPE). First, we examined the effect of P ion implantation on the photoluminescence (PL) peak shift after QWI. P ions were implanted with a dose of 1×10^{15} cm^{-2} into samples with an implantation energy of 3 keV, 5 keV, 10 keV, 20 keV, or 30 keV. Rapid thermal annealing (RTA) was carried out at 650 °C for 6 min to induce QWI after a 10-nm-thick Al_2O_3 layer was deposited. Fig. 21(a) shows the PL peak shift as a function of implantation energy. As the implantation energy increased toward 30 keV, the PL shift gradually increased to 62 nm. On the other hand, when the implantation energy was 3 keV, the PL shift markedly increased to 94 nm. We found by numerical simulation that almost all the vacancies were in the 25-nm-thick InP top cladding layer only when the implantation energy was 3 keV. This suggests that to promote QWI, it is important to generate vacancies only in the InP top cladding layer. To investigate this phenomenon further, P ion implantation was carried out with thickness of the Al_2O_3 mask varied from 1 to 10 nm and the implantation energy varied from 3 to 20 keV to control the number of vacancies. Fig. 21(b) shows the relationship between the PL peak shift and the density of vacancies in the InP top cladding layer for each sample. It was found that the PL shift is proportional to the number of vacancies in the InP upper cladding layer regardless of the Al_2O_3 thickness. We concluded that QWI can be promoted by forming vacancies only in the InP top cladding layer through ion implantation and that the PL shift can be controlled precisely by adjusting the implantation conditions.

Using the optimized QWI condition, we fabricated a multiple-bandgap III-V-OI wafer. P ion implantation was carried out in an MQW wafer at an energy of 3 keV with a dose of 3×10^{15} cm^{-2} after the deposition of a 3-nm-thick Al_2O_3 layer and patterning. QWI was then carried out at 650 °C for 30 min. Then, the MQW wafer was bonded on a thermally oxidized Si wafer. Fig. 22 shows the PL spectra obtained from the regions of the fabricated multiple-bandgap III-V-OI wafer without and with ion implantation. The PL peak was at 1561 nm in the region without ion implantation and at 1466 nm in the region with ion implantation. We achieved a similar PL peak shift of approximately 100 nm by applying QWI directly to a III-V-OI wafer [46]. We can selectively perform QWI on the III-V-OI wafer by selective implantation with a photoresist mask, enabling active/passive integration on the III-V-OI wafer. Since we used the implantation-enhanced interdiffusion method for QWI, the free-carrier absorption might not be dominant. However, the evaluation of propagation loss in passive waveguide is important for future studies.

B. Optical Switch and Variable Optical Attenuator

A lateral PIN junction is a fundamental device structure for integrating active components on a III-V-OI wafer. Owing to the strong optical confinement, low-threshold-current LDs with lateral PIN junctions have been demonstrated [47], [48]. We have also investigated a carrier-injection InGaAsP Mach-Zehnder interferometer (MZI) optical switch on the III-V CMOS photonics platform [43] as shown in Fig. 23. One of the most important

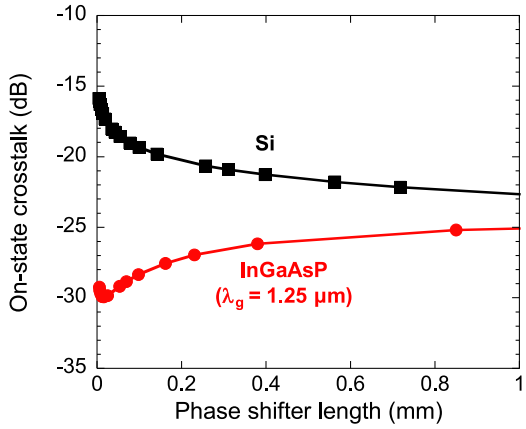

Fig. 24. Phase-shifter-length dependence of the on-state crosstalk in InGaAsP and Si MZI optical switches.

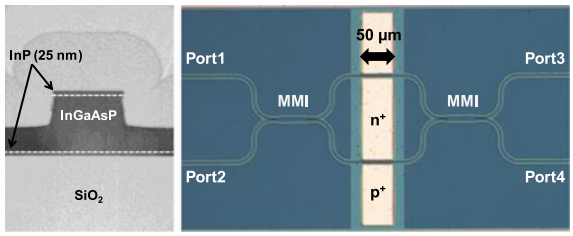

Fig. 25. (a) Cross-sectional TEM image of InGaAsP rib waveguide on III-V-OI wafer and (b) plan-view photograph of an InGaAsP photonic-wire switch.

advantages of the InGaAsP switch is its low on-state crosstalk. Since carrier-induced absorption is unavoidable upon carrier-induced refractive index modulation, the on-state crosstalk in the Si switch degrades when the length of the phase shifter decreases, as shown in Fig. 24. On the other hand, the carrier-induced refractive index modulation in InGaAsP is significantly greater than that in Si. As a result, the on-state crosstalk in an InGaAsP switch is superior to that in a Si switch. In particular, the low on-state crosstalk with a short phase shifter makes an InGaAsP switch attractive for large-scale integration.

We fabricated a 2×2 InGaAsP optical switch on a III-V-OI wafer containing a 350-nm-thick InGaAsP layer ($\lambda_g = 1.25\,\mu$m) sandwiched by 25-nm-thick InP layers. An InGaAsP rib waveguide was then formed by dry etching as shown in Fig. 25(a). Lateral PIN junctions were also formed by ion implantation. Si and Be were implanted at acceleration energies of 15 keV and 10 keV with doses of Si and Be of $2 \times 10^{14}\,\mathrm{cm}^{-2}$ and $1 \times 10^{15}\,\mathrm{cm}^{-2}$, respectively. Activation annealing was then carried out at 600°C for 10 s. Finally, Pt electrodes were formed by sputtering and a lift-off process. A plan-view photograph of the InGaAsP MZI optical switch with a $50-\mu$m-long phase shifter is shown in Fig. 25(b). Fig. 26 shows the static 2×2 switching characteristics of the InGaAsP MZI optical switch at a 1.55 μm wavelength. When the input signal was injected to port 1, the cross output from port 4 was successfully switched by a driving current of approximately 7 mA. In this case, we achieved on-state crosstalk of approximately -28 dB, which is approximately 10 dB lower than the theoretical limit of the Si MZI switch. A similar cross-switching characteristic was ob-

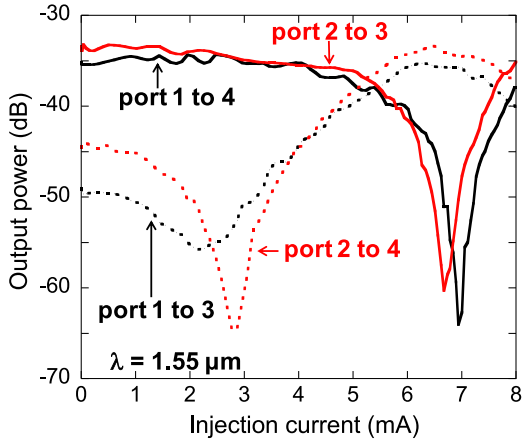

Fig. 26. Static characteristics of a 2×2 optical switch with a 50-μm-long phase shifter.

tained in the case of switching from port 2 to port 3. The bar-switching characteristics from port 1 to port 3 and from port 2 to port 4 exhibited similar on-state crosstalk. We observed the initial phase error between the two MZI arms, which resulted in the drift of the off state in the bar switching. Although the phase error makes it difficult to evaluate the switching current, the switching current seems a few mA, comparable to that in Si devices. Since the electron-induced refractive index in InGaAsP is much greater than in Si, we expect the switching efficiency can be improved by optimizing the formation process of the lateral PIN junction. This phase error can be tuned by implementing an additional phase-tuning section.

We also examined a carrier-injection InGaAsP variable optical attenuator [49]. To achieve large carrier injection through a lateral PIN junction, we introduced Zn diffusion from a spin-on glass and a Ni-InGaAsP alloy to form p^+- and n^+-regions, respectively [50]. Zn diffusion is superior to Be implantation in terms of hole activation, resulting in a low-resistivity p^+-InGaAsP region. We also found that Ni deposited on InGaAsP forms a Ni-InGaAsP alloy upon 350 °C annealing. The Ni-InGaAsP alloy exhibits approximately ten times lower sheet resistance than Si-implanted InGaAsP. Since the Schottky barrier height between the Ni-InGaAsP alloy and n-InGaAsP is as low as 0.3 eV, the Ni-InGaAsP acts in the same way as n^+-InGaAsP in terms of carrier injection. We formed Zn-diffused p+-InGaAsP and Ni-InGaAsP regions along an InGaAsP ($\lambda_g = 1.41\,\mu$m) waveguide for carrier injection as shown in the inset of Fig. 27. Fig. 27 shows the absorption modulation characteristic as a function of injection current measured at a 1.55 μm wavelength. We observed 45 dB/mm absorption modulation upon 40 mA/mm current injection, which was mainly attributable to intervalence-band absorption. The kink in the absorption modulation property may be due to defects induced at the edge of the Ni-InGaAs alloy, although further investigation is required.

C. *Waveguide InGaAs PD*

An InGaAs waveguide PD [51], [52] monolithically integrated with an InP strip waveguide on a III-V-OI wafer was investigated [53]. To couple an input light signal, we also inte-

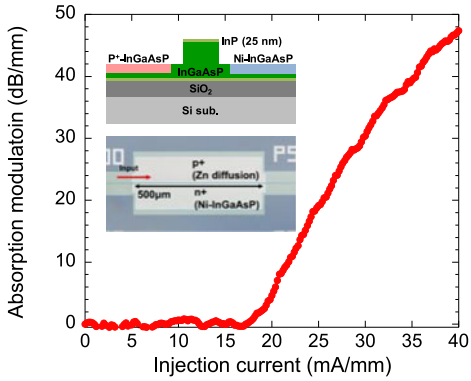

Fig. 27. Absorption modulation in InGaAsP variable optical attenuator [49].

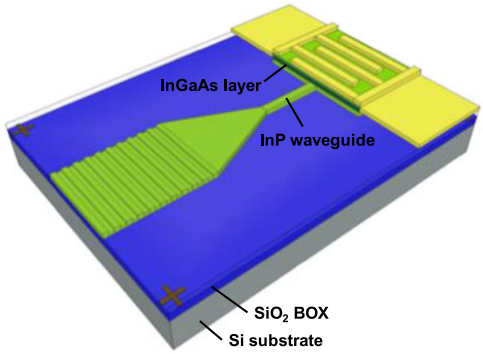

Fig. 28. Waveguide InGaAs PD monolithically integrated with an InP strip waveguide and grating coupler [53].

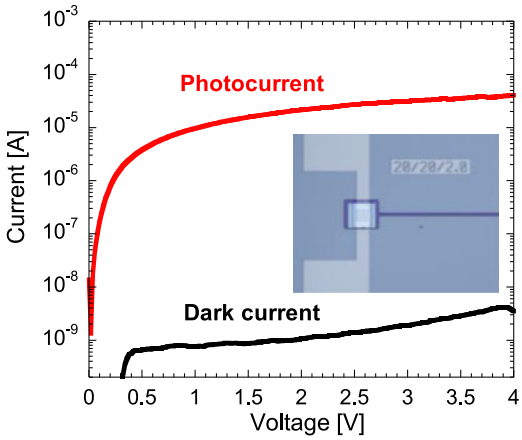

Fig. 29. Dark current and photocurrent of waveguide InGaAs PD [53].

grated an InP grating coupler as shown in Fig. 28. An InGaAs absorbing layer was formed on the InP waveguide layer to achieve evanescent coupling from the InP waveguide. An interdigitated Ni electrode was used to form a metal-semiconductor-metal (MSM) configuration to detect optical signals. To suppress the dark current, an InP/InAlAs layer was inserted between the InGaAs layer and Ni electrode as a Schottky barrier enhancement (SBE) layer. The dark current of the waveguide InGaAs MSM PD is shown in Fig. 29. Owing to the SBE layer, we obtained a dark current of less than 1 nA at a 1V bias voltage. The photocurrent was measured by injecting a 0-dBm optical signal at a 1.55 μm wavelength. By taking into account the coupling efficiency of the grating coupler, we estimated the intrinsic responsivity to be approximately 0.2 A/W. Since the responsivity can be improved by introducing a graded SBE layer, its wide operating wavelength range up to 1640 nm and low dark current operation make the InGaAs PD more attractive.

V. Conclusion

We have presented the heterogeneous integration of SiGe, Ge, and III-V semiconductors on Si for CMOS photonics. Since SiGe is a CMOS-compatible material, there is no fundamental difficulty to fabricate the presented SiGe optical modulator in standard CMOS fab. We expect that the SiGe optical modulator can be widely used for many applications. Although the introduction of III-V-OI devise into CMOS fab takes time with additional cost, the high-performance III-V-OI devices will be suitable for high-end applications. Mid-infrared photonic integrated circuits based on the Ge CMOS photonics is expected to be very useful for emerging sensing applications, opening up a new market for Si photonics technology. Therefore, CMOS photonics based on the heterogeneous integration of SiGe, Ge, and III-V semiconductors on Si provides many opportunities to extend the functionalities of Si photonics.

Acknowledgment

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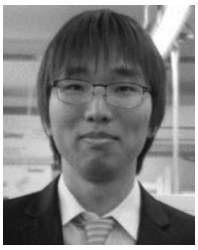

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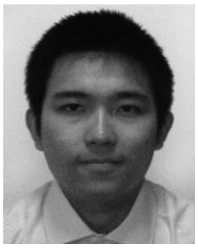

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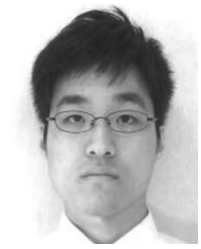

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