A Novel Approach to Photonic Packaging Leveraging Existing High-Throughput Microelectronic Facilities

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Abstract—**Silicon photonics leverages microelectronic fabrication facilities to achieve photonic circuits of unprecedented complexity and cost efficiency. This efficiency does not yet translate to optical packaging, however, which has not evolved substantially from legacy devices. To reach the potential of silicon photonics, we argue that disruptive advances in the packaging cost, scalability in the optical port count, and scalability in the manufacturing volume are required. To attain these, we establish a novel photonic packaging direction based on leveraging existing microelectronics packaging facilities. We demonstrate two approaches to fiber-to-chip interfacing and one to hybrid photonic integration involving direct flip-chip assembly of photonic dies. Self-alignment is used throughout to compensate for insufficient placement accuracy of high-throughput pick and place tools. We show a self-aligned peak transmission of −1.3 dB from standard cleaved fibers to chip and of −1.1 dB from chip to chip. The demonstrated approaches are meant to be universal by simultaneously allowing wide spectral bandwidth for coarse wavelength division multiplexing and large optical-port count.**

Index Terms—**Integrated optoelectronics, optical fiber communication, packaging, optical polymers, flip-chip devices.**

I. INTRODUCTION

O PTICAL devices employed in fiber optical communication have had a notable impact by enabling an increasingly connected world. However, their cost has been a barrier
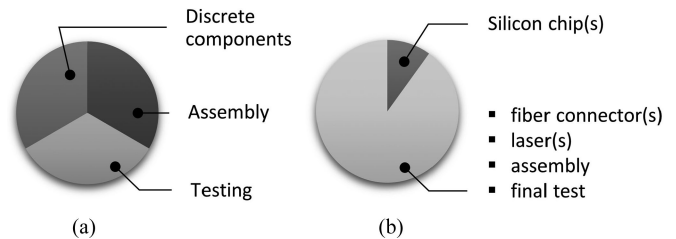
Fig. 1. Schematic representation of the cost structure of (a) legacy optical devices and (b) silicon photonic devices. The total cost of silicon photonic devices is substantially lower than of legacy devices and is dominated by anything but the Si chips. To fulfill the potential of Si photonics, disruptive improvements in cost and scalability of its packaging are required.

to their use in a wider spread of applications. Cost is more than a commercial concern as it can define the accessibility of a technology. The success of microelectronics is largely owned to its cost-efficiency in addition to its scalability in both circuit complexity and manufacturing volume. To seek these characteristics in photonic circuits, silicon photonics leverages existing microelectronics wafer facilities, with decades of microelectronics planar processing optimization, for photonic chip fabrication [1]–[3].

Silicon photonics has changed the cost structure of optical devices. As schematically shown in Fig. 1, the cost of legacy devices made of discrete components was roughly evenly distributed among components, assembly and the various stages of testing. Photonic integration, in general, reduces the number of components and hence the cost of their individual packaging, assembly and testing. Silicon photonics, in particular, brings higher yield and lower chip cost to photonic integration. Complex photonic circuits are effectively pre-assembled by lithography on chips that are fabricated at very low cost. Testing can be done on wafer scale with relieved requirements permitted by higher fabrication reliability. The result is the cost of a silicon photonic device being limited by anything but the complex silicon photonic circuit. Components or assembly steps that were of no substantial cost relevance before can be cost-limiting now.

To fulfill the potential of silicon photonics, we argue that disruptive improvements in photonic packaging cost, scalability in optical port count, and scalability in manufacturing volume are required. Photonic packaging has changed little from legacy optical devices with heavy reliance on manual assembly and active alignment. In this paper, we present an overview of a new direction in single-mode photonic packaging. To improve cost and scalability disruptively, we propose to leverage existing

TABLE I
100 Gb/s ETHERNET STANDARDS AND AGREEMENTS

Name	Number of wavelengths	Wavelength spacing	Number of fibers
LR4	4	4.5 nm	2
PSM4	1	N/A	8
CWDW4	4	20 nm	2
CLR4	4	20 nm	2

Detailed information can be found in [4]–[7].

TABLE II
A FEW 400 Gb/s ETHERNET PROPOSALS

Name	Number of wavelengths	Wavelength spacing	Number of fibers
LR8	8	4.5 nm	2
PSM4	1	N/A	8
4×100G	4	20 nm	2
8×50G	8	4.5 – 10 nm	2

Additional information and proposals are found in [8]–[9].

microelectronics packaging facilities for photonic assembly. This is analogous to silicon photonics already leveraging microelectronic wafer fabrication facilities to improve notably the cost and scalability of photonic circuit fabrication.

Enabling photonic packaging in existing microelectronics packaging facilities does not come without challenges. First, the placement uncertainty of high-throughput pick and place tools can be as large as +/– 10 μm, which is highly inadequate for single-mode photonics where even the large mode of a standard cleaved fiber requires an alignment to at least 1–2 μm for acceptable coupling efficiency. This first issue is addressed by mode engineering and self-alignment schemes. The aligned optical connections are taken at maximum mode delocalization to maximize alignment tolerances with self-alignment bridging the rest of the gap from the +/– 10 μm placement accuracy. Second, the handling capability of high-throughput pick-and-place tools is limited to what is generally required for microelectronic chip placement: vacuum picking with pressure sensitive movement in the vertical direction only. This second issue is addressed by modifying photonic components and customizing vacuum pick tips and chip holders. These customized elements are then introduced into standard high-throughput tools to enable them for photonic assembly.

We reduce photonic packaging to two key challenges: optical inputs and outputs (I/Os) on silicon photonic chips and hybrid photonic integration. Optical I/Os generally refer to optically connecting single-mode fibers to chips as fibers remain the optical wires of choice. The spectral bandwidth and number of connections required can be deduced from driving applications and standards in development [4]–[9]. The key characteristics of various 100 Gb/s ethernet (GE) standards and agreements are shown in Table I [4]–[7] with a few 400 GE proposals shown in Table II [8], [9]. For a universal approach, a bandwidth of at least 73 nm is required for compatibility with coarse wavelength division multiplexing [6], [7] and is generally defined at 1 dB penalty. A port count of up to 8 fibers is needed for core applica-
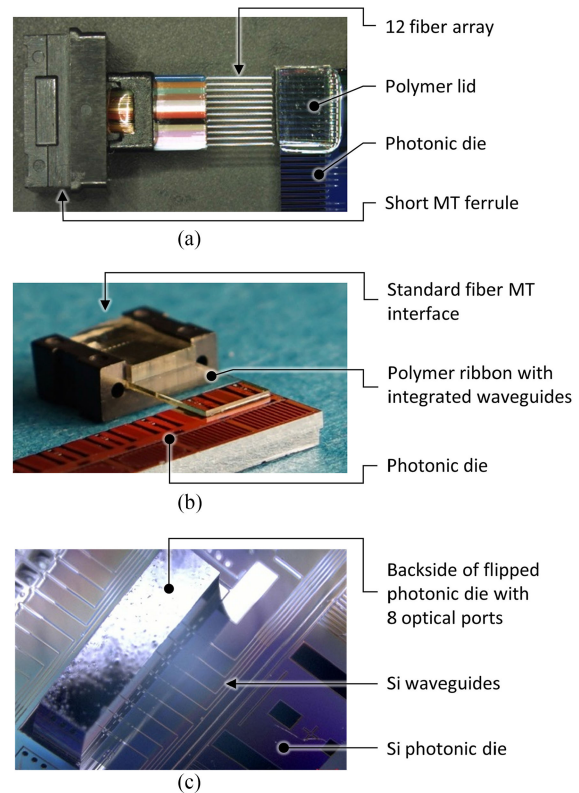

Fig. 2. Photonic packaging approaches compatible with existing high-throughput microelectronic packaging facilities. (a) Parallelized 12-fiber assembly to photonic chips. (b) Compliant polymer interface between standard 12-fiber connectors and photonic chips. (c) Self-aligned direct flip-chip bonding of photonic dies for hybrid photonic integration.

tions [5]. Emerging applications, such as communication hubs and on-chip fiber switches [10], can require port counts of up to tens of fibers per chip but port counts of hundreds of fibers per chip are not currently anticipated in volume applications.

Hybrid photonic integration is the assembly of multiple, optically connected, photonic chips. The most obvious example is integration of light sources with silicon photonic circuits. Other applications, such as hybrid integration of non-linear optical devices with silicon photonic circuits, can be foreseen as well. Hybrid integration is required for technologies that cannot be monolithically integrated and is desired for technologies that cannot be cost-efficiently, monolithically integrated. As illustrated in microelectronics, multi-chip configurations can be preferred even if technology permits full integration on one chip. For instance, integrating memory and logic on one microelectronic chip is possible but a multi-chip configuration is preferred and enabled by low-cost assembly of chips with gradually increasing intimacy to minimize the downside of the multi-chip configuration [11], such as lower memory interface bandwidth and higher memory interface power.

We demonstrate multiple photonic packaging approaches that are compatible with existing high-throughput microelectronics packaging facilities. These are shown in Fig. 2. We show two approaches to optical I/Os and one approach to hybrid photonic integration. Optical I/Os are addressed with parallelized fiber
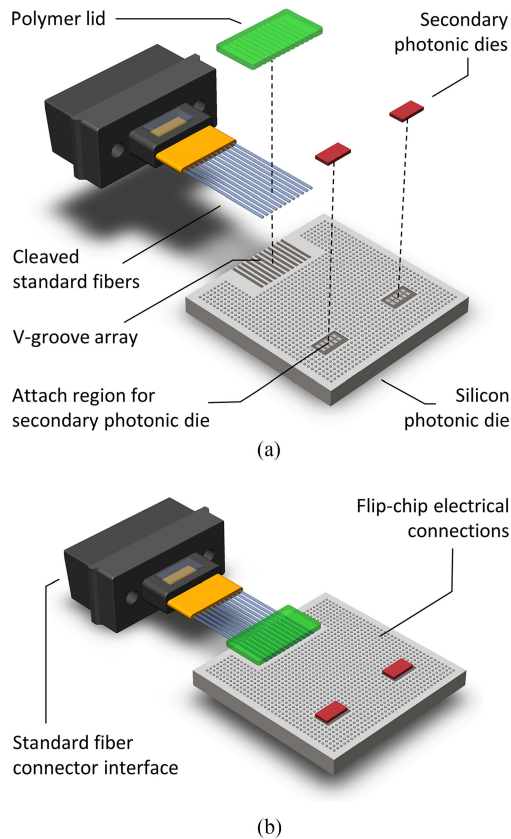
Fig. 3. Schematic representation of parallelized 12-fiber assembly to photonic chips combined with direct flip-chip bonding of secondary photonic dies, such as III-V light sources. An exploded view is shown in (a) and an assembled view is shown in (b). A fiber stub with cleaved fiber ends is assembled to a V-groove array integrated on chip with high-throughput pick-and-place tools. A polymer lid facilitates fiber handling.

assembly and the compliant polymer interface. Hybrid photonic integration is addressed with direct flip-chip bonding of photonic dies, which can be combined with any of the two approaches to optical I/Os. Self-alignment is used throughout with mode engineering to maximize alignment tolerances within typical manufacturing constraints. We report self-aligned coupling efficiencies reaching −1.3 dB from standard cleaved fiber to chip and −1.1 dB from chip to chip. All approaches shown here are universal as they enable both wide spectral bandwidth and large optical port count.

II. PARALLELIZED FIBER ASSEMBLY

A conceptual view of parallelized direct fiber assembly is presented in Fig. 3. A fiber stub, including a short mechanical transfer (MT) ferrule and a standard cleaved fiber ribbon, is assembled, with high-throughput pick-and-place tools, to a matching V-groove array integrated on the Si photonic chip. A polymer lid can be pre-assembled to the cleaved fiber ribbon to enable vacuum pick-tip handling of fibers, as required by high-throughput pick and place tools. The lid further ensures the fibers are positioned within the ~40 μm re-alignment range of the V-grooves on chip. Parallelized fiber assembly can be combined with direct flip-chip bonding of secondary
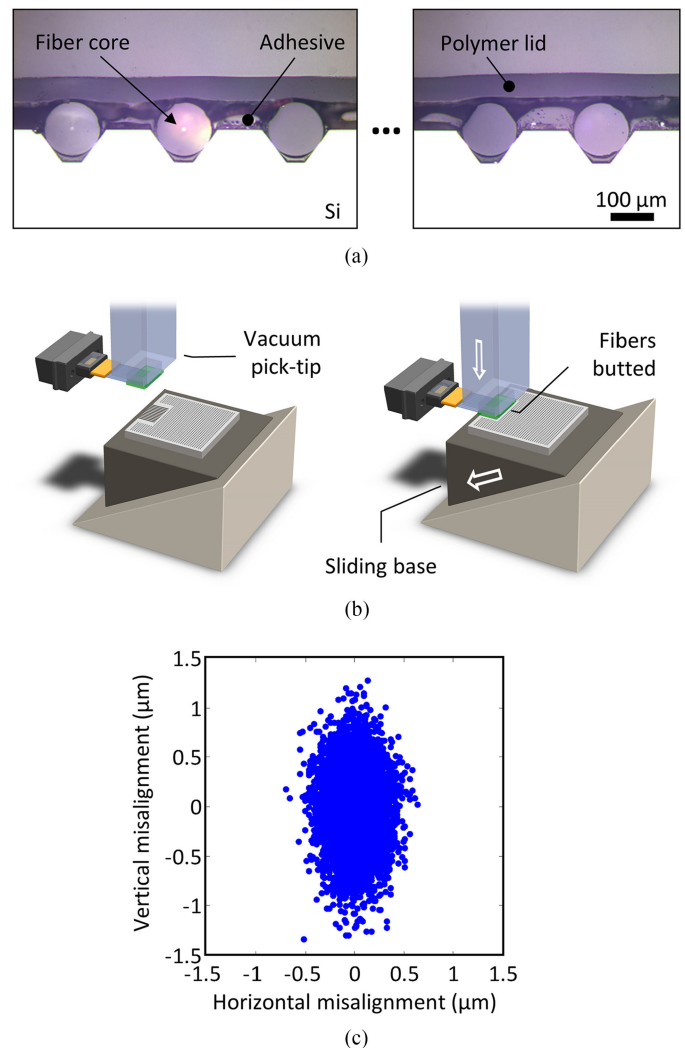

Fig. 4. Self-alignment in parallelized fiber assembly. (a) Cross-sectional optical micrograph across a 12-fiber ribbon assembled to a V-groove array integrated on the photonic chip. All fibers are properly seated warranting vertical and lateral alignment. (b) Schematic of the sliding base used for butting of fibers in high-throughput pick and place tools where a pressure sensing movement can be exerted in the vertical direction only. (c) Total fiber-core to waveguide coupler misalignment for 10 000 random error combinations. This Monte Carlo analysis demonstrates the manufacturability of fiber self-alignment with a 3σ misalignment below +/− 1.3 μm [12].

photonic dies to enable the integration of III-V light sources or other materials. Both the fiber and the secondary die assembly can be used with flip-chip electrical connections by providing required clearances through laminate cutouts. The examples shown here use 12-fiber arrays due to the popularity of 12-fiber connectors. However, an arbitrary number of fibers can be used as long as they are arranged in a one-dimensional array.

The V-groove array integrated on the Si photonic chip permits the vertical and lateral self-alignment of individual fibers to their corresponding waveguide couplers. A cross-sectional micrograph across an assembled 12-fiber ribbon is shown in Fig. 4(a). To achieve alignment in the third dimension, to butt fibers on waveguide couplers, handling limitations of high-throughput tools must be overcome. As mentioned above, these tools have

pressure sensitive movement capability in the vertical direction only. Insertion of fibers into grooves followed by fiber butting would require sequential pressure sensing movements in two directions. To overcome this limitation, we employ an angled-sliding base under the chip that transforms trigonometrically a portion of the vertical placing movement into a fiber butting force. As shown in Fig. 4(b), this achieves both V-groove placement and fiber butting in one vertical pressure-sensing motion.

Once the fibers are in adequate contact with the V-grooves, the resulting alignment between fiber core and waveguide coupler depends on the accuracy of the fiber and the V-groove. A Monte Carlo analysis of residual misalignment with 10 000 random fabrication error combinations is shown in Fig. 4(c). It includes typical fiber tolerances on diameter, core concentricity, and ellipticity as well as V-groove manufacturing tolerances on lithography, hardmask opening, and anisotropic etch chemistry. It demonstrates the manufacturability of fiber self-alignment with a 3σ residual misalignment below $+/-$ 1.3 μm. Such alignment is well suited to coupling of standard cleaved fibers with 9–10 μm mode diameter. However, a significant coupling penalty could be experienced with small mode fibers at this misalignment level, making V-groove self-alignment with small mode fibers problematic. As mentioned above, it is preferred to use the largest mode possible at the aligned connection and hence to go through the additional complexity of expanding the mode on chip to match a standard fiber. Additional details on the fiber assembly procedure and the Monte Carlo analysis can be found in [12].

For a universal approach, in plane coupling of fibers is preferred to achieve the wide spectral bandwidth required for compatibility with CWDM schemes. Despite recent enhancements [13], diffractive vertical couplers remain inherently limited in bandwidth with significant transmission penalty at two-polarization operation [14]. Our waveguide coupler is shown in Fig. 5. It is a metamaterial converter formed of a single silicon layer embedded in a suspended oxide membrane. Silicon posts, of period significantly below the diffraction edge, act as an engineered optical material to form a fiber coupler with greater mode shape control and fabrication tolerances than inversed tapers. The mode is first transformed by adiabatic non-linear tapering of the silicon posts. A butt-coupling junction is then used to move into a hybrid waveguide, which is adiabatically transformed into a standard silicon waveguide. The metamaterial is similar to a subwavelength grating [15] although we prefer the metamaterial terminology which implies index homogenization without diffraction while subwavelength gratings technically include mainstream diffractive devices such as Bragg gratings.

To enable appropriate mode matching between the fiber coupler and a 9–10 μm fiber mode, one must allow mode expansion beyond the standard 2–3 μm buried oxide thickness of silicon on insulator wafers. This is done by undercutting the silicon handle under the mode converter. This undercut is then filled with low-index adhesive at assembly. The resulting optical performance with self-alignment is presented on Fig. 6 for a metamaterial converter in the O-band [16]. We show a
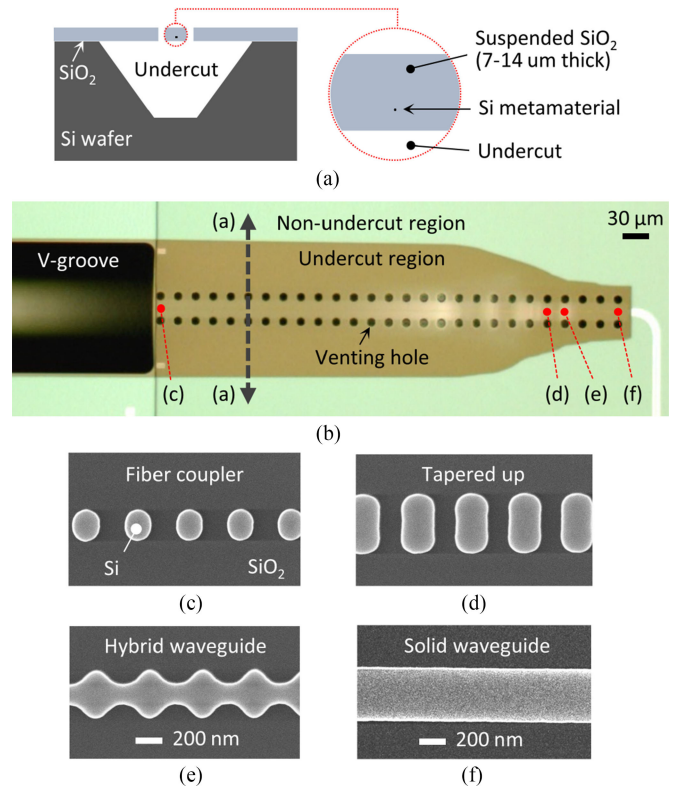

Fig. 5. Metamaterial waveguide converter interfacing a standard cleaved fiber to a common silicon wire waveguide. A top-view optical micrograph of an S-band converter is shown in (b) with the positions of the cross-sectional diagram of (a) and the top-view electron micrographs of (c)–(f). The fiber is inserted in the V-groove and butted on the fiber coupler, which is made of a single silicon layer embedded in a suspended oxide membrane. The substrate is undercut to enable sufficient mode expansion for efficient coupling to 9–10 μm fiber modes. The undercut is filled with low-index adhesive at fiber assembly. The metamaterial is similar to a subwavelength grating [15].
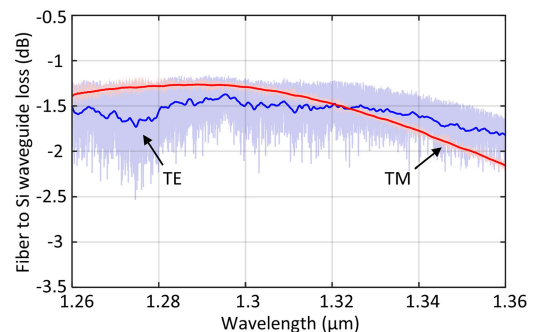
Fig. 6. Optical performance of an O-band metamaterial converter with fiber self-alignment in V-grooves. A peak transmission of −1.3 dB is seen with 0.8 dB penalty over a 100 nm bandwidth and all polarizations. Polarization-dependent Fabry–Perot fringes were filtered out for clarity and the resulting curve superimposed on raw data. They were attributed to a lithographic defect at the metamaterial to hybrid waveguide junction creating a reflection point. More information is found in [16].

−1.3 dB peak coupling efficiency to a standard cleaved fiber with 0.8 dB maximum penalty over a 100 nm bandwidth and all polarizations. This converter was fabricated in a microelectronic wafer foundry. The fibers were placed into the V-grooves manually with isopropanol employed as index matching fluid.

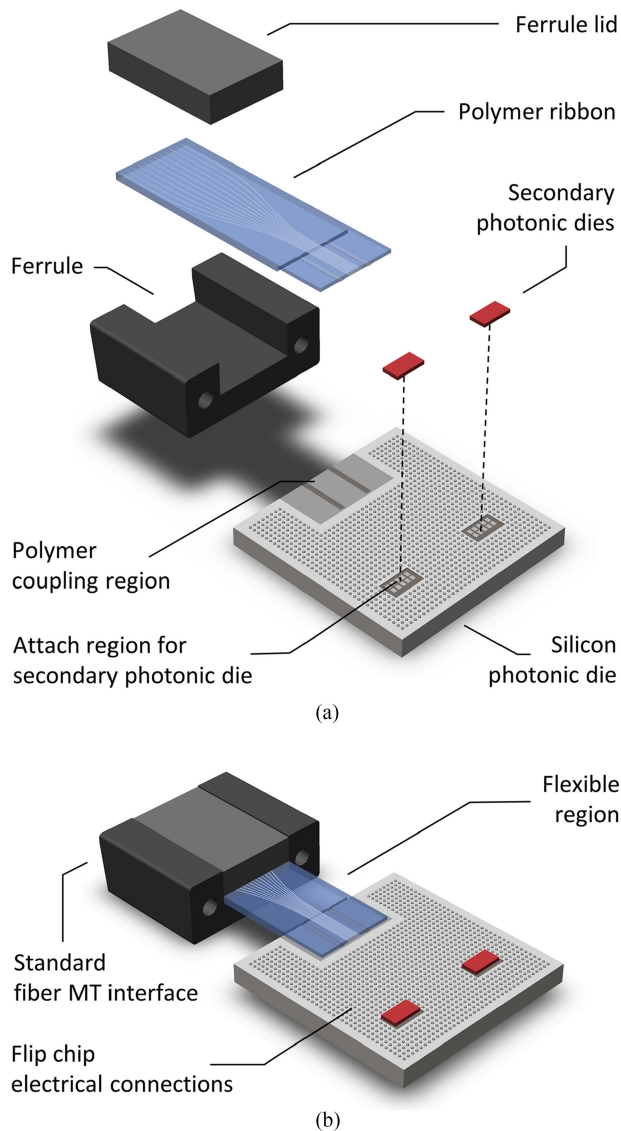Fig. 7. Schematic representation of the compliant polymer interface in (a) exploded view and (b) assembled view. A polymer ribbon with lithographically defined waveguides is assembled to a custom ferrule and enclosed with a ferrule lid. This sub-assembly is then picked and place onto a photonic die. The result is a standard fiber connector interface that can be combined with standard flip-chip electrical connections and direct flip-chip assembly of secondary photonic dies.
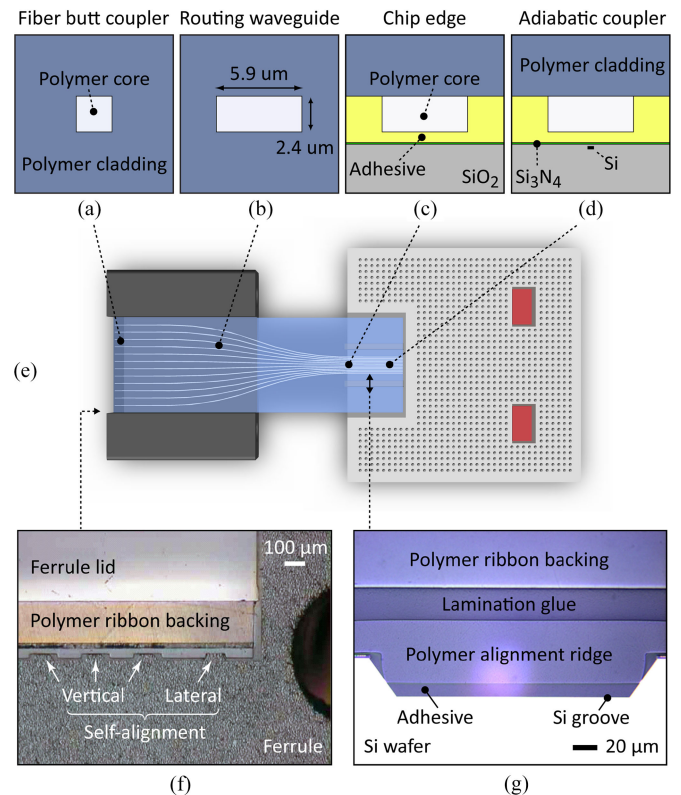

Fig. 8. The optical path through the compliant polymer interface is shown in the waveguide cross-sections of (a)–(d). Their location is shown in (e), which is a top-view with the ferrule lid removed for waveguide routing clarity. Standard fibers in an MT ferrule are butt-coupled to the polymer waveguides of (a), which are then adiabatically transformed into the routing waveguide of (b). An adiabatic crossing is used for transitioning from the polymer to a Si nanotaper, as shown in (d). Self-alignment structures at the ferrule-to-ribbon interface are shown in the optical micrograph of the polished ferrule facet of (f). Self-alignment structures at the ribbon-to-chip interface are shown in the cross-sectional optical micrograph of (g). The polymer ribbon backing of (f) and (g) is optional as described in [22].

Optical performance of metamaterial converters centered on the S-band is reported with manual and automated fiber assembly in [17].

III. COMPLIANT POLYMER INTERFACE

The mechanically compliant polymer interface employs lithographically defined optical waveguides on a polymer ribbon for fiber-to-silicon optical interfacing. The concept is shown in Fig. 7. A thin ribbon with lithographically defined waveguides is picked and placed onto a modified ferrule and enclosed with a ferrule lid for thermo-mechanical stability. This sub-assembly is then picked and placed onto a photonic die with matching optical and self-alignment interface. Both the ribbon to ferrule assembly and the ribbon to photonic die assembly are compatible with

high-throughput pick-and-place tools. As with parallelized fiber assembly, the result is a standard optical fiber interface attached to a photonic die with flip-chip electrical connections. A 12-fiber MT interface is shown here but other standards can be used as long as an arbitrary number of optical ports is disposed in a 1D array. The compliant polymer interface can be combined with direct flip-chip assembly of secondary photonic dies. One key difference with parallelized fiber assembly is the flexible region in the polymer interface providing mechanical decoupling between the fiber connector and the chip, which is expected to improve the package's thermo-mechanical reliability. Another distinction to fiber assembly is the lower thickness of the polymer ribbon, which could be used with flip-chip electrical connections without requiring laminate cutouts for additional clearances.

The optical design of the polymer interface is shown in Fig. 8(a)–(e). The ferrule lid was removed in the schematic of Fig. 8(e) for waveguide routing clarity. Standard fibers in an MT ferrule are connected to the left edge of Fig. 8(e) and butt-coupled to polymer waveguides. The standard pin-and-hole self-alignment of MT ferrules warrants polymer waveguide to fiber alignment at the MT connection. As the polymer waveguide couplers are mode-matched to standard fibers, the polymer-to-fiber

MT interface has similar alignment requirements to a standard fiber-to-fiber MT interface. From the fiber coupler, the polymer waveguide cross-section is adiabatically transformed to a higher confinement waveguide for routing and adiabatic coupling to chip. A simple pitch conversion is used here but any routing is possible. The cladding of the polymer waveguide is lithographically discontinued just prior to the photonic chip edge to expose the polymer waveguide core for adiabatic coupling to the chip. An optical UV adhesive acts as the effective optical cladding in that region. A non-linear silicon adiabatic taper creates an adiabatic crossing between the polymer and the silicon waveguide. The polymer waveguide cross-section is kept constant throughout the adiabatic transition with only the silicon side being tapered. As part of the mode transformation from the fiber mode to the silicon is accomplished in the polymer ribbon, the mode at the adiabatic crossing is sufficiently confined for a typical 2-μm oxide lower cladding to be used with no undercut required to prevent substrate leakage. The details of the polymer interface optical design with extensive tolerance analysis are shown in [18]. The polymer material used is described in [19], [20].

Two-dimensional self-alignment is used at both the ferrule to polymer ribbon interface and the polymer ribbon to chip interface. Self-alignment in the directions transverse to the waveguides (vertical and lateral) is required but typical high-throughput tool placement accuracy in the direction longitudinal to the waveguides is accommodated by design. The corresponding self-alignment structures are shown in Fig. 8(f) and (g), respectively. Slanted ridges in the precision injection molded ferrule are combined with grooves in the ribbon's lithographically patterned polymer cladding for ferrule to polymer ribbon self-alignment. Multiple vertical alignment references are used with ridges disposed in between the waveguide couplers in oversized polymer grooves not to over constrain the system laterally. The details of ferrule to ribbon assembly are presented in [21], [22]. We demonstrate a re-alignment accuracy to better than 1.5 μm. At the other end of the polymer ribbon, two polymer ridges are used with two matching slanted silicon grooves for polymer ribbon to chip self-alignment. Computational tolerance analysis shows that up to a 2 μm lateral misalignment can be tolerated at the adiabatic crossing [18]. We go beyond this optical requirement by demonstrating in [21] a lateral self-alignment to +/– 1-2 μm from the +/–10 μm initial alignment provided by high-throughput tools. The adhesive thickness, in between the polymer waveguide and the chip, is preferred to be of no more than 1 μm throughout the adiabatic crossing. A thicker adhesive near the chip edge is desired to prevent mode scattering due to the abrupt cladding index change experienced at that location. We demonstrate such adhesive profiles in [23] by using a combination of a pneumatic base for overall assembly pressure uniformity and a non-planar pick-tip to increase adhesive thickness near the chip edge.

The optical performance of the compliant interface is shown in Fig. 9. As seen in Fig. 9(a)–(b), automated assembly was used at the chip to polymer interface but a ferrule was not assembled to the ribbon requiring active alignment between a standard MTP fiber connector and the polymer ribbon end. Consequently, the spectral performance of Fig. 9(c) includes all sources of loss of the compliant interface concept but for
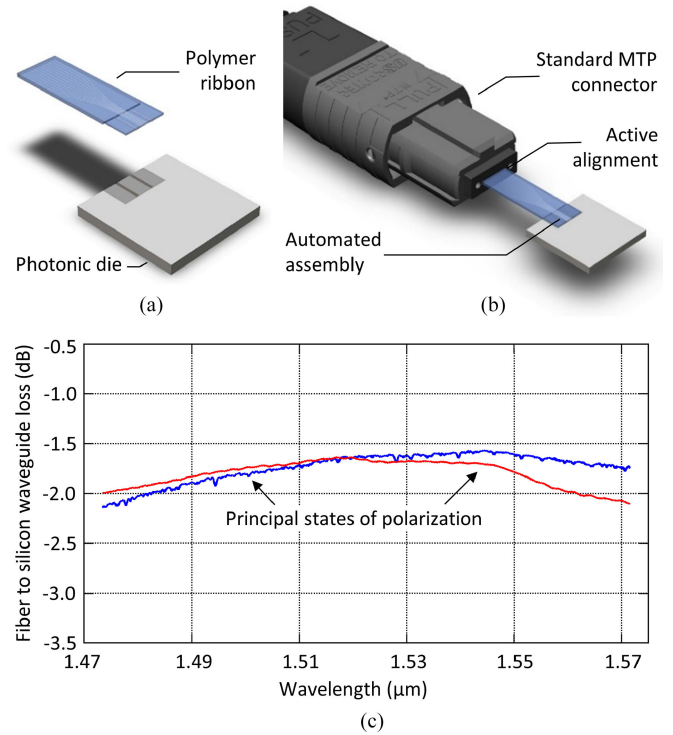

Fig. 9. Optical performance of the compliant polymer interface. (a) and (b) show the device measured here. Automated assembly was used at the ribbon to chip interface but active alignment was used at the ribbon to fiber connector interface as a ferrule was not assembled to the ribbon to enable passive MT connection. Accordingly, the compliant interface loss of (c) includes all loss sources but for possibly underestimating fiber-to-polymer alignment loss by up to 0.5 dB. We demonstrate a peak fiber-to-silicon transmission of –1.6 dB with 0.6 dB penalty over a ∼100 nm bandwidth and all polarization, an improvement over our previous results of [24].

possible additional polymer to fiber misalignment. The resulting additional loss is expected to be under 0.5 dB. We demonstrate a peak transmission of –1.6 dB, between a standard fiber and a full width Si waveguide, with 0.6 dB penalty over a ∼100 nm bandwidth and all polarizations. This is an improvement over the –2.4 dB peak transmission and the 1.5 dB penalty, over a 100 nm bandwidth and all polarizations, reported in [24]. The improved performance was attained by increasing the polymer waveguide confinement at the adiabatic crossing to reduce chip-edge scattering and by refining the polymer ribbon fabrication process [25]. The current design is centered at 1.55 μm but the compliant interface is expected to show similar performance if centered at 1.31 μm. Two counteracting effects differentiate operation at the 1.31 and 1.55 μm bands. On one hand, most optical polymers show lower propagation loss at 1.31 μm. On the other hand, the 15% shorter wavelength accentuates the fabrication and alignment tolerance penalty.

IV. SELF-ALIGNED FLIP-CHIP PHOTONIC ASSEMBLY

We address hybrid photonic integration by self-aligned, direct, flip-chip bonding of photonic dies. The size of the achievable mode for chip-to-chip coupling requires some consideration. As discussed above, a large fiber-matched mode can be cost-efficiently integrated on a silicon photonic platform by leveraging wafer processing originally developed for
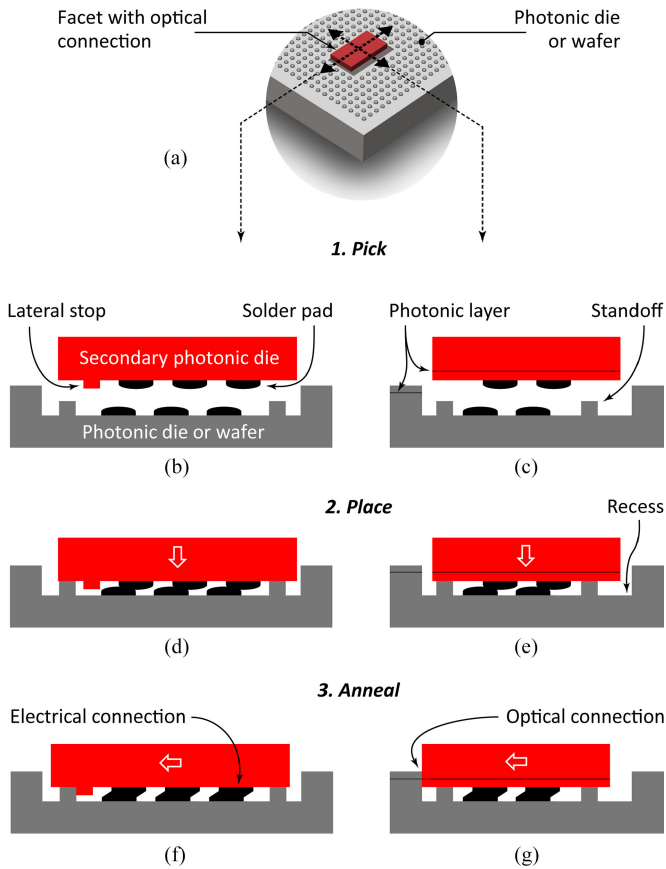
Fig. 10. Conceptual schematic of self-aligned, direct flip-chip assembly of photonic dies. (a) Perspective view indicating the cross-sectional orientation of (b)–(g). The sections of (b), (d), and (f) are taken across the waveguide couplers while the sections of (c), (e), and (g) are taken along the waveguide couplers. The secondary photonic die is picked with a high-throughput tool and placed with a purposeful offset on a primary photonic die or wafer. At anneal, the solder surface tension pulls the secondary chip into optimal alignment defined by the butting of lithographically patterned alignment stops. The result is a scalable optical, electrical and thermal connection to the primary photonic die.
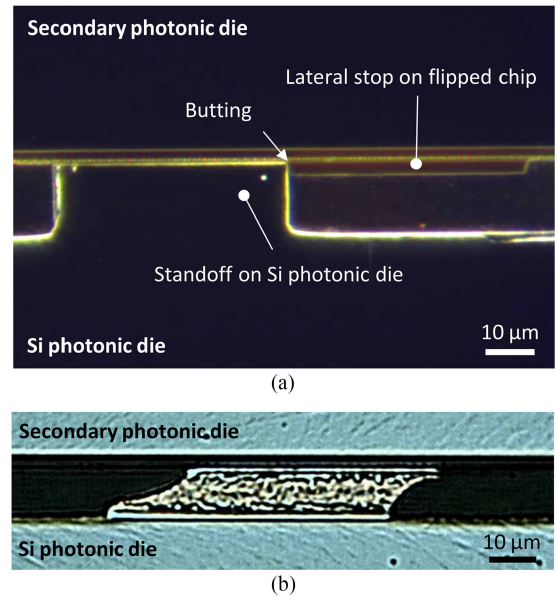

Fig. 11. Cross-sectional optical micrographs of a self-aligned direct flip-chip assembly. (a) Dark-field micrograph of a lateral stop, on a secondary die, butted on a standoff, on the Si die, acting as both a vertical and lateral position reference. At butting, the fabrication accuracy of alignment stops defines residual misalignment. A simple ridge is used as the stop here but the optimal shape depends on fabrication capabilities. (b) An SnAg pad after re-alignment. A residual offset is desired to maintain pressure on the alignment stops. Other solders, such as AuSn, can be used as well.

fabrication of micro-electro-mechanical structures. However, enabling technologies, such as bulk microfabrication processing, are not available in all material systems and a realistic expectation should be that such large modes would not be universally achievable on secondary photonic dies. As a consequence, one must work with the assumption that only a smaller mode will be universally achievable at chip-to-chip coupling. The result is a stringent requirement on alignment accuracy. The 1–2 μm alignment requirement of optical I/Os is replaced by the necessity of sub-micron alignment here.

Our solution to self-aligned photonic die assembly with sub-micron accuracy is presented in Fig. 10. The cross-sections of Fig. 10(b), (d) and (f) are taken across the coupling waveguides while the cross-sections of Fig. 10(c), (e) and (g) are taken along the coupling waveguides. A secondary photonic die is picked and placed on a silicon photonic die with a purposeful offset from its desired final position. This offset must be sufficiently large to prevent die positioning tolerances and die fabrication accuracy to result in the lateral stop landing on top of a standoff or the secondary die edge landing on the top-corner of the silicon photonic chip recess. The assembly is then annealed resulting in the solder melt displacing the secondary

photonic die towards solder pad alignment to minimize solder surface energy. The force exerted by the solder on the chip can be two orders of magnitude larger than gravity. Lithographically defined stops intercept the solder-induced movement to position the secondary die for optimal optical coupling. Once the stops are in contact, the alignment accuracy is defined by the stops patterning accuracy. With well-chosen stop fabrication options, three-dimensional self-alignment with sub-micron accuracy can be achieved in high-volume production. The standoffs, along with properly defined regions on the secondary die, provide vertical alignment, the lateral stop provides alignment in the direction lateral to the coupling waveguides, and the secondary die's butting on the edge of the silicon photonic recess defines the alignment stop in the direction longitudinal to the coupling waveguides. The solder pads used for self-alignment further provide electrical connections to the secondary photonic die and its thermal sinking. This flip-chip assembly can be performed either to a silicon photonic die or to a silicon photonic wafer, prior to it being diced.

The concept of solder-induced self-alignment has been discussed in research environments for decades [26]–[28]. What is novel here is the level of three-dimensional accuracy sought and the tackling of tolerancing issues that can negate the secondary's chip movement and, in turn, the assembly yield. For example, conventional solder re-alignment designs show excessive sensitivity to solder volume plating tolerances. This is described and resolved in [29] and [30], respectively.

Cross-sectional micrographs of self-aligned flip-chip assemblies are shown in Fig. 11. A simple ridge is shown here, as the lateral stop on the secondary die, but other structures have been investigated and may be preferred based on fabrication
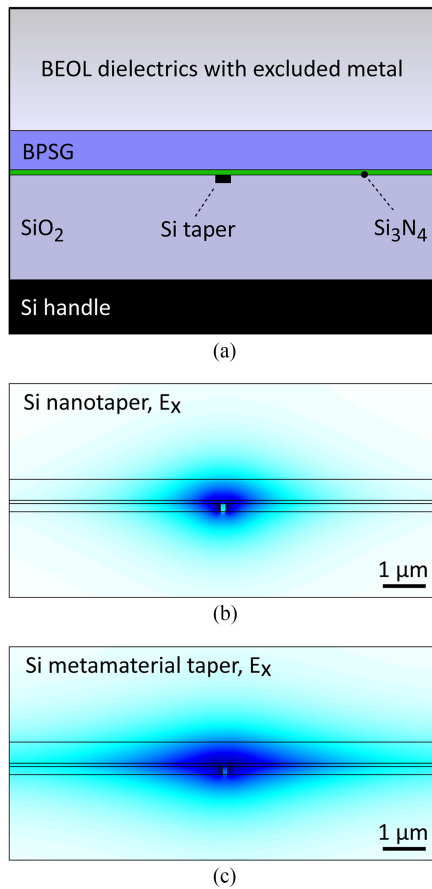
(a)

(b)

(c)

Fig. 12. Chip-to-chip coupler design. For a universal approach across various material systems we choose butt coupling with an elongated mode echoing the larger uncertainty on lateral positioning than on vertical positioning of chips. A structure resembling a strip-loaded waveguide is implemented on the Si chip re-using a common material stack of CMOS-integrated photonics [2]. A cross-sectional schematic is shown in (a). Mode profiles with a nanotaper and a metamaterial taper are shown in (b) and (c), respectively. They are matched to InP rectangular coupler waveguides with >95% mode overlap.
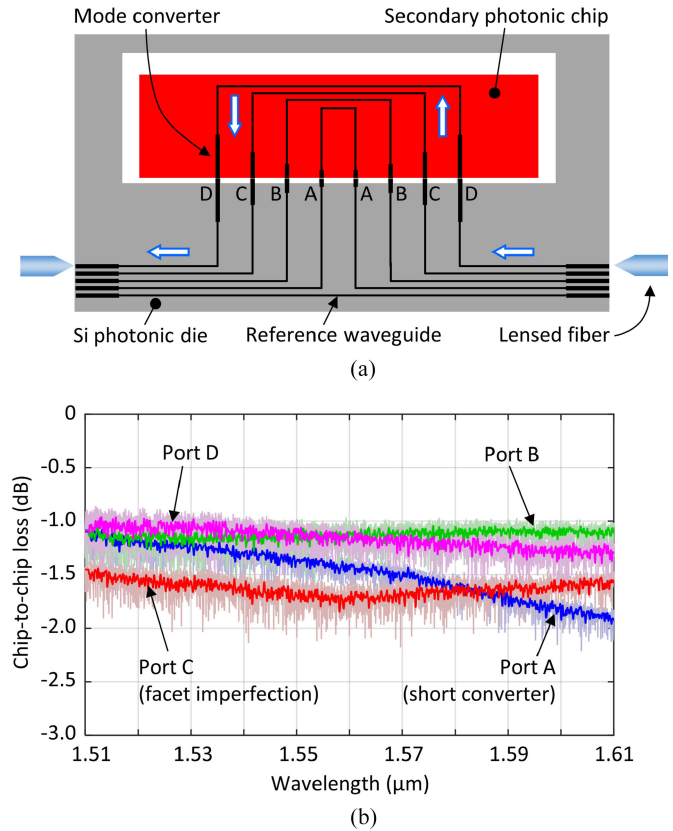

(a)

(b)

Fig. 13. Optical performance of self-aligned flip-chip photonic connections. The experimental setup is shown in (a). A secondary photonic die with integrated loopbacks was flip-chip assembled using solder-induced self-alignment. The coupler of Fig. 12(b) was used here with an optically equivalent SiON layer replacing the BPSG layer. A spread of mode converter lengths provided 37.5, 75, 150, and 250 um long converters at ports A, B, C, and D, respectively. The chip-to-chip loss is shown in (b) and corresponds to the roundtrip loss normalized to the reference waveguide loss and then divided by two to account for two chip interfaces per roundtrip. Raw data is superimposed with data where the Fabry–Perot fringes from the lensed-fiber interfaces were filtered out. A peak chip-to-chip transmission of –1.1 dB is shown for the TE polarization with 0.1 dB penalty over a 100 nm bandwidth.

capabilities. The lithographic layers chosen for the alignment references are of particular importance to the stops accuracy and, in turn, to residual misalignment. As shown in Fig. 11(b), a residual solder pad offset is desired after full re-alignment. It warrants a strong re-alignment force at butting and can mitigate creep concerns, a key reliability issue, as displacement of the chip away from the butted position would come at a notable cost in the thermodynamic free energy of the system through its surface energy component. Various solder materials can be used. Our work focused on SnAg as it is the solder of choice in microelectronics and the anticipation of lower creep concerns here suggests that a hard solder, such as the expensive AuSn, may not be required. Nonetheless, AuSn and other solders could be used as well.

The optical chip-to-chip interface is shown in Fig. 12. For a universal approach between potentially widely different die materials, we chose a butt coupling interface. Adiabatic coupling between chips has been proposed and can provide gains in alignment tolerances [31]. However, adiabatic crossings inher-

ently require the crossing of the effective indices of the waveguide employed [32]. This can be accomplished in most circumstances with nanotapers or metamaterial waveguides as long as the claddings show similar refractive indices. In the universal case, however, the claddings can be of substantially different indices making an adiabatic crossing impossible. An example is the difficulty in crossing the effective index of a channel waveguide in a silicon oxide or polymer cladding with the effective index of a waveguide in a III-V cladding.

Fabrication tolerances indicate that the residual vertical misalignment is generally smaller than the residual lateral misalignment. Hence, we choose a correspondingly asymmetric mode for the coupling interface. Its implementation on the silicon photonics side is shown in Fig. 12(a) and reuses a common material stack found in CMOS integrated photonic approaches [2]. An elongated mode resembling a strip-loaded waveguide is used here. A silicon nanotaper or metamaterial taper can be employed based on the mode size achievable on the secondary

die. The larger the mode, the larger the alignment tolerances. Other options are available as well [33]. The modes of Fig. 12(b) and (c) were matched to a typical InP laser coupler and a wide multimode InP laser coupler, respectively.

The optical chip-to-chip coupling performance with self-aligned, direct, flip-chip assembly was demonstrated using silicon photonic secondary dies. The experimental setup is presented in Fig. 13(a) with optical spectra in Fig. 13(b). The assembly is similar to the micrograph shown in Fig. 3(c). The filtered spectral response on port B shows a peak transmission per chip interface of –1.1 dB with 0.1 dB penalty over a 100 nm bandwidth. This loss includes spot-size conversion on both the primary and secondary die as well as mode mismatch and residual alignment loss. The coupler mode of Fig. 12(b) was used on both sides of the interface although the mode was vertically flipped on the secondary die resulting in a small 1.3% mode mismatch. A spread of non-linear adiabatic transition lengths from coupler to routing waveguide was used among the ports with lengths of 37.5, 75, 150, and 250 μm on ports A, B, C, and D, respectively. The transmission penalty on port A is attributed to the shortness of the spot-size convertor while the penalty on port C relates to a visible facet defect on the secondary die. The Fabry–Perot fringes in the raw data are dominated by reflections at the lensed-fiber interface to the primary photonic die. Isopropanol was used as index matching fluid between the primary and secondary die for optical characterization. Its index of ∼1.37 is lower than optimal for reflection management. An optical underfill would be used instead at manufacturing. This demonstration was done with measurements centered around a wavelength of 1.55 μm. However, this design could be effortlessly scaled to the 1.31 μm O-band.

V. CONCLUSION

We have demonstrated a novel direction in photonic packaging based on leveraging existing high-throughput microelectronic packaging facilities to bring disruptive improvements in photonic packaging cost, scalability in optical port count, and scalability in manufacturing volume. This strategy is analogous to silicon photonics leveraging microelectronics fabrication facilities to achieve photonics circuits of unprecedented complexity and cost efficiency. For a complete solution, we have demonstrated two approaches to optical I/Os and one to hybrid photonic integration. Self-alignment has been used throughout to bridge the gap between the 10-μm placement inaccuracy of high-throughput pick-and-place tools and the micron-level accuracy required by single-mode silicon photonics. We have shown self-aligned peak transmission reaching –1.3 dB from standard cleaved fiber to chip and –1.1 dB from chip to chip. The approaches demonstrated here aim to be universal by simultaneously enabling wide spectral bandwidth and large optical port count.

For completeness, we are pursuing two approaches to optical I/Os offering non-overlapping risks and rewards. The choice between the two is application dependent. On one hand, direct fiber assembly currently shows higher peak coupling efficiency

and brings the certitude of known optical fiber reliability from decades of field deployment. On the other hand, the polymer interface is expected to show better thermo-mechanical robustness and its chip interface is simpler to integrate with standard microelectronics fabrication flows. A number of additional factors are also to be considered such as differences in cost scaling with optical port count between the two solutions.

Our current focus is on demonstrating yield and environment reliability with adequate statistics. Our preliminary reliability and yield assessments, through materials study, Monte Carlo analysis, and experimental self-alignment data, demonstrate the soundness of the concepts but additional experiments are required to meet industry standards.

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