Demonstration of a High Extinction Ratio Monolithic CMOS Integrated Nanophotonic Transmitter and 16 Gb/s Optical Link

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(Invited Paper)

***Abstract*—We present a 16-Gb/s transmitter composed of a stacked voltage-mode CMOS driver and periodic-loaded reverse biased pn junction Mach–Zehnder modulator. The transmitter shows 9-dB extinction ratio and 10.3-pJ/bit power consumption and operates with 1.3 μm light. Penalties as low as 0.5 dB were seen as compared to a 25-Gb/s $LiNbO_3$ transmitter with both a monolithic metal–semiconductor–metal receiver and a reference receiver at 16-Gb/s operation. We also present an analytic expression for relative transmitter penalty (RTP), which allows one to quickly assess the system impact of design parameters such as peak-to-peak modulator drive voltage, modulator figure of merit, and transmitter extinction ratio to determine the circumstances under which a stacked CMOS cascode driver is desirable.**

***Index Terms*—Electrooptic modulators, integrated optics, electrooptic devices.**

I. Introduction

CMOS integrated nano photonics (CINPs) could bring traditional semiconductor industry efficiency and low cost manufacturing to the application space of optical interconnects, which has the potential to enable large scale deployment of broadband communication links [1]. IBM has recently announced its sub-100 nm CINP technology (CMOS9WG), which includes WDM filters, germanium (Ge) photodetectors (PDs), silicon modulators, optical couplers, etc., monolithically integrated with analog and mixed-signal circuits [2]. IBM's CMOS9WG photonics components are integrated into the CMOS front end thereby minimizing extra processing steps, additional required mask levels, and component parasitics. Monolithic integration can also minimize packaging and handling steps, potentially reducing the end product cost. However, technology solutions range from the hybrid approach [3]–[8], which separates electrical and optical components on separate chips, to a fully monolithically integrated solution [9]–[15]. A hybrid solution allows the designer to focus on optimizing the optical and electronic functions separately, and also this approach allows picking the best chip technology for each purpose. Drawbacks of the hybrid approach include interface related parasitics that can degrade performance, and final functionality can only be tested when a pair of chips is assembled. In addition, a co-optimization of hybrid components is more challenging due to the disconnected optical and electrical design environments. However, for the monolithic approach co-optimization is very natural due to a single design environment enabled for both electrical and photonic components [2]. Furthermore, maintaining enough electrical content on the photonics chip as is necessary for fully functional wafer level testing and chip disposition prior to assembly invokes the concept of the "smart partitioning" of the technology to optimize yield and minimize cost, which ultimately can open this technology up for use in a broader range of applications.

In the following we report on a 16 Gb/s transmitter (TX) with a monolithically integrated stacked voltage-mode CMOS driver [16]–[18] and periodically loaded MZM operated with 1.3 μm light. In addition, we demonstrate a link between a CMOS9WG TX and a separate CMOS9WG receiver that is a Ge metal–semiconductor–metal (MSM) photo-detector monolithically integrated with a CMOS transimpedance amplifier (TIA) and limiting amplifier (LA) [19]. All hardware was manufactured in IBM's CMOS9WG technology node. In addition, we present an analytic expression for RTP based on the peak-to-peak modulator drive voltage, modulator figure of merit (FOM), and TX extinction ratio (ER), which allows us to easily assess the system impact of these design parameters and determine circumstances under which a stacked CMOS cascode driver is preferred. In Section II we present our analytic expression for RTP, and use it to consider high level TX and system design considerations. Section III reviews our specific CMOS and MZM designs demonstrated, and Section IV presents the

Manuscript received October 8, 2014; revised November 25, 2014; accepted November 29, 2014. Date of publication December 18, 2014; date of current version January 27, 2015.

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Digital Object Identifier 10.1109/JSTQE.2014.2381468

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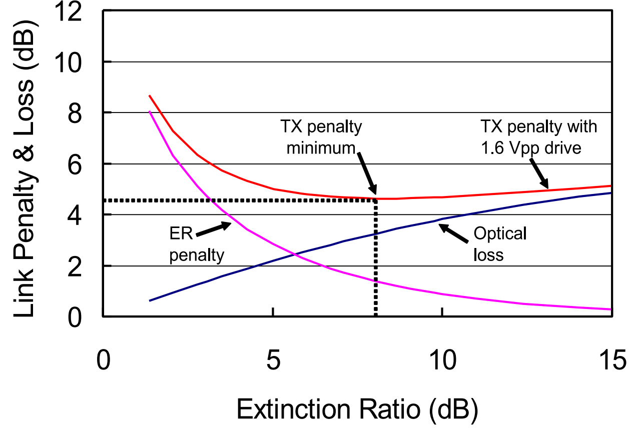
TX characterization results with a reference receiver. Section V describes our monolithic receiver design, and Section VI provides CMOS9WG link results. Section VII gives discussion and conclusions.

II. TX and System Design Considerations

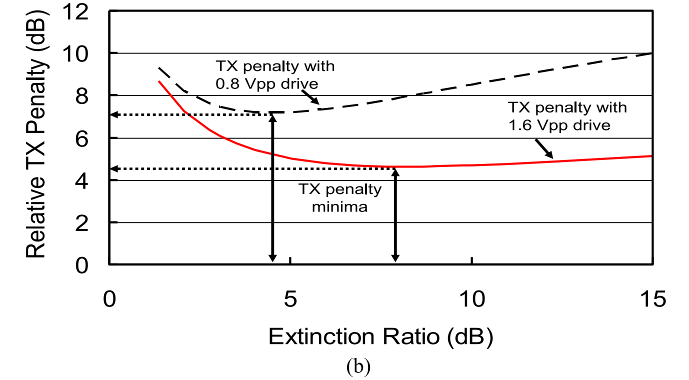
Significant progress has been reported on the design and manufacturing of CMOS compatible Mach–Zehnder modulators (MZMs) [9]–[15], [20]–[39] and reverse biased plasma dispersion electro-optic phase shifters [39]–[48]. However, designing a monolithic TX implies limits on attainable CMOS direct drive voltages according to the capabilities of the technology. In developing a TX design strategy it is essential to weigh pertinent performance criteria from the full link. For example, two significant sources of link power consumption are the TX CMOS and the continuous wave (CW) laser drive power. In addition, the TX CMOS and CW laser drive power are related in that one can maintain an identical unamplified link margin by using high laser power and lower TX drive power (generating lower optical ER), or lower laser power and higher TX drive power (generating larger ER). Since we are implementing a monolithic CMOS9WG technology platform, there are two straightforward architectural choices to consider for TX circuit design, either a current-mode CMOS driver (e.g., the VCSEL driver in [19]) or a voltage-mode CMOS driver [16]–[18]. The advantage of the voltage-mode CMOS driver is that it can provide about twice the peak-to-peak drive voltage (V_{pp}) compared to a current-mode CMOS driver, when the voltage-mode driver uses stacking/cascoding to increase its output voltage tolerance [16]–[18]. However, the increased voltage swing comes at the cost of higher power consumption. In the following we consider the difference in power consumption needed between the current-mode and stacked voltage-mode CMOS TX driver designs, and relate this to associated laser power consumption expectations in order to maintain a given link margin.

A key aspect in understanding this tradeoff is to quantify the relative penalty the TX imparts on the link, hereafter called the RTP. In unamplified links there is a quantifiable trade-off between the accessible MZM radio frequency (RF) V_{pp}, the TX optical ER, and the optical absorption loss created by the reverse-bias plasma-dispersion MZM. A key parameter in understanding the RTP for a given link is the MZM efficiency-loss [47], [48] FOM defined by the product of the phase shifter propagation loss and its Vπ-L product. The FOM can be written as FOM = $V\pi\text{-}L*\alpha_{\text{phase shifter}}$, and has units of (V·cm)∗(dB/cm) → V·dB. The details of how these TX design tradeoffs impact link budget depends on the transmission format used. We have previously shown in [47] that for the non-return to zero (NRZ) transmission format the RTP is governed by:

RTP = {NRZ ER penalty in dB} + {Modulator optical loss in dB}



(a)



(b)

Fig. 1. (a) RTP, ER penalty, and MZM optical insertion loss for a stacked voltage-mode CMOS drive TX with a 1.6 V_{pp} RF drive. This figure shows that a minimum penalty is achieved with a ∼8 dB ER. (b) A comparison of the MZM-based RTP using current-mode CMOS with 0.8 V_{pp} drive versus a stacked voltage-mode CMOS drive with 1.6 V_{pp}, which gives 2.6 dB reduction in penalty from the TX.

The RTP essentially represents changes in the ratio between the input laser power and the output TX optical modulation amplitude (OMA), which quantifies the margin degradation in an unamplified link due to limitations in TX ER and optical loss from a MZM-based TX. Note that this definition of RTP does not include additional margin penalties incurred due to TX bandwidth limitations.

For example, if we consider the RTP from a stacked voltage-mode CMOS TX driver design, we need to first define the expected TX RF drive V_{pp} and MZM FOM, which for the purposes of this discussion are V_{pp} ∼1.6 V and MZM phase shifter FOM = (1.67 V·cm)∗(12 dB/cm) = 20 V·dB, respectively (numerical values correspond to the monolithic TX characterized in Section III below). Applying these values to Eq. (1) [see at the bottom of this page], the RTP can be plotted as a function of MZM ER as shown in Fig. 1(a) and (b). We note that in practice, the *x*-axis

$$\mathrm{RTP} = \left\{10\mathrm{L}og_{10}\frac{(10^{\mathrm{ER}/10}-1)}{(10^{\mathrm{ER}/10}+1)}\right\} + \left\{\frac{\mathrm{FOM}}{2V\mathrm{pp}}\left(1-\frac{4\arccos\left(\sqrt{\frac{1}{1+10^{\frac{\mathrm{ER}}{10}}}}\right)}{\pi}\right)\right\}. \tag{1}$$

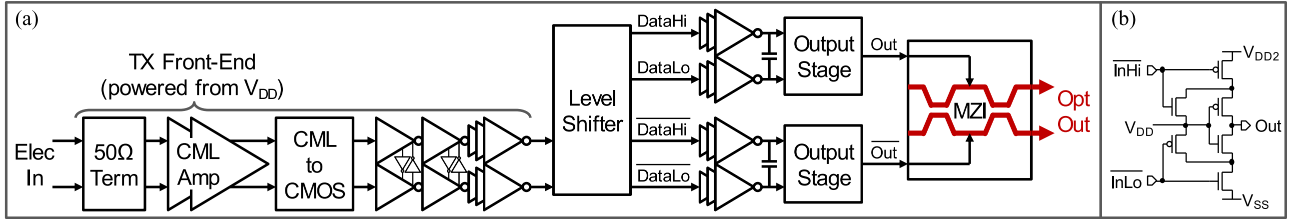


Fig. 2. (a) TX block diagram. (b) CMOS driver output stage schematic.

ER in Fig. 1(a) and (b) can be varied by changing the length of the MZM, since $V_{\rm pp}$ and FOM are fixed. The curve marked "Optical loss" in Fig. 1(a) indicates how MZM optical loss increases as its length and ER increases. The curve marked "ER penalty" shows how the NRZ penalty from a limited ER decreases as the MZM is made longer and the ER increases. The RTP = "NRZ ER penalty" + "Modulator optical loss" shows a minimum at an ER of ∼8 dB, which also indicates that the maximum attainable OMA is realized at this design point, assuming a fixed input CW laser power. For unamplified links this RTP minimum corresponds to the most efficient design point for the TX for the FOM value of 20 V·dB. The resulting RF/optic interaction length for this design is ∼0.27 cm for each MZM arm. We note that as shown in Fig 1(a) the TX penalty changes less than 0.5 dB for MZMs designed to have ERs ranging from ∼5 to >10 dB. In this MZM design space the increase in optical loss penalty is nearly the same as the decrease in ER penalty, and so a reasonably broad range of MZMs designs could be implemented with minimal impact on link performance in unamplified optical links.

The same calculus can be performed for a current-mode CMOS RF driver, which provides ∼0.8 $V_{\rm pp}$ RF drive. This curve is shown in Fig. 1(b) and is labeled as "TX penalty with 0.8 $V_{\rm pp}$ drive". Fig. 1(b) compares the current-mode CMOS TX RTP to that of the stacked voltage-mode CMOS driver TX design. This figure shows that using the current-mode CMOS drive increases the optimum RTP by 2.6 dB. However, we note that the optimum design for the current-mode CMOS TX is when a ∼4.5 dB ER is attained, which corresponds to an RF/optic interaction length of ∼0.33 cm in each MZM arm. Accordingly, Fig. 1(b) indicates the current-mode CMOS TX would require an additional 2.6 dB of input CW laser power in order to match the link performance obtained for the stacked voltage-mode CMOS TX design in an unamplified link.

III. TX Circuit and MZM Design

The TX block diagram is shown in Fig. 2(a). The electrical input has a 50 Ω on-chip termination and a current-mode logic (CML) amplifier to boost weak input signals to CML levels, followed by a CML-to-CMOS converter. Cross-coupled CMOS inverters minimize timing error between the complementary signals. The front-end accepts single-ended or differential inputs. The level shifter [17] provides Lo ($V_{\rm SS}$ to $V_{\rm DD}$) and Hi ($V_{\rm DD}$ to $V_{\rm DD2}$) CMOS outputs, which are buffered by inverter chains to drive the stacked output stage [18]. The stacked output stage, Fig. 2(b), uses cascoding to limit the static voltage across any device to $V_{\rm DD}$ while providing $V_{\rm SS}$ to $V_{\rm DD2}$ output swing

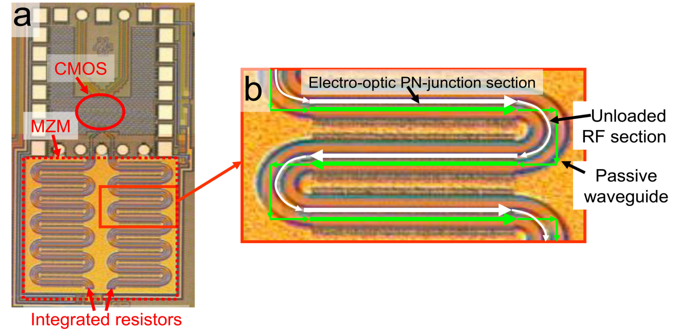


Fig. 3. (a) Image of monolithic TX with stacked CMOS drive and periodic loaded MZM. The MZM has a total push-pull RF/optic interaction length of 6 mm (3 mm per MZM arm). (b) Magnified view of periodically loaded electrode in MZM.

[16]–[18]. Electrical testing at $V_{\rm DD} = 1.5$ V, $V_{\rm DD2} = 3$ V gave 2 $V_{\rm pp}$ into 50 Ω (25 Ω output impedance), or 4 V peak-to-peak differential ($V_{\rm ppd}$) push-pull to 50 Ω MZM electrodes. The CMOS driver circuits were designed for a high-ER optical TX targeting short-reach optical interconnect applications at up to 16 Gb/s (e.g., PCI Express 4.0, Fibre Channel, Infiniband). The measurements presented below demonstrate performance out to 20 Gb/s.

An MZM electro-optic modulator is used in the TX due to its relatively temperature insensitive operation. The MZM has lateral PN junctions with 4×10^{17} cm^{-3} peak p and n doping concentrations (as indicated by simulations of the processing implant conditions and thermal budget), a ∼135 nm SOI thickness, and 2 μm BOX appropriate for a ∼1.3 μm wavelength of operation. The pn junctions show a leakage current on the order of nanoamps with a 1 V reverse bias, and so have a shunt resistance on the order of hundreds of mega-ohms. An image of the TX is shown in Fig. 3(a). The CMOS driver differential output is coupled directly into a periodically loaded push-pull MZM. The MZM incorporates unloaded RF electrode segments to increase the electrode effective line impedance. The unloaded RF segments are transmission line sections that are not connected to pn junctions and are periodically inserted into the MZM electrode. Fig. 3(b) shows the loaded sections (electrode sections coupled to a pn-junction) are the straight horizontal electrode segments highlighted by thick white arrows, and the unloaded sections are the 180° turn segments denoted by the narrow white arrows. Each MZM arm has ten 300 μm long electrode sections loaded with optical pn-junctions (3 mm total loaded electrode length in each MZM arm) and nine 157 μm long unloaded elec-

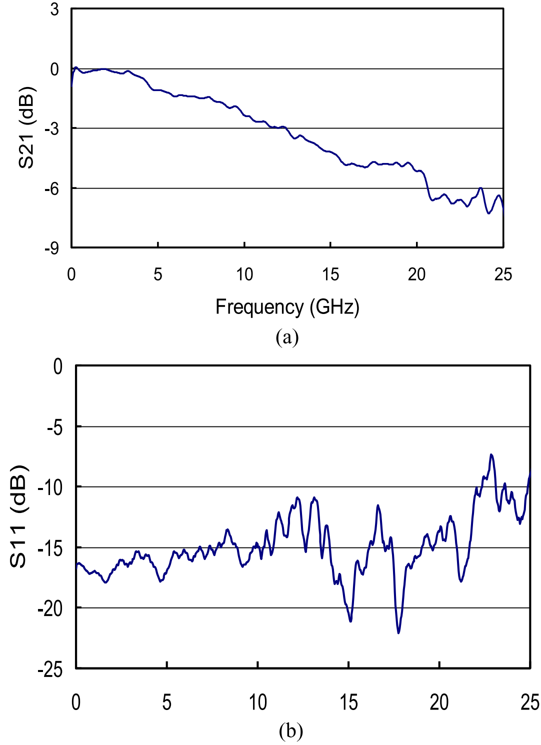


Fig. 4. (a) S21 electro-optic bandwidth measurement from a stand alone MZM that was not connected to CMOS, and was nominally identical to that shown in Fig. 3(a), (b) S11 response from the same device as used in (a).

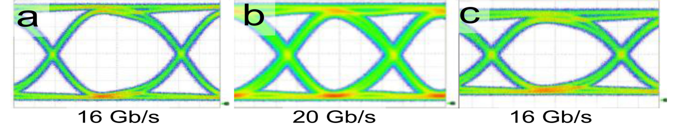


Fig. 5. (a) 10.4 dB ER 16 Gb/s eye diagram with $2^{31}-1$ PRBS, $V_{\rm DD} = 1.5$ V, $V_{\rm DD2} = 3$ V, $\sim$1.7 $V_{\rm pp}$ from the CMOS driver, and 278 mW power consumption from the CMOS driver. (b) 10.4 dB ER 20 Gb/s eye diagram with $2^{31}-1$ PRBS, $V_{\rm DD} = 1.5$ V, $V_{\rm DD2} = 3$ V, $\sim$1.7 $V_{\rm pp}$ from the CMOS driver, and 278 mW power consumption from the CMOS driver. The 1.7 $V_{\rm pp}$ signal in the MZM phase shifter is consistent with the 35 Ω line impedance measured for the MZM pn-junction sections. (c) 9.0 dB ER 16 Gb/s eye diagram with $2^{31}-1$ PRBS, $V_{\rm DD} = 1.2$ V, $V_{\rm DD2} = 2.4$ V, $\sim$1.6 $V_{\rm pp}$, and 165 mW power consumption from the CMOS driver. For all of the eye diagrams the *y*-axis scale is 160 μW/div and the *x*-axis scale is 10 ps/div.

trode sections, resulting in a $\sim$68% loading and 4.41 mm total electrode length. Since the unloaded electrode sections have low capacitance their relative contributions to RF propagation losses are small. The passive RF sections have a line impedance of $\sim$87 Ω and the loaded sections have a line impedance of $\sim$35 Ω, as extracted from transmission line measurements. Therefore, the effective line impedance from the combined loaded and unloaded sections is calculated via a weighted average to be $\sim$52 Ω across the RF frequency range of interest. The MZM has integrated terminating resistors that are nominally designed to have a 50 Ω resistance. However, this hardware was designed using a process design kit (PDK) for bulk 90 nm CMOS that was not centered for photonics-enabled SOI substrates. Therefore, the fabricated MZM terminating resistor had a value of $\sim$58 Ω. The MZM also has nine passive optical waveguide sections $\sim$218 μm long (narrow green arrows, in proximity to the unloaded RF sections), summing to 1.967 mm of passive waveguide in each MZM arm.

The termination mismatch between the MZM effective line impedance of 50 and the 58 Ω terminating resistor at the end of the MZM created an RF reflection back into the RF/optic interaction region that negatively impacted the MZM S21 electro-optic bandwidth. Therefore, we used a focused ion beam (FIB) to deposit a wire in parallel with the integrated terminating resistor to reduce the value of the terminating resistance. The bandwidth from a stand-alone MZM that was not connected to a CMOS drive circuit and whose terminating resistor was modified using a FIB wire deposition is shown in Fig. 4(a). The FIB deposition created an additional electrical connection with a 200 Ω resistance that was in parallel with the 58 Ω integrated terminating resistor. The 200 Ω FIB wire in parallel with the 58 Ω integrated termination provided a final MZM terminating resistance of $\sim$45 Ω for this bandwidth measurement. The bandwidth was measured to be $\sim$12 GHz when a dc bias of -0.8 V was applied, which is the bias supplied by the stacked voltage-mode CMOS driver during operation. The S11 response from the same modulator is shown to be < -12 dB out to $\sim$12 GHz in Fig. 4(b).

Fig. 5(a) and (b) show 16 and 20 Gb/s optical eye diagrams at an operating wavelength of 1.31 μm, having 10.4 dB ERs from the monolithic TX. The CMOS directly provides the reverse bias required for high speed operation of the MZM PN diode phase shifters, and so no external MZM biases were needed. The TX CMOS supply voltages were run at $V_{\rm DD2} = 3.0$ V and $V_{\rm DD} = 1.5$ V, and at these settings the TX CMOS consumed 278 mW for 20 Gb/s operation ($\sim$14 pJ/bit), whereas its power consumption at 16 Gb/s was $\sim$16 pJ/bit. Fig. 5(c) shows a 16 Gb/s eye diagram with 9 dB ER from the TX when reduced supply voltages of $V_{\rm DD2} = 2.4$ V and $V_{\rm DD} = 1.2$ V were used. For these settings the driver consumed 165 mW, or 10.3 pJ/bit. Therefore, the power consumption is reduced by 110 mW in conjunction with a 0.3 dB OMA penalty, when running the CMOS at these reduced biases.

The total MZM optical insertion loss was estimated to be $\sim$5.4 dB, which includes excess losses from several optical subcomponents. The MZM phase shifter loss and passive waveguide losses were measured on separate structures with three different "cut-back" waveguide lengths, and were found to be 12.4 and 4.1 dB/cm for the 0 V biased pn-junction and passive ridged waveguide, respectively. Therefore, we estimate there was $\sim$4.7 dB loss from the phase shifters, $\sim$0.6 dB loss from the passive ridged waveguides, and $\sim$0.5 dB loss from each of the thermally tunable couplers at the input and output of the MZM arms. Each thermally tunable coupler was itself a MZM composed of an input 3 dB directional coupler, thermo-optic phase shifters, and an output 3 dB directional coupler.

Measurements indicated the pn-junction loaded electrode sections have a line capacitance of $\sim$0.44 fF/μm and an RF group index of $\sim$3.2. Using this result in conjunction with simulations of the unloaded RF electrode, the weighted average effective RF

propagation constant through the MZM is estimated to be ∼3.0. The optical group index of the ridged waveguides was measured to be ∼3.64, which was extracted by determining the round trip delay in ring devices. The high speed MZM $V_\pi * L$ product was determined to be 1.67 V·cm by correlating eye diagram ER at 16 Gb/s to a given $V_{\rm ppd}$ drive, in MZM devices not connected to CMOS. Using the MZM $V_\pi * L$ product, RF/optic interaction length, and output eye ER we calculate the $V_{\rm pp}$ drive in the pn-junctions was ∼1.6 $V_{\rm pp}$ on each MZM arm (or 3.2 $V_{\rm pp}$ differential drive with $V_{\rm DD} = 1.2$ V and $V_{\rm DD2} = 2.4$ V), 15% less than standalone electrical measurements into a 50 Ω test system.

We next consider the relative impact the velocity mismatch, electrode loss, and impedance matching have on the MZM bandwidth. Equation (2) is an analytic expression for the bandwidth of a traveling wave MZM [49], [50]:

$$M(\nu) = \frac{e^{-(\alpha(\nu)L/2)} \sin^2\left(\frac{\gamma L}{2}\right) + \left(\frac{1}{4}\right)(1 - e^{-(\alpha(\nu)L/2)})^2}{\left(\frac{\gamma L}{2}\right)^2 + \left(\frac{\alpha(\nu)L}{4}\right)^2} \tag{2}$$

where $\alpha(\nu)$ is the frequency-dependent microwave *power* attenuation coefficient, L is the active length of the device, and $\gamma = 2\pi\nu(N_m - N_o)/c$ where N_m is the effective microwave index, N_o is the effective optical index, and c is the speed of light in vacuum. The solution to the transcendental equation $M(\nu) = 0.5$ is what is referred to as the 3-dB electrical (dBE) bandwidth. The impact of velocity mismatch can be better understood by calculating the expected MZM bandwidth using the optical group index of 3.64, an RF group index of 3, and an electrode length of 4.41 mm, and assuming negligible RF propagation loss, perfect impedance matching, and neglecting carrier dynamics. The resulting expected MZM bandwidth considering only velocity mismatch was calculated to be ∼47 GHz. Therefore, the major contributors to MZM bandwidth limitation are the electrode RF propagation losses and impedance mismatch issues within the device and measurement environment [51], [52].

The TX circuitry characterized above was designed using a bulk 90 nm CMOS PDK, since at the time of this particular design a PDK calibrated to photonics-enabled SOI substrates was still under development. More recently, we have completed a PDK with hardware-correlated device models derived from dedicated SOI hardware. Circuit simulations performed with the updated models indicate that a 1.7 $V_{\rm pp}$ output from a nominally biased stacked voltage-mode driver is a reasonable expectation across process and environment corners.

IV. TX Characterization

The CMOS9WG TX was characterized using a 40 Gb/s Discovery Semiconductor R411 reference receiver. The CMOS9WG TX performance was compared to that of a 25 Gb/s $LiNbO_3$ TX, realized using a 40 Gb/s EOspace $LiNbO_3$ modulator model AZ-OV1-25-PFU-SFU-130-SIB612, having a bandwidth of ∼30 GHz, in conjunction with a 17.5 GHz bandwidth RF filter to limit the modulator bandwidth. Fig. 6(a) and (b) shows bit error ratio (BER) curves versus received OMA for both the CMOS9WG TX and the $LiNbO_3$ TX at a bit rate of 16 Gb/s. Fig. 6(a) shows sensitivity curves when the CMOS9WG TX had CMOS bias settings of $V_{\rm DD} = 1.2$ V and $V_{\rm DD2} = 2.4$ V, illustrating that the CMOS9WG TX has a 1 dB penalty at a BER of 1×10^{-12} as compared to the $LiNbO_3$ TX when operated at 16 Gb/s. Fig. 6(b) shows a similar comparison when the CMOS9WG TX had CMOS bias settings of $V_{\rm DD} = 1.5$ V and $V_{\rm DD2} = 3.0$ V, and shows a 0.5 dB penalty at 16 Gb/s relative to the $LiNbO_3$ TX.

V. CMOS9WG Receiver Circuit and MSM PD Design

The silicon photonic receiver circuit consisted of a CMOS TIA and LA monolithically integrated with a MSM Ge PD [53]. The RX block diagram is shown in Fig. 7. The RX is an adapted version of the T-coil RX circuit published in [19], and was designed using 90 nm bulk CMOS models, as SOI models were not available at design time. The targeted gain and data rate were >10 kΩ and ≥25 Gb/s, respectively. The TIA is realized as a pair of CMOS inverters with resistive feedback, one active and one a replica. A differential pair steers current into the TIA input nodes for dc offset compensation. The LA is an 8-stage differential amplifier using T-coils for bandwidth extension. The low pass filter amplifies the difference between the dc levels at the LA output and returns it to the TIA for dc offset compensation. The output stage (OUT) is an inductively-peaked differential amplifier. The nominal supply voltage is 1.2 V.

The PD cathode was connected to a 1.5 V supply. The photodiode anode was self-biased by the receiver front-end at ∼0.5 V. At the resulting bias of ∼1.0 V, the MSM PD exhibited a responsivity of 0.45 A/W and a dark current of 14.4 μA. PD responsivities of 0.55 A/W have been demonstrated in similar designs [53]. The power consumption in the receiver was 90 mW, and so consumed ∼4.5 pJ/bit at 20 Gb/s and ∼5.6 pJ/bit at 16 Gb/s. The receiver showed open eyes beyond 25 Gb/s [53].

VI. CMOS9WG Link Measurements

Link measurements were performed with the CMOS9WG TX and RX hardware described above, and also with a 25 Gb/s $LiNbO_3$ based reference TX for comparison (assembled as described in Section IV above). Fig. 8(a) shows a schematic diagram of the CMOS9WG-TX/CMOS9WG-RX link where CW 1.31 μm laser light was edge coupled into the TX chip using active alignment with a single mode lensed fiber, giving an estimated facet loss of ∼1.9 ± 0.4 dB/facet (as measured from a separate straight waveguide reference site). A 32 Gb/s Centellax SSB16000 pattern generator was used to directly drive the CMOS9WG TX CMOS with a 0.4 $V_{\rm pp}$ $2^{31} - 1$ psuedo random bit sequence (PRBS) signal via 40 GHz high speed GGB probes. The modulated light was edge coupled out of the TX and carried to the RX chip via 10 m standard single mode fiber. The signal was edge coupled into the RX CMOS9WG chip and the electrical output of the CMOS9WG chip was coupled into an Anritsu 28 Gb/s MP1800A signal analyzer BER tester via high speed probes to generate sensitivity curves. Fig. 8(b) shows a schematic diagram for the 25Gb/s-$LiNbO_3$/CMOS9WG-RX link where the system configuration was similar, but CW light

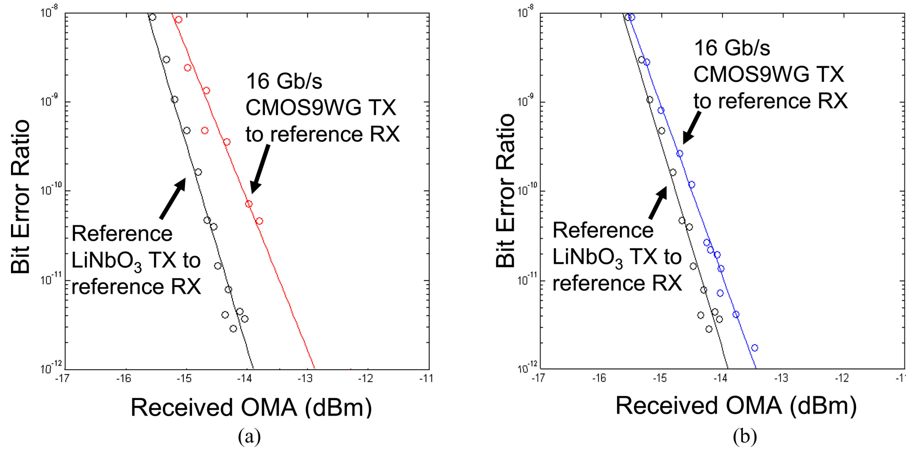


Fig. 6. (a) 16 Gb/s sensitivity curves for the CMOS9WG-TX with CMOS biases set to $V_{\mathrm{DD}} = 1.2$ V and $V_{\mathrm{DD2}} = 2.4$ V and the reference-$\mathrm{LiNbO_3}$-TX linked to a reference receiver. (b) Same as in (a) except $V_{\mathrm{DD}} = 1.5$ V and $V_{\mathrm{DD2}} = 3.0$ V.

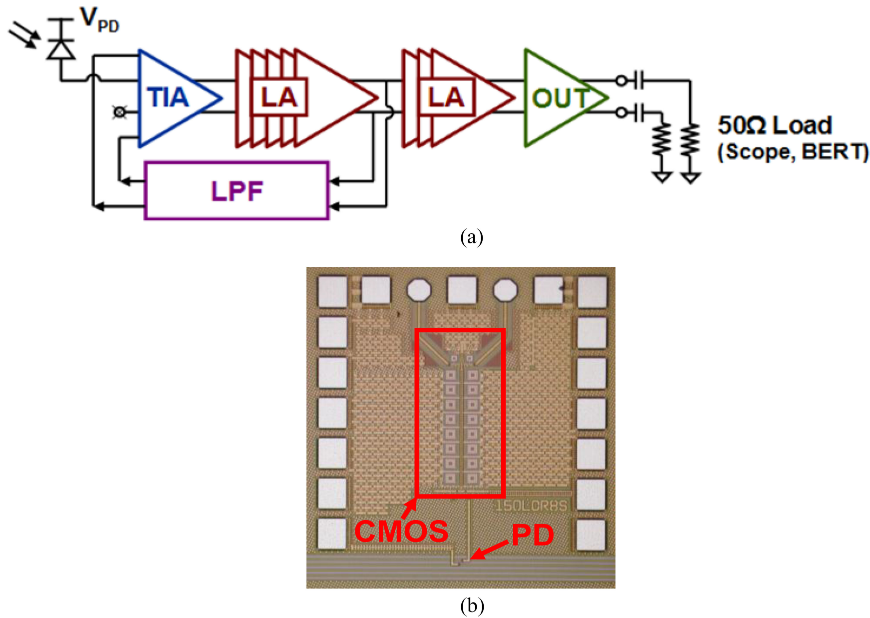


Fig. 7. (a) Schematic diagram of the RX CMOS design. (b) Picture of the monolithic CMOS and MSM PD.

was coupled into an EO-space $\mathrm{LiNbO_3}$ modulator that was driven single ended with a Centellax 32 Gb/s RF amplifier from the output of the 28 Gb/s Anritsu pulse pattern generator.

Receiver output electrical eye diagrams from the measured 16 Gb/s links are shown in Fig. 9(a)–(d). Fig. 9(a) shows the RX data port electrical eye from the CMOS9WG-TX/ CMOS9WG-RX link at $\sim 1 \times 10^{-12}$ BER, whereas Fig. 9(b) shows the data-bar output from the same link. The CMOS9WG-TX was biased at $V_{\mathrm{DD}} = 1.5$ V and $V_{\mathrm{DD2}} = 3.0$ V for these measurements. Fig. 9(c), shows a 16 Gb/s data port electrical eye from the $\mathrm{LiNbO_3}$/CMOS9WG-RX link at $\sim 1 \times 10^{-12}$ BER, and Fig. 9(d) shows the data-bar output from the same link. All of the 16 Gb/s eye diagrams show minimal inter-symbol interference. A sensitivity curve with a $2^{31} - 1$ PRBS for the CMOS9WG link at 16 Gb/s is shown in Fig. 10(a). Also shown in Fig. 10(a) is a sensitivity curve from the $\mathrm{LiNbO_3}$ based TX linked to the CMOS9WG RX. The received OMA is calculated from the measured average received photocurrent, the separately measured modulator ER, and photodiode responsivity. The OMA is referenced to the power in the on-chip waveguide at the photodiode input. Fig. 10(a) shows the CMOS9WG link at 16 Gb/s required -7 dBm of (OMA) at the MSM detector for a 1×10^{-12} BER, whereas the link between the $\mathrm{LiNbO_3}$ TX and CMOS9WG RX required -7.5 dBm of OMA. Therefore, the CMOS9WG TX showed 0.5 dB penalty compared to the $\mathrm{LiNbO_3}$ TX at 16 Gb/s.

Receiver electrical eye diagrams from the measured 20 Gb/s links are shown in Fig. 11(a) and (b). Fig. 11(a) shows the RX data port electrical eye from the CMOS9WG-TX/CMOS9WG-RX, whereas Fig. 11(b) shows the 20 Gb/s data port electrical

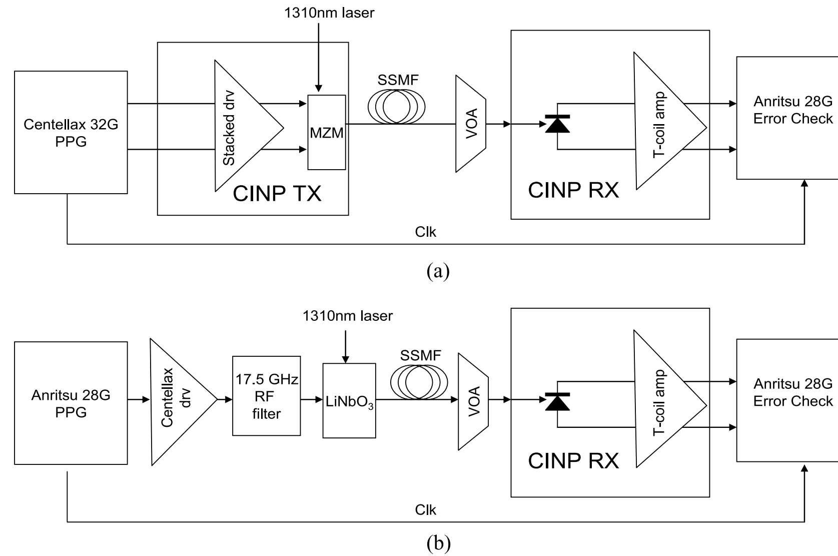


Fig. 8. (a) Schematic of CMOS9WG TX to CMOS9WG RX link, (b) schematic of reference-$LiNbO_3$-TX to CMOS9WG-RX link.

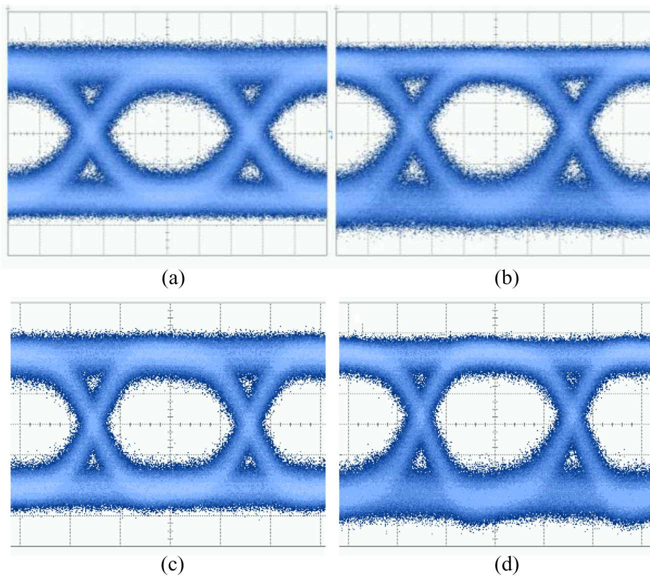


Fig. 9. (a) 16 Gb/s data port electrical eye from the CMOS9WG-TX/CMOS9WG-RX link at $\sim 1 \times 10^{-12}$ BER with $V_{DD} = 1.5$ V and $V_{DD2} = 3.0$ V. (b) 16 Gb/s data-bar port electrical eye from the 16 Gb/s CMOS9WG-TX/CMOS9WG-RX link at $\sim 1 \times 10^{-12}$ BER. (c) 16 Gb/s data port electrical eye from the reference-$LiNbO_3$/CMOS9WG-RX link at $\sim 1 \times 10^{-12}$ BER. (d) 16 Gb/s data-bar port electrical eye from the reference-$LiNbO_3$/CMOS9WG-RX link at $\sim 1 \times 10^{-12}$ BER.

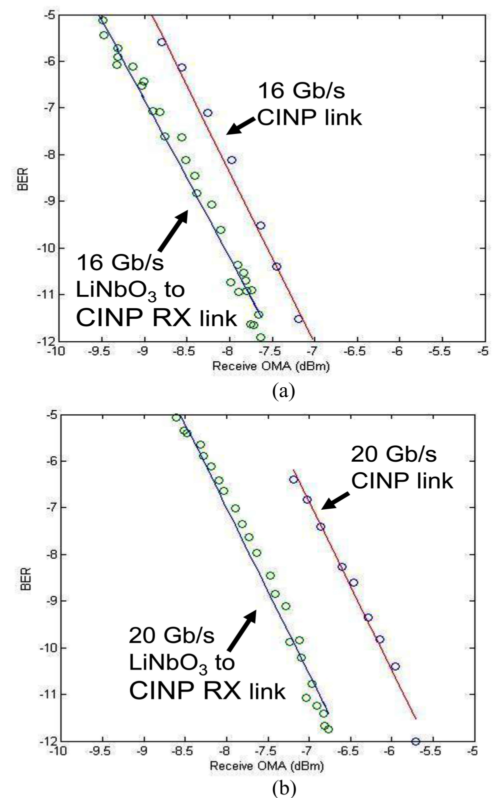


Fig. 10. (a) 16 Gb/s sensitivity curves for the CMOS9WG-TX/CMOS9WG-RX link and the reference-$LiNbO_3$-TX/CMOS9WG-RX link. (b) 20 Gb/s sensitivity curves for the CMOS9WG-TX/CMOS9WG-RX link and the reference-$LiNbO_3$-TX/CMOS9WG-RX link.

eye from the $LiNbO_3$-TX/CMOS9WG-RX link. The sensitivity curve with a $2^{31} - 1$ PRBS for the CMOS9WG link at 20 Gb/s is shown in Fig. 10(b). Also shown in Fig. 10(b) is a sensitivity curve for the $LiNbO_3$ based TX linked to the CMOS9WG RX. At 20 Gb/s the CMOS9WG link required -5.6 dBm OMA for a 1×10^{-12} BER, whereas the $LiNbO_3$ TX and CMOS9WG RX link required an OMA of -6.6 dBm. Therefore, the CMOS9WG TX showed 1.0 dB penalty compared to the 25 Gb/s $LiNbO_3$ TX at 20 Gb/s.

VII. TX Power Consumption Discussion

A 16 Gb/s current-mode CMOS TX delivering 0.8 V_{pp} drive is estimated to use approximately 100 mW of power, based on simulations using SOI CMOS models correlated to early hard-

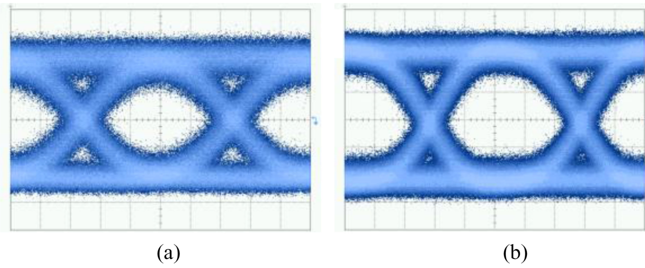


Fig. 11. (a) 20 Gb/s data port electrical eye from the CMOS9WG-TX/CMOS9WG-RX link. (b) 20 Gb/s data port electrical eye from the reference-$LiNbO_3$/CMOS9WG-RX link.

ware. In comparison, the 16 Gb/s stacked voltage-mode CMOS TX uses 165 mW of power while delivering 1.6 V_{pp} drive. The stacked voltage-mode CMOS TX reduces the required input laser power by 2.6 dB, but requires an additional 65 mW of power to supply the stacked voltage-mode TX CMOS. Therefore, if the reduction in required laser power is equal to or greater than 65 mW, the stacked voltage-mode CMOS TX design will offer a more efficient system solution in terms of power performance. The change in relative laser power consumption for an uncooled transceiver is estimated by assuming a ~10% wall plug efficiency at a maximum operating temperature of ~85 °C [54]. Therefore, a change in laser electrical power consumption of 65 mW equates to ~6.5 mW optical output power. If we then scale this 6.5 mW to be 2.6 dB of the total optical power required for a current-mode CMOS TX link, then we find the threshold for "power consumption neutrality" happens when the current-mode CMOS TX link needs ~14.5 mW or ~11.6 dBm of optical power at the TX input. For comparison, a 15% laser wall plug efficiency has "power consumption neutrality" when the current-mode CMOS TX link requires ~22 mW of input optical power.

There are many considerations that dictate the required laser power for a given link, including optical input and output coupling efficiency to the silicon photonic chip, whether polarization diversity, wavelength division multiplexing, or power splitting components are required, and what the receiver sensitivity and link budget will be. A more detailed discussion of the laser power required for a given link configuration is beyond the scope of this manuscript. However, we have outlined the conditions under which power consumption neutrality exists between the current-mode and stacked voltage-mode CMOS TX designs and so the reader can apply specific link requirements to consider which solution may be best for a given application.

VIII. Conclusion

We have demonstrated a 16 Gb/s monolithic TX manufactured in the IBM CMOS9WG technology node. We have also demonstrated a 20 Gb/s link between a monolithic TX and separate monolithic RX manufactured in the IBM CMOS9WG technology node. The TX showed a 0.5 dB OMA penalty as compared to a 25 Gb/s $LiNbO_3$ TX at 16 Gb/s operation, and a 1 dB penalty at 20 Gb/s. We note that the CMOS circuits demonstrated here were designed using a PDK for a 90 nm bulk CMOS technology node, in which the device models were not centered for the photonics-enabled SOI substrates on which the circuits were fabricated. Improved performance is expected from alternate monolithic circuits currently under fabrication, which have been designed with hardware-correlated models. The 20 Gb/s performance limitations in this link are solely due to the TX, which was specifically designed for 16 Gb/s operation. Our results show that unamplified single-mode optical links at 16 Gb/s and beyond are well within the capabilities of the IBM CMOS9WG technology, which could enable low-cost large-scale deployment of these optical data links.

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