Ultra-Compact Silicon Photonic 512 × 512 25 GHz Arrayed Waveguide Grating Router

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***Abstract*—This paper discusses design, fabrication, and characterization of a 512 × 512 arrayed waveguide grating router (AWGR) with a channel spacing of 25 GHz. The dimensions of the AWGR is 16 mm × 11 mm and is fabricated on a 250 nm silicon-on-insulator platform. The measured channel crosstalk is approximately −4 dB without any compensation for the phase errors in the arrayed waveguides. The AWGR spectrum in the arrayed waveguide grating arms were characterized by using an optical vector network analyzer. Fabrication details of obtaining low loss silicon ridge waveguides are also discussed.**

***Index Terms*—Integrated optical devices, waveguide filters, optical interconnects, data centers, wavelength-division-multiplexing (WDM).**

I. Introduction

THERE has been extensive research on silicon photonics as a promising future technology to meet the demands of high-capacity, energy-efficient, and cost-effective on-chip communications [1], [2]. In most applications, it is widely recognized that wavelength-division-multiplexing (WDM) techniques are critical in achieving high aggregate bandwidth for optical communications [3], [4]. In the WDM scheme, multiple sources are modulated and encoded to carry optical signals [5], [6]. The data rate for each channel is limited by the modulations speed, however the total bandwidth is scaled by the wavelength number (channels) used in the optical communication system via the arrayed waveguide grating (AWG) [5], [7]. Typically the channel count (spectral resolution) of an AWG can be increased by increasing the interference order of the grating or the number of arrayed waveguides and so therefore, AWGs have been used not only for WDM applications, but optical sensing [8], [9] and optical spectrometers [10] as well. Significant work has been done to develop high-performance AWGs based on a number of various material platforms such as buried InP/InGaAsP ridge waveguides [3], [4], [11]–[13], silicon-on-insulator (SOI) ridge waveguides [14], SOI nanowires [15]–[19], silica-on-Si buried waveguides [20]–[22], polymer waveguides [23], and nano-core Si_3N_4 waveguides [5], [7], [24]. Silica AWGs have reached commercialization owing to its high performance; however, the bending radius is usually very large because of its low index-contrast (∼1.5%) [25] compared to SOI (>40%). For this reason, high density integration on a small footprint is problematic. SOI-nanowires have an ultra-high index contrast, which enable several tens of micron-scale bending radius to be implemented on-chip. However, the drawback of SOI-nanowires are the phase-errors that cause channel crosstalk degradation and on-chip losses. On the other hand, Dai *et al.* have demonstrated a low loss Si_3N_4 16 channel-200 GHz AWG with a reported loss of 0.03 dB/cm for a 2 mm bend radius, and we have demonstrated high-contrast 40 channel-100 GHz AWG based on silicon rib waveguides on SOI [26].

TABLE I
Brief Survey of State-of-the-Art High Resolution AWG

AWG Device Type	Channel spacing [GHz]	Channel number [#]	Bend radius [μm]	Channel cross talk [dB]
Si-Wire [10]	25	50	-	∼-7
Si-Wire [18]	100	4	-	∼-9
Si-Wire [16]	200	16	4	∼-9
Si-Rib [this work]	25	512	85	∼-4
Silica [21]	25	400	2000	∼-25
Silica PEG [34]	100	64	-	-32
Si-Rib [14]	100	40	400	-15
Si-Rib [35]	200	32	10	-18
Silica [36]	50	64	-	-31
InP/InGaAsP [4]	10	100	500	-17

Aside from WDM communications, the unique wavelength routing characteristics of arrayed waveguide grating routers (AWGRs) have been proposed and demonstrated as a viable optical interconnect architecture for future high-performance-computing (HPC) due to its wavelength parallelism, dense interconnectivity, and all-to-all connectivity [27]–[31]. HPC architectures based on AWGR include LIONS (formally DOS) [32], Petabit, and IRIS [33] have shown that limiting factors that prevent such systems from being deployed on a large scale is the port count on a single AWGR [27].

In this work, we design, fabricate, and demonstrate a high port count 512 × 512 AWGR on a SOI material platform. First, we present AWGR based design parameters. Detailed fabrication steps are discussed to realize low-loss silicon waveguides followed by experiments. Table I shows the current state-of-the-art high resolution AWGs on various material platforms.

II. AWG Fundamental Concepts and Design

The theory of AWG can be found in [37]–[39] and is reviewed here to define parameters used in designs later in this paper. As Fig. 1 illustrates, the AWG consists of input and

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output waveguides, two free-propagation slab regions, and arrayed waveguides where each neighboring waveguide have a constant path length difference of ΔL. The input light is launched into the first slab region from the left where the beam diffracts and excites the arrayed waveguides. After traveling though the arrayed waveguides, the light beam constructively interferes at a particular focal point in the second slab region. The location of the focal points depend on the signal wavelength λ_n due to the relative phase delay in each arrayed waveguide [37], [38].

After traversing the arrayed waveguide arms, the signal in each arm should theoretically acquire a constant linear phase increment from the adjacent waveguide by $\Delta L/\lambda$. The path length difference of two adjacent light beams in the arrayed waveguide arms must be an integer multiple of 2π for constructive interference at the output slab region location denoted as x. This interference condition is given by [37], [38]:

$$\begin{aligned}&\beta_s(\lambda_0)\left(f_1-\frac{d_1x_1}{2f_1}\right)+\beta_c(\lambda_0)\left[L_c+(i-1)\Delta L\right]\\&+\beta_s(\lambda_0)\left(f+\frac{dx}{2f}\right)=\beta_s(\lambda_0)\left(f_1+\frac{d_1x_1}{2f_1}\right)\\&+\beta_c(\lambda_0)\left[L_c+(i-1)\Delta L\right]+\beta_s(\lambda_0)\left(f-\frac{dx}{2f}\right)-2m\pi\end{aligned}\tag{1}$$

where β_s is the propagation constant in the slab region, β_c is the propagation constant in the arrayed waveguide arms, λ_0 is the center wavelength, f is the radius of curvature in the slab region, L_c is the minimum length of the arrayed waveguide arm, and m is an integer. The phase matching condition can further be reduced as follows [38]:

$$\beta_s(\lambda_0)\frac{d_1x_1}{f_1}-\beta_s(\lambda_0)\frac{dx}{f}+\beta_c(\lambda_0)\Delta L=2m\pi.\tag{2}$$

The relationship between the light input position at x_1 and x is such that:

$$\frac{d_1x_1}{f_1}=\frac{dx}{f}\tag{3}$$

when the phase term $\beta_c(\lambda_0)\Delta L=2m\pi$ and the center wavelength:

$$\lambda_0=\frac{n_c\Delta L}{m}.\tag{4}$$

Dispersion at each location of the second slab at x is found by differentiating (2) and results in the following [37]:

$$\frac{\Delta x}{\Delta\lambda}=-\frac{N_cf\Delta L}{n_sd\lambda_0}\tag{5}$$

where n_s is the effective index of the slab and $N_c=n_c-\lambda(dn_c/d\lambda)$ is the group index of the effective index of the arrayed waveguide arm. Similarly, the dispersion at the input side of the first slab region x_1 is given as [37]:

$$\frac{\Delta x_1}{\Delta\lambda}=-\frac{N_cf_1\Delta L}{n_sd_1\lambda_0}.\tag{6}$$

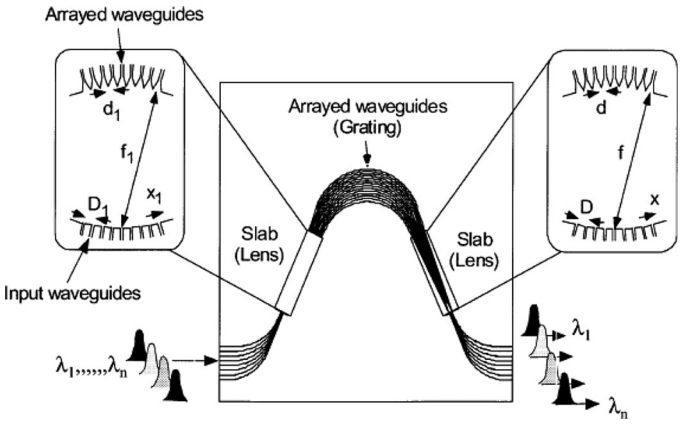

Fig. 1. Schematic of N×N AWGR operation [38].

The wavelength spacing at the input and output regions are as follows [37]:

$$\Delta\lambda_{\text{out}}=\frac{n_sdD\lambda_0}{N_cf\Delta L}\tag{7}$$

$$\Delta\lambda_{\text{in}}=\frac{n_sd_1D_1\lambda_0}{N_cf_1\Delta L}.\tag{8}$$

As a result, the path length difference between the adjacent arrayed waveguide arms can be calculated as [37]:

$$\Delta L=\frac{n_sdD\lambda_0}{N_cf\Delta L}.\tag{9}$$

The free spectral range (FSR) of the AWG between the mth and $(m+1)$th beams is thus:

$$X_{\text{FSR}}=x_m-x_{m+1}=\frac{\lambda_0f}{n_sd}.\tag{10}$$

The amount of available wavelength channels can therefore be determined by dividing the FSR value by the output waveguide separation D and is given as [37], [38]:

$$N_{\text{ch}}=\frac{X_{\text{FSR}}}{D}=\frac{\lambda_0f}{n_sdD}.\tag{11}$$

However, high-resolution AWGs on SOI require very long lengths such that any slight non-uniformity in the waveguide refractive index or dimension due to fabrication, will result in non-uniformity of the propagation constant for the different arms [22], [40], [41]. This in turn, induces non-uniform phase distortions at the output slab region known as phase errors. The phase errors cause de-focusing of a clean focal point at the output slab region and they are the main source of channel crosstalk [4], [16], [18], [42], [43].

The 512 × 512 25 GHz AWGR design is outlined in Table II above. The device structure uses a SOI layer structure with a 250 nm thick top silicon layer and a 2 μm buried oxide (BOX) which results in a total chip footprint of 11 mm × 16 mm. The input, output and arrayed waveguide gratings are partially etched with an etch depth of 100 nm. Fig. 2 illustrates the waveguide structure and optical mode field.

AWG design starts with the system parameters, including number of channels N_{ch}, center wavelength λ_0, and channel

TABLE II
SUMMARY OF 512 × 512 AWGR DESIGN PARAMETERS

Design Parameters	Symbol	Design values
Number of channels	N_{ch}	512
Center wavelength	λ_0	1.55 μm
Channel spacing	$\Delta\lambda$	0.2 nm
Number of arms	N_{scr}	1200
Arrayed WG pitch	d	450 nm
Arrayed WG width	w	950 nm
Input WG pitch at slab region	D	450 nm
Input WG width at slab region	w_{in}	1.55 μm
Input/output WG width	W_c	3 μm
Path length difference	ΔL	6.011 μm
Grating order	m	11
AWG slab(lens) radius	f	2796.531 μm
Bend radius	R_{min}	85 μm
Waveguide height	RH	250 nm
Waveguide slab height	SH	150 nm
Buried oxide (BOX) height	BH	2 μm

*WG=waveguide.

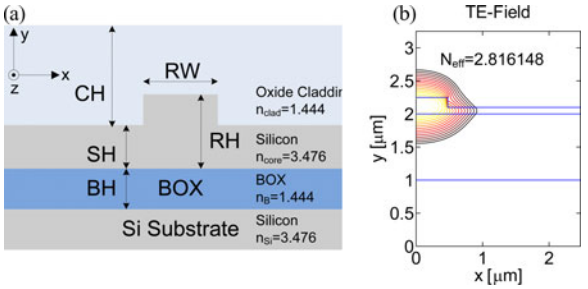

Fig. 2. (a) SOI waveguide cross-section and associated parameters. (b) Half-field simulation of optical mode in arrayed waveguide arm.

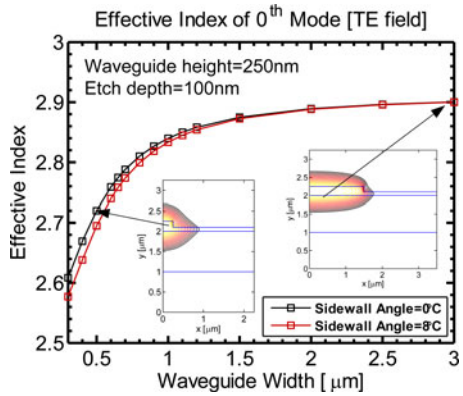

Fig. 3. Simulated TE-polarized mode of a SOI ridge waveguide and associated effective index versus waveguide width versus sidewall angle from etching.

spacing $\Delta\lambda$. Based on the limits in SOI waveguide fabrication, we determine the waveguide height RH, waveguide slab height SH, BOX height BH, arrayed waveguide pitch d and input/output waveguide pitch D. Then, we calculate the path length difference ΔL and radius of curvature in the slab region f, using (9) and (11).

The optical mode simulations are performed with a full-vectorial-eigenmode solver that computes the complex propagation constant that includes the propagation loss associated

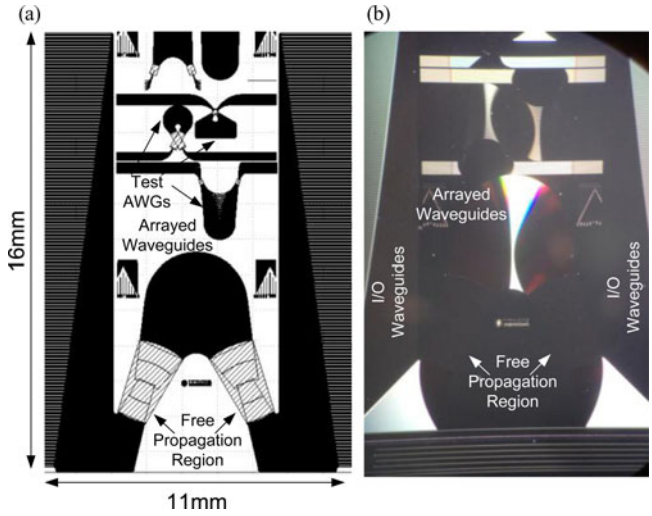

Fig. 4. (a) Mask layout of a single 512 × 512 25-GHz AWGR device. (b) Fabricated device on SOI with footprint of 11 mm × 16 mm.

TABLE III
HBR PLASMA BASED TCP ETCH RECIPE

Step	Oxide etch step	Silicon etch step	Si overetch step
Pressure [mtorr]	13	12	80
TCP RF [watt]	200	300	100
Bias RF [watt]	40	150	150
Electrode gap [cm]	6	6	6
HBr [sccm]	0	150	100
CF_4 [sccm]	100	0	0
He clamp [sccm]	4	4	4
Time [sec]	10	vary	10

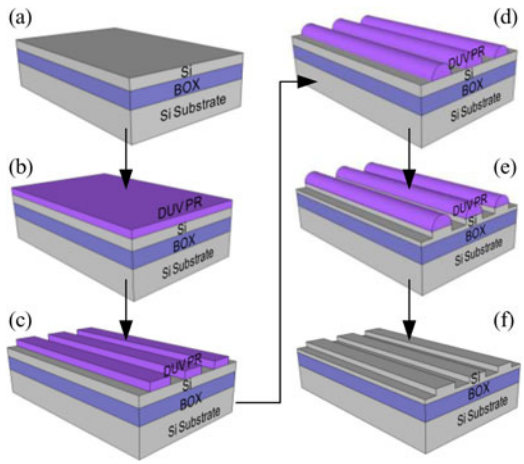

Fig. 5. Generalized fabrication process flow for low-loss silicon waveguides. (a) Starting 6″ SOI wafer, (b) DUV photoresist coating, (c) DUV lithography, (d) photoresist reflow, (e) waveguide RIE dry etch, and (f) DUV photoresist removal.

with radiation into the silicon substrate. Fig. 3 shows the simulated mode profiles that covers and range of widths that are used in the AWGR design. The simulations also examine the realistic case of effective index dependence on sidewall angle due to our plasma dry etching. This will be discussed in the fabrication section. Fig. 4 shows the waveguide mask

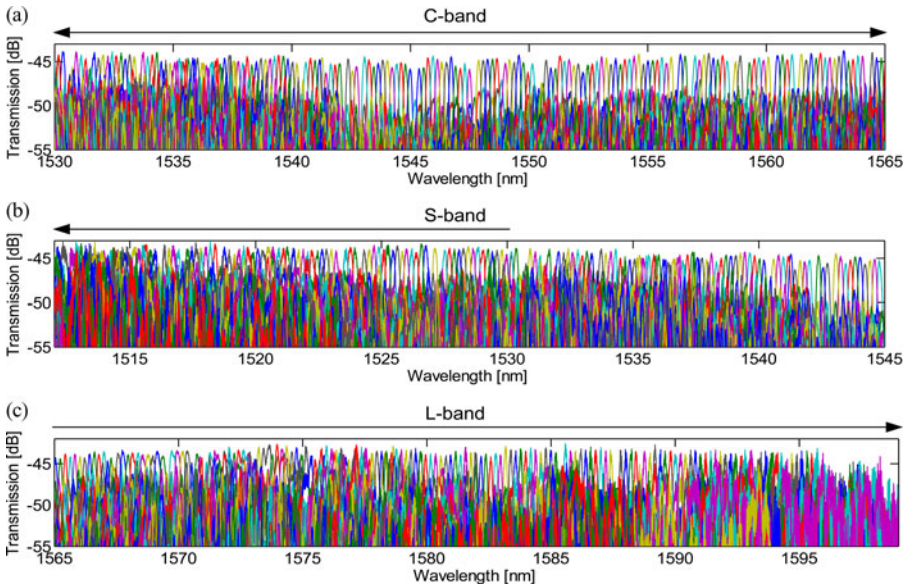

Fig. 6. De-multiplexing properties of 512 × 512 25 GHz AWGR (a) in C-band, (b) in S-band, and (c) in L-band.

layout of the 512 × 512 AWGR device alongside the fabricated chip. Comparing to orthogonal type layout, where bend radius is kept fixed and incremental lengths in the array are induced in the straight sections only, we use a "Smit" type layout so that the bends are also part of path length difference. Such design helps us reduce the device dimension for a high channel count AWGR.

III. Fabrication

Fabrication begins with a 6″ SOI wafer from SOITEC which consists of a 250 nm thick top silicon layer and a 2 μm BOX. The wafer goes through initial RCA-1 and RCA-2 cleaning and is then coated with 900 nm of Rohm Haas UV210-0.6 photoresist, soft-baked at 130 °C for 60 s and then exposed with a ASML DUV stepper using a 248 nm-KrF light source at 18 mJ/cm^2 with appropriate focus correction. The sample goes through a 130 °C post-exposure bake for 1 min and then developed in Rohm Haas MF26A developer for 60 s at 20 °C. In order to reduce the photoresist roughness due to the standing wave interference from the DUV exposure, we employ photoresist reflow at 156 °C for 120 s on a hotplate. Next, a LAM TCP plasma etcher is used to etch the silicon with an optimized hydrogen bromide (HBr) recipe as shown in Table III. After plasma dry etching, the photoresist is removed using oxygen plasma at a pressure of 3.75 torr, RF power = 400 W at a chuck temperature of 250 °C for 120 s. The wafer then goes through a complete RCA-1 and RCA-2 cleaning again. Finally, dry thermal oxidation is performed to further reduce sidewall roughness in a horizontal furnace at 1000 °C. The wafers are then dipped in a HF : H_2O (1:25) solution to remove thermal oxidation. Next, the wafer is coated with a 1 μm thick low temperature LPCVD oxide, and the samples are then cleaved and the input and output facets are polished to a mirror finish for subsequent optical testing.

Fig. 5 shows the generalized fabrication flow discussed. Near isotropic etching was achieved by using a pure HBr etch which reduces the passivation layer by exposing the silicon atoms to Br radicals [44], [45].

IV. Experimental Results

The spectral response of the fabricated devices were characterized with an optical vector network analyzer (OVNA). The OVNA is capable of high spectral resolution and uses a continuously swept mode-hop-free laser to measure transmission intensity of the AWG [46]. We first evaluated the waveguide loss for a width of 750 nm based on the Fabry–Perot-loss equation [47], and it was determined to be 2.78 dB/cm. The waveguide loss is on the high side compared to e-beam-based resist (hydrogen silsesquioxane) fabrication which yields 0.92 ± 0.14 dB/cm [48]. However, the waveguide loss is low enough to observe the transfer function of various devices. The facet power reflection was determined to be 31% based on 3D-FDTD simulations. The estimated coupling loss at each facet is calculated to be 11.3 dB. Fig. 6 shows the measured spectrum across the 512 channels. The measured channel is spacing is 25 GHz with an estimated channel cross-talk of approximately −4 dB. The measurement was done at input port #323, close to the center of all AWG inputs. We believe that the phase errors caused by accumulation of the non-uniformity in the effective refractive index in the arrayed waveguides due to fabrication tolerance is the source of major phase errors giving rise to the relatively high channel cross-talk [10], [18], [41]. We believe that channel cross-talk performance can be further improved by optimizing our fabrication process through oxide sidewall smoothening [49].

V. Crosstalk Versus Phase Errors

The challenge of high resolution and high channel count silicon photonic AWGRs is phase errors and resulting crosstalk. Especially in high contrast waveguides like silicon photonic waveguides, even a small amount of fabrication tolerance

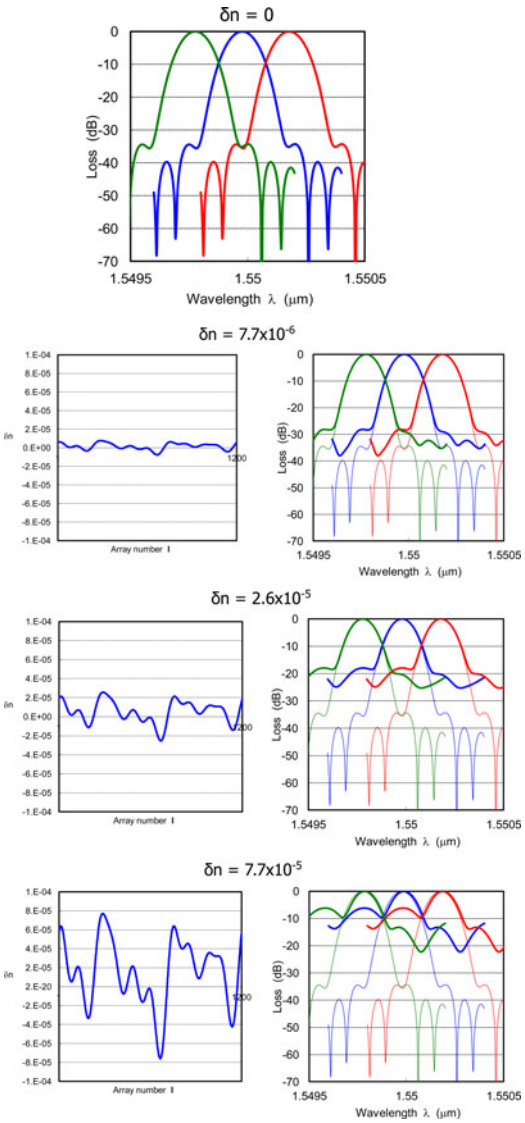

Fig. 7. Simulation of the relation between phase errors and crosstalk characteristics.

induced by waveguide thickness or width variations will give rise to relatively large effective index variations and large phase errors compared to low contrast waveguides like doped silica waveguides [22], [37], [50]. Fig. 7 shows calculated passband spectra for various root-mean-square variations of the effective index δn. At $\delta n = 7.7 \times 10^{-5}$ (approximately 22 parts per million) the contrast of the passband has reduced to below 10 dB due to significant increase in crosstalk.

VI. Conclusion

This paper demonstrates the design, fabrication, and optical characterization of 512×512 SOI AWGR with 25 GHz channel spacing. The overall device footprint is 11 mm $\times$ 16 mm. We believe, this is the highest channel count SOI AWGR reported so far alongside with the highest resolution. The measured channel crosstalk was approximately -4 dB. Although the present device has high channel crosstalk, we believe this can be further improved with optimized fabrication process to lower the phase errors derived from the waveguide sidewall roughness.

We have also presented a fabrication process to realize low-loss silicon waveguides with a measured loss value of 2.78 dB/cm for a silicon waveguide height and width of 250 nm and 750 nm respectively. With further improvement on high resolution and high channel-count AWGRs, chip-scale HPC systems can be realized.

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