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Double zinc diffusion optimization for charge persistence reduction in InGaAs/InP SPADs

Fabio Telesca, Fabio Signorelli and Alberto Tosi, *Member, IEEE*

***Abstract*—We present an in-depth characterization of the impact of the double zinc diffusion 2D profile on the charge persistence effect in InGaAs/InP Single-Photon Avalanche Diodes (SPADs). Charge persistence might be mitigated by increasing the operating temperature, so as to reduce minority carriers' lifetime, as well as by increasing the number of grading layers. However, the first approach leads to higher dark count rate due to stronger thermal generation of dark carriers, while the latter is technologically challenging. We show that, by adjusting the depth and radius of the shallow zinc diffusion, the electric field profile in the InGaAs layer outside the active area can be optimized in order to effectively mitigate charge persistence, achieving also its complete suppression in specific structures. Our study is based on both TCAD simulations and experimental measurements of different SPADs, whose only difference is in the geometrical shallow diffusion parameters.**

***Index Terms*—charge persistence, InGaAs/InP, near-infrared detector, Single-Photon Avalanche Diode, SPAD, single photon detector, photon counting**

I. INTRODUCTION

THE ability to detect single-photons in the near-infrared range has been gaining a lot of interest in the recent years, as it is the enabling technology for many applications, such as quantum communication [1], quantum cryptography [2] and quantum optics experiments [3], eye-safe light detection and ranging (LIDAR) [4] and near-infrared spectroscopy (NIRS) [5]. Given their advantages in terms of cost, size and ease of use, $In_{0.53}Ga_{0.47}As$/InP single-photon avalanche diodes (SPADs) are among the best near-infrared (NIR) single-photon detectors for such applications.

InGaAs/InP SPADs are usually operated in gated mode at low temperature (typically, < 250 K), to reduce the primary noise contribution, i.e., thermal carrier generation in the InGaAs region. However, lower temperature operation worsens afterpulsing probability (which ultimately limits the maximum photon count rate), as well as an often-overlooked phenomenon called *charge persistence*. Charge persistence is a source of noise originating from holes thermally- or photo-generated inside the InGaAs absorption layer at the periphery of the active area and that diffuse towards the central active area [6]. In gated mode operation, holes generated in the InGaAs layer are less likely to cross the hetero-barrier during the off time (T_{OFF}), especially in the peripheral region outside the active area, since the lower electric field is linked to a lower tunneling probability. Therefore, a longer T_{OFF} leads to a larger number of holes accumulating at the hetero-interface: in the subsequent ON interval (T_{ON}, when the SPAD bias is beyond the breakdown level), some of the trapped holes may tunnel in correspondence of the active area (where the electric field is higher) and reach the multiplication region, thus igniting spurious avalanches.

Charge persistence is highly undesirable, and it cannot be exploited as a charge-focusing effect for extending the active area by collecting the photons absorbed outside the central active area, as it is based on the slow diffusion charge transport, thus leading to tails in the instrument response function that are in the nanosecond range. Moreover, charge persistence of thermally-generated carriers adds up to DCR.

Such detrimental effect can be mitigated by either increasing the electric field at the heterointerface (with the drawback of increasing field-assisted carrier generation) or by incrementing the number of grading layers to facilitate tunneling even with a lower electric field (although increasing fabrication complexity).

In this paper, we investigate the effects of charge persistence on the main performance metrics of an InGaAs/InP SPAD (photon detection efficiency – PDE, dark count rate – DCR, and instrument response function) and describe how it can be mitigated by tailoring the design of the double zinc diffusion 2D profile.

II. DEVICE STRUCTURE

The devices under tests are InGaAs/InP SPADs designed at Politecnico di Milano, but different works described the charge persistence effect in other similar InGaAs/InP SPADs designed and fabricated by other groups [6] - [8]. Our front-illuminated SPADs have the typical separate absorption, grading, charge and multiplication (SAGCM) structure, as described in [9] and shown in Fig. 1. The SPAD active area is

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defined by p^+ doping the cap InP layer with a double zinc diffusion.

To assess the effect of the shape of the double zinc diffusion on charge persistence, we tested SPADs with 25 µm active area diameter taken from two different wafers (which will be called wafer W1 and wafer W2 hereafter), grown in the same batch with identical epitaxial structures and with the same deep diffusion depth (d_D), but with wafer W2 having a shallow diffusion 100 nm deeper than that of wafer W1 (i.e., $d_{S2} = d_{S1} + 100$ nm). As a reference, this difference is less than 50% of d_D - d_{S1}. The two d_S values were chosen after an extensive modeling and simulation work aimed at finding the upper limit of the shallow diffusion depth. A different d_S is obtained by only varying the duration of the zinc diffusion process, while leaving all other process parameters unchanged. This assures that d_S is the only dimension affected, while leaving the double zinc diffusion profile unaltered.

In a first comparison, we tested SPADs with a shallow diffusion radius 7 µm larger than the deep diffusion radius, i.e., $\Delta r = 7$ µm. Then, in order to further investigate the effect of the shallow diffusion radius on charge persistence, we also tested devices with $\Delta r = 4$ µm and $\Delta r = 10$ µm taken from wafer W2, whose devices show lower charge persistence.

III. TCAD Simulations

The main purpose of the shallow zinc diffusion is to limit premature edge breakdown, so that DCR is not increased. Moreover, the double zinc diffusion profile affects the uniformity of the bidimensional avalanche triggering probability across the active area: a uniform avalanche probability distribution positively impacts the instrument response function, PDE and noise. Using Synopsys Sentaurus [10] TCAD simulator, we determined that the minimum radius difference required to suppress premature edge breakdown is $\Delta r = 4$ µm at $V_{EX} = 5$ V (where V_{EX} is the excess bias voltage, i.e., the difference between the SPAD voltage and its breakdown level), which is the target excess bias value for these detectors. If the radius of the shallow diffusion is further increased, there are no significant changes in the avalanche triggering probability distribution (as an example, Fig. 2 shows simulation results for the wafer W2 SPADs with $\Delta r = 4$ µm and 10 µm). A similar observation can be made about the electric field: no major differences are visible in the active areas of the two devices. However, since the shallow diffusion of the SPAD with $\Delta r = 10$ µm spans over a much wider area, the depleted region extends more outside the active one, therefore the region around the active area where electric field is non-negligible is also increased (see Fig. 3).

Regarding d_S, there are no substantial differences between wafers W1 and W2 in of the simulated avalanche triggering probability distribution, but the deeper shallow diffusion of wafer W2 leads to a higher electric field in the InGaAs layer beneath, as is shown in Fig. 4, which reports a mono-dimensional plot of both parameters for both wafers along a

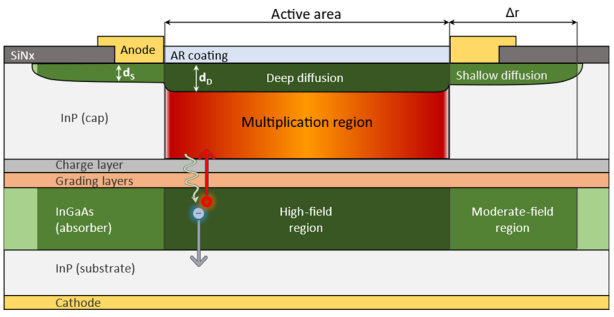

Fig. 1. Schematic representation of an InGaAs/InP SPAD with the separate absorption, grading, charge and multiplication (SAGCM) structure. Layers and regions are labelled in the figure, as well as other features such as the difference between deep and shallow diffusion radius (Δr) and the schematic distribution of electric field in the InGaAs layer: high in the active area, moderate beneath the shallow diffusion and negligible elsewhere.

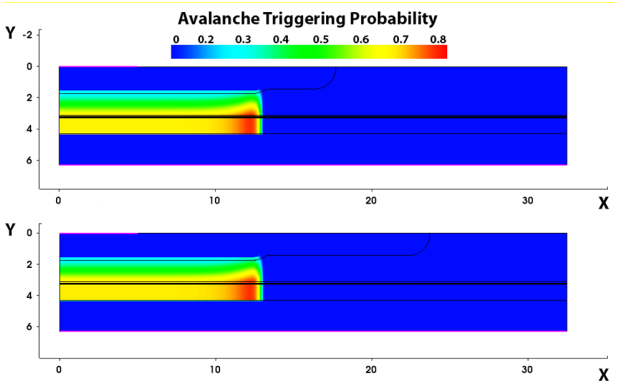

Fig. 2. TCAD simulation of avalanche triggering probability at $V_{EX} = 5$ V at 225 K for W2 SPADs with $\Delta r = 4$ µm (top) and $\Delta r = 10$ µm (bottom), showing the probability that a free carrier generated anywhere in the device may ignite a self-sustaining avalanche. Increasing the shallow diffusion radius above 4 µm has no further benefits in terms of active area confinement and uniformity.

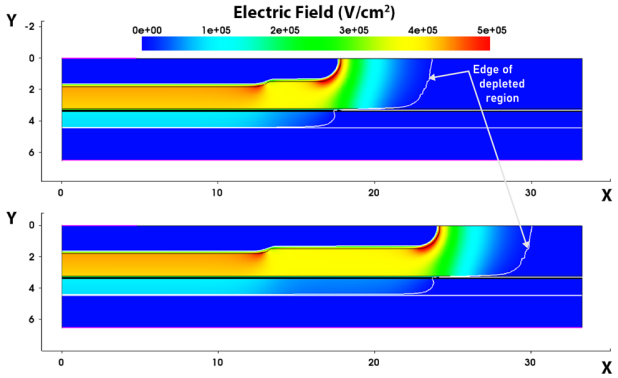

Fig. 3. TCAD simulations of electric field at $V_{EX} = 5$ V at 225 K for W2 SPADs with $\Delta r = 4$ µm (top) and $\Delta r = 10$ µm (bottom). The white line indicates the edge of the depleted region. The avalanche triggering probability (shown in **Fig. 2**) does not depend on the local peaks of the electric field, but rather on the overall electric field experienced by carriers along their path to the collecting contact.

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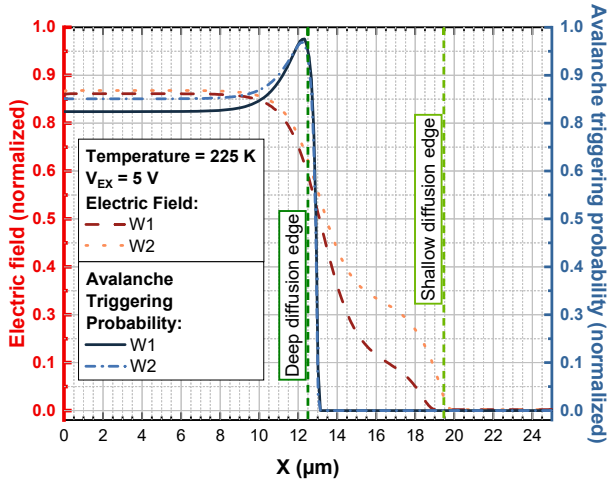

Fig. 4. Mono-dimensional plot of electric field (left Y axis) and avalanche triggering probability (right Y axis) along a horizontal cut at the interface between the first grading layer and the InGaAs layer, obtained by simulating a SPAD with $\Delta r = 7$ μm for both wafers W1 and W2. The avalanche triggering probability distribution is roughly unchanged between the two wafers, but the electric field below the shallow diffusion is about double for W2 with respect to W1, due to the larger d_{S2}.

horizontal cut at the interface between the first grading layer and the InGaAs layer. According to simulations, the upper limit to d_S is roughly d_{S2} + 100 nm: after that, the electric field below the shallow diffusion is so high that premature edge breakdown occurs below the shallow diffusion edge at $V_{EX} = 5$ V, thus blunting the vertical confinement of the device active area and causing a detrimental effect on noise (see Fig. 5). As a conservative choice, we decided to fabricate SPADs with d_{S2} that is 100 nm below the upper limit.

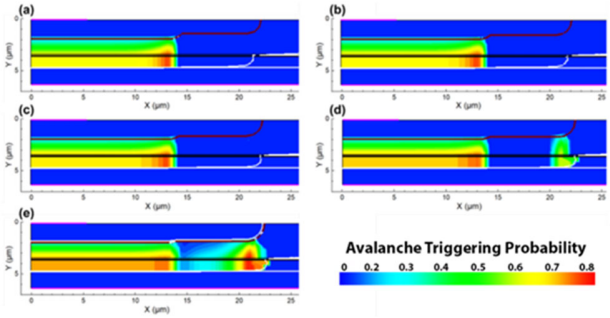

Fig. 5. Avalanche triggering probability with increasing depth of the shallow diffusion, from (a) to (e) (100 nm steps), at $V_{EX} = 5$ V. Wafers W1 and W2 are (b) and (c), respectively. Exact values are confidential.

Since there is no premature edge breakdown below the shallow diffusion of SPADs from wafer W2, we conclude that the higher electric field in the InGaAs layer of W2 is still below a value that would cause a DCR increase, but high enough to enhance tunneling in correspondence of the shallow diffusion and thus reduce output pulses due to charge persistence.

IV. Experimental Characterization

To experimentally characterize the impact of the double zinc diffusion profile on charge persistence and, subsequently, the main metrics of the SPAD, we performed measurements of PDE, DCR and instrument response function, at different temperatures and gating frequencies. For all the measurements here presented, the excess bias is $V_{EX} = 5$ V, which is the target excess bias for these detectors, but we experimentally observed the same trends also at $V_{EX} = 3$ V and $V_{EX} = 7$ V: the charge persistence effect is much stronger at $V_{EX} = 3$ V, while it is weaker at $V_{EX} = 7$ V, as a consequence of the overall lower and higher electric field, respectively.

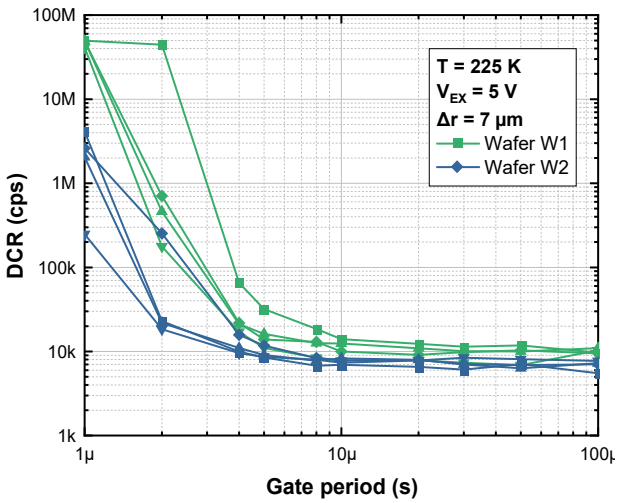

Fig. 6. Dependence of DCR on gate period for SPADs from wafers W1 and W2, both with $\Delta r = 7$ μm. The lower DCR of SPADs from W2 is traceable to a reduced impact of charge persistence thanks to the higher electric field beneath the shallow diffusion.

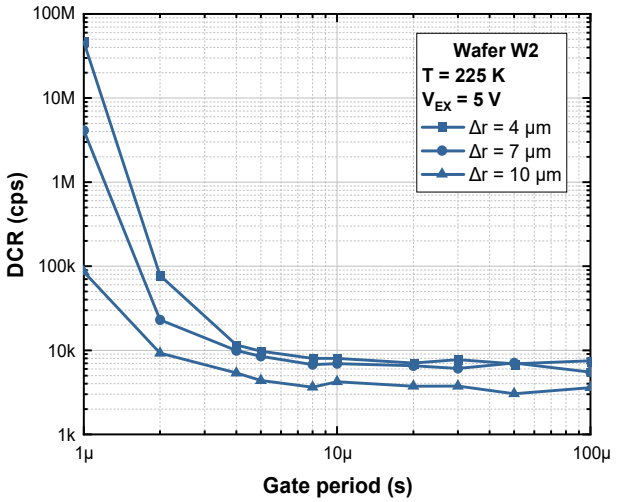

Fig. 7. Dependence of DCR on the gate period for SPADs with increasing Δr taken from wafer W2. The DCR decrease with a wider shallow diffusion further confirms the dependence of DCR on the electric field distribution below the shallow diffusion.

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A. Dark count rate vs. Gate period

To measure DCR, the SPADs were placed in a vacuum chamber and cooled down to 225 K. A square wave was fed to the cathode contact to drive the devices in gated mode, with a fixed ON time (i.e., T_{ON} = 50 ns) while continuously varying the gating period, so that T_{OFF} would vary as T_{OFF} = Gate period - T_{ON}. The device was DC biased 0.5 V below breakdown and the amplitude of the square wave was set to 5.5 V, so to have V_{EX} = 5 V.

For SPADs with Δr = 7 µm, results are shown in Fig. 6. The SPADs taken from W1 typically have a higher DCR with respect to those from W2 (10 kcps *vs.* 7 kcps). Given the almost identical avalanche triggering probability profile in the active area, we ruled out the possibility that the higher DCR of wafer W1 could be due to a higher tunneling generation in correspondence of the deep diffusion edge. On the other hand, the higher electric field beneath the shallow diffusion of W2 may be linked to a higher tunneling probability through the hetero-barrier of holes that, being thermally generated in the InGaAs layer, are sunk by the anode contact without crossing the multiplication region and, thus, not igniting an avalanche.

For shorter periods, DCR is dominated by afterpulsing, which causes a steep increase in the curve. Fig. 7 shows DCR measurements on SPADs with Δr = 4 µm, 7 µm, and 10 µm taken from wafer W2: the wider shallow diffusion is linked to lower DCR because the depleted region is wider and, consequently, holes have a higher probability of crossing the hetero-barrier without reaching the central active region.

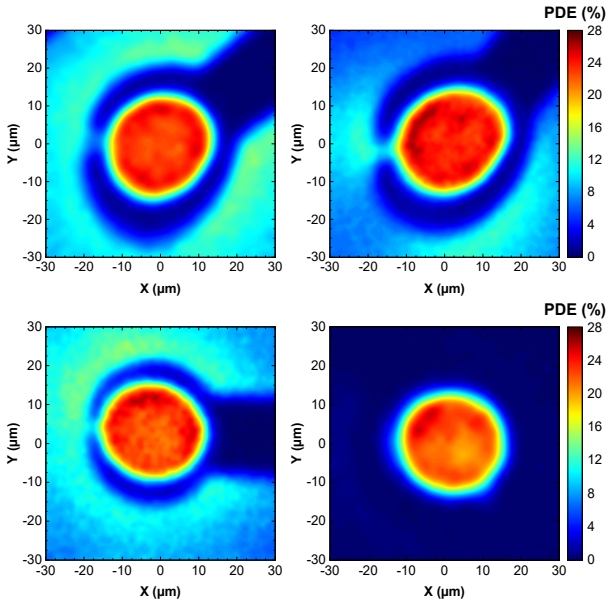

Fig. 8. PDE maps at V_{EX} = 5 V and T = 225 K, for SPADs with Δr = 7 µm taken from wafers W1 (top left) and W2 (top right), and for SPADs from wafer W2 with Δr = 4 µm (bottom left) and Δr = 10 µm (bottom right), measured with a 1550 nm CW laser. The probability of detecting photons absorbed outside the active area decreases (i.e., photogenerated carriers cross the hetero-barrier before reaching the active area) as the shallow diffusion is made deeper and wider.

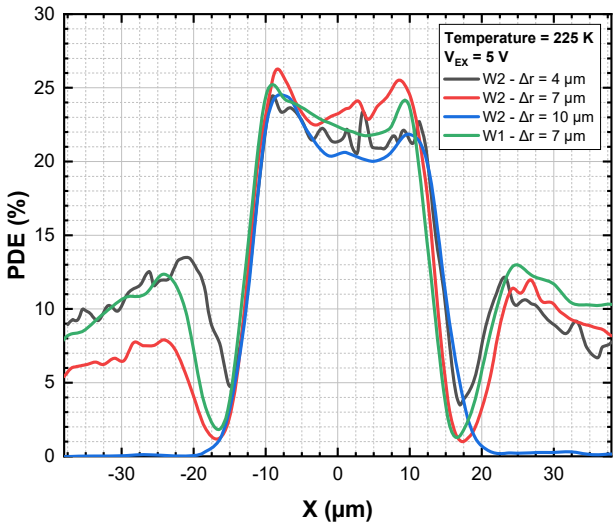

Fig. 9. PDE along diagonal cuts passing through the device center of the maps shown in **Fig. 8**.

B. *Photon detection efficiency at 1550 nm*

The photon detection efficiency maps at 1550 nm of SPADs from both wafers were measured by using a fiber-coupled CW laser and a calibrated photodiode to monitor the optical power. All devices were tested in the same operating conditions: cooled down to 225 K in a vacuum chamber and operated in gated mode with V_{EX} = 5 V, T_{ON} = 50 ns and T_{OFF} = 50 µs (which is long enough to rule-out afterpulsing). The vacuum chamber was placed on three micro-positioning axes that allowed to move it with 500 nm steps. The laser was focused on the SPAD with a collimator and a single lens in a ~5 µm spot, and the whole chip area was scanned by moving the chamber in the XY directions. Results are shown in Fig. 8.

For SPADs with the Δr = 7 µm from wafer W1 and W2, the PDE in the active area is similar, with an average value of 24% and local peaks of ~27% (first row in Fig. 8). For both SPADs, the probability of detecting a photon when the laser spot was focused outside the SPAD area is in the order of 10%, visible in the maps as a non-uniform cyan hue surrounding the device. The dark blue circle and diagonal segment are due to the shadows of the anode metals. Minor image distortions that are visible in some of the measurements are due to artifacts introduced by the motorized axes.

The main difference between the two wafers is that for wafer W1 the probability of detecting a photon absorbed outside the SPAD area is higher with respect to wafer W2, as can be also seen in the mono-dimensional plots along diagonal cuts shown in Fig. 9 (green and red curve, respectively). This shows that charge persistence is indeed stronger in wafer W1 than in wafer W2 and, given that the only difference between the two is d_S, conclusions of section III.A are confirmed.

Regarding SPADs with Δr = 4 µm and 10 µm from wafer W2, PDE in the active area is still similar for both devices (~ 23%), as shown in Fig. 8 and Fig. 9.

In the case of the Δr = 4 µm SPAD, PDE outside the active area is in the order of 10% up to ~ 35 µm away from the SPAD center. This shows that the effect of charge persistence

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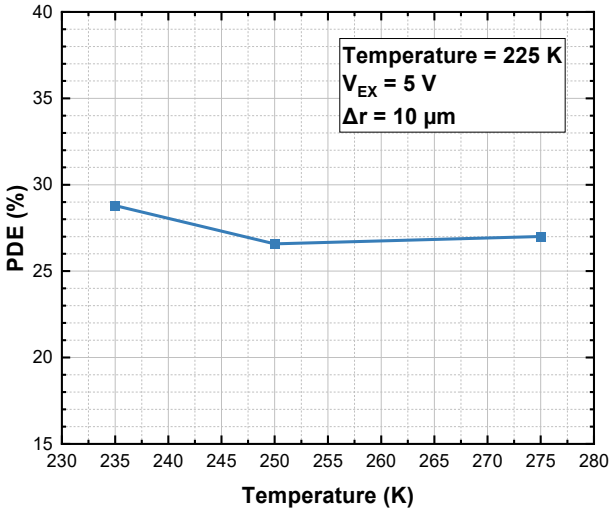

Fig. 10. PDE at 1550 nm estimated by flood-illuminating the SPAD with $\Delta r = 10$ μm from wafer W2. For temperatures below 20 K, charge persistence distorts PDE estimation.

is dominant, due to the small shallow diffusion diameter. On the other hand, PDE outside the SPAD area is greatly reduced when $\Delta r = 10$ μm, meaning that the wider shallow diffusion and, consequently, wider depleted region in the InGaAs layer, mitigates charge persistence.

We also measured the PDE of the SPAD with $\Delta r = 10$ μm by illuminating the whole die area with 1550 nm wavelength photons, at different temperatures. The PDE maps showed that the actual SPAD opening diameter is 27 μm rather than the nominal 25 μm, due to the fact that the metal opening is 2 μm wider than the deep diffusion mask, therefore the photon-sensing area was considered to be a 27 μm diameter circle. The PDE was measured by operating the SPAD in gated mode with a fixed $V_{EX} = 5$ V and changing the bias so that it was always 0.5 V below breakdown at each temperature. We found a PDE of ~26% at both 275 K and 250 K, while it increased to 29% at 235 K (see Fig. 10). It is known that, if the excess bias is kept constant (5 V in our measurements), the PDE at lower temperatures is higher, due to the decrease of the breakdown voltage with temperature which leads to the excess bias being a larger share of the total applied voltage. However, the reported increase in PDE is present only for low temperatures and it is too sharp to be ascribed to such effect. Moreover, it was not possible to perform a PDE measurement at 225 K: if we keep assuming the SPAD active area to be a 27 μm diameter circle, the measured PDE at 225 K was higher than 100%, which is meaningless. Our conclusion is that, at lower temperatures, the actual area where absorbed photons are detected is much wider than the nominal one due to charge persistence and, even at 225 K for the SPAD with $\Delta r = 10$ μm, although charge persistence is not dominant according to the measurements shown in Fig. 8, it is still too high to estimate PDE by flood-illuminating the detector.

On the other hand, for the SPAD with $\Delta r = 4$ μm it was not possible to measure PDE with flood-illumination at any temperature, since the effect of charge persistence is always dominant.

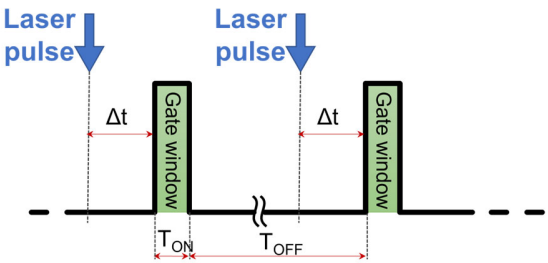

Fig. 11. Scheme for PDE measurements with a laser pulse reaching the device before the gate window.

D. PDE maps with pulsed laser before gate window

To better quantify the intensity of charge persistence in the SPADs from wafer W2, we acquired additional PDE maps, but with a pulsed 1550 nm laser focused on the SPAD chip surface and arriving at a given Δt time before the gate window, as exemplified by the scheme in Fig. 11. With such approach, we could estimate the percentage of photons absorbed outside the SPAD generating carriers that do not recombine before reaching the multiplication region. The measurements were performed at 225 K, with $V_{EX} = 5$ V.

Measurement results are shown in Fig. 12: the probability to detect a photon from a circular area up to 10 μm away for the SPAD with $\Delta r = 4$ μm is in the order of 3% with $\Delta t = 10$ ns, and it is still around 1% with $\Delta t = 50$ ns. We also noticed that the events resulting from charge persistence are often unevenly distributed in space, probably because they are closely related to local peaks in the electric field, which may depend on defects in the device. The maps in Fig. 12 suggest that most of the charge persistence effect is ascribable to

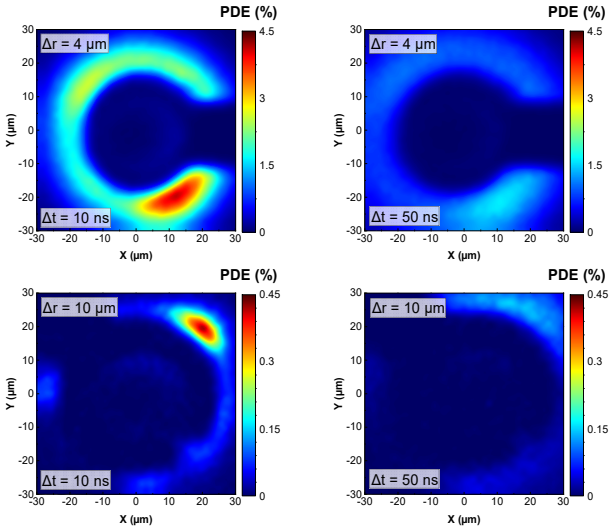

Fig. 12. PDE maps built by scanning a pulsed 1550 nm laser focused on the SPAD area at $\Delta t = 10$ ns (left column) and $\Delta t = 50$ ns (right column) before the gate window for SPADs from wafer W2 with $\Delta r = 4$ μm (top row) and 10 μm (bottom row). As Δr is increased, charge persistence is reduced, therefore photons absorbed before the gate window are less likely to be detected.

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carriers absorbed just before the gate window, but some events are still detected with $\Delta t = 50$ ns. On the other hand, for the SPAD with $\Delta r = 10$ µm, these probabilities drop by an order of magnitude, which is in line with what was shown in the bottom row of Fig. 8.

E. Instrument response function

Finally, the instrument response function of SPADs from wafer W2 was measured illuminating the whole die area with a 1550 nm pulsed laser.

The SPAD with $\Delta r = 10$ µm has a timing jitter (measured as full-width at half-maximum – FWHM – of the instrument response function) of 157 ps at 225 K, which increases slightly with temperature, up to 174 ps at 275 K (see Fig. 13). For the SPAD with $\Delta r = 4$ µm, a FWHM of 290 ps was measured at 225 K, and it raised to 391 ps at 275 K (see Fig. 14). Most of the increase of FWHM is due to the higher number of scattering phenomena occurring at higher temperature. Besides such FWHM variation, the main difference between the two devices is in the diffusion tail of the instrument response function: the SPAD with $\Delta r = 4$ µm shows a marked tail at 225 K, with a time constant in the order of several nanoseconds, which gradually decreases as the temperature rises. Such trend indicates that the tail is due to the slow diffusing carriers that give rise to charge persistence: at higher temperatures, the minority carrier lifetime swiftly decreases, leading to the reduction of the tail. Similarly, the instrument response function of the SPAD with $\Delta r = 10$ µm also has a tail at low temperature, although much less pronounced, meaning that charge persistence is much less important for this device, but still present. Additionally, such tail disappears at temperature above 240 K. These results confirm that it was possible to measure PDE for the SPAD with $\Delta r = 10$ µm for temperature above 250 K, while this was not the case for the other detector.

V. Conclusions

We characterized the dependence of charge persistence on shape and depth of the shallow zinc diffusion in InGaAs/InP SPADs operated in different conditions, by investigating how it affects the main parameters of a SPAD: DCR, PDE and instrument response function.

Specifically, we observed that charge persistence can be mitigated by designing a deeper and wider shallow diffusion, since both design choices result in a higher electric field in the InGaAs layer around the active area, thus increasing tunneling probability of holes diffusing from the surrounding region, allowing to drain them towards the anode before they reach the central active area, where they would trigger avalanches.

We conclude that, even without modifying the epitaxial structure of the device, charge persistence can be reduced with a design targeted for operating the detector at higher temperatures (namely, above 250 K) and with higher electric field in the absorption layer.

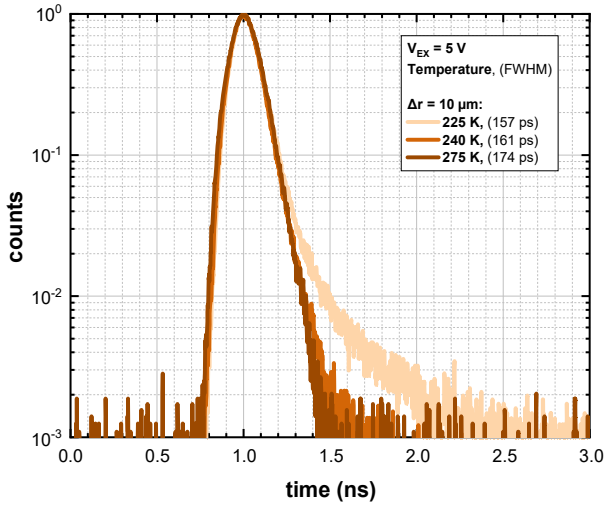

Fig. 13. Instrument response function of SPADs from wafer W2 with $\Delta r = 10$ µm at different temperatures. The exponential tail after the main peak is related to charge persistence.

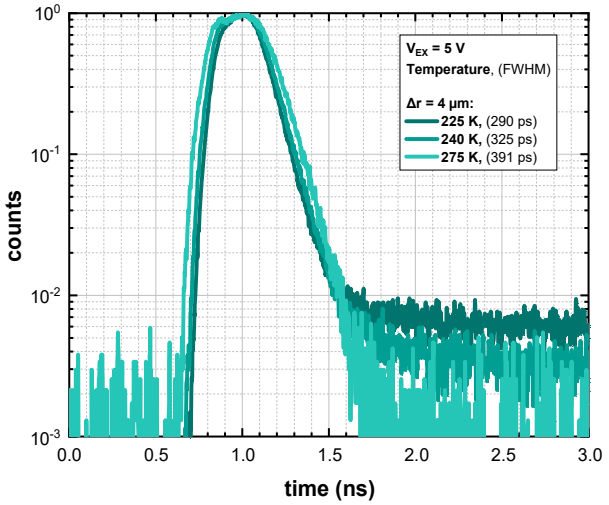

Fig. 14. Instrument response function of SPADs from wafer W2 with $\Delta r = 4$ µm at different temperatures. The diffusion tail due to charge persistence is much more prominent than that of SPADs with $\Delta r = 10$ µm, even at higher temperatures.

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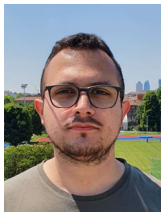

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