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Plasmonic Transceivers for the Terabaud Age

David Moor, Juerg Leuthold, Yuriy Fedoryshyn, Michael Möller, and Ueli Koch

***Abstract*—This work summarizes the recent progress towards a Terabaud electronic-plasmonic circuit integration platform. The conventional (2D), flip-chip and monolithic electronic-photonic integrated circuit (EPIC) platform are compared side-by-side. The novel plasmonic-electronic approach is introduced and discussed with respect to advantages and challenges of the predominant photonic electronic integration technologies. A recent 222 GBd OOK plasmonic 2D integration and latest result on a 185 GBd OOK monolithic plasmonic EPIC are discussed in more detail. Recent advancements in the fields of plasmonic modulators and detectors are reviewed. In light of progress with components and integration, a path towards Terabaud-class transceivers is described.**

***Index Terms*— Plasmons, integrated optoelectronics, integrated circuit fabrication, integrated optics, BiCMOS analog integrated circuits, transceivers, optical communication, ultra-high-speed integrated circuits, monolithic integrated circuits, hybrid integrated circuit packaging**

I. INTRODUCTION

INTEGRATION of electronic and photonic components is considered a solution to overcome ongoing challenges with the exchange of information between increasingly complex and faster electronic circuits, boards, racks, and data centers. Increasing the level of integration promises smaller footprint, higher bandwidth and a reduced power consumption. There is increasing demand for a new class of disruptive electronic-photonic integrated transceivers. For instance, switch application specific integrated circuits (ASIC's) have increased their bandwidth capacity 40-fold over the last 10 years from 1.28 Tb/s in 2012 [1] to 51.2 Tb/s in 2022 [2]. To keep up with the ASIC development, the transceivers also need to increase the throughput by a factor of 2 every two years to guarantee continued datacenter interconnect (DCI) scaling. Similarly, global high-performance computing (HPC) capacity is increasing exponentially [3]. This comes with an increase of data exchange. It is therefore necessary that the energy-bandwidth efficiency for data exchange is improved significantly, otherwise the fraction of energy dedicated to communications will at one point even supersede the energy dedicated to computation [3]. Likewise, cloud computing is growing – among which applications for artificial intelligence are surging – and in fact driving the data exchange. In view of potential energy crises and global efforts to consume less energy, the amount of energy consumed in data centers becomes increasingly concerning. An increasing fraction of this energy is consumed by data exchange [3]. One way to address this is to introduce energy-efficient, compact, highest speed transceivers that can meet the needs of next generation DCI and HPC infrastructure.

Research in the last decade has led to a large variety of scalable, high-symbol-rate transmitter, receiver and transceiver implementations [4-44]. Fig. 1 captures the last 10 years of experimentally demonstrated assemblies consisting of electronic integrated circuits (EICs) and photonic integrated circuit (PICs). The type of integration is divided into three categories: *2D*, *Flip-Chip* and *Monolithic*.

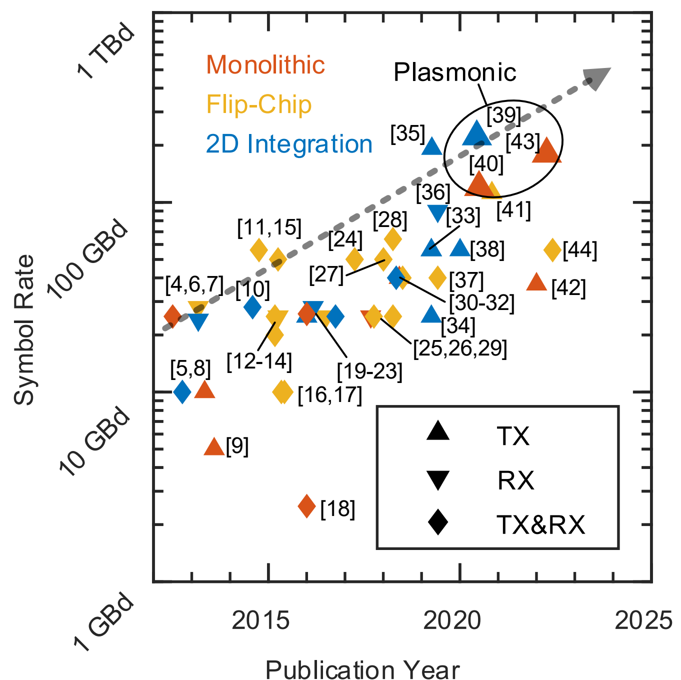

Fig. 1. The symbol rate is currently doubling every 2.5 years (grey dashed pointer). If the exponential trend is extrapolated, a TBd transmitter assembly can be expected within the next 5 years. So far, the performance discrepancy between the three integration paradigms is minimal. In the long run, parasitics in 2D assemblies will make it challenging to reach the TBd.

In this paper, *2D*, *flip*-chip- and *monolithic* integration methods are discussed. They are compared for their strengths

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and limitations regarding performance, scalability and cost. While *monolithic* integration [45] is expected to eventually outperform the others, *flip-chip* assemblies offer good performance with comparably low expenses. Furthermore, as plasmonics offers a solution for integration at highest symbol rates, the latest results on plasmonic modulators and detectors is reviewed. A recent *2D* plasmonic transmitter operating at 222 GBd OOK is discussed. Also, a new highest-speed transmitter *monolithically* integrated in a BiCMOS-plasmonic platform is demonstrated, which is capable of 200 GBd OOK. Finally, plasmonics is discussed as a key element for the upcoming Terabaud age.

The paper is organized as follows. The different integration technologies are elaborated in more detail in section II. Section III reports on the current state of electronic-plasmonic transceivers and plasmonic transceiver components. The plasmonic transmitters highlighted in Fig. 1 are discussed in more detail. In section IV, a 200 GBd OOK plasmonic *monolithic* EPIC is discussed. Section V outlines a path towards Terabaud transceivers and section VI concludes with the key insights into the plasmonic technology for the upcoming Terabaud age.

II. Integration Of PIC and EIC

Historically, interconnect systems were purely electrical. As speed increases, there is a trend towards optical interconnects, which require cointegration of electronic and photonic circuits.

Here, three categories of cointegration methods are distinguished: *2D*, *flip-chip* and *monolithic*, see Fig. 2 (a). In most of the current prototypes [1, 46], the components are heterogeneously integrated into packages and connected through wire/ribbon bonds or traces on a common substrate (often called 2D integration). Sometimes, the chips are flip-chip bonded to a common substrate such as a PCB, a ceramic or a silicon interposer (often called 2.5D integration). In this paper, both of these approaches are summarized under the category "*2D Integration*". In more advanced products, EIC's are flip-chip bonded directly onto PIC's to reduce footprint, microwave losses and thereby improve energy efficiency and bandwidth density. This is also called "3D integration". In this paper, they are summarized in the category "*Flip-Chip*". The ultimate cointegration is fabrication of *monolithic* EPIC's. Be it through materials that inherently serve both purposes [9, 18, 31], heteroepitaxial growth [47, 48], or wafer-bonding/deposition of active optical layers on top of an electronic platform [40, 43]. In this paper, this technology is summarized by the category "*Monolithic*". For the purpose of this work, the integration of gain media is neglected, but the importance of the integration of lasers and amplifiers directly into the photonic platform is recognized. As shown in Fig. 1, all three integration techniques have been demonstrated beyond 100 GBd. Overall, an exponential trend can be observed with the record symbol rate doubling every 2.5 years or growing 30% yearly.

The advantages and limitations of the three options for integration are qualitatively illustrated in Fig. 2 (b). The following list explains the considerations corresponding to the axes of the spider graph.

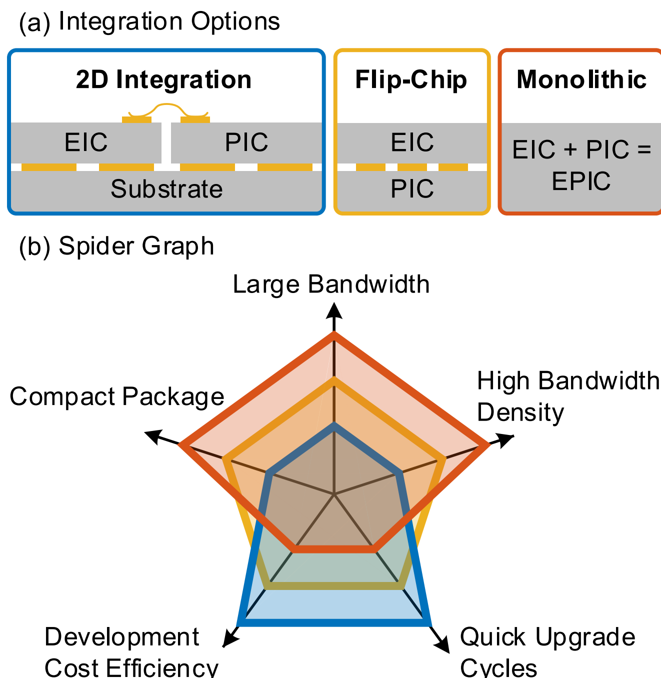

Fig. 2 (a) Comparison of integration options. (b) The qualitative graph represents the individual strengths of the three integration options depicted in (a). *2D integration* (blue) is considered to be superior with respect to development cost and upgrade time. *Monolithic integration* (red) offers the largest bandwidth and smallest footprint. *Flip-chip integration* (yellow) is a compromise between the other two options.

1) **Large Bandwidth**
   Monolithic has the lowest parasitics, the shortest radio frequency (RF) path and optics can be integrated into the layer stack of the EIC. *Flip-chip* integration has very little pad capacitance and rather short RF paths. *Flip-chip* integration has been demonstrated beyond 300 GHz [49], where the losses so far are dominated by microwave propagation losses. *2D integrated* packages can be engineered to hundreds of GHz bandwidths [50]. As frequencies increase, pad capacitance and bond wires cause significant degradation in signal quality and loss [51].
2) **Compact Package**
   On the one hand, smallest total EIC+PIC chip sizes can be obtained by *monolithic* integration. On the other hand, optical and electrical interfaces may dominate the package size depending on the application. Yet, they should be kept minimal as a larger package size implies that microwave signals need to travel further, inducing more RF losses. Given that microwave losses increase with frequency, the reduction of interconnect losses will gain even more importance in the future.
3) **High Bandwidth Density**
   Data rates of *monolithic* EPIC's will be limited only by the optical IO density and thermal constraints caused by the EIC. So far, the photonic density is low as photonic components typically require mm^2 of footprint. Recent trends towards ring modulators help increase the photonic density. However, the smallest and highest bandwidth

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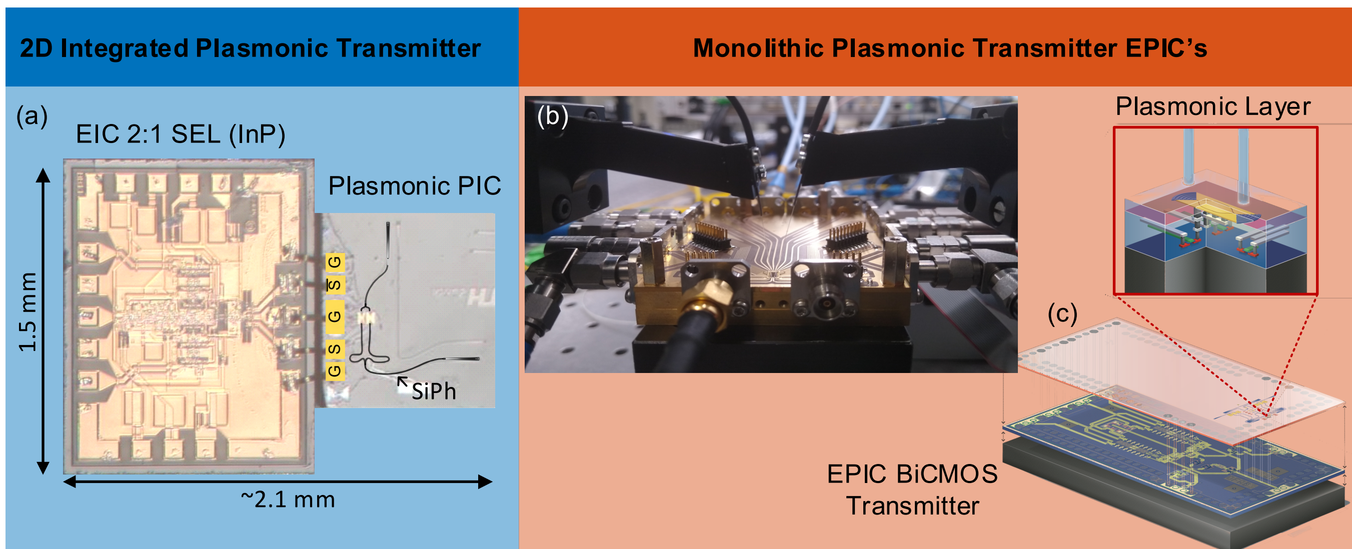

Fig. 3 Recent progress in electronic-plasmonic integration. (a) With 222 GBd OOK, the fastest symbol-rate transmitter assembly to date is based on *2D integration* of a silicon-plasmonic PIC with an indium-phosphide EIC [39, 57]. (b,c) *Monolithic* EPIC integration of a plasmonic modulator [40, 43]. (b) Photograph of the *monolithic* transmitter prototype with a reported bandwidth capable of at least 180 GBd OOK. (c) Conceptual illustration of *monolithic* integration of the plasmonics (red layer) on top of the BiCMOS electronics (blue layer). The inset shows an ultra-compact modulator for highest bandwidth-density.

modulators and detectors are currently based on plasmonics, which require at most a few tens of μm^2 of footprint. In both *flip-chip* and *2D assemblies*, a large fraction of the footprint is consumed by the electrical interfaces. In *flip-chip* assemblies, the whole surface of the chip is available for electrical interfaces. They require a 20-40 µm pitch. *2D* wire bonded assemblies require hundreds of micrometers of channel spacing along the edge of the chip, limiting the number of channels.

4) **Development Cost Efficiency**
The closer the optics are to the electronics, the harder it is to define interfaces and develop components under the constraints posed by the other. *Monolithic* integration requires more elaborate fabrication steps and will always come with a higher assembly complexity. Also, thermal constraints are tougher and material incompatibilities more restrictive. On the other hand, *flip-chip* integration can benefit from recently established EIC integration progress. Conversely, *2D assemblies* are well established and only require a proper RF design and assembly.

5) **Quick Upgrade Cycles**
Technology evolves at a rapid pace and similar to the initial research and development efforts, the interdependencies of *monolithic* chips impose constraints. Therefore, with each upgrade, the higher the integration density, the more time and effort is required. Here, *flip-chip* and *2D assemblies* offer quicker turn-around times.

Finally, one could add an axis on the **Unit Cost** in Fig. 2. At this point we refrain from a direct comparison on costs as they are to a large extent a matter of scaling, automation and manufacturing location. Here, we only remark that the bulk of the unit cost goes into packaging. Some *monolithic* assemblies require more specialized fabrication, however, zero-change [4] CMOS photonics has demonstrated that the fabrication cost of *monolithic* assemblies can be low. Furthermore, as component testing can be performed at the wafer-level using vertical coupling, the *monolithic* approach might have an advantage. On the other hand, development costs also make up a certain fraction of the retail price. The complexity of the product and the volume of the market can change the equation and favor the flexibility of *flip-chip assemblies.*

III. Plasmonic Transceivers

Electronic-plasmonic integration holds promise for significant improvements in optical interconnects. Plasmonics offers a solution for Terabaud transceivers, where extreme bandwidths [52, 53], compact devices [54] and flexible integration [55] is required. Such unique features make this integration approach most attractive. At the ECOC 2019 in Dublin, both the *2D* and *monolithic* integration of plasmonic transmitters were shown for the first time [56, 57]. The two concepts are discussed in more details in section III.A. Plasmonic *flip-chip* assemblies have not been explored so far, but might be very interesting as it allows for a flexible integration with standardized components.

Plasmonic modulators [58] and detectors [59] are key elements of a plasmonic transceiver. They have proven to be fast [54, 60], compact [54, 61-63], compatible with silicon photonics [54, 60] and silicon nitride photonics [64], and can be deposited on almost any substrate [55]. They are therefore ideally suited for integration in high-speed transmitters and receivers. The state-of-the-art of individual plasmonic components is reviewed in section III.B.

A. Plasmonic Transmitter Assemblies

Two successful attempts towards plasmonic transmitters were demonstrated to date, which are illustrated in Fig. 3. The first approach is based on a ribbon bonded, *2D*, side-by-side assembly of a high-speed indium-phosphide EIC with a custom plasmonic PIC [39]. The second approach targets *monolithic*

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integration into the metallization layers of a high-speed BiCMOS EIC [40, 43] and is further explained with new results in section IV. Both assemblies presented in Fig. 3 rely on organic electrooptic materials which are being actively researched.

The *2D* integrated plasmonic transmitter [39, 57], see Fig. 3(a), demonstrated a flexible and scalable way to integrate plasmonic PICs with EICs. In this demonstration, a 0.7 µm indium phosphide double-heterojunction bipolar transistor technology with $f_T/f_{max} \sim 400$ GHz was used to build a > 110 GHz 2:1 multiplexing selector [65, 66]. The transmitter has a footprint smaller than 3.15 mm^2, while the Mach-Zehnder modulator occupies less than 0.05 mm^2. The RF interface consisted of 25 µm wide and < 200 µm long ribbon bonds in a GSG$\bar{S}$G configuration. A drive voltage of 0.6 $V_{pp,diff}$ was used. 222 GBd OOK transmission by this *2D* integrated plasmonic assembly has been demonstrated.

The *monolithic* EPIC, see Fig. 3(b,c) is the first demonstration of a *monolithic* plasmonic transmitter. A 0.13 µm silicon-germanium heterojunction bipolar CMOS technology with $f_T/f_{max} = 350/450$ GHz was used to build a 4:1 multiplexer [67, 68]. The transmitter had a footprint of 4.5 mm^2. The plasmonic modulator in the 100 GBd data transmission experiment [40] had a footprint of 29×6 µm^2 including fiber coupling. The RF interface consisted of an array of vias in GSG [40] or S$\bar{S}$S [43] configuration. A drive voltage of 2 $V_{pp,diff}$ was applied. This value was derived from circuit simulations. In this work, a significantly improved *monolithic* plasmonic EPIC is introduced that offers data transmission of up to 185 GBd OOK. Details are given in section IV.

B. Plasmonic Modulators and Detectors

Plasmonic electro-optic components such as modulators and photodetectors are particularly suited for high-symbol-rate applications and co-integration with electronics due to their inherent speed, efficiency, compactness and compatibility with many platforms.

B.1 Plasmonic Modulators

Plasmonic modulators are extremely compact: Mach-Zehnder devices can be as small as 10 µm in length [54] and ring modulators can feature radii of 1 µm [61]. The compact size is due to the capability of plasmonic waveguides to confine light beyond the diffraction limit. Plasmonic modulators are not only small, they have also shown operation up to 500 GHz [52] and beyond [69]. The high-speed characteristic stems from the fact that plasmonic modulators rely on the fast electro-optical Pockels effect, which induces a refractive index change proportional to the RF field between the electrodes. As the electrodes are defining the plasmonic waveguide, strong light-matter interaction and small resistance are observed. The small size further results in a small capacitance and therefore a small RC time constant. Furthermore, the small and purely capacitive load leads to a high power efficiency. For instance, IQ modulators, see Fig. 4(e), can be operated with as little as 0.426 V_{pp} and consume only 0.6 fJ/b at 200 Gb/s QPSK [70]. This low energy consumption is again a result of the small capacitance and the low drive voltage. Lastly, the plasmonic technology is compatible with many materials and platforms. Plasmonic modulators have been shown with nonlinear organic materials [60, 71], and also with ferroelectrics such as $BaTiO_3$ (BTO) [64, 72-74] or $LiNbO_3$ [75]. Plasmonic modulators are compatible with silicon photonics [64, 72-74], with the silicon nitride platform [64] and can simply be put down on a glass substrate [55].

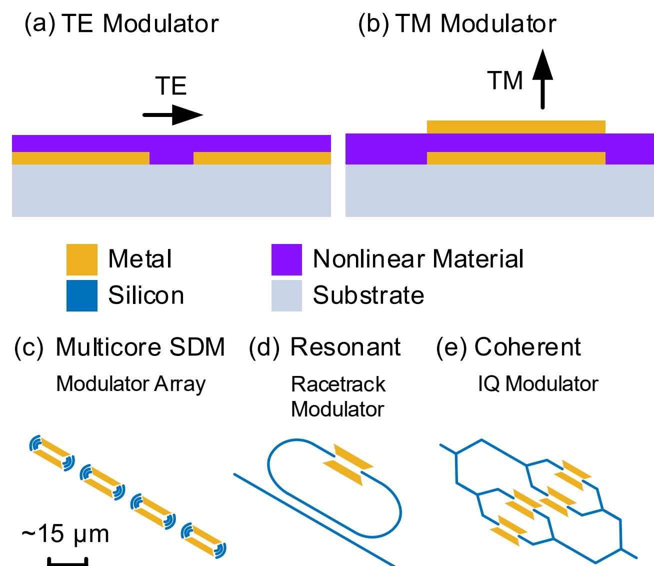

Fig. 4 (a,b) Device cross-sections of plasmonic modulators. (a) Plasmonic modulators for TE polarization. The nonlinear material can be organic [71] or ferroelectric [73]. (b) Plasmonic modulators for TM polarization [72, 76]. (c-e) Plasmonic modulator concepts. (c) An array of phase shifters [77] coupled to a single fiber. (d) A resonant intensity modulator [78]. (e) A coherent IQ modulator [70].

B.1.1 Plasmonic TE Modulators

The most established high-speed plasmonic modulator scheme is based on a transverse electric (TE) metal slot waveguide, which is filled with a nonlinear electro-optic material of either organic or ferroelectric nature, see Fig. 4(a). The plasmonic organic hybrid (POH) technology has proven to be widely applicable for phase [60, 77, 79], intensity [54, 80] and IQ [70, 81] modulation, achieving electro-optical bandwidths beyond 500 GHz [52], CMOS-compatible drive voltages below 0.2 V [82], and energy-efficient operation in the sub-fJ/b range [70]. Furthermore, extremely compact footprints < 100 µm^2 have been achieved by exploiting pitch-reduced fiber arrays [77] as shown in Fig. 4(c). As a unique advantage, the technology is independent of a photonic substrate. This has been shown by the fabrication of a plasmonic modulator in a single metal layer on glass without a need for silicon waveguides [81]. This allows fabrication of plasmonic ICs into the metallization stack of EICs. Recently, reduced optical loss of 1.2 dB in resonantly enhanced plasmonic racetrack modulators, c.f. Fig. 4(d) has been shown [78]. This led to the demonstration of standalone symbol rates of 220 GBd OOK and a maximum data rate of 408 Gb/s. Using polybinary schemes in combination with plasmonic Mach-Zehnder modulators, 304 GBd and 432 Gb/s PAM8 transmission has been shown [83]. Also recently, the plasmonic ferroelectric modulator has been introduced [73]. It exploits an inorganic

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ferroelectric alternative to the organic materials offering comparable nonlinearity, but higher temperate stability beyond 130°C [73]. Recent demonstrations have shown that BTO plasmonics provides broadband modulation larger than 270 GHz [74] and therefore it is another promising nonlinear material for fast modulation. Exploiting BTO in data modulation experiments, symbol rates of 72 GBd [62, 84, 85] and 216 GBd [64] have already been shown using silicon or silicon nitride photonics, respectively.

B.1.2 Plasmonic TM Modulators

High-speed plasmonic modulators for TM polarization as shown in Fig. 4(b) are of interest because they can potentially be produced using conventional lithography techniques with relaxed requirements in terms of alignment accuracy and critical dimensions. The critical dimensions are now in the vertical direction, which can be well controlled by the thickness of the deposited materials. Such plasmonic TM modulators have been tested for operation in the O- and C-band and have already experimentally demonstrated symbol rates up to 100 GBd in a POH structure [76]. The wide optical bandwidth makes such devices also interesting for sensing applications. In an alternative configuration using n-doped silicon instead of the bottom conductor and BTO as the active material, beyond 150 GHz bandwidth was measured and 32 GBd symbol rate was achieved in a data modulation experiment [72]. This hybrid photonic-plasmonic approach offers a path towards devices with high coupling efficiency [86] and low propagation loss [72, 86]. BTO also allows for wafer-scale fabrication by using a wafer bonding technique [64, 87]. In conclusion, the TM approach promises high speed and low-cost production.

B.2 Plasmonic Detectors

Plasmonic detectors [59], see Fig. 5, feature compact footprints and can be shorter than 10 µm [63]. In the plasmonic technology, the metal serves two purposes: it is the electrical contact to extract carriers and it confines the light. Plasmonic high-speed detectors have so far been demonstrated for TE polarization based on graphene – exploiting either the bolometric [62, 84] or the photovoltaic [53] effect – or the photoconductive effect in germanium [63, 88]. The plasmonic confinement hereby enables extremely short drift paths to extract the generated carriers.

The photovoltaic graphene detector [53], see Fig. 5(d), shows large optoelectronic bandwidth covering the frequency range from kHz to 500 GHz. This is, to the best of our knowledge, the most broadband photodetector. Although offering only mA/W responsivity, it outperforms current state-of-the-art detectors because it features a high saturation power in excess of 20 dBm. This way, it can be used in shot-noise limited communication systems. Remarkably, in a plasmonic-to-plasmonic link, it was tested for symbol rates of 132 GBd [53]. The detector is based on direct illumination from an optical fiber and exploits the concept of plasmonic metamaterial perfect absorbers (MPAs) to maximize the absorption in the detector.

Waveguide-based alternatives, see Fig. 5(c), using the bolometric effect in graphene have shown flat frequency responses beyond 110 GHz. They have demonstrated 0.5 A/W responsivity and have been tested for 100 GBd data reception [62]. More recently, for both the bolometric and the photovoltaic effect, a bandwidth exceeding 330 GHz was measured [53, 85]. Besides graphene detectors, germanium-based plasmonic detectors have been demonstrated, which are compatible with standard fabrication processes and available in waveguide-integrated configurations as shown in Fig. 5(e). These plasmonic detectors take advantage of the photoconductive effect in germanium, which is inherently fast. Experiments confirm an optoelectronic bandwidth beyond 100 GHz, an external quantum efficiency of 0.36 and data reception at 72 GBd in the O-band [63, 88].

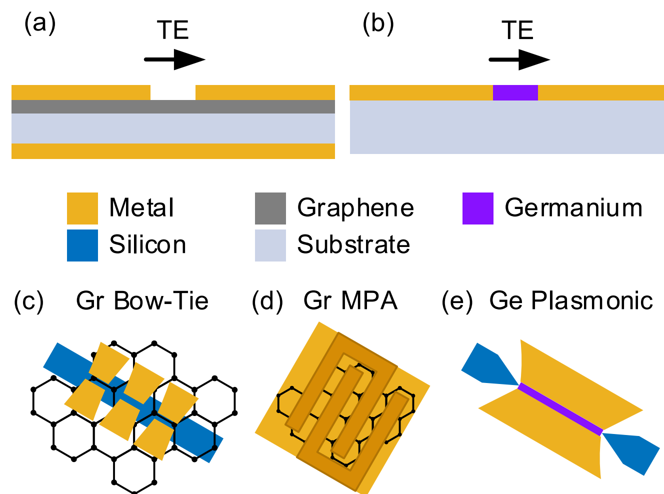

Fig. 5 (a,b) Device cross-sections for plasmonic detectors exploiting (a) graphene (Gr) or (b) germanium (Ge) as absorbing material. (c) Waveguide-coupled plasmonic graphene detectors [62]. (d) Plasmonic graphene photodiode exploiting the concept of metamaterial perfect absorbers. (e) A germanium-based plasmonic photodiode [63].

IV. 208/185 GBD MONOLITHIC TRANSMITTER

The *monolithic* electronic-plasmonic transmitter is to the best of our knowledge the fastest EPIC transmitter. The circuit, the experimental setup and the summarized results are depicted in Fig. 6. The EPIC consists of a 1.5×3 mm^2 chip with a layer stack comprising of SiGe BiCMOS layers and a *monolithically* integrated plasmonic modulator layer.

The electronic circuits were designed by the Saarland University and MICRAM Microelectronic GmbH [67, 68] and the electronic layers were manufactured by IHP – Leibniz-Institut für innovative Mikroelektronik in a modified SG13G2-process. The electronic circuit offers a built-in pseudo random bit sequence (PRBS) generation stage (PRBS-7). An option for feeding in externally generated signals is provided as well. Four PRBS are multiplexed in two multiplexer (MUX) stages. The 2nd stage is comprised of a power multiplexer (PMUX), which provides a differential output signal with a single-ended voltage swing of $V_{pp,SE}$ = 1 V. An external clock at ¼-cycle frequency is fed to the chip. An on-chip clock doubler provides the ½-cycle clock for the PMUX. An additional on-chip clock divider provides the clock for synchronization with the off-chip PRBS source.

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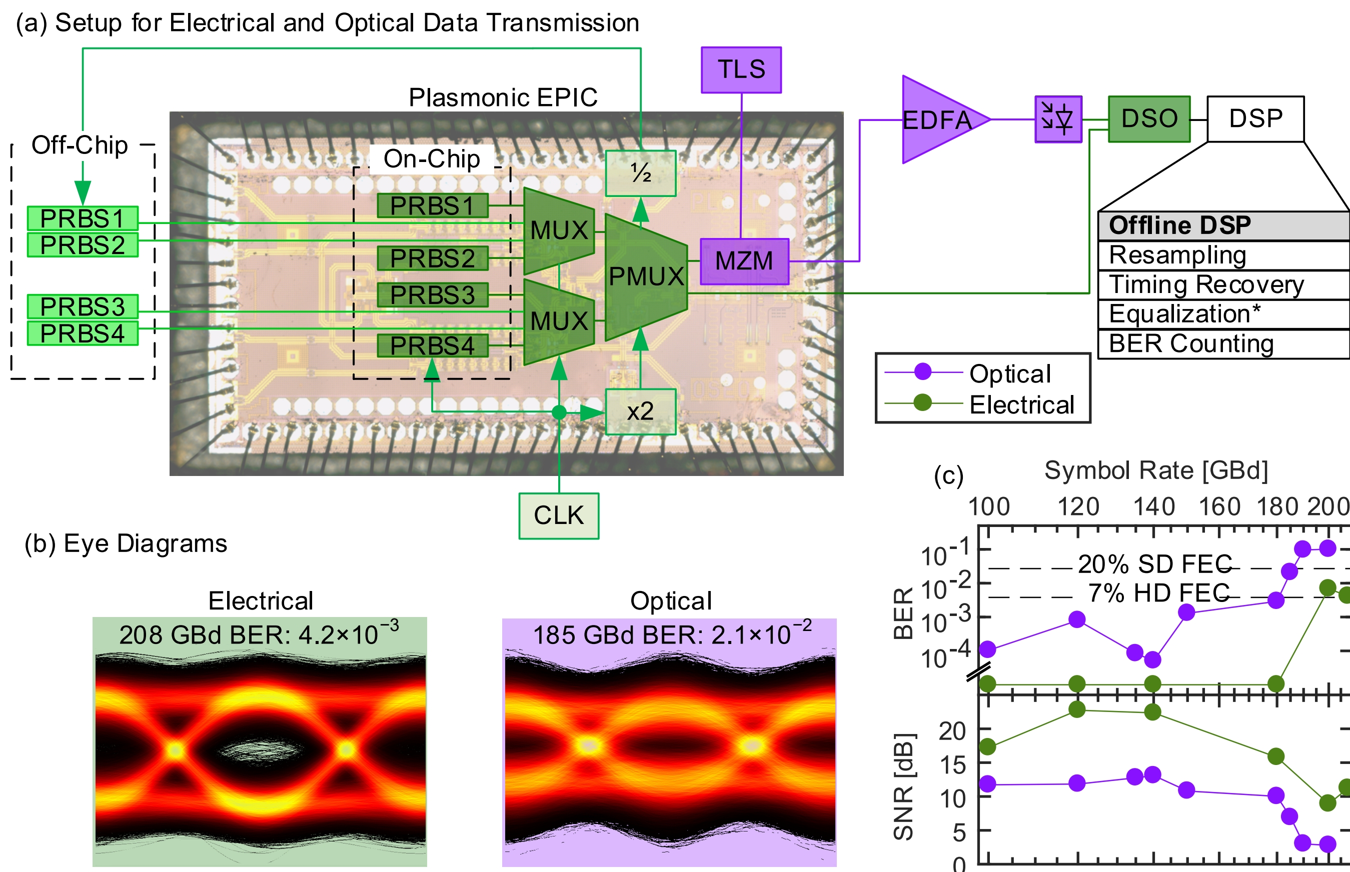

Fig. 6. Data modulation experiments. Up to 208 GBd OOK electrical and 200 GBd OOK electro-optical operation of the *monolithic* plasmonic transmitter EPIC is demonstrated. Electro-optical data transmission below the 7% HD-FEC limit is demonstrated with symbol rates of up to 180 GBd, and below the 20% SD-FEC limit with symbol rates up to 185 GBd. 100 GBd OOK and 150 GBd OOK are received without equalization below HD- and SD-FEC, respectively.

The C/L-Band plasmonic/photonic layer was designed and manufactured into the metallization layers of the BiCMOS chip by ETH Zürich. More details on the post-processing can be found in [40]. It comprises passive silicon photonic sections with grating couplers, waveguides, MMI splitters, and the active plasmonic modulator section. The modulator consists of a 15 µm long active section with a 100 nm gap size. As an electro-optical material in the slot, BAHX was chosen. It is a crosslinkable variant of the high-performance BAH13 material [89, 90]. It was poled electrostatically and crosslinked [90]. This material is stable for operation up to 130°C [40].

The electronic circuit was characterized for its performance using a separate EIC and PCB. In a first test, a four-channel 52 GBd off-chip PRBS source was used from an arbitrary waveform generator (AWG) and fed into the chip. After multiplexing, a 208 GBd signal was received. The eye diagram of the electrical signal is shown in Fig. 6 (b). The signal was detected in a 245 GHz photodiode and sampled with a 256 GSa/s digital sampling oscilloscope (DSO). Afterwards, it underwent a digital signal processing (DSP) stage, which included resampling, timing, nonlinear equalization and bit error counting. A bit-error ratio (BER) of 4.2×10^{-3} was found. The symbol rate was then varied between 100 and 208 GBd and the respective BER and signal-to-noise ratio (SNR) were recorded. The results for the different symbol rates are shown in Fig. 6 (c) (green dots).

The optical experiments were performed with two *monolithic* assemblies. The first (A) was used in tests covering the range up to 185 GBd. In subsequent experiments, a second assembly (B) was used to show experiments at higher symbol rates. The Mach-Zehnder modulators (MZMs) were first characterized for their optical characteristics. An extinction ratio of >20 dB was found. The V_π was measured to be 4 V. This value was retrieved from a reference modulator, where an external signal was applied to perform the characterization. On-chip optical losses of 13 dB were found for the modulators through the cut-back method. Due to optimizations of the fabrication process, the conventional silicon grating couplers on (B) were marginally more efficient than on (A) with a loss of 4.5 dB per grating as opposed to 5.5 dB. However, the peak wavelength on (B) was slightly redshifted.

In the data transmission experiment, PRBS data was generated (A) on-chip or (B) off-chip and fed into the multiplexer stages. Laser light from a tunable laser source (TLS) was coupled from a single-mode fiber into the chip. The 15 µm long plasmonic modulators utilize a dual-drive design [91], effectively dividing the V_π by a factor 2 to a $V_{\pi/2}$ of 2 V. The differential data signal is subsequently encoded onto the laser light. In setup (A), light between 1540 and 1550 nm was used, while in setup (B), the wavelength was about 1590 nm. The modulated light is transmitted through a short (<10 m) span of fibers, polarization controllers and an optical amplifier

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before being received in a 145 GHz photodiode. The same sampling and offline DSP as for the electronic back-to-back experiment were performed and the received BER and SNR are plotted in Fig. 6 (c) (purple dots).

In previous publications [89, 90], the electrical part of the *monolithic* chip was characterized for up to 180 GBd. Further analysis of the same circuit reveals that the electrical circuit comprising of a MUX and driver stage even operates beyond 200 GBd and up to 208 GBd below SD-FEC if characterized with a more advanced setup including a higher bandwidth DSO and DSP. The result is shown by the green dots in Fig. 6 (c).

The *monolithic* assembly was then tested for its electrical-to-optical performance. With setup (A) and the internal PRBS, operation up to 185 GBd with BER below the 20% SD-FEC limit was found. The internal PRBS generator limited further measurements at higher symbol rates. With setup (B) and an external PRBS, operation up to 200 GBd was demonstrated, however, with a BER above the SD-FEC limit. The result is shown by the purple dots in Fig. 6 (c).

The plot in Fig. 6 (c) also shows that the SNR degradation of the received signal of the electrical-to-electrical and the electrical-to-optical experiments at high frequencies follow a similar trend. Due to the strong correlation (R = 0.92) between the optical and the electrical SNR measurements, the bandwidth limitation of this setup does not seem to come from neither the optical components nor the vias connecting the driver with the modulator.

A summary of the key performance metrics of the EPIC transmitter in this work compared to state-of-the-art monolithic plasmonic transmitters is given in Table I.

TABLE I
PERFORMANCE METRICS OF MONOLITHIC PLASMONIC TRANSMITTERS

	Reference [40]	**This Work**
Max. Symbol Rate OOK	120 GBd	200 GBd
Max. Symbol Rate SD-FEC	120 GBd	185 GBd **(1.5x)**
Max. Net Data Rate	N/A	176.6 Gb/s
SNR @ 100 GBd	8.14 dB	11.51 dB **(+3.4 dB)**
BER @ 100 GBd w/ EQ	9.21×10^{-3}	1.04×10^{-4}
BER @ 100 GBd w/o EQ	N/A	2.40×10^{-3}
BER @ 150 GBd w/o EQ	N/A	2.58×10^{-2}

V. THE TERABAUD AGE

Terabaud-class transceiver systems are emerging as the bandwidth demand increases relentlessly. Commercially available transceivers are projected to increase in symbol rate by only 10% per year. In contrast, a 30% yearly increase is observed in research, see Fig. 1. Yet, both diverge from the demanded growth of HPC and DCI applications, which depending on the industrial sector, is about 30%-70% [92]. For example, latest switch ASICs with 800 GbE interfaces have just reached a throughput of 51.2 Tb/s [2] and they are scaling by 45% yearly [1]. The divergence between available and demanded increase in symbol rate will soon require disruptive technologies.

To keep up with the increase of interconnect data rates, a variety of technologies beyond the current single-lane PAM are investigated. These include wavelength division multiplexing (WDM), space division multiplexing (SDM), higher-order modulation formats, coherent systems and polarization diversity. The economic perspective of HPC and DCI applications, however, favors solutions of lowest complexity in the receiver and the DSP. Therefore, the rather simplistic PAM format in a single polarization is quite attractive to this day – despite the higher SNR requirements over more complex coherent solutions. If PAM or other intensity-modulated formats are pursued further, then symbol rates need to increase. In the meantime, cost for highest-speed electronic components decreases. Even more, synergies in optoelectronic technologies with next-generation wireless [93] and THz [94] communication systems will reduce the development cost and lead to favorable pricing for co-integrated high-bandwidth devices.

To realize Terabaud transceivers, progress in components and integration method is needed. However, more important is the needed improvement in interdisciplinary collaboration between device and integration research. The building blocks towards the Terabaud age are illustrated in Fig. 7 and further elaborated below.

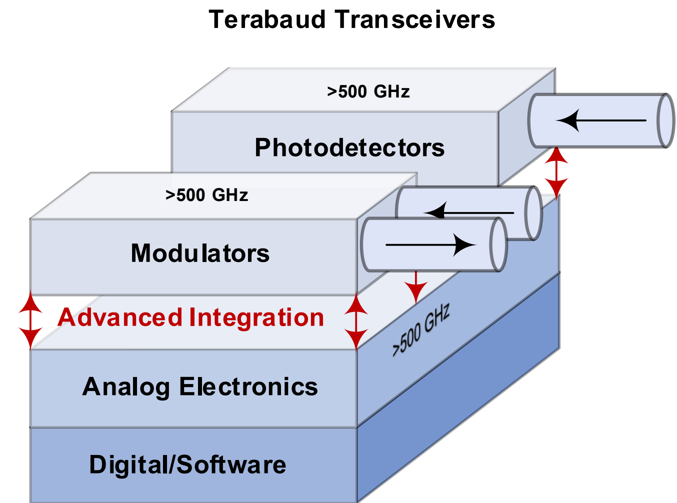

Fig. 7 Terabaud transceivers will be built from advanced components in digital and analog electronics, and in modulator and detector photonics. State-of-the-art components already have sufficient bandwidth to reach Terabaud speed. However, the challenge to integrate them is yet to be solved.

1) **Digital/Software**
DSP has to be able to handle highest-speed real-time communications with high energy efficiency. Towards this goal, highly parallelized algorithms that operate at the much lower clock rates are needed. Furthermore, modulation formats that offer high spectral efficiency and that can be processed at highest speed with lowest latency are of interest. So far, conventional PAM NRZ coding is still attractive [78, 83]. Other examples in this direction are the efforts on Faster-than-Nyquist (FTN) coding, where polybinary coding or M-BCJR coding have been exploited

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to encode 304 GBd and 570 GBd signals with a 65 GHz and a 100 GHz channel, respectively [83, 95].

2) **Analog Electronics**
Analog electronics already offers impressive bandwidths. Recent advances in SiGe BiCMOS [96] have drawn a lot of attention towards this technology. A SiGe BiCMOS node with f_{Max}/f_T of > 700/470 GHz is now offered commercially, while experimental results are already showing transistors with f_{Max}/f_T of 720/505 GHz [97]. It is foreseeable that with the latest technology and optimized circuits, amplifiers operating at > 500 GHz may be realized. This is based upon the observation that amplifiers with a net gain at 330 GHz have already been demonstrated with a SiGe technology offering f_T/f_{max} of 350/450 GHz [98]. Alternatively, III-V transistors with f_{Max}/f_T of 1200/475 GHz have been demonstrated [99] and circuits with > 110 GHz analog bandwidth were used for high-symbol-rate demonstrations [39, 57].

3) **Modulators**
Multiple plasmonic modulator options (POH, plasmonic BTO) are already available, which are meeting the bandwidth requirements for Terabaud transmission, see section III.B.1. Bandwidths in excess of 500 GHz have been shown [52].

4) **Photodetectors**
Plasmonic graphene photodetectors (Graphene PD) or germanium photodetectors (Germanium PD) already meet the bandwidth requirements for Terabaud transmission, see section III.B.2. Plasmonic photodetectors have already shown flat frequency response up to 500 GHz [53] and SiGe photodetector have recently shown to operate with 3dB bandwidths of 265 GHz [100]. All of which shows that photodetectors already now offer sufficient bandwidth.

5) **Advanced Integration**
Compact integration is critical to avoid deterioration of high-speed electrical signals. *Monolithic* integration into EPICs naturally offers the highest bandwidth. However, a cost/benefit tradeoff must be accounted for. *Flip-chip* and *monolithic* integration are both viable options for Terabaud transmission. *Flip-chip* integration of components operating at 320 GHz was already demonstrated in 2014 [49]. At these frequencies, *flip-chip* interconnects require particularly careful design of the interface to not excite substrate modes [51]. Short-term dominance for *flip-chip* integration is expected due to the technological readiness of the individual components, while *monolithic* integration is expected to take over in the future due to its ultimate performance and scaling advantages.

The short progress summary above shows one thing: The necessary EIC and PIC technologies and the integration methods to enter the Terabaud age are ready or upcoming. Significant work in this direction is highlighted in Fig. 1. However, it can be observed that *flip-chip* and *monolithic* integrated transmitters, receivers and transceivers do not yet outperform *2D integrated* devices. The remaining challenge is to combine the available components with the most suitable integration method into complete transceivers, which requires interdisciplinary efforts, research and development from the design to the implementation.

VI. Conclusion

Plasmonics is the fastest technology for Terabaud transceivers. Also, it offers lowest drive energy/bit operation with record-low 600 aJ/bit at 200 Gb/s and meanwhile low optical losses with as little as 1.2 dB on-chip optical losses in plasmonic racetrack modulators [78]. It is compatible with all three integration options and capable of both detection and modulation. Two plasmonic transmitters in the 200 GBd range were reviewed: one using *2D-integration* and one using *monolithic* EPIC technology. *Monolithic* integration promises the highest efficiency and potentially the highest bandwidth. The maturity of *flip-chip* integration might make it more economical for the near future and has sufficient bandwidth for Terabaud operation. Plasmonic receivers are yet to be demonstrated, but the detector technology is compatible with all three integration categories.

A 185 GBd *monolithic* EPIC has demonstrated the highest data rate in the field of *monolithic* transmitters. In the meantime, a commercial node with 50% faster transistors [101] is being set up. If the same electronics would be fabricated with the latest technology node, even higher symbol rates would be available already today. As the individual components of a Terabaud transceiver have been demonstrated to offer sufficient bandwidth, the challenge will be to integrate them into one platform. For those symbol rates, with 500 GHz bandwidths and readiness to be integrated using *flip-chip* or *monolithic* integration technology, plasmonic modulators and detectors are the ideal candidates.

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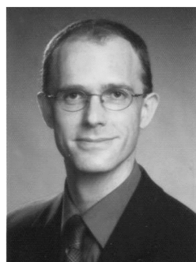

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