A 73% Peak PDP Single-Photon Avalanche Diode Implemented in 110 nm CIS Technology with Doping Compensation

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***Abstract*—In this paper, we present 10 µm diameter SPADs fabricated in 110 nm CIS technology based on an N^+/HVPW junction, with enhanced sensitivity at short wavelengths. To reduce tunneling noise due to the highly-doped layers in the process, a doping compensation technique is used, which allows to adjust the doping profile of the HVPW. Thanks to this technique, DCR is reduced by a factor of 24 at 2 V excess bias voltage when compared to non-compensated devices. Furthermore, the maximum achievable PDP is enhanced by 49% thanks to the much lower DCR leading to a PDP of 73%, the highest ever reported at 440 nm, while the DCR is 12.5 cps/µm^2, all at the 5 V excess bias. Since the junction is formed very close to the surface, the SPAD has excellent sensitivity in the UV spectrum, with a PDP of 43% at a wavelength of 350 nm. The proposed SPAD also achieves a PDP of 7% with a timing jitter of 68 ps at 850 nm at 5 V excess bias, which makes the device very useful for RGB-Z (RGB-D) sensors.**

***Index Terms*—Single-photon avalanche diodes, CMOS image sensor technology, doping compensation, high sensitivity, RGB-Z multispectral camera.**

I. Introduction

INCREASING demands in applications that require photon detection under low light conditions and attaining temporal information of photons have accelerated the developments of single-photon detector technologies. In this sense, providing high sensitivity in detection and high timing accuracy has rendered SPADs among the best candidates for time-resolved imaging, quantum imaging, and biophotonics [1]–[6]. CMOS-compatible and standard CMOS single-photon avalanche diodes (SPADs) have seen considerable advances, driven by industrial requirements for high visible to near-infrared (NIR) sensitivity. However, standard CMOS, originally developed for designing analog and digital circuits, is not the most convenient process to achieve the best performance in optoelectronic devices. As a result, CMOS image sensor (CIS) processes have recently been developed to improve noise and sensitivity performance, especially for imagers, and SPAD designs have also been demonstrated in various technology nodes [7]–[10].

In addition to finding the most suitable fabrication process for device design, another important aspect is reducing pixel size. Shrinking pixels has the advantage of enhancing density, hence enabling advanced functionality on chip, and resolution, hence achieving multi-megapixel SPAD arrays [2]. For these reasons, moving to smaller technology nodes is vital in SPAD design. Implementation of SPADs in smaller technology nodes also has the benefit of lowering power consumption and cost. On the other hand, designers need to pay more attention to layer selection, due to the increased doping concentrations in smaller nodes, which results in smaller depletion width and higher electric field in the junction. Therefore, tunneling noise tends to increase and dominate the overall noise, hence numerical analysis has become essential to find the best possible trade-offs.

Our motivation in this work is to develop a SPAD pixel that can be used in an RGB-Z (also known as RGB-D) multispectral camera configuration where Z can be, for instance, at near-ultraviolet (NUV) or NIR wavelengths. In conventional methods, different cameras are utilized for visible, NUV and NIR imaging as the same camera cannot provide high performance in such a wide wavelength spectrum. However, in an RGB-Z camera, a high performance is achieved for either NUV or NIR wavelengths in addition to the visible. Since RGB-Z camera pixels have to function in a broader wavelength range, the primary challenge of this type of camera is reduced color resolution under low light conditions. Resolution loss can occur because of background noise, crosstalk between colors, or not being able to set the exposure time correctly such that highly sensitive wavelengths are not saturated, and likewise, information from wavelengths with less sensitivity is not lost [11]–[14]. Besides improving data acquisition on the read-out side, another way to solve the color resolution problem in an RGB-Z camera pixel is to enhance the sensitivity at device level, especially for Z wavelengths. However, this is not straightforward, as detector noise must be kept low, whereas there is a trade-off between noise and sensitivity. Therefore, we aim to find a generalized method that can be utilized in any CMOS technology and provide a way to increase the efficiency of SPAD devices while keeping noise low enough. In order to achieve this goal, we have utilized a doping compensation technique to benefit from the enhanced efficiency at NUV or NIR, while realizing less complex RGB-Z multispectral

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camera systems. A similar approach has been applied in a linear mode APD to separate the multiplication and absorption zone of the device [15], which was then also characterized as a SPAD [16]. Here, we have implemented the technique for the first time to design the multiplication zone of a Geiger-mode APD. The devices presented in this study have all been fabricated in 110 nm CIS technology. Nevertheless, doping compensation is expandable to any CMOS/CIS technology; it gives designers an opportunity to obtain more desirable doping profiles without any modifications of the fabrication process, thus coping with the limitations of available foundry processes and widening the possibility of implementing various doping concentrations. However, it should also be noted that since the resulting doping profile is determined by the compensation between two layers, the process variability and tolerances will have an impact on the device performance.

The paper is organized as follows, we first describe the doping compensation technique, and then, we provide simulation results of various device designs, while comparing SPADs with and without compensation. Then, we provide the full characterization results of compensated SPADs. Afterwards, we look at the influence of guard-ring (GR) size on device performance. Finally, we compare our performance with the state-of-the-art.

II. Device Structures and TCAD Simulation Results

In this study, we aim to achieve very high photon detection probability (PDP) at short wavelengths while keeping the noise at a minimum. For this purpose, we start with a junction of N^+/high-voltage p-well (HVPW), where we form a thin depletion region close to the surface with highly-doped layers and obtain a high breakdown probability due to the high electric field in this thin avalanche region. The high breakdown probability will boost the PDP, whereas the small depletion region will increase the tunneling noise in the devices. In order to reduce tunneling noise, therefore, we exploit the doping compensation technique, which alleviates high doping concentration in the HVPW layer. The technique is based on a reverse type layer available in the technology, and consequently, a wider depletion region is achieved without modifying the process. Proper doping compensation helps preventing tunneling noise while keeping PDP high. Furthermore, since the GR can act as another noise source in SPADs, we developed modified GRs to mitigate dark count rate (DCR), whose characterization results will be presented in the next section. Thanks to the improved performance at near blue and the ultraviolet wavelengths, the doping-compensated SPAD design is also a very promising candidate for applications such as positron emission tomography (PET), fluorescence lifetime imaging microscopy (FLIM), deep-space UV astronomy or light detection and ranging (LiDAR) in submarine environments [6, 17].

A. Doping Compensation Technique and Device Structures

When a semiconductor is doped with both donors and acceptors, it is called compensation [18]. In this special case, in addition to the regular ionization process of donors and acceptors, the electrons of the donor atoms also fill the vacancies created by acceptor atoms. Under complete ionization, from the charge neutrality equations, the steady-state hole concentration is expressed as:

$$p = \frac{N_{\mathrm{A}} - N_{\mathrm{D}} + \sqrt{(N_{\mathrm{A}} - N_{\mathrm{D}})^2 + 4{n_{\mathrm{i}}}^2}}{2}, \qquad (1)$$

where N_A, N_D, and n_i correspond to ionized acceptor density, ionized donor density, and intrinsic carrier concentration, respectively [18]. In other words, N_D is the total electron density that is set free for the conduction band when semiconductor atoms are replaced by dopant atoms having more bonding electrons. Similarly, N_A is the total hole density that is created in the valence band when dopant atoms have fewer bonding electrons than intrinsic levels. In addition, n_i represents the electron and hole concentration when the semiconductor is undoped. From equation (1), it can be seen that hole concentration in a compensated semiconductor can be controlled by impurity (dopant) concentrations. Therefore, although it may degrade the transport properties, compensation gives the freedom to adjust the total doping of a semiconductor. We have applied this approach to our SPAD designs in which we made use of doping compensation to alter the already defined layer doping existing in the 110 nm CIS technology and to result in a better performing doping profile.

The cross-section of the structure without doping compensation can be seen in Fig. 1(a). The device is based on the N^+/HVPW junction and has a circular shape with a 10 µm active diameter (HVPW width), and it has a virtual GR around the active area. In order to modify the doping profile of the highly-doped HVPW layer and expand the depletion region, we investigated an n-type layer named as high-voltage n-well (HVNW). The cross-section for the compensated SPAD is provided in Fig. 1(b). This layer existing in the technology node has the potential to change the junction according to its concentration and depth, achieving new detection properties.

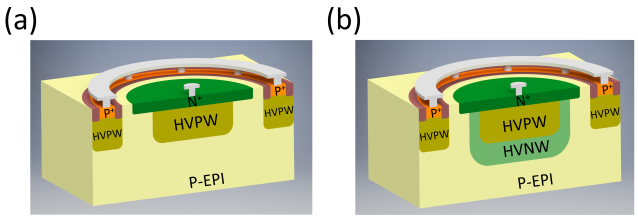

Fig. 1. Cross-sections of (a) N^+/HVPW junction with a virtual GR and (b) N^+/HVPW junction with the HVNW doping compensation layer and a virtual GR.

B. TCAD Simulation Results

Whilst moving to a new technology node, it is also very important to perform numerical analysis to predict device characteristics before design and fabrication and to find an optimized layer combinations according to application needs. From the SPAD design perspective, one should engineer the electric field inside the structure in order to achieve and confine impact ionization in the multiplication region while

suppressing premature edge breakdown. Considering also to have higher doping concentrations at smaller nodes, all possible junction configurations should be investigated, so as to compare different structures and to optimize especially the noise. In this study, we utilized the Sentaurus TCAD numerical tool to determine the energy band diagrams, doping profiles, electric field distributions, avalanche breakdown voltages, and I-V characteristics of our designs [19]. In the simulations, coupled Poisson and electron-hole drift-diffusion equations are solved while the Shockley-Read-Hall (SRH) recombination mechanism is selected. SRH rates are established by defining electron and hole recombination lifetimes, and trap-assisted tunneling is also modeled through the electric field dependence of recombination lifetimes with the Schenk model [20]. Position-dependent breakdown probabilities are determined based on the McIntyre model [21], and the Okuto-Crowell model is used to identify the avalanche breakdown point in silicon [22]. Moreover, the employed doping profiles in TCAD correspond to the exact values provided by the foundry, which cannot be disclosed for confidentiality reasons.

The energy diagrams obtained for the non-compensated and compensated devices are shown in Fig. 2. In this figure, E_c and E_v represent the conduction band and valence band energies, respectively. In order to observe how the compensation layer modifies the energy band of the non-compensated device, simulations were performed at 1 V reverse voltage. As the slope of the conduction or valence band is related to the electric field in the depletion region, it can be concluded that the high electric field in the non-compensated device is reduced thanks to the HVNW compensation layer. Therefore, we can expect to achieve lower noise and a higher breakdown voltage in the compensated device.

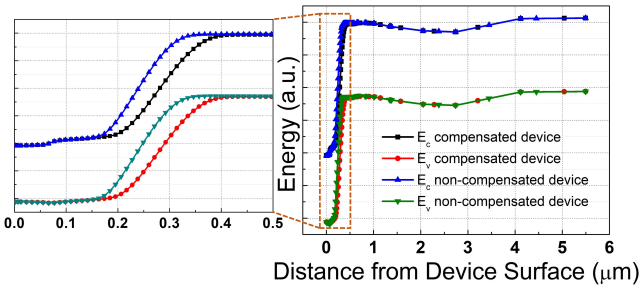

Fig. 2. Energy band diagram simulations of compensated and non-compensated SPADs at 1 V reverse voltage.

Then, electric field simulations were performed to quantify the magnitude of the electric field in the designed structures. The simulation results of the non-compensated structure are given in Fig. 3(a). In this figure, the actual doping profile implemented in TCAD, and electric field distribution at breakdown voltage are analyzed. As demonstrated, the electric field is fully confined in the multiplication region without having edge breakdown, however, as the junction is constituted between two highly-doped layers, the depletion width of the device is 0.28 μm which is rather thin. The thin depletion region leads to a very high electric field (5.63×10^5 V/cm) in the junction at the breakdown condition. Even though high electric field is useful to improve photon detection efficiency, it can also degrade the DCR of the device because of the increased tunneling rates. In addition, the junction occurs very near to the surface (0.23 μm) which indicates that the peak of the PDP curve will be at shorter wavelengths.

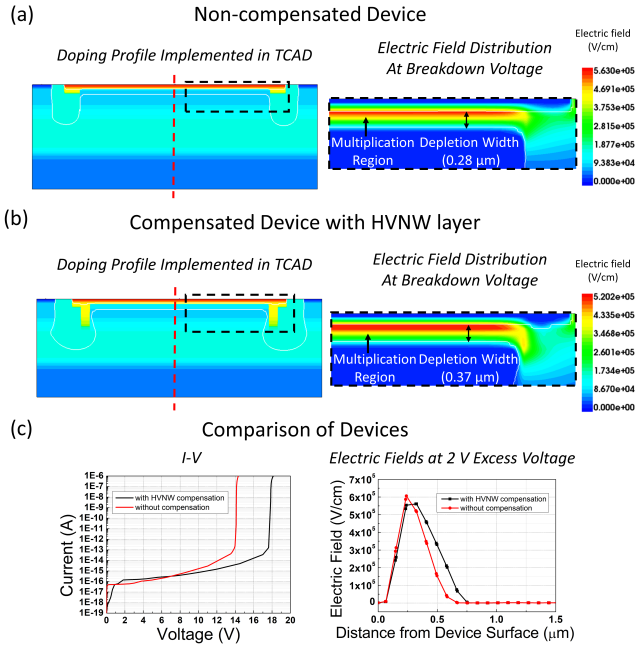

Fig. 3. Doping profile and electric field distribution at breakdown point of the (a) non-compensated SPAD and (b) compensated SPAD with HVNW layer. (c) I-V curves and electric fields at 2 V excess bias voltage taken through red dashed lines drawn in (a) and (b) of the devices.

After achieving Geiger-mode behavior with this initial structure, we have optimized further to increase the depletion region and consequently to decrease tunneling noise. For this purpose, as discussed, we have utilized doping compensation to modify the acceptor level in the HVPW layer and to adjust the doping profile. We have considered several n-type layers existing in the technology node to improve the performance, and we have selected a promising candidate, where compensation is realized by the HVNW layer while keeping the same active diameter (10 μm) and GR. HVNW layer is suitable for its depth and peak concentration, which can offer an appropriate modified HVPW profile. TCAD results of HVNW compensated SPADs are shown in Fig. 3(b). In this structure, the depletion region expands to 0.37 μm, while keeping a high electric field up to 5.2×10^5 V/cm. Besides, the junction still occurs very close to the surface (0.23 μm away) in the compensated SPAD. Hence, with this structure, we aimed to lower the tunneling component of the noise. In Fig. 3(c), the comparison of the proposed devices is presented in terms of I-V characteristics, and electric field at 2 V excess bias. First, the breakdown voltages were identified as the first points where the slope of the I-V curve changed abruptly. As expected, we observe relatively low breakdown voltage (14 V) in non-compensated SPADs, while it increases to 17.6 V in the compensated device. From the electric field graph, it can be seen that its peak magnitude remains higher in the non-compensated case. On the other hand, the electric field

profile becomes more uniform in the compensated device, and it is extended due to wider depletion region. In conclusion, by reducing the peak electric field magnitude thanks to the doping compensation, we expect to reduce tunneling noise and enhance the PDP particularly at short wavelengths of the visible spectrum and in the NUV region, by keeping the breakdown probability high.

III. Characterization Results

A. Compensation Layer Optimization

The simulations in TCAD were followed by designs and fabrication in 110 nm CIS technology. A sample SPAD image after fabrication is provided in Fig. 4(a). Each SPAD has a round shape with a 10 µm active diameter, and also, different GR diameters have been implemented to obtain the best performance in devices. In this section, the proposed SPAD's GR size is 1.5 µm. Light emission test results of a compensated sample are shown in Fig. 4(b). The SPAD is operated beyond avalanche breakdown without quenching, and light emissions from the avalanche region are observed through a digital microscope (Hirox KH-8700) connected to a charge-coupled device (CCD) camera. The images show that there is no edge breakdown, and the light-sensitive area has a 10 µm diameter, which is the same as in the drawn layout. In the remaining measurements, SPADs were passively quenched and recharged with a 220 kilo-ohms external resistor, and avalanche pulses are read through a digital oscilloscope (Teledyne LeCroy WavePro 760Zi-A) by measuring the voltage across this resistor.

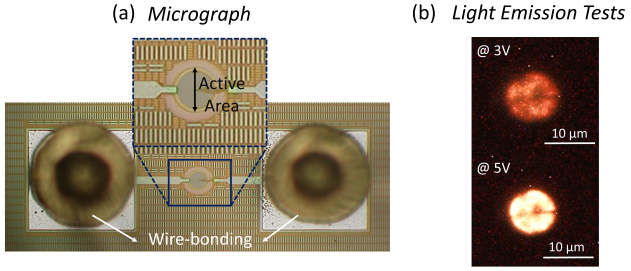

Fig. 4. (a) Micrograph of the chip showing the fabricated SPAD. (b) Light emission test results of the compensated SPAD sample.

I-V characteristics of the fabricated N^+/HVPW junction based SPADs with and without the compensation layer are given in Fig. 5(a) under both dark and illumination conditions. The current compliance in the I-V measurements was 1 mA. From dark I-V curves, we deduce the avalanche breakdown voltages as 14 V, and 17.2 V, respectively. These values are well-matched to TCAD simulations. However, the breakdown voltage between the compensated devices might differ slightly since the final depletion width depends on the resulting doping profile after compensation, which is also affected by process variability. I-V curves also indicate that there is almost no difference in dark current, while changing the compensation layers except of the variation in the breakdown voltage, as predicted by simulations. Considering the slope and voltage dependence of these I-V curves, it appears that tunneling noise is not completely eliminated in the compensated device, even if the peak electric field is decreased. This phenomenon will be investigated further with Arrhenius plots in the next section. The current saturation above its breakdown voltage for each device is due to the series resistance of the device and the space-charge effect [23]. Finally, I-V curves under illumination demonstrate that both devices are sensitive to visible wavelengths.

In addition, DCR versus PDP comparison in Fig. 5(b) shows that the noise in the compensated device is much lower than in the non-compensated device at room temperature (RT). In the compensated device, we observed a factor of 24 decrease in DCR at 2 V excess bias. The high DCR of non-compensated devices is attributed to enhanced tunneling noise due to the narrow depletion region. A $10\times$ increase in DCR between 1 V and 2 V excess bias voltage also supports this statement. We have tested 5 samples of each with and without compensation layer, and the decrease in DCR is systematic in our measurements. The provided DCR values in Fig. 5b correspond to the median values of the 5 tested samples for each case. Furthermore, Fig. 5(b) shows that we achieve similar PDP values in both devices. However, the maximum achievable PDP increases to 49% in the compensated device because of the reduced noise. As in breakdown voltage, DCR and PDP values in the compensated devices might yet differ because of process variability and tolerances. Nevertheless, we consider the HVNW-based compensated SPAD as an optimized version of this configuration where we reduce tunneling noise while still keeping PDP high, thanks to the expansion of depletion region and the drop of peak electric field in the multiplication region. After demonstrating that significantly lower noise is achieved in HVNW doping compensated SPAD, in the remainder of the paper, we will focus on the detailed characterization of this device.

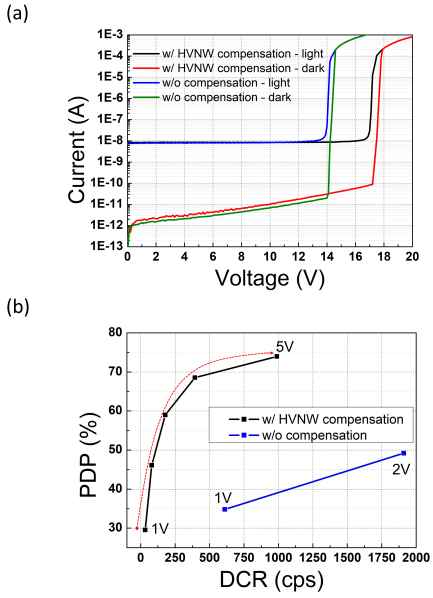

Fig. 5. (a) I-V characteristics with and without doping compensation under both light and dark conditions. (b) Peak PDP vs. DCR comparison between the compensated and not doping controlled N^+/HVPW SPADs at RT.

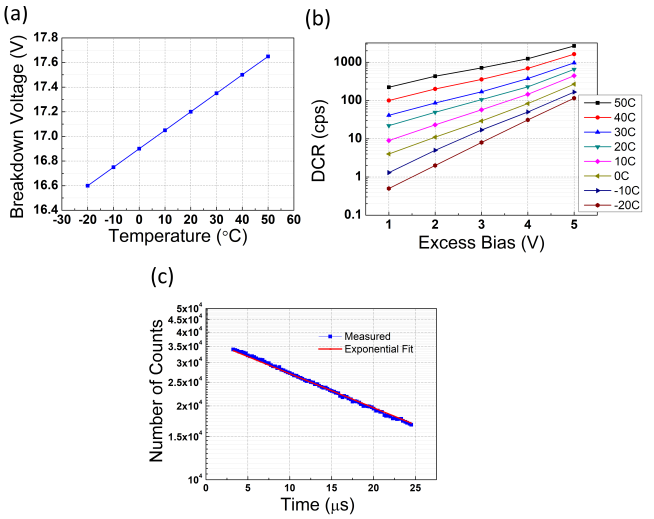

Fig. 6. (a) Breakdown voltage variation with temperature. (b) DCR vs. excess bias curves under different temperatures. (c) Inter-arrival time histogram of the N+/HVPW SPAD with the HVNW compensation.

B. Measurement Results of N+/HVPW SPADs with a Virtual GR and HVNW Compensation Layer

The variation of breakdown voltage with respect to temperature can be seen in Fig. 6(a) where we observe 15 mV change per °C. As expected, the breakdown voltage increases with temperature because electron and hole ionization coefficients degrade due to enhanced phonon scattering. DCR versus excess bias voltage under various temperatures is plotted in Fig. 6(b), where the dead time was set to around 3 μs by means of an externally connected resistor. Measured afterpulsing histogram based on the inter-arrival time method is shown in Fig. 6(c). Afterpulsing probability is defined as the area between the measured and fitted curve divided by the area beneath the fit curve, and it is calculated as 0.15%. At 30 °C, the device has 0.52 cps/μm^2, 2.15 cps/μm^2, and 12.26 cps/μm^2 DCR at 1 V, 3 V, and 5 V, respectively. Furthermore, starting from 10 °C, the increase in DCR is more rapid after 4 V which means that tunneling noise is starting to dominate due to electric field enhancement. However, this crossover is not very obvious in the graphs, which can indicate that either (a) tunneling phenomena is not strong in our devices or (b) it is already contributing significantly. To verify our hypothesis, we made use of Arrhenius plots; the analytic relation between DCR and temperature is exponential and it is given as:

$$DCR\,\alpha\, e^{\frac{-E_a}{kT}}, \tag{2}$$

where k is the Boltzmann constant and E_a is the trap activation energy.

Fig. 7 shows the Arrhenius curves, where it is clear that there is a crossing point at 30 °C, above which thermal generation dominates the noise. This switching point becomes less clear starting from the 4 V excess bias because of tunneling noise, which is a consistent observation seen in Fig. 6(b). In addition, in this figure, the 30 °C crossover point is much clearer even at the high excess bias. At 2 V excess bias, the trap activation energy beyond 30 °C is calculated as 0.68 eV after fitting. Although we observe the same crossover temperature, this activation energy is lower than other reported devices in this technology [24]–[26], in which the authors see 1.1 eV activation energy, indicating that the dominant mechanism is direct thermal generation in their devices [24]–[26]. Also, this high-temperature activation energy in our devices changes with voltage (e.g. 0.43 eV at 5 V). These results indicate that, even at high temperature and under low bias, there is a significant contribution from trap-assisted thermal generation and/or tunneling in our devices, since activation energy shows high field dependency and it is always lower than silicon bandgap. This also explains why our DCR is higher than other reported devices. In order to reduce the DCR further, it is obvious that the defects should be more aggressively handled during processing.

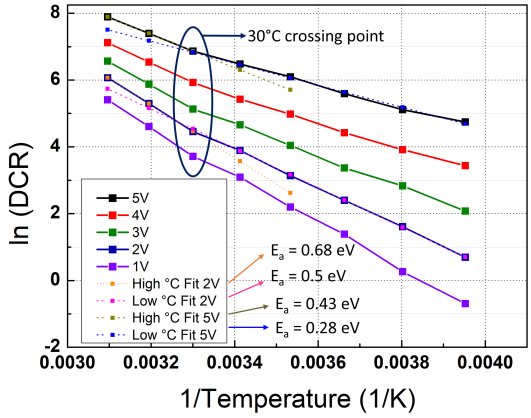

Fig. 7. ln(DCR) vs. 1/K curves from 1 V to 5 V with corresponding activation energies after data fitting.

In order to measure PDP, we utilized the setup introduced in Fig. 8(a). In this configuration, we used a Xenon lamp with a large wavelength spectrum, a monochromator (Newport 74000) with wavelength accuracy and precision of 0.5 nm and 0.11 nm, respectively, to select the wavelength, and an integrating sphere to provide spatially uniform light at the output ports. A calibrated Hamamatsu silicon photodiode (S2281-01) is used as a reference detector to accurately estimate the impinging photon count. PDP measurements taken with this experimental setup are shown in Fig. 8(b). In the PDP calculations, the utilized active diameter of the SPAD was 10 μm, which was determined from the light emission tests in Fig. 4b. This diameter also corresponds to the drawn active diameter in the layout. In this study, we reach around 73% PDP at 440 nm wavelength and 5 V, which is the highest PDP achieved in 110 nm CIS technology, and also with any CMOS-based technology, to the best of our knowledge. As expected from the simulations, the PDP peak occurs at short wavelengths since the junction is very close to the surface, and for the same reason, we also obtain high PDP in the UV region (43% at 350 nm and 5 V). Even though the device is not originally designed for infrared wavelengths, thanks to the high electric field and increased breakdown probability in the depletion region, we observe around 10.5% and 7% PDP at 5 V, and respectively at 800 nm and 850 nm wavelengths.

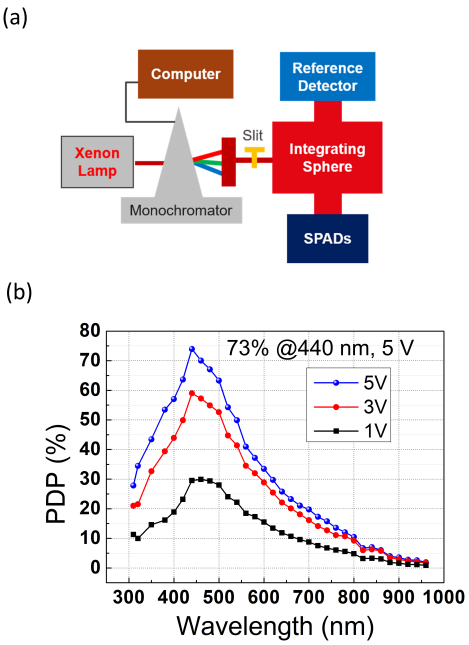

Fig. 8. (a) Experimental setup for PDP measurements. (b) PDP vs. wavelength curves at three different excess bias voltages.

In this study, timing jitter is measured with the time-correlated single-photon counting (TCSPC) technique. In the measurement configuration, fiber-coupled pulsed lasers are used as an illumination source for the SPAD. The source power is attenuated to the single-photon level with the help of absorptive neutral density filters. A Teledyne LeCroy digital oscilloscope is utilized to take the time difference between the laser clock signal and the rising edge of avalanche pulses and to construct the associated histogram. The jitter was measured with 850 nm (A.L.S. GmbH), and 405 nm (PicoQuant LDH-P-C) laser sources at 200 kHz repetition frequency. The histogram recorded at 850 nm wavelength for 3 V and 5 V excess bias voltages is given in Fig. 9(a). FWHM is obtained as 79 ps at 5 V, and it includes also the jitter of the laser source. The total jitter can be expressed as:

$$\sigma_{\text{total}}{}^2 = \sigma_{\text{SPAD}}{}^2 + \sigma_{\text{circuit}}{}^2 + \sigma_{\text{laser}}{}^2, \quad (3)$$

assuming statistical independence of all sources of jitter. After deconvolution of the laser pulse, we obtain a SPAD jitter of 68 ps and 92 ps (FWHM) at 5 V and 3 V of excess bias, respectively. Even if our depletion region is small, there is negligible diffusion tail in the SPAD response. Similarly, in Fig. 9(b), the jitter curve achieved with a 405 nm excitation is provided. The jitter of the SPAD is calculated to be 157 ps after deconvolution. Thanks to the thin multiplication region, the device does not suffer from any diffusion tail effects. Jitter at 405 nm is higher, if compared to that obtained at 850 nm. This observation is consistent with other devices fabricated in 110 nm CIS technology [24]–[26], where jitter increases at shorter wavelengths in both shallow junctions and deep junctions. Acquired FW1/100M values at 850 nm and 405 nm wavelengths are also 371 ps and 490 ps at 5 V, respectively. These low jitter values and lack of diffusion tails render the device appealing for high timing resolution applications, especially whenever high dynamic range is required.

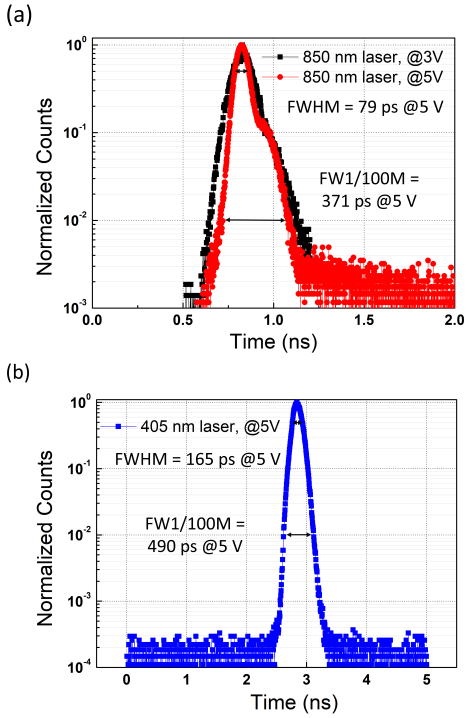

Fig. 9. Jitter measurement results obtained with (a) an 850 nm and (b) a 405 nm pulsed laser.

C. GR Optimization in N⁺/HVPW SPADs with the HVNW Compensation Layer

GR optimization is a critical process in SPAD designs since GRs adjust the electric fields at the device periphery where edge fields have an impact on the leakage current and noise of a SPAD. In this work, we prefer the extension of the N^+ layer to implement a virtual GR. In addition to the layer type, another parameter to check is the width of the GR. As the lateral diffusion lengths of junction layers are usually not exactly known, we inserted different GR sizes in order to optimize the GR. The results presented in sections III.A and III.B were based on 1.5 µm GR, which is the smallest value we achieve. In Fig. 10 and 11, we demonstrate the result of increasing GR width in our N^+/HVPW junction based devices with 10 µm active diameter by providing a comparison between devices with 1.5 µm and 2 µm GR in terms of simulations and experimental results.

Fig. 10(a) and 10(b) relate to the electric field distribution simulation results obtained in TCAD for 1.5 and 2 µm GR devices, respectively. Corresponding GR regions are also shown in each device. Fig. 10(c) shows the electric field magnitude along the dashed cut line in Fig. 10(a), and 10(b). Although there is no change in the electric field inside the multiplication region, the electric field on the GR segment reduces in the device with 2 µm GR. This is an important conclusion of our study, since the generated carriers in the GR region can drift into the multiplication region and trigger additional avalanche

multiplication processes which result in the increase of both noise and sensitivity.

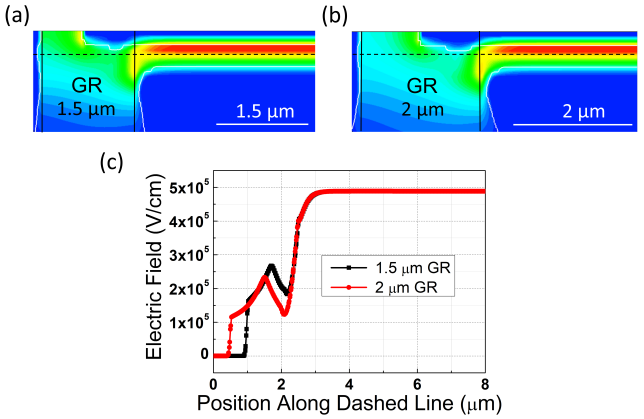

Fig. 10. Electric field distributions of the SPADs at the breakdown voltage with (a) 1.5 μm GR and (b) 2 μm GR. (c) Electric field magnitude taken at the breakdown voltage along the black dashed lines in both devices.

Fig. 11(a) shows the negligible change of breakdown voltage between the devices, which indicates that the electric field in the center of the multiplication region does not vary with GR size. However, from the dark I-V curve, we observe that the dark current of the device with large GR is almost flat with voltage. Since the main junction (N^+/HVPW) forming the avalanche region does not change, we can easily conclude that the additional dark current is introduced by the diodes (N^+/P-epi) in GR regions. Considering the high dependency of its dark current to the voltage and the slope of its I-V curve, we can also say that there is additional tunneling in device with small GR.

In Fig. 11(b), the DCR comparison of these devices is given. We can deduce that the difference in DCR is originated from the same tunneling effect where more carriers can drift to the avalanche region from GRs because of the higher electric field. Furthermore, tunneling crossover in the depletion region is much more obvious at 4 V in devices with large GR, indicating that the effect of tunneling in GRs was rather weak up to 3 V of excess bias. PDP of the 2 μm GR device is provided in Fig. 11(c). In this device, we achieve 59% PDP at 440 nm and 5 V. By comparing this result with Fig. 8(b), we can say that with 1.5 μm GR, photo-generated carriers near the peripheries can drift more effectively thanks to the higher electric field. On the other hand, the noise is also higher which signifies the tradeoff between DCR and PDP with respect to the electric field.

IV. Comparison with State-of-the-Art

In Table 1, we present the comparison between our novel SPADs implemented with doping compensation and other state-of-the-art SPADs produced in the 110 nm CIS technology node. In Fig. 12(a), and 12(b), DCR per unit area versus peak PDP is given for both front-side (FSI) and back-side-illuminated (BSI) SPADs; this includes not only SPADs fabricated in any CIS technology, but also the best SPADs achieved in any CMOS technology. To the best of our knowledge,

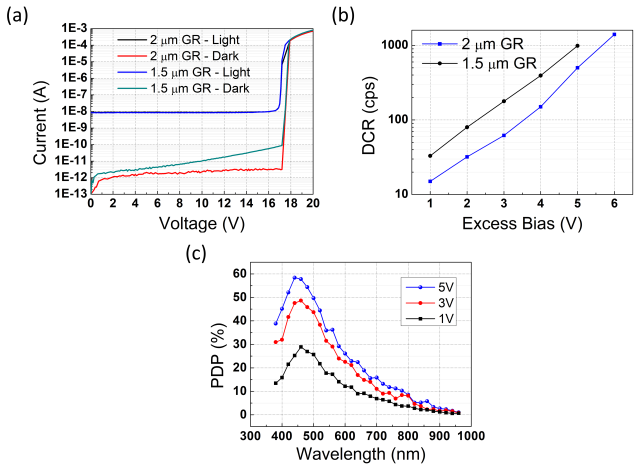

Fig. 11. Comparison of the GR widths in the compensated SPAD in terms of (a) I-V, (b) DCR vs. excess bias voltage, (c) PDP vs. wavelength at different excess bias voltages.

our SPAD with 1.5 μm GR demonstrates the highest PDP (73%) in any CMOS technology. The peak wavelength of our SPAD at 440 nm is the shortest among those surveyed. The proposed devices also have the lowest breakdown voltage and highest electric field, which increases avalanche triggering probability. This leads to an increase in tunneling noise, but also enhancement of PDP as measured in our SPAD structures. Yet, according to Fig. 12(a), our 2 μm GR SPAD can provide the lowest noise if 50% PDP is acceptable. Another aspect of this work worth mentioning is that our NUV efficiency is also very high (30% at 300 nm), thanks to the junction, which is formed very close to the surface.

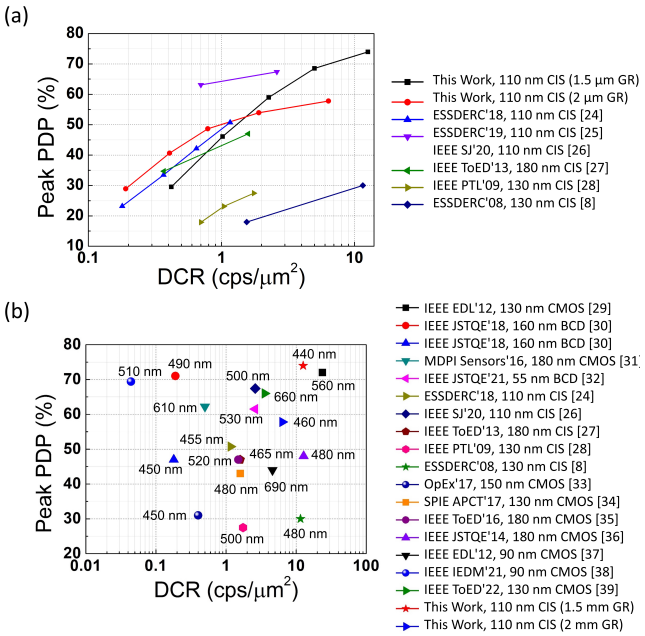

Fig. 12. Peak PDP vs. DCR comparisons of state-of-the-art FSI and BSI SPADs (a) fabricated with CIS technologies under various voltages, and (b) fabricated in various technology nodes with their corresponding peak detection wavelength.

TABLE I
SUMMARY OF ALL PERFORMANCE PARAMETERS OF STATE-OF-THE-ART SPADS FABRICATED IN 110 NM CIS TECHNOLOGY

	This Work (1.5 μm GR) @ 5 V	This Work (2 μm GR) @ 5 V	[24] @ 5 V	[25, 26] @ 5 V
Technology	110 nm CIS	110 nm CIS	110 nm CIS	110 nm CIS
Junction	N^+/HVPW with HVNW	N^+/HVPW with HVNW	P^+/LDNW with DNW	P^+/DNW
GR	Virtual	Virtual	Virtual	Polysilicon
Active Area (μm^2)	78.5	78.5	385	78.5
$V_{breakdown}$ (V)	17.2	17.2	20	18
DCR (cps/μm^2)	12.6	6.3	1.16	2.61
PDP Peak	73% @ 440 nm	58.4% @ 440 nm	50.7% @ 455 nm	67.4% @ 500 nm

V. CONCLUSIONS

In this paper, we presented novel SPAD structures designed in 110 nm CIS technology. The SPAD is based on an N^+/HVPW junction with a virtual GR. The active area of every measured SPAD is 78.5 μm^2. Since the initial design utilizes two highly-doped layers, we observe a very thin depletion region and a very high electric field in the simulations. This causes an increase in the noise of a device because of the favored tunneling rates. Therefore, in order to reduce the electric field in the multiplication region, we used doping compensation technique, which allowed us to adjust the doping profile in the structure. Compensation layer doping is chosen according to the peak concentration of the HVPW layer so as to decrease hole concentration in it. In this study, we used deep HVNW layer, which decreased the electric field and the tunneling noise while still keeping PDP high and increasing the breakdown voltage only by 3.2 V, but the final electric field magnitude and device performance are subject to process variability, as this will determine the resulting doping profile after compensation. In the HVNW compensated device, we reduced the DCR by a factor of $24\times$ at 2 V excess bias voltage compared to the non-compensated device. Moreover, the maximum achievable PDP was enhanced by 49% thanks to the much lower noise and being able to operate the device at higher voltages. To the best of our knowledge, we showed the highest PDP (73% at 440 nm) achieved with any CMOS technology. PDP in the NUV region is also very high ($> 30\%$ at 320 nm, 5 V) thanks to formed depletion very close to the device surface. Due to high triggering probability, PDP in NIR is yet acceptable (10.5% and 7% at 800 nm, 850 nm, 5 V) even though the device is not originally designed for this spectrum. The timing jitter of the device was measured at 68 ps, at 850 nm, and 5 V of excess bias. It is clear that the noise can be improved further with a higher concentrated compensation layer since tunneling is still contributing. Nevertheless, these results prove that, with the doping compensation, we offer a new pixel architecture for next-generation RGB-Z type CMOS cameras, where Z pixels can operate in either UV or NIR, and problems such as adjusting exposure time for all spectrum or reduced color resolution under low light conditions can be further solved at the device level with higher detection efficiency. Thanks to the tunability of the doping profile offered by the compensation technique, we believe we can further lower noise while keeping PDP at the same levels. These results demonstrate that the proposed doping compensation technique is applicable to SPADs and that it can be generalized to any CMOS/CIS technology node. In particular, as the CMOS technology node shrinks, higher doping concentrations of available layers will be a challenge to reduce noise in thinner junctions. Therefore, we believe that doping compensation will alleviate these issues, so as to achieve devices with enhanced performance in the near future.

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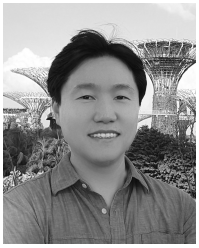

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