A Back-Illuminated SPAD Fabricated With 40 nm CMOS Image Sensor Technology Achieving Near 40% PDP at 940 nm

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***Abstract*—This article introduces a back-illuminated (BI) single-photon avalanche diode (SPAD) based on 40 nm CMOS image sensor (CIS) technology which is the most advanced technology node for the fabrication of a SPAD up to date. It's based on a P-well (PW) and deep N-well (DNW) junction, and the DNW is deeply implanted to form a wide absorption region resulting in very high and wide photon detection probability (PDP). Thanks to the retrograde DNW, the premature edge breakdown phenomenon is completely prevented and the whole area of the planar junction becomes a high-efficient avalanche multiplication region. In addition, an anti-reflection coating on the backside of the SPAD and a metal reflector at the bottom reduce the reflection of incoming photons and improve the efficiency at long wavelengths, respectively. With the most advanced CIS technology for BI SPADs, the presented SPAD accomplishes a dark count rate (DCR) of 70 cps/μm^2, peak PDP of 81% at 675 nm, and PDP of 39% at 940 nm. The timing jitter is 79 ps full width at half-maximum width (FWHM), which is the best timing jitter performance among BI SPADs reported so far. All the values are obtained with the excess bias voltage of 6 V.**

***Index Terms*—Avalanche photodiode (APD), back-illuminated single-photon avalanche diode (SPAD), CMOS image sensor (CIS) technology, detector, diode, Geiger-mode avalanche photodiode (G-APD), high-volume manufacturing, integrated optics device, integrated optoelectronics, integration of photonics in standard CMOS technology, light detection and ranging (LiDAR), near infrared (NIR), optical sensing, optical sensor, photodetector, photodiode, photomultiplier, RGB-D sensor, semiconductor device, sensor, silicon, wafer-scale integration.**

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I. Introduction

As single-photon avalanche diode (SPAD) based sensors have proven their feasibility in various scientific and industrial applications which require high sensitivity, they have been getting a lot of attention [1]–[4]. In addition, the development of SPADs in deep-submicron CMOS technologies enables the capability of monolithic integration with on-chip electronics that perform the functions of time-resolved measurement and histogram process required for time-correlated single-photon counting (TCSPC) and consequently large arrays, while reducing production costs. As a result, the CMOS-based SPAD sensor solutions are being applied to various applications requiring time-resolved imaging, such as light detection and ranging (LiDAR) to control and navigate autonomous vehicles [3]–[6], airborne laser mine detection system (ALMDS) to identify a target in military applications [7], service drones [8], machine vision [9], security, and biomedical imaging including fluorescence lifetime imaging (FLIM) [10], positron emission tomography (PET) [11], and near-infrared optical tomography (NIROT) that can diagnose the human brain and body [12]. One challenge of the CMOS-based approach is that the on-chip electronics occupy a considerable area and it becomes more severe as more functionalities like counting, timestamping, processing, and compression are required, which results in a small area to implement the SPAD, i.e., low fill factor (FF) [13], [14]. Such a trade-off not only limits the spatial resolution of a SPAD sensor but also increases the chip size and cost. In order to overcome the trade-off, a possible solution is using a more advanced CMOS technology. A SPAD in a deeper-submicron CMOS technology has a comparative advantage in terms of power consumption as well as FF, but it still suffers from the space problem with the on-chip electronics. Furthermore, as the doping concentrations increase as the technology node decreases, the available depletion regions become narrower, resulting in a high tunneling noise and low and narrow photon detection probability (PDP). Another critical issue with the CMOS-based SPAD sensor solutions is that the PDP in the near-infrared (NIR) range is low, and unlike the fill-factor problem it cannot be dramatically improved even if an advanced CMOS technology is utilized [15], [16]. The reason is that the

TABLE I
PERFORMANCE COMPARISON OF STATE-OF-THE-ART FI AND BI SPADS

	[15]	[16]	[23]	[24]
Type	FI	FI	BI	BI
V_B [V]	22	31.5	30	22
V_E [V]	6	7	2.5	3
Peak PDP [%]	55 (@ 480 nm)	62 (@ 530 nm)	69.4* (@ 510 nm)	50.5** (@ 800 nm)
PDP @ 940 nm [%]	3.2	4.2	24.4*	20.5**

PDE with *microlens and pyramid surface or **microlens and light trapping.

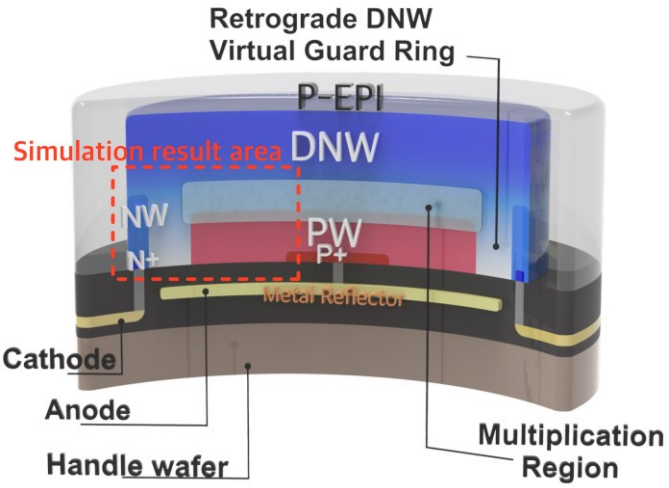

Fig. 1. Cross-section of the proposed BI SPAD.

PN junctions are usually formed within 1~3 μm under the surface while the penetration depth of NIR in Si is much deeper than the junctions.

A recent paradigm shift in CMOS SPADs is the development of back-illuminated (BI) SPADs in CMOS image sensor (CIS) technology compatible with three-dimensional stacking technology. The stacking technology places the CMOS circuitry under the SPAD array so that significantly improves the FF while enabling higher functionality, lower power consumption, and larger array production. In addition, since it is possible to select and utilize a more appropriate CMOS technology for the top-tier and bottom-tier chip, respectively, the SPAD can avoid the negative effects caused by high doping concentrations, and as a result, dark count rate (DCR) and PDP can be significantly improved. Furthermore, as the top-tier chip is fabricated a BI CIS technology, the junction of the SPAD is formed at a deeper position compared to that of the front-illuminated (FI) case, and thus higher PDP can be achieved in the NIR wavelength range. To date, there have been several attempts on the BI 3D-stacked SPADs and various results have been reported [17]–[24]. Table I shows the performance comparison between FI and BI SPADs reported lately, and it clearly shows that the SPAD PDP at 940nm can be greatly increased with the BI approach.

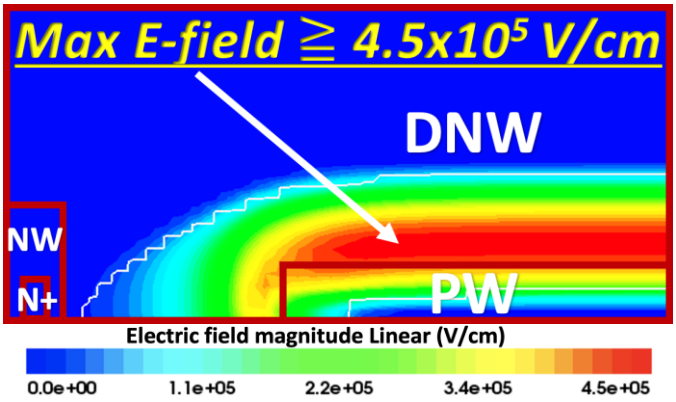

Fig. 2. TCAD simulation result for the BI SPAD: E-field profile at V_E = 1 V.

Although these attempts report substantial performance improvement, especially in NIR efficiency, it can be increased further, and particularly the timing jitter performance should be improved to achieve a better depth resolution of SPAD-based sensors.

In this paper, we present and fully characterize a single BI SPAD fabricated in 40 nm CIS technology which is the most advanced CIS technology for SPAD fabrications. Thanks to the wide absorption region, high E-field at the planar junction enabling efficient avalanche multiplication, optimized backside etching/thinning, and the use of a metal reflector and anti-reflection coating (ARC), the proposed SPAD achieves an excellent peak PDP of 81% at the wavelength of 675 nm along with high PDP in the NIR wavelength range. In addition, it achieves the best timing jitter, 79 ps at the full width at half maximum (FWHM) among the BI SPADs reported so far. This article is organized as follows. In Section II, the SPAD structure and its TCAD simulation result are explained. Section III presents the full characteristics of the SPAD including a demonstration of the active area, I-V characteristics, noise, temperature dependence, sensitivity, and timing performance. Section IV concludes this paper.

II. SPAD Structure and TCAD Simulation

Fig. 1 shows the cross-section of the proposed BI SPAD fabricated in SK hynix 40 nm CIS technology. The SPAD is based on a P-well (PW) and deep N-well (DNW) junction, and a virtual guard ring (GR) based on the retrograde DNW surrounds the junction to prevent the premature breakdown at the edge of the junction. The SPAD is implemented in a round shape with a 5 μm diameter active area, 2 μm GR, and 0.5 μm cathode, resulting in a FF of 25%. The GR and cathode sizes were chosen as conservative design parameters, and therefore the FF can be improved in future generations with optimized parameters and the use of microlens. In addition, it can be further improved by sharing the cathode between SPADs. The thickness of the Si epi layer remained after the backside etching/thinning process is optimized considering the absorption coefficient in silicon and the depth of DNW.

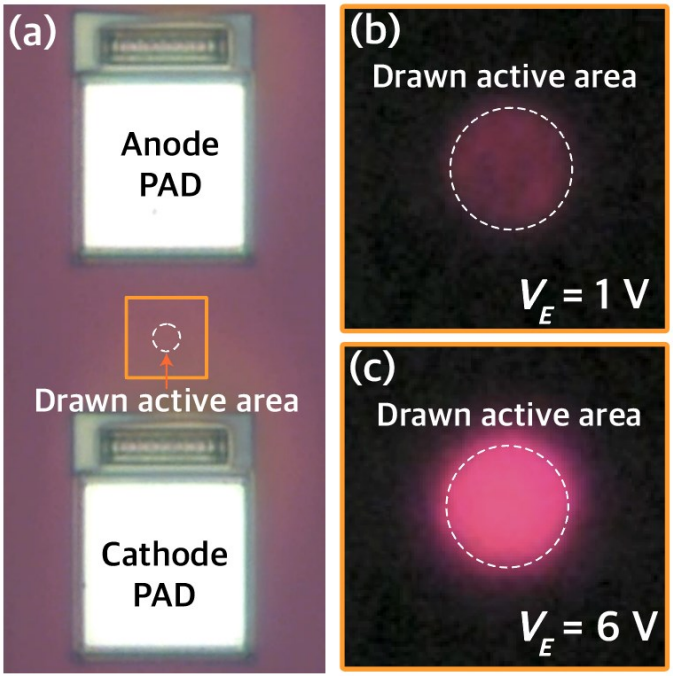

Fig. 3. (a) Micrograph of the BI SPAD and light-emission-test results at V_E = (b) 1 V and (c) 6 V.

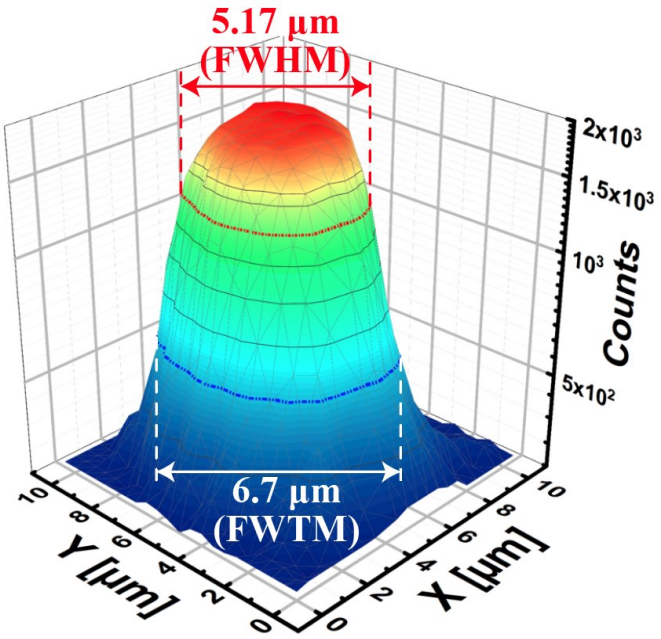

Fig. 4. Laser-scanning-microscope result of the BI SPAD: 3D-plot at V_E = 4 V.

Through this process, the BI SPAD is able to achieve a wide spectral range as well as high efficiency. In addition, thanks to the metal reflector that covers the active area completely and the ARC formed on the top of the SPAD backside, the detection efficiency can be further improved.

In order to demonstrate the depletion region and E-field profile, TCAD simulation was performed at the excess bias voltage, V_E, of 1 V. The simulation area in Fig. 2 corresponds to the red-dashed square in Fig. 1. Thanks to deep and retrograded DNW, the virtual GR prevents the premature edge breakdown completely so that a wide avalanche multiplication region is uniformly formed at the planar PW/DNW junction, which contributes to achieving a high and wide efficiency along with the wide depletion region over 1 µm and broad absorption region based on the lightly-doped deep DNW.

III. Experimental Results

Fig. 3(a) shows the micrograph of the BI SPAD having an anode and cathode pad which is used for experiments in this paper. Figs. 3(b) and (c) show light-emission-test results at V_E = 1 V and 6 V, respectively. The area emitting light clearly indicates that the SPAD does not suffer from any premature edge breakdown and has a uniform and high E-field over the active area. In order to investigate more precisely the effective active region where a photon-generated carrier can trigger an avalanche multiplication, a measurement with a laser-scanning microscope was performed. The laser beam passes through the optical system and reaches the scanning equipment consisting of a single Galvo mirror that can scan the X-Y axis. When the single Galvo mirror scans over the SPAD, the number of

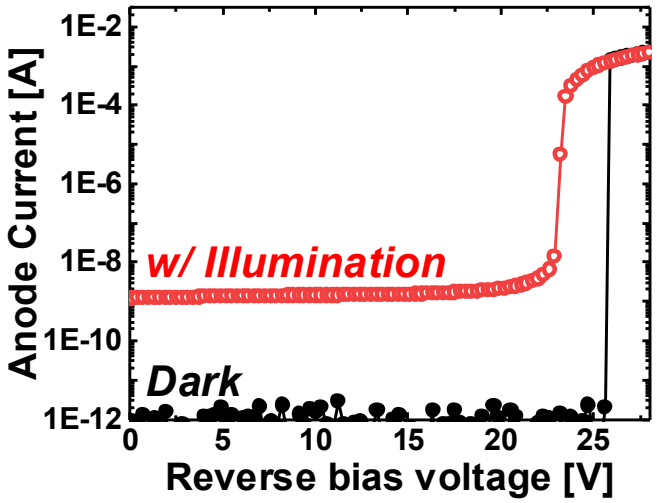

Fig. 5. I-V characteristics of the BI SPAD without and with illumination at room temperature.

SPAD output pulses varies depending on the location of the laser, and the number of the pulses is measured with an oscilloscope in real-time. The result is shown in Fig. 4 at V_E = 4 V with a 637 nm continuous laser. It clearly demonstrates that the avalanche multiplication occurs over the whole active area and the FWHM is about 5.2 µm. This result proves again that the proposed SPAD does not suffer from premature edge breakdown, matching well with the TCAD-simulation and the light-emission-test results shown in Figs. 2 and 3, respectively. The full width at tenth maximum (FWTM) is about 6.7 µm, which means that some of the photon-generated carriers at the GR region contribute to the avalanche multiplication.

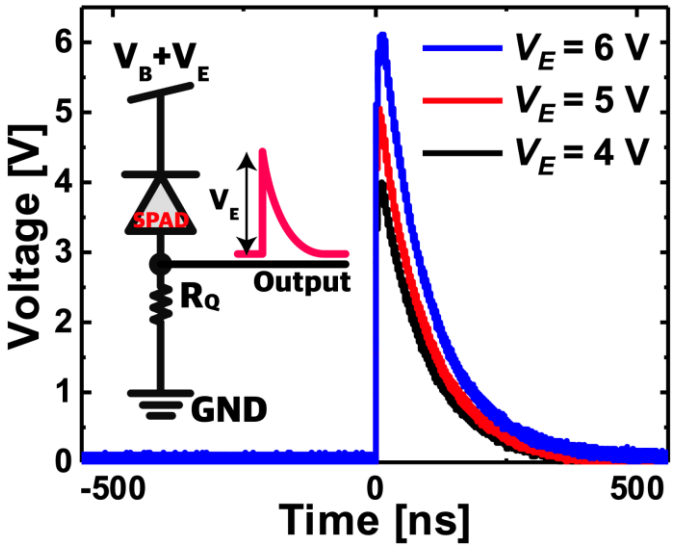

Fig. 6. Output waveforms of the device at three different bias conditions.

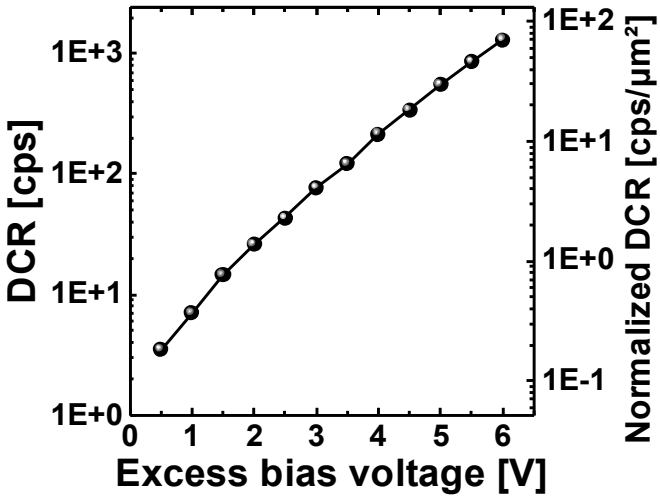

Fig. 7. DCR and normalized DCR of the BI SPAD versus V_E at room temperature.

The I-V characteristics of the SPAD in Fig. 5 show that the breakdown voltage is about 23.2 V and the SPAD has very low dark currents below 1 pA, which is the minimum limit of the measurement setup at room temperature. The breakdown in the dark condition occurs at a larger reverse bias voltage than under illumination, and it indicates that the number of dark carriers is low, which should result in a low DCR performance.

The inset of Fig. 6 shows a simple schematic for measuring the proposed SPAD. An external passive quenching resistor of 200 kΩ was used to measure the output voltage pulses, and a reverse bias voltage was applied to the cathode. The measurements were performed with a high-performance digital oscilloscope. Although the measured pulse widths are a little wide due to the external capacitance components, it can be seen that the height of each output pulse matches well with the applied V_E.

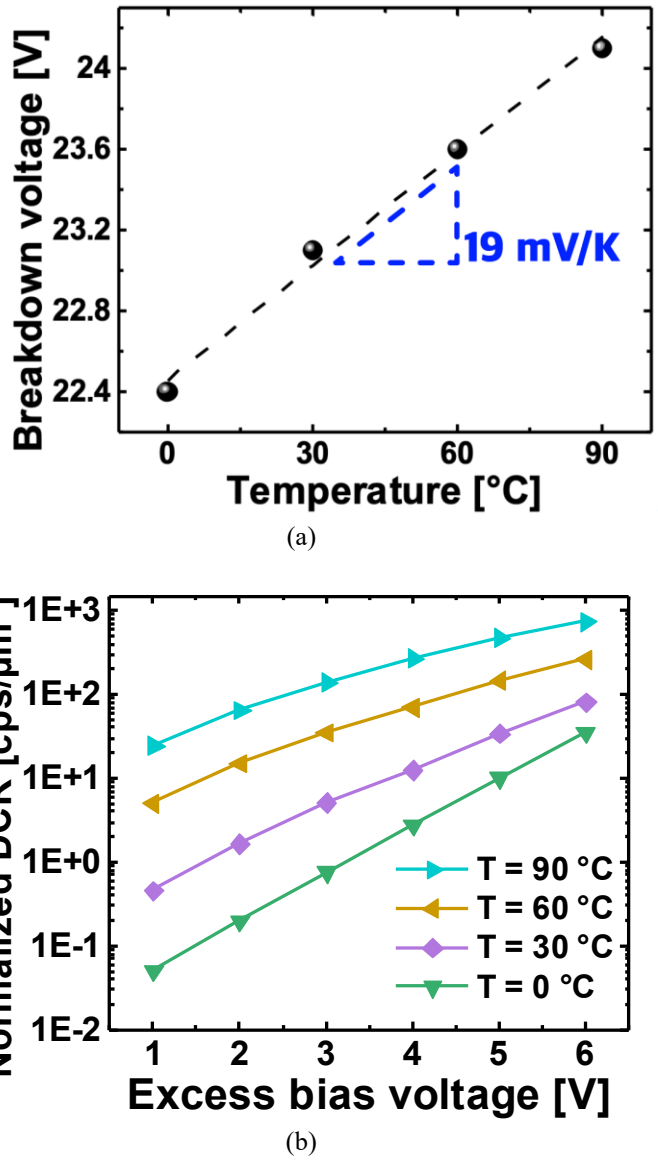

Fig. 8. Temperature-dependent-measurement results: (a) breakdown voltage variation versus temperature and (b) normalized DCR versus V_E at four different temperatures.

DCR measurement was performed at room temperature as a function of V_E, from 0.5 V up to 6 V, and the result is shown in Fig. 7. The SPAD exhibits a low DCR, about 0.2 cps/μm^2 at V_E = 0.5 V, and therefore V_E can be increased to enhance the PDP performance. At V_E = 6 V, it still shows below 100 cps/μm^2 DCR. One of the factors increasing DCR in the BI SPAD is the dangling bonds on the Si epi surface after the backside etching/thinning process. However, thanks to the structural advantage of the proposed SPAD, i.e., isolating the SPAD active region from the P-epi using DNW, the SPAD is not exposed to the dangling-bond defects so that it can achieve a low DCR even at the high excess bias condition.

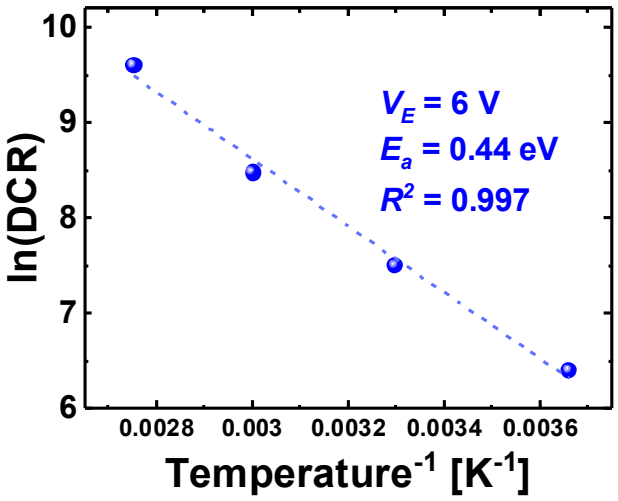

Fig. 9. Arrhenius plot with extracted activation energy and the coefficient for the curve fit at V_E = 6 V.

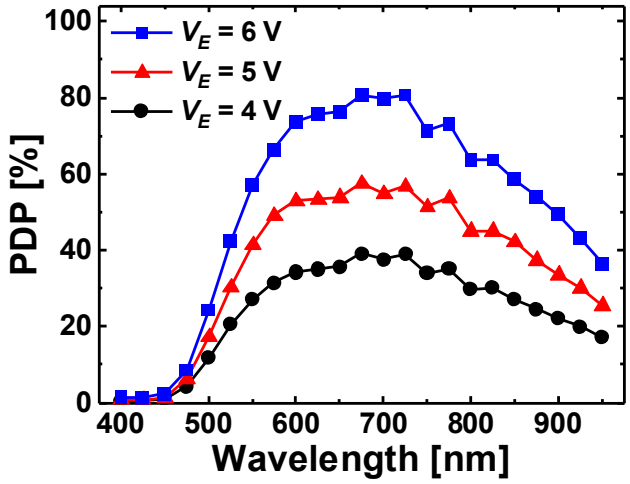

Fig. 10. PDP spectra of the BI SPAD at three different V_E.

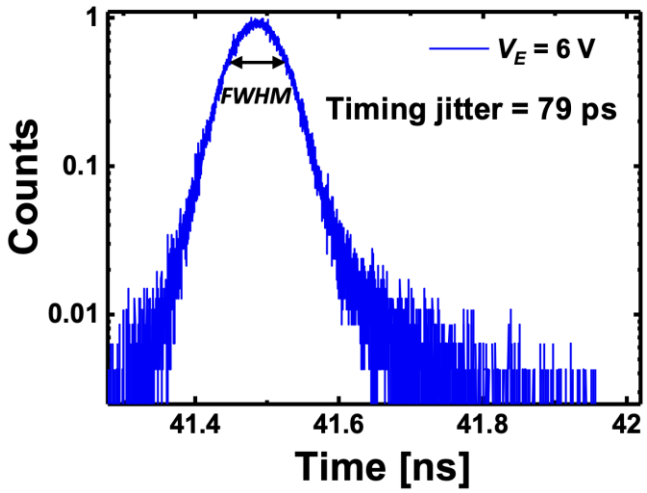

Fig. 11. Timing jitter of the BI SPAD at V_E = 6 V when using a 940 nm picosecond pulsed laser.

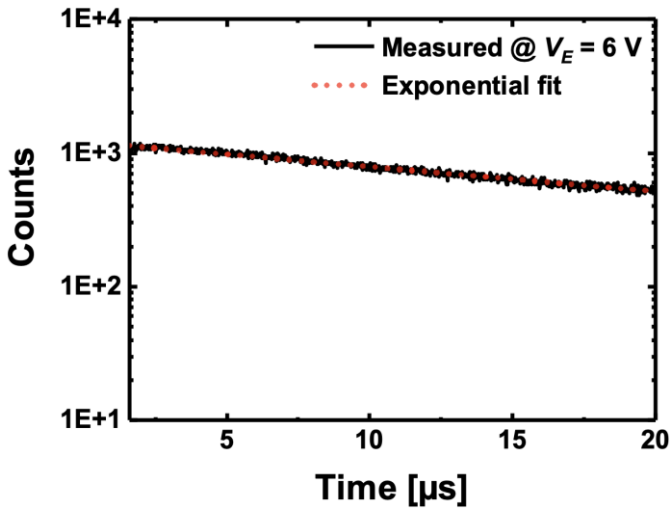

Fig. 12. Inter-avalanche time histogram measured at V_E = 6 V along with a fitted exponential curve.

The temperature dependence of the breakdown voltage was investigated from 0 to 90 ℃ with a temperature chamber, and the results are shown in Fig. 8(a). The temperature coefficient of the breakdown voltage is about 19 mV/K. The DCR was also characterized at different temperatures, from 0 to 90 ℃, and the device shows acceptable DCR, below 1 kcps/μm^2, even at 90 ℃ as can be seen in Fig. 8(b). The measurement results indicate the main contributor to its DCR is the trap-assisted thermal generation, and this can be confirmed by the activation energy, E_a, extracted from the Arrhenius plot depicted in Fig. 9. The extracted value is 0.44 eV at V_E = 6 V, and it implies that the traps can be generated by the implantation of phosphorus [25].

Fig. 10 shows the PDP spectra of the BI SPAD for V_E from 4 to 6 V. The SPAD achieves a peak PDP of 81% at 675 nm and PDP of about 39.2% at 940 nm at V_E = 6 V. It is notable that the cut-off wavelength in PDP appears at around 450 nm, and it corresponds to the penetration depth of about 400 nm in silicon. It means that the remaining P-epi thickness above the deep DNW after the backside etching/thinning process is just about 400 nm, which was done by considering the photon absorption coefficient and the deeply formed DNW. Therefore, the SPAD can collect most of the photon-generated carriers, achieving a wide spectral range and very high PDP. Such performance will play a key role in many applications that require high PDP.

The timing-jitter measurements were performed at room temperature. A 940 nm picosecond pulsed laser was used as the laser source and a high-performance oscilloscope providing TCSPC function was used to measure the time difference between the laser triggering pulse and the SPAD output pulse. Fig. 11 shows the result of normalized histogram values on a log scale. The result shows the FWHM value at V_E = 6 V and the result is 79 ps. The excellent timing jitter of this SPAD is achieved thanks to the wide and high E-field at the junction and the DNW blocking diffused carriers from the P-epi.

Fig. 12 shows the inter-avalanche time histogram of the SPAD at V_E = 6 V. Although the dead time is relatively large, about 1.6 μs, because the measurement was conducted by using an external passive quenching resistor, it can be greatly improved with an integrated active recharge circuit. As the measured histogram is well matched with the exponential curve, which indicates the Poissonian nature of the SPAD output pulses, it suggests that the afterpulsing probability is negligible with a dead time longer than 1.6 μs.

IV. Conclusion

We demonstrate a high-performance BI SPAD fabricated in 40 nm CIS technology. Through the TCAD simulation, light-emission test, and laser-scanning microscope, the avalanche multiplication area is clearly demonstrated, and the device is fully characterized, including temperature-dependent noise characteristics. The thickness of the Si epi selected in considering both the depth of avalanche multiplication region and photon absorption coefficient enabled wide-spectral PDP and best timing jitter. Thanks to the wide absorption region, high and wide E-field at the planar junction, optimized backside process, metal reflector, and ARC, the proposed SPAD achieves a DCR of 70 cps/μm^2, peak PDP of 81%, PDP of 39.2% at 940 nm, and timing jitter of 79 ps at V_E = 6 V. The SPAD achieves, to the best of our knowledge, the highest PDP and the lowest timing jitter among reported BI SPADs so far. We expect that this SPAD can play a key role in various applications.

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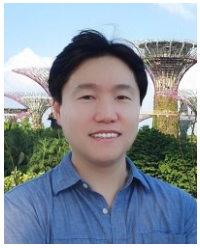

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