A Single-Source Switched-Capacitor-Based Step-Up Multilevel Inverter With Reduced Components

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***Abstract*—Switched-capacitor-based multilevel inverters (SC MLIs) have received a great deal of interest that reduces the dc source requirement and improves the power quality. However, multiple dc sources and the requirement of a large number of switches to generate a high-quality boost output are the fundamental issues in the SC MLIs. This article presents a step-up 17-level SC MLI using reduced number of switches, three capacitors, and a single dc source. The steady-state voltage across the capacitors is maintained in the ratio 1:2:0.5 that contributes to quadruple boosting ability without using any auxiliary capacitor voltage balancing circuit. Besides, lower switch count in the conduction path and operation of 50% of the switches at fundamental frequency ensures total power loss reduction in the proposed circuit. A comparative assessment with recently developed 17-level MLIs in terms of the number of components, gain, stress, and cost factor elucidates the advantages of the proposed MLI. After a detailed circuit analysis and loss evaluation, simulations are performed to verify the step-up and inherent balancing features of the proposed MLI. Further, using both the fundamental frequency and high-frequency switching techniques, extensive experimental test results are presented under different transient conditions to validate the operational feasibility of the 17-level prototype.**

***Index Terms*—Multilevel inverter (MLI), reduced components, self-voltage balance, single-source, switched-capacitor (SC), voltage gain.**

I. Introduction

DEVELOPMENT of multilevel inverters (MLIs) has been a recent trend for a variety of low-, medium-, and high-power applications [1]–[5]. This is due to the competence of MLI in generating a sinusoidallike output using the combination of switches and dc sources. Diodes and capacitors are the additional components used in the MLI to strengthen structural flexibility. MLIs are used in different applications that include photovoltaic (PV) systems, electric vehicles, STATCOM, traction drives, high-frequency power distribution, etc. [5]–[7] to enhance the power quality, efficiency, and reliability. Popular MLI topologies are the neutral-point clamped (NMLI), flying-capacitor MLI (FMLI), and cascaded H-bridge MLI (CMLI). Both the NMLI and FMLI are subjected to voltage balancing problems and collapsing of the whole module due to the series connection of switches [6], [8]. CMLI, on the other hand omits the requirement of additional clamping diodes/capacitors. However, the requirement of large number of semiconductor devices remains a concern in these MLIs for generating higher voltage levels at the output. Based on the requirement and application, CMLI can be operated using equal (symmetrical), unequal (asymmetrical), and varying dc sources [9], [10]. Symmetrical MLIs have simpler control while the asymmetrical structures can increase the voltage levels using less number of dc sources. The CMLI structure in [5] is equipped with capacitors in one of the modules to reduce the number of dc sources. Even though this circuit creates five levels at the output, the boosting factor (ratio of the output voltage to input voltage) is still one. The voltage boosting is elemental in PV systems to match the output voltage with the grid/load requirement.

Several structural modifications have been done in recent years to reduce the number of switches, dc sources, and control complexity [7], [11]. These structures can be broadly classified into two types, i.e., reduced source switched-capacitor (SC)-based boost type topologies and multi-dc nonboosting MLIs. The switched-source and switched-diode MLIs without the inherent boosting feature are esteemed as the nonboosting type MLIs. Toward an attempt to reduce the number of dc sources, structures are developed in [12] and [13]. The input voltage is equally distributed among the capacitors, which appear across the load and consequently lack the ability to boost the output. The circuit proposed in [14]–[16] for the renewable energy application uses series diodes in the conduction path. Thus, their operation in highly inductive loads is unfeasible. However, the voltage level enhancement integrating a floating capacitor is an additional advantage of the circuit proposed in [14]. An additional switch in [15] can eliminate the voltage spike appearing due to the inductive loads only in the first voltage step.

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The MLI presented in [17] is suitable for PV systems. However, the circuit requires multiple input sources identical to the conventional CMLI. The above-discussed structures embody a back-end H-bridge for generating the negative levels. Excluding the full bridge, potential nonboosting structures are disclosed in [18]–[20], which reduce the voltage stress significantly.

Apart from this, significant research interest is growing in recent years to develop SC MLIs with inherent boosting ability. Voltage balancing of SCs without auxiliary sensors and voltage boosting without additional inductor/transformers makes the SC MLIs suitable for the PV applications and high-frequency ac power distribution [8], [21]–[23]. The MLI topologies presented in [24]–[26] use the same basic unit to generate high output voltage levels using reduced number of components. The basic unit consisting of one dc source and a capacitor can create a two-step twofold boosted output. The charging of the capacitor in parallel and discharging in series with the source enables self-voltage balancing. Single-phase extension of these circuits requires more number of dc sources. On the other hand, this offers an opportunity to increase the voltage levels (17-level, 25-level, 49-level, 81-level) by operating the MLI in symmetrical as well as asymmetrical modes. A novel basic module proposed in [27] synthesizes nine-level twofold boost output using a single dc source. However, the extended version of this structure requires multiple dc sources. SC MLI introduced in [28] requires a number of series-connected dc sources to obtain the desired output. The basic module of the disclosed structure in [29] can produce threefold three-step output. However, the switch count and the number of dc sources increase when high-quality voltage is intended to be produced at the output.

Most recent research also involves the design of SC MLIs with single input even in the extended forms. Charging spike in SCs is addressed in [23] by developing such MLI with a quasi-resonant front-end structure integrated with a back-end full bridge. All the capacitors are equally charged and the input voltage is divided among the capacitors. Consequently, this topology lacks in boosting the voltage. The MLI circuits proposed in [30] and [31] reduce the voltage stress satisfyingly at the cost of a large number of circuit components. Research effort is also made in [32] to develop a single-dc hybrid NMLI-based structure to reduce the stress on the switches while generating 7-level, 9-level, and 11-level output. However, the voltage gain in 11-level inverter is limited to 2.5 times the input voltage. Recently configured MLIs in [22], [33], and [34] attain high voltage gain (six times, four times, and three times) using lower number of components. Conventional H-bridge is not required in these circuits to generate the ac voltage output. Including further extension to the nine-level circuit proposed in [22] toward voltage quality improvement using a lower number of components, an improved SC MLI is proposed in this work with the following prominent features.

1) Single dc source is required to generate a 17-level output.
2) Only 12 switches and three capacitors are used in the circuit.
3) The capacitor voltages are self-balanced without auxiliary sensors/closed-loop controller.
4) Four times boosting ability of the circuit ($V_o = 4V_{\text{in}}$).

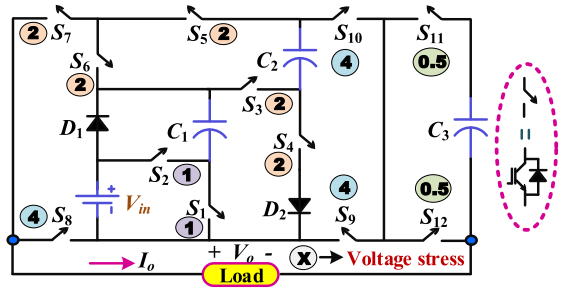

Fig. 1. Proposed 17-level SC MLI topology.

5) More than 50% of switches operate at a low frequency; as a result, switching loss is reduced.
6) The proposed circuit can adequately operate under any loading power factor (PF).

The next section introduces the proposed topology as well as the capacitor sizing and self-balancing mechanism. The power loss analysis is discussed thoroughly in Section III. A comparison with the recent-art MLIs in Section IV confirms the structural advancement. Followed by a detailed discussion on the modulation scheme in Section V, Sections VI and VII present extensive simulation and experimental investigation, respectively, to validate the workability of the 17-level SC MLI. Concluding remarks are provided in Section VII.

II. SC MLI Topology and Its Operational Principles

The proposed 17-level SC MLI circuit is shown in Fig. 1. The proposed circuit consists of 12 switches (S_1–S_{12}), three capacitors (C_1–C_3), two diodes (D_1 and D_2), and a single dc power supply (V_{in}). All the switches have an antiparallel diode connected across it. The circuit produces a 17-level quadruple boost output (0, $\pm 0.5V_{\text{in}}$, $\pm 1V_{\text{in}}$, $\pm 1.5V_{\text{in}}$, …, $\pm 4V_{\text{in}}$) without using an H-bridge for changing the polarity. The switch pairs $S_1 - S_2$ and $S_{11} - S_{12}$ are complementary, thus reduces the control complexity. The switches S_5–S_{10} operate in fundamental frequency and switch pair $S_3 - S_4$ operates at lower frequency, which results in low switching losses. In addition, the voltage stress across each switch in Fig. 1 implies that only three switches S_8–S_{10} withstand peak load voltage stress. The ratio of voltage across the capacitors C_1, C_2, and C_3 (V_{C1}:V_{C2}:V_{C3}) is naturally maintained at 1:2:0.5 in the steady state. To verify the inherent balancing of the capacitors, the operation of the 17-level SC MLI is analyzed hereafter.

In the positive half-cycle of the output voltage, the first voltage step ($+0.5V_{\text{in}}$) is produced by discharging only the capacitor C_3. The second voltage step ($+V_{\text{in}}$) is produced by including the source voltage in the load current path and bypassing the capacitor C_3. During this, the diode D_1 is in forward conduction and the voltage across the capacitor C_1 is clamped to V_{in} by turning ON the switch S_1. By additionally turning ON the switch S_{11}, the capacitor C_3 voltage is again added with the input voltage and thus, $+1.5V_{\text{in}}$ is obtained at the load. In the next level ($+2V_{\text{in}}$), the capacitor C_1 discharges to the load in series with V_{in} by turning ON switch S_2 and C_2 is charged during this instant by triggering the switch S_4. The diode D_2 is connected

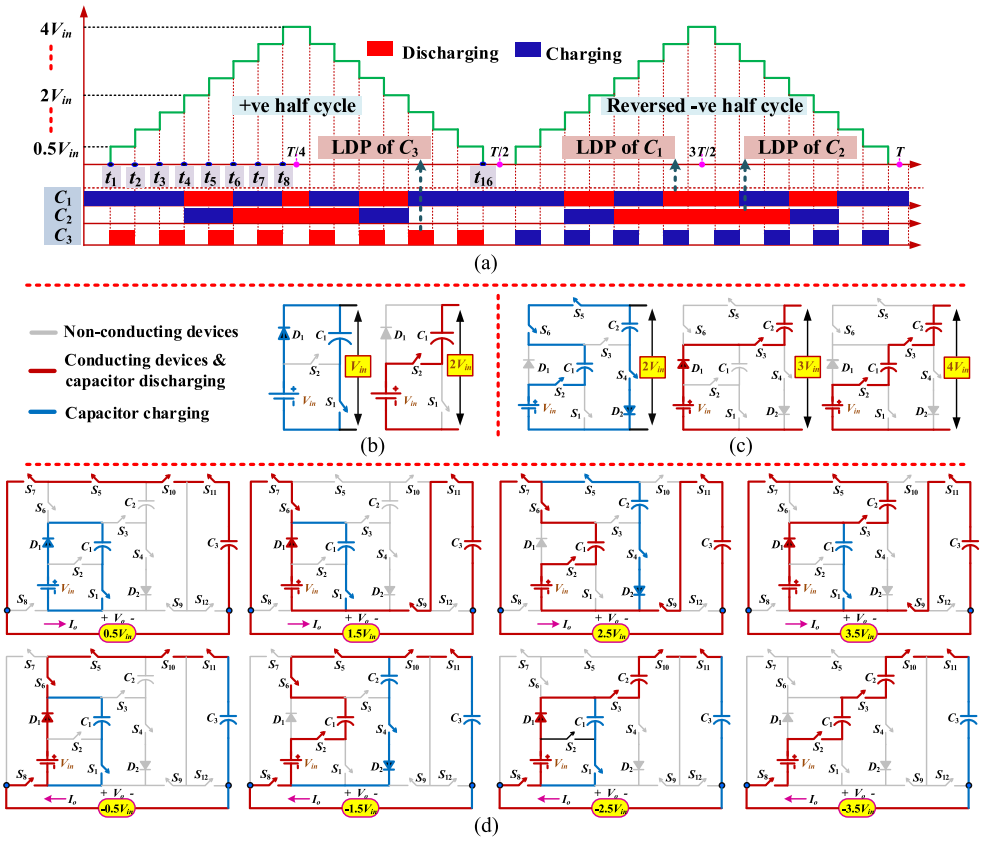

Fig. 2. Operation of the proposed circuit. (a) Output pattern of the proposed SC MLI, charging–discharging operation of (b) C_1, (c) C_2, and (d) C_3.

TABLE I
SWITCHING PATTERN OF THE PROPOSED 17-LEVEL SC MLI

Conducting switches in Positive half-cycle	Voltage steps	Conducting switches in Negative half-cycle
$S_1 - S_5 - S_7 - S_{10} - S_{12}$	0	$S_1 - S_8 - S_9 - S_{12}$
$S_1 - S_5 - S_7 - S_{10} - S_{11}$	$\pm V_{in}/2$	$S_1 - S_5 - S_6 - S_8 - S_{10} - S_{11}$
$S_1 - S_5 - S_6 - S_7 - S_9 - S_{12}$	$\pm V_{in}$	$S_1 - S_5 - S_6 - S_8 - S_{10} - S_{12}$
$S_1 - S_5 - S_6 - S_7 - S_9 - S_{11}$	$\pm 3V_{in}/2$	$S_2 - S_4 - S_6 - S_8 - S_{10} - S_{11}$
$S_2 - S_4 - S_6 - S_7 - S_9 - S_{12}$	$\pm 2V_{in}$	$S_2 - S_4 - S_6 - S_8 - S_{10} - S_{12}$
$S_2 - S_4 - S_6 - S_7 - S_9 - S_{11}$	$\pm 5V_{in}/2$	$S_1 - S_3 - S_6 - S_8 - S_{10} - S_{11}$
$S_1 - S_3 - S_5 - S_7 - S_9 - S_{12}$	$\pm 3V_{in}$	$S_1 - S_3 - S_6 - S_8 - S_{10} - S_{12}$
$S_1 - S_3 - S_5 - S_7 - S_9 - S_{11}$	$\pm 7V_{in}/2$	$S_2 - S_3 - S_8 - S_{10} - S_{11}$
$S_2 - S_3 - S_5 - S_7 - S_9 - S_{12}$	$\pm 4V_{in}$	$S_2 - S_3 - S_8 - S_{10} - S_{12}$

to avoid unwanted discharging of the capacitor C_2. The voltage steps $+2.5V_{\rm in}$ and $+3.5V_{\rm in}$ are obtained by discharging the capacitor C_3 as mentioned earlier. Discharging of C_2 in series with the source produces $+3V_{\rm in}$ at the output and the load voltage becomes $+4V_{\rm in}$ when both the capacitors (C_1 and C_2) discharge in series with the source. In the negative half-cycle, the voltage steps $-V_{\rm in}$, $-2V_{\rm in}$, $-3V_{\rm in}$, and $-4V_{\rm in}$ are produced similarly by turning ON the switches (S_8, S_{10}, S_{12}) instead of the switches (S_7, S_9, S_{11}). The capacitor C_3 is charged during the intermediate voltage levels $-0.5V_{\rm in}$, $-1.5V_{\rm in}$, $-2.5V_{\rm in}$, and $-3.5V_{\rm in}$. It is also worth noting that there always exists a path for the reverse flow of current, which facilitates successful operation of the proposed circuit under different load PF.

Table I presents the switching states to synthesize the 17-level output with any loading PF and the output waveform of the proposed SC MLI with capacitor charging–discharging pattern is shown in Fig. 2(a). Fig. 2(b) shows that the capacitor C_1 charges in parallel with the dc source to $V_{\rm in}$ and discharges in series with the source. The capacitor C_2 is charged in parallel with $V_{\rm in} + V_{C1}$ and discharges in series the accumulated energy ($2V_{\rm in}$) to the load, as depicted in Fig. 2(c). The capacitor C_3 is discharged in the whole positive half-cycle and charged symmetrically in the negative half-cycle, thus maintaining $0.5V_{\rm in}$ voltage across it. Fig. 2(d) shows the equivalent circuit and conduction path during the intermediate voltage steps in the positive and negative cycle. Thus, the natural balancing ability of all the three capacitors is confirmed.

A. Steady-State SC Analysis

Fig. 2(a) implies that the overall charging time of the capacitors is significantly lower than the total output voltage duration, attesting quick recovery of the capacitor voltages after the discharging period. The low parasitic resistance path and adequate charging instant further warrant retaining the desired capacitor voltage. To select the suitable capacitance, different factors, i.e., the largest discharging period (LDP) duration of the capacitors (C_1 and C_2), total discharging time in the whole positive half cycle (C_3), nominal frequency, lower voltage ripple, and type of loading, are considered. Assuming equal duration for all the voltage steps, the discharging amount of the capacitors C_1–C_3 can be expressed as in (1)–(3) in the following, considering φ as the lagging angle between the load current (I_o) and fundamental

voltage where the peak fundamental load current is $I_{o\max}$:

$$\Delta Q_{C1} = 2\int_{t_7}^{T/4} I_{o\max}\sin(\omega t-\varphi)\,dt \tag{1}$$

$$\Delta Q_{C2} = 2\int_{t_5}^{T/4} I_{o\max}\sin(\omega t-\varphi)\,dt \tag{2}$$

$$\Delta Q_{C3} = 4\int_{t_1}^{t_2} I_{o\max}\sin(\omega t-\varphi)\,dt. \tag{3}$$

Further, based on the fundamental frequency switching output voltage shown in Fig. 2(a), one half-cycle ($T/2$) can be divided into 16 time steps ($t_1 - t_{16}$) and therewith, t_1, t_2, t_5, and t_7 (in s) are expressed in (5) using (4) as follows [29]:

$$t_i = \frac{\sin^{-1}\left(\frac{i-0.5}{N_s}\right)}{\omega} = \frac{\sin^{-1}\left(\frac{2i-1}{N_l-1}\right)}{\omega} \tag{4}$$

where N_s is the number of voltage steps and N_l is the number of levels in the output.

$$t_1 = \frac{\sin^{-1}(1/16)}{\omega},\ t_2 = \frac{\sin^{-1}(3/16)}{\omega},\ t_3 = \frac{\sin^{-1}(5/16)}{\omega},$$
$$t_4 = \frac{\sin^{-1}(7/16)}{\omega}$$
$$t_5 = \frac{\sin^{-1}(9/16)}{\omega},\ t_6 = \frac{\sin^{-1}(11/16)}{\omega},\ t_7 = \frac{\sin^{-1}(13/16)}{\omega},$$
$$t_8 = \frac{\sin^{-1}(15/16)}{\omega}. \tag{5}$$

The corresponding voltage ripple (ΔV_{rC}) is expressed in (6) and capacitance is given in (7), as follows, considering $k\%$ voltage ripple in the capacitors:

$$\Delta V_{rC} = \frac{\Delta Q_C}{C} \tag{6}$$

$$C_1 \geq \frac{\Delta Q_{C1}}{kV_{\text{in}}}, C_2 \geq \frac{\Delta Q_{C2}}{k(2V_{\text{in}})} \text{ and } C_3 \geq \frac{\Delta Q_{C3}}{k(0.5V_{\text{in}})}. \tag{7}$$

Applying (1), (2), (3), and (5), the capacitance is finally expressed as

$$C_1 \geq \frac{2I_{o\max}}{k\omega V_{\text{in}}}\left[\cos(0.9484-\varphi)-\sin\varphi\right] \tag{8}$$

$$C_2 \geq \frac{I_{o\max}}{k\omega V_{\text{in}}}\left[\cos(0.5974-\varphi)-\sin\varphi\right] \tag{9}$$

$$C_3 \geq \frac{8I_{o\max}}{k\omega V_{\text{in}}}\left[\cos(0.0625-\varphi)-\cos(0.1886-\varphi)\right]. \tag{10}$$

Using the series–parallel charge balancing principle and with the selected values given in (8) and (9) considering $k\%$ of voltage ripple, the capacitors C_1 and C_2 naturally maintain the voltage in a 1:2 ratio. However, capacitor C_3 symmetrically discharges and charges in the positive and negative half-cycles, respectively. Thereby, the self-balancing nature of C_3 can also be verified considering any intermediate voltage steps. For instance, consider the equivalent circuit shown in Fig. 3 for the synthesis of $\pm 2.5V_{\text{in}}$ output voltage. The net charge (ΔQ_{C3}) is zero, which

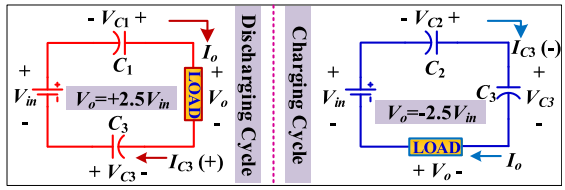

Fig. 3. Equivalent circuit of proposed circuit during $V_o = \pm 2.5V_{\text{in}}$.

can be expressed as follows:

$$\Delta Q_{c3} = \left[I_{C3}(+) - I_{C3}(-)\right]\ T \tag{11}$$

where I_{C3} is the current flowing through the capacitor C_3. Assuming the net impedance Z, the following expressions are derived from the equivalent circuit:

$$I_{C3}(+) = \frac{V_{\text{in}} + V_{C1} - V_o + V_{C3}}{Z} = \frac{2V_{\text{in}} - V_o + V_{C3}}{Z} \tag{12}$$

$$I_{C3}(-) = \frac{V_{\text{in}} + V_{C2} + V_o - V_{C3}}{Z} = \frac{3V_{\text{in}} + V_o - V_{C3}}{Z}. \tag{13}$$

Using (12) and (13), $\Delta Q_{c3} = [\frac{2V_{C3}-V_{\text{in}}}{Z}]T$ and hence, $V_{C3} = 0.5V_{\text{in}}$ at the steady state.

The above deduction demonstrates the inherent voltage balancing and selection process of suitable capacitance in the proposed SC MLI. Considering about 5%–7% of voltage ripple, the proposed circuit is developed and examined further.

III. Power Loss Evaluation for the Proposed Circuit

Switching loss (P_{sl}), ripple loss (P_{rl}), and conduction loss (P_{cl}) are the three major losses associated with the SC boost type MLIs [23], [29], [31]. These losses are evaluated in the following sections for the proposed 17-level MLI.

A. Switching Loss

The time delay between the transitions of a switching state produces switching power loss (P_{sl}). The blocking voltage (V_B) across a semiconductor switch during its OFF-state charges the built-in parasitic capacitor (C_p) linearly. Further, C_p discharges from the magnitude V_B to zero during the ON-state of the switch. Therefore, the energy loss (E_{sl}) by a semiconductor switch for one transition state can be evaluated using (14). Thereby the switching power loss during the switching actions can be calculated using (15), as follows:

$$E_{sl} = \frac{1}{2}\,C_p {V_B}^2 \tag{14}$$

$$P_{sl} = f_s\ E_{sl} = \frac{1}{2}\,f_s C_p {V_B}^2. \tag{15}$$

As can be noted from Fig. 1, the switches S_5–S_{10} block sum-total voltage stress of $18V_{\text{in}}$ and operate in a fundamental frequency (considering purely resistive loading). Thus, considering f_s and f_o as the switching and fundamental frequencies,

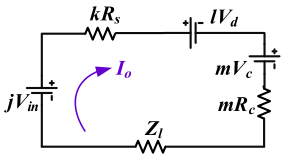

Fig. 4. Generalized equivalent circuit of the proposed MLI.

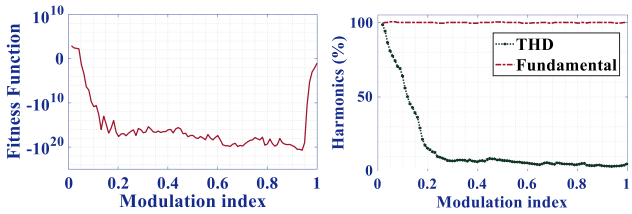

Fig. 5. Fitness function and THD evaluation using SSC technique.

(15) can be further simplified as follows:

$$P_{sl} = \frac{1}{2}\, C_p {V_{\rm in}}^2\, [18 f_o + 7 f_s]. \tag{16}$$

B. Ripple Loss

Internal resistances of the capacitor and semiconductor devices that are in the charging path of capacitors (C) generate ripple loss in the SC MLI. The voltage difference (ΔV_c) between the actual and desired voltage of the capacitor is the key influencing parameter of the ripple energy loss (E_{rl}) that is evaluated in terms of the charging time (t_c) and charging current (I_c)

$$\Delta\, V_c = \frac{1}{C} \int_0^{\rm t_c} I_c\,(t)\, dt \tag{17}$$

$$E_{rl} = \frac{1}{2}\, C \Delta {V_c}^2. \tag{18}$$

From (17) and (18), the ripple power loss (P_{rl}) can be calculated by (19). It can be observed that the larger value of the capacitance can minimize P_{rl}. However, a tradeoff is vital between the sizing and the ripple loss due to capacitors

$$P_{rl} = f_o E_{rl} = \frac{f_o}{2C} \left[\int_0^{\rm t_c} I_c\,(t)\, dt\right]^2. \tag{19}$$

C. Conduction Loss

The loss incorporated by the parasitic elements of the conducting devices in the load current path results in the conduction loss (P_{cl}). Fig. 4 shows the generalized equivalent circuit for the proposed MLI for synthesizing any voltage level. Therein, the output current expression (I_o) is given by

$$I_o = I_{o\max}\, \sin \omega t \;= \frac{m_i V_{o\max}}{Z_l}\, \sin \omega t \tag{20}$$

where m_i is the modulation index, which is the ratio of reference voltage (desired value) to the maximum obtainable fundamental voltage and Z_l is the load impedance. The conduction loss can be evaluated by considering the duration of each voltage level. For instance, the time duration (t_1–t_2) in Fig. 2(a) represents the voltage level $0.5V_{\rm in}$. Consequently, the energy loss is expressed in (21), considering the ON-state switch resistance (R_s), the internal resistance of the capacitor (R_c), and forward voltage drop of the diode (V_D)

$$E_{cl\ (0.5V_{\rm in})} = \int_{\rm t_1}^{\rm t_2} {I_o}^2\, (4R_s + R_c)\, dt. \tag{21}$$

The diode voltage drop is not included in (21) as it is in reverse bias during $0.5V_{\rm in}$. Consequently, the total conduction loss of the proposed MLI considering all the voltage levels is

$$P_{cl} = \; 8 f_o \sum_{i\,=\,0.5,1,\,\cdots\,4} E_{cl\ (iV_{\rm in})}. \tag{22}$$

Taking into account the losses derived in (16), (19), and (22), the power losses and overall efficiency of the proposed MLI are evaluated in Section VI using

$$\eta \;= \frac{\text{output power}}{\text{output power} + P_{sl} + P_{rl} + P_{cl}}. \tag{23}$$

IV. Comparative Evaluation

To assess the advantages of the proposed SC MLI, a comparison is carried out in Table II with recently developed 17-level MLI topologies based on different parameters and taking into account symmetrical configurations. As stated earlier, the compared topologies are categorized into two broad categories. The switched-dc or switched-diode-based circuits basically consist of multiple dc sources and do not possess the boosting ability. The SC-based topologies reduce the source count and feature the boosting ability. A number of capacitors and switches are used in such circuits to produce a high-quality output voltage. However, the proposed circuit aims at reducing the number of components to produce a 17-level output.

Except the MLI proposed in [23], the required number of dc sources ($N_{\rm dc}$) in all the nonboosting structures is more than one. Most of the SC MLIs also require multiple input sources when extended to create 17-level output, unlike the proposed MLI. In view of the least number of switches ($N_{\rm sw}$) and drivers ($N_{\rm dr}$), the proposed circuit ranks first among other SC MLIs. The MLI disclosed in [14] involves fewer switches and drivers but at the cost of large number of dc sources. The single-dc SC MLIs [30] and [31] do not require discrete diodes ($N_{\rm dd}$), but involve a large number of switches. On the contrary, the proposed 17-level topology uses only two diodes. Although the use of capacitors supports voltage boosting, the inrush current increases with increase in number of capacitors. Lower number of capacitors ($N_{\rm cap}$) in the proposed circuit limits the inrush current and increases the reliability. More number of switches in the conducting path increases the power loss. The proposed MLI is also superior among all the MLI topologies on account of maximum number of switches in the conduction ($N_{\rm ms}$) for 17-level operation.

Total standing voltage (TSV) and maximum standing voltage (MSV) are further evaluated for MLI topologies. TSV is calculated taking into account voltage stress across all the switches. The proposed MLI reduces the TSV to a great extent as the conventional full bridge is avoided for producing ac output.

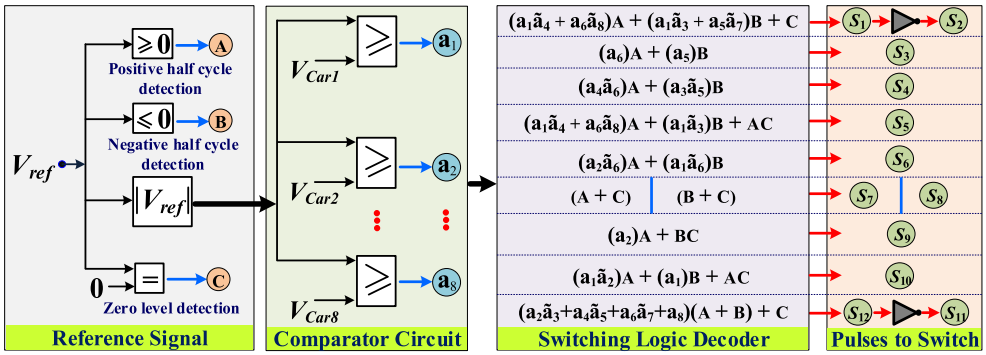

Fig. 6. Block diagram of PPC scheme with switching logic.

TABLE II
COMPARISON OF THE SYMMETRICAL 17-LEVEL MLI TOPOLOGIES

Parameters			N_{dc}	N_{sw}	N_{dr}	N_{dd}	N_{cap}	N_{ms}	MSV (x V_{in})	TSV (x V_{in})	Gain	C_f (δ=0.5)	C_f (δ=1.5)	Full-bridge
Switched-dc/diode	Non-boosting	[12]	4	20	20	0	8	10	8	48	1	14.35	15.76	YES
		[14]	6	9	9	3	1	6	4	20	1	10.76	12.53	YES
		[15]	8	13	13	8	0	10	8	47	1	22.09	24.85	YES
		[17]	8	20	20	0	0	10	8	48	1	24.94	27.76	YES
		[18]	8	18	18	0	0	9	8	36	1	22.24	24.35	NO
		[19]	8	18	18	0	0	9	2	32	1	22.12	24	NO
		[23]	1	18	18	8	8	10	8	56	1	3.85	4.26	YES
Switched-capacitor	Boosting	[24]	4	24	24	4	4	12	2	40	2	16.59	17.76	YES
		[25]	2	18	18	6	6	8	8	44	4	6.91	7.56	NO
		[26]	4	20	20	4	4	10	8	40	2	14.24	15.41	NO
		[27]	2	18	14	2	4	6	4	40	2	5.47	6.06	NO
		[29]	2	18	18	2	6	7	8	58	4	6.43	7.28	NO
		[30]	1	39	39	0	7	16	1	39	8	6.08	6.37	NO
		[31]	1	20	16	0	5	10	2	21.5	4	3.16	3.47	NO
		Proposed	1	12	12	2	3	6	4	25	4	2.30	2.67	NO

The MLIs proposed in [14] and [31] have the minimum TSV. However, the former requires almost double the number of switches than the proposed MLI and the latter is a multi-dc topology that lacks the boosting ability. Proposed MLI has a quadruple boosting gain using minimum number of switches. Besides, cost factor (C_f) is chosen as a parameter to establish the design superiority, which is defined as

$$C_f = \frac{(N_{\rm sw} + N_{\rm dr} + N_{\rm dd} + N_{\rm cap} + N_{\rm ms} + \delta.{\rm TSV_{pu}})\, N_{\rm dc}}{N_l}. \tag{24}$$

C_f is evaluated considering different values of the weightage coefficient δ (low for more weightage to the number of components and high for more weightage to the TSV). The proposed MLI has the least C_f among the other MLIs under both the conditions ($\delta = 0.5$ and 1.5). Hence, the proposed MLI is a suitable alternative to the recently developed MLIs for obtaining high-quality output using least switch count.

V. MODULATION SCHEME

Fundamental switching control and high-frequency switching control are the two main categories of pulsewidth modulation (PWM) control schemes generally employed to verify the MLI working. Selective harmonic elimination switching control (SSC) is one of the former category of control schemes which aggressively eliminates the targeted lower order dominant harmonics and thereby maintains the highest quality of output waveforms [9], [11], [14], [16]. The fundamental component of staircase output voltage waveform in terms of Fourier series equations can be expressed as follows, which is valid for any single-phase MLI:

$$V_1 = \frac{4V_d}{\pi}\left\{\cos n\alpha_1 + \cdots + \cos n\alpha_p\right\}\sin(n\omega t). \tag{25}$$

Here, α_p (proportional to t_i), n, and V_d are the symbolic representation of switching angles, order of harmonics, and nominal value of the dc voltage, respectively. Further, p is directly associated with the number of voltage levels (N_l) as

$$p = (N_l - 1)/2. \tag{26}$$

For any voltage level, the switching angle values can be determined within the modulation index (m_i) range of [0, 1] to eliminate the targeted lower order harmonics from the system, and thus, it can be regarded as the key control parameter. The expression of m_i in terms of the fundamental and nominal

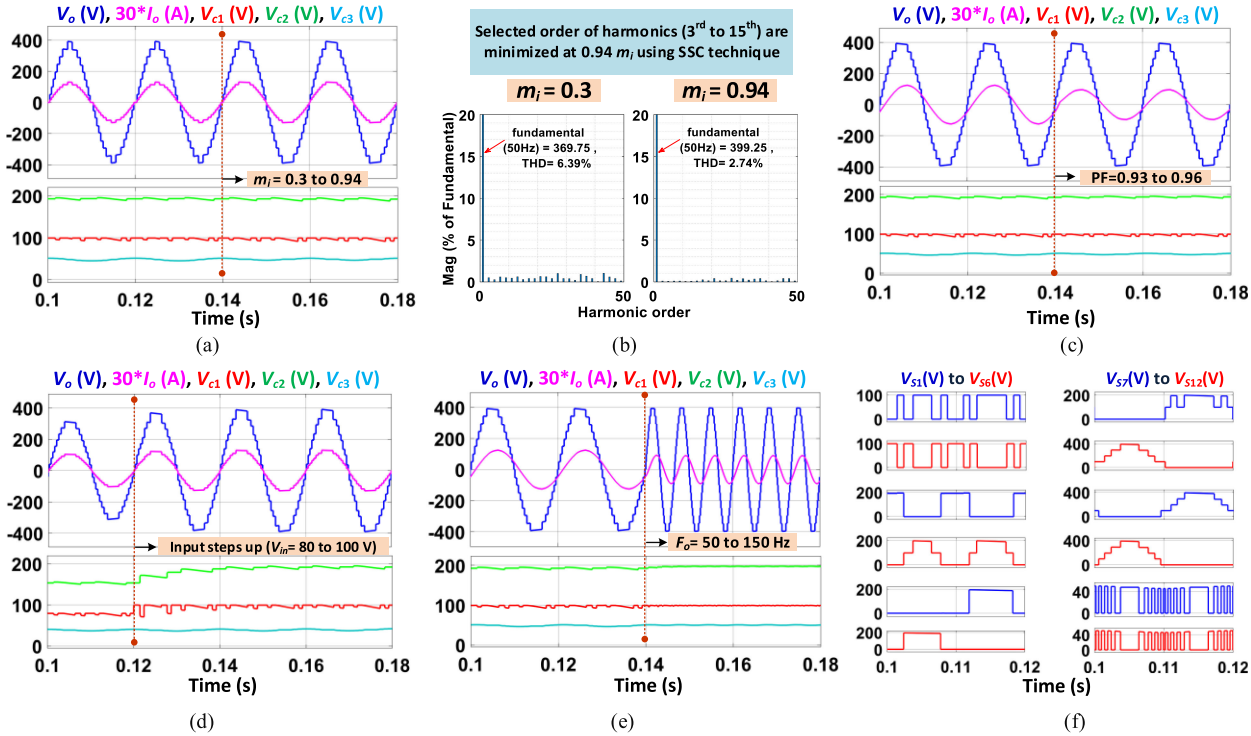

Fig. 7. Simulation analysis. (a) Change in modulation index. (b) Harmonic analysis of the load voltage. (c) Change in loading PF. (d) Change in input voltage. (e) Change in nominal frequency. (f) Voltage stress across all the switches.

dc voltage is given as follows:

$$m_i = \frac{\pi V_1}{(4pV_{d1})}, 0 \le m_i \le 1. \tag{27}$$

The proposed MLI is designed to output a 17-level staircase voltage waveform. Considering the expressions (25) and (27), the associated nonlinear equations for the MLI are given in (28) with the target to eliminate the 3rd to 15th order harmonics. To extract the optimal solutions (α_p), particle swarm optimization algorithm (PSO) is employed, taking into account the angle constraint in (29) and fitness function given in [16]

$$\begin{cases} \cos\alpha_1 + \cdots + \cos\alpha_8 = 8m_i \\ \cos 3\alpha_1 + \cdots + \cos 3\alpha_8 = 0 \\ \vdots \\ \cos 15\alpha_1 + \cdots + \cos 15\alpha_8 = 0 \end{cases} \tag{28}$$

$$0 < \alpha_1 < \alpha_2 < \cdots < \alpha_8 \le \pi/2. \tag{29}$$

Moreover, the performance of the optimization process for the proposed MLI can be verified from Fig. 5. Corresponding to the minimum value of the fitness function (i.e., in the range 0.9–0.94), switching angles are selected to verify the operation of the proposed circuit. The figure also implies that the total harmonic distortion (THD) level decreases with the increase in m_i and also the fundamental value is retained at the desired level even under a lower m_i value. This is one of the dominant features of the SSC technique and thus, the number of levels in the output voltage and current does not reduce with the decrease in m_i although an increase in THD can be expected in such a scenario. Besides the optimum values of the switching angles chosen corresponding to the minimum fitness function value, a lower m_i value of 0.3 is taken as reference to verify the SSC principle in the next section.

The fundamental frequency SSC scheme maintains the required fundamental value of the output and thus cannot regulate the ac output (or the voltage gain), which is generally required in different applications of an MLI. In such a case, the phase-disposition PWM control (PPC) scheme [14], [19], [33] may be employed. In the PPC scheme, multiple carrier signals are compared with the reference sinusoidal signal to generate the PWM signals through the pulse logic decoder, as shown in Fig. 6. In the decoder circuit, the switching logic presented in Table I is synthesized through the appropriate combination of logic gates. The PPC scheme does not involve any complex equations to retain the fundamental component, unlike the SSC technique. Nevertheless, the conversion ratio of the proposed circuit can be varied in the range of $0.5V_{\text{in}}$ to $4V_{\text{in}}$ by varying m_i.

VI. Simulation Analysis

The proposed 17-level MLI consisting of 12 IGBT switches is simulated in MATLAB/Simulink environment. The input dc source is considered 100 V and the inverter is operated with a 50-Hz nominal frequency unless otherwise specified. The capacitance values are accordingly calculated using (8)–(10) and C_1, C_2, and C_3 are chosen as 3300, 4700, and 2200 μF,

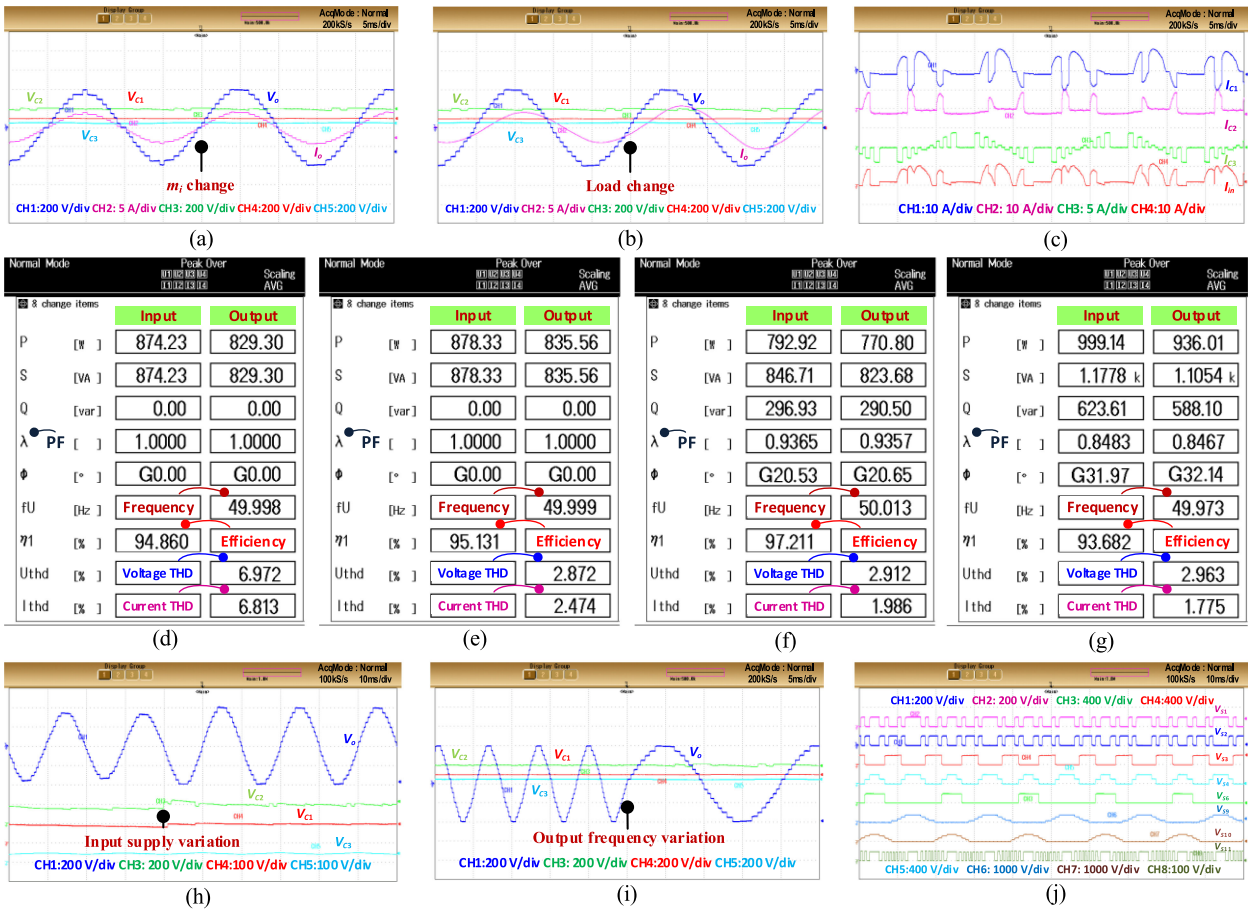

Fig. 8. Experimental output voltage and current waveform (a) Sudden variation in m_i. (b) Change in loading PF. (c) Current through the capacitors and input current. (d) Parameters at $m_i = 0.3$. (e) Parameters at $m_i = 0.94$. (f) Parameters under *RL*-1. (g) Parameters under *RL*-2. (h) Input supply step-up. (i) Sudden change in output frequency. (j) Voltage stress across (S_1, S_2, S_3, S_4, S_6, S_9, S_{10}, S_{11}).

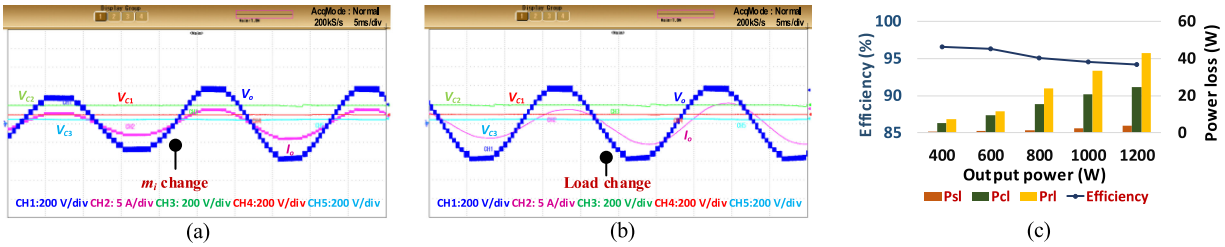

Fig. 9. Experimental verification of the proposed MLI with PPC scheme (a) Change in m_i. (b) Change in loading PF. (c) Efficiency and loss evaluation.

respectively. Using the SSC technique, the eight switching angles corresponding to different m_i are saved in a lookup table for the generation of switching pulses.

To validate the 17-level operation using the SSC technique, first the results are obtained in Fig. 7(a) under dynamically varying m_i condition at constant loading of 90 Ω. The 17-level output is acquired even with low m_i due to fundamental switching SSC principle, whereas the THD in the load voltage reduces [see Fig. 7(b)] with the increase in m_i. Quadruple step-up ability with the inherent balancing of capacitor voltages V_{C1}, V_{C2}, and V_{C3} is in accordance with the theoretical analysis. Fig. 7(c) verifies the working under a change in load PF with the change in loading from 90 Ω-108 mH to 120 Ω-108 mH. The capacitor voltage ripple decreases with an increase in R value for fixed C_1, C_2, and C_3. The capacitor voltages inherently settle to the original value under sudden variation in input from 80 to 100 V, as shown in Fig. 7(d), which verifies the successful performance of the proposed SC MLI. Fig. 7(e) depicts that the voltage ripple decreases considerably and the load current drops due to an increase in frequency from 50 to 150 Hz (switching angles corresponding to 150 Hz are also saved in lookup table) in the presence of inductive loading. Evidently, the proposed MLI

can act as a potential high-frequency ac source for different applications. Fig. 7(f) shows that the voltage stress across all the unidirectional switches is in accordance with Fig. 1. It is also apparent that apart from switches S_1, S_2, S_{11}, and S_{12}, all other switches operate at a low frequency, which thus results in low power loss in the circuit.

VII. Experimental Verification

To verify the suitable real-time operability, a test setup of the proposed 17-level MLI is developed in the laboratory. A programmable dc supply is initially set to 100 V. As the output voltage is boosted to four-times the input, the rms value of the load voltage is about 280 V. IGBT switches 12N60A4D with integrated antiparallel diodes are considered for S_1–S_{12} and two MUR860 are used as D_1 and D_2. Selected values of the capacitance (C_1–C_3) are the same as in simulation with internal resistances 36, 18, and 54 mΩ, respectively. A DSP controller with Simulink interfacing is used to produce the switching pulses of (0–5) V. An isolated driver circuit built using TLP250 is then used to amplify these pulses (about 20 V) which drive the switches. In addition, the driver circuit also provides adequate isolation between the power circuit and control circuit. A ScopeCoder (DL850E) is used to capture the voltage–current waveforms and the performance parameters are obtained using a WT1800 power analyzer.

Identical to the result shown in Fig. 7(a), experimental outputs are obtained with a change in m_i and with fixed resistive loading of 90 Ω in Fig. 8(a). The desired 17-level output is obtained with a change in switching pulse in conjunction with variation in m_i from 0.3 to 0.94. Further, tests follow considering higher m_i value (0.94). The rms value of load current varies from 2.9 to 3.9 A and the PF varies from 0.93 to 0.85 as the load changes from 90 Ω-108 mH (*RL*-1) to 60 Ω-120 mH (*RL*-2) in Fig. 8(b). The output voltage and capacitor voltages are undistorted during the sudden load transient. Self-balancing of the capacitors in both Fig. 8(a) and (b) is obtained due to appropriate charging–discharging. Herein, the capacitor currents and the source current are depicted in Fig. 8(c) with 90 Ω load, which implies symmetrical charging pattern of the capacitors in a full cycle. The current spikes are reduced using a small inductor (0.03 mH) in the charging loop that is not shown in the circuit analysis for the sake of simplification. The captured power analyzer results in Fig. 8(d)–(g) show the change in active–reactive power (P, Q), PF (λ), phase angle (Φ), efficiency ($\eta 1$), voltage THD, and current THD. Fig. 8(d) and (e) is obtained in accordance with Fig. 6(a) at fixed resistive loading and change in m_i. The THD varies with the change in m_i. Fig. 8(f) and (g) is obtained in accordance with Fig. 8(b) with a change in load from *RL*-1 to *RL*-2. A proportional increase in the active power and change in efficiency is witnessed with decrease in the impedance and PF. Fig. 8(h) and (i) further verifies the self-balancing and step-up abilities of the proposed circuit with sudden variation in input voltage (90 to 100 V) and output frequency (150 to 50 Hz), respectively. Similar observation as in Fig. 7(f), the voltage stress on switches is testified in Fig. 8(j).

To verify the adequate operation of the proposed circuit, experimental tests are further performed with PPC technique considering a switching frequency and nominal frequencies of 2 kHz and 50 Hz, respectively. Initially, the proposed inverter produces a 13-level output with 0.6 m_i and the desired 17-level output is obtained, as shown in Fig. 9(a), once m_i is changed to unity. Fig. 9(b) ascertains a clean sinusoidal load current, undistorted load voltage, and self-balanced capacitor voltages with a change in loading from *RL*-1 to *RL*-2 under the PPC scheme. The efficiency of the prototype is further evaluated with the corresponding output power considering pure resistive loading of 90 Ω. It is clear from Fig. 9(c) that the switching power loss, conduction loss, and the ripple losses increase with an increase in the output power.

VIII. Conclusion

This work introduced a reduced switch single-source SC MLI with quadruple boosting ability. Using only 12 switches and three capacitors, the proposed MLI is able to synthesize a 17-level output with a reduced number of devices in the conducting path. The capacitors C_1 and C_2 can inherently balance the voltage in 1:2 ratio using the series–parallel charge balancing principle and the capacitor C_3 self-regulates the voltage at $0.5V_{\text{in}}$ due to symmetrical charging–discharging in a full cycle. Thus, the use of auxiliary voltage balancing circuit/sensors is avoided. The operating principles, voltage balancing ability, steady-state analysis of the SCs, and power loss evaluation have been addressed thoroughly. The comparative assessment with recent-art 17-level structures demonstrates the benefits on lower number of components, minimum cost factor, and no requirement of polarity reversal H-bridge. Simulation and experimental investigations of the 17-level MLI under change in m_i, sudden change in supply voltage, change in PF, and frequency variation fully testify the structural operability. Moreover, high step-up operation with adequate inherent voltage balancing without additional dc–dc converter makes the proposed MLI suitable for PV applications.

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