Flying-Capacitor Linear Amplifier With Capacitor Voltage Balancing for High-Efficiency and Low Distortion

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***Abstract*—This article presents a flying-capacitor linear amplifier (FCLA) that achieves high efficiency, low harmonic distortion, and low electromagnetic interference (EMI). A conventional class-B linear amplifier cannot be used in power conversion applications, because the power loss generated in active-state MOSFETs is high compared with the loss generated in switching operations. In the proposed FCLA, multiple series-connected MOSFETs are used, and only one MOSFET operates in the active state at a time. Thus, the power loss generated in the MOSFETs can be reduced, and the FCLA can achieve high efficiency without performing the switching operation. In this study, the features of the FCLA and conventional linear amplifiers are theoretically compared and evaluated. Moreover, a voltage balancing control for flying capacitors is proposed and verified through simulations and experiments. It is demonstrated that the prototype 12-series FCLA achieves over 89% efficiency and generates low harmonics and low EMI. The proposed configuration is useful for increasing the number of series MOSFETs, and it contributes to realizing a power converter with advantages such as low harmonic distortion, low EMI, and high efficiency.**

***Index Terms*—Diode-clamped linear amplifier, efficiency, electromagnetic interference, flying-capacitor multilevel converter, harmonic distortion, linear amplifier, power conversion.**

I. Introduction

In general power conversion circuits, the switching operation of semiconductor power devices is widely utilized to achieve high efficiency. However, the switching operation causes harmonic distortion and electromagnetic interference (EMI) because the respective voltage and current on the switching power converters change abruptly [1], [2]. The passive components in a circuit should be large to reduce the harmonic distortion of the waveforms. Moreover, the structure of power converters should be designed considering the stray inductance, which increases the surge voltage.

Some types of linear amplifiers, such as the class-B amplifier, have been used to achieve low distortion waveforms. However, their efficiency is quite low compared to that of the pulse width modulation (PWM) power converters for the switching operation. For example, the efficiency of the class-B amplifier is 78.5%, even in the ideal case, which implies that the power capacity of the linear amplifier is limited.

Certain types of linear amplifiers that combine multiple conversion stages have been reported so far. Most of the proposed linear amplifiers aim to realize a fast dynamic response, high frequency, and high efficiency. An amplifier combining a high-fidelity class-A amplifier and class-D amplifier as a variable power supply was proposed in [3]. It was reported that the measured efficiency was 77% at 100 W, and the distortion was approximately the same as that of the class-A amplifier. In [4], a highly efficient power amplifier for an inkjet printer was presented. The proposed topology was configured by combining a multi-level converter as the first stage with multiple voltage sources, a voltage level selector as a second stage, and a linear amplifier as the third output stage. It was reported that the proposed topology achieved 30–50% power savings in comparison with a general power amplifier with constant voltages. In [5], an RF envelope amplifier based on a combination of a multi-level converter and a linear regulator was proposed for communication systems. It was shown that a prototype circuit achieves an efficiency of 68.3% at a 2 MHz sinusoidal output case. References [6] and [7] also proposed an envelope tracking power amplifier that combines a multi-level converter and linear amplifier. The prototype circuit achieves 76% efficiency at a 10 W output peak power. In [8], various topologies of switched-mode assisted linear power amplifiers were presented. These circuits consist of a general linear amplifier and a switched-mode current dumping circuit. It was reported that the proposed circuit configurations do not require an output filter and can achieve a fast dynamic response. However, the efficiency of these amplifiers is not very high from the viewpoint of power conversion because they have multiple power conversion stages.

Efficient amplifiers with a single power conversion stage were reported to solve these issues. In [9]–[11], a diode-clamped

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linear amplifier (DCLA) was proposed to realize high-efficiency and low distortion simultaneously. The circuit topology of the DCLA was configured based on a diode-clamped multi-level converter [12]–[14]. As another solution, the authors proposed a flying-capacitor linear amplifier (FCLA) [15], [16] configured based on a flying-capacitor multi-level converter [12], [13], [17], [18]. In addition, the concept of voltage balancing control for flying capacitors in the FCLA was proposed and validated by simulation [19].

In this study, the proposed voltage balancing control for flying capacitors is investigated in detail and is experimentally verified. The feasibility of the FCLA with high efficiency, low harmonic distortion, and low EMI is assessed. This paper preferentially presents the general usefulness of the proposed circuit and shows the results of a basic study to apply various usages such as motor drives that require EMI reduction and grid-connected inverters that require severe harmonic suppression. In the general motor drive application, the motor current becomes a smooth waveform by the motor inductance. However, the input voltage of the motor is usually PWM waveform with high dv/dt. This high dv/dt negatively affects to leakage current and breakdown between motor windings, and increasing EMI particularly when the cable between the power converter and the motor is long [20], [21]. In this case, dv/dt of the switching needs to be suppressed preferentially at the expense of efficiency. The FCLA is expected to suppress dv/dt and EMI more effectively than the PWM power converter.

The remainder of this article is organized as follows. The circuit operation of the FCLA is analyzed, especially from the viewpoint of the power conversion efficiency in Chapters II and III. The proposed voltage balancing control of the flying capacitors is investigated and verified by simulations and experiments in Chapter IV. Design and experiments using prototype circuits with a module configuration are presented in Chapter V. Then, finally, the relationship between the efficiency and the number of series MOSFETs is discussed considering the capacitor voltage balancing in Chapter VI.

II. Fundamentals of Flying-Capacitor Linear Amplifier

A. Circuit Configuration

Fig. 1 shows the circuit configuration per phase of the n-series FCLA. In the n-series FCLA, n-series n-channel MOSFETs and n-series p-channel MOSFETs are connected between the positive pole of the dc side and the AC output terminal, and the negative pole of the dc voltage E side and AC output terminal, respectively. Flying-capacitors C_k, that fix the voltage of $(n-k)E/n$ are connected between the source terminals of the n-MOSFET Q_k and p-MOSFET Q_{pk}. A common gate signal is used for each gate terminal of the MOSFETs as the input voltage $v_{\rm in}$ of the linear amplifier. In the gate circuits, gate resistors and Zener diodes are connected to avoid overcurrent and overvoltage. Unlike the general PWM power converter, the FCLA circuit with the common gate input shown in Fig. 1 does not perform sharp switching operation at all, but performs linear operation. The gate resistance does not have to be as small as that in the general PWM converters. Moreover, it is not necessary to configure the isolated power supplies for each MOSFET. The source terminal voltage of each MOSFET follows the input voltage, which means that the FCLA operates as a current amplifier with equivalent input and output voltages.

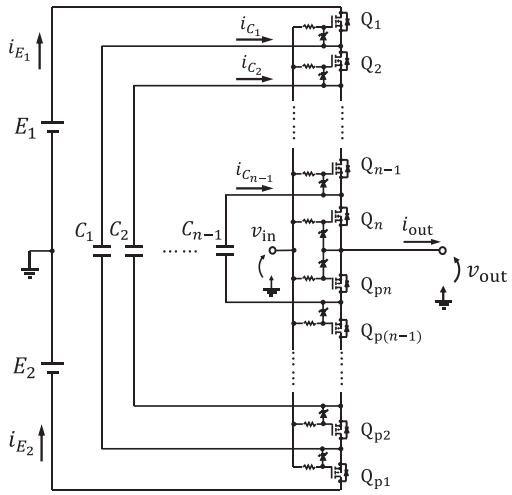

Fig. 1. Circuit configuration of n-series Flying-Capacitor Linear Amplifier.

TABLE I
Operation States in 4-Series FCLA With Common Gate Input

v_{out}	Q_1	Q_2	Q_3	Q_4	Q_{p1}	Q_{p2}	Q_{p3}	Q_{p4}	C_1	C_2	C_3
$E/4<v_{\rm out}<E/2$	act.	on	on	on	off	off	off	off	-	-	-
$0<v_{\rm out}<E/4$	off	act.	on	on	fwd	off	off	off	D	-	-
$-E/4<v_{\rm out}<0$	fwd	off	off	off	off	act.	on	on	D	-	-
$-E/2<v_{\rm out}<-E/4$	off	off	off	off	act.	on	on	on	-	-	-

Note: act.: active state, fwd: on-state of FWD, D: discharge.

B. Operation Principle

Fig. 2 and Table I shows the operating modes of the 4-series FCLA. When the input voltage $v_{\rm in}$ is within the region (a) $E/4<v_{\rm in}<E/2$, only MOSFET Q_1 operates as the active state and the other MOSFETs Q_2-Q_4 in the upper arm are in the on-state. The MOSFETs $Q_{p1}-Q_{p4}$ in the lower arm are in the off-state. The drain terminal voltage of Q_1 is $E/2$, which is the same as the drain terminal voltage of the upper arm MOSFET in the class-B linear amplifier. Q_1 changes voltage drop of the drain-source voltage v_{ds1} within 0 to $E/4$ according to the input voltage. The output voltage becomes $(E/2-v_{ds1})$ in this operating mode.

When $v_{\rm in}$ is within the region (b) $0<v_{\rm in}<E/4$, Q_1 is in an off-state, and Q_2 operates in an active state. The drain terminal voltage of Q_2 is $E/4$, and Q2 changes the voltage drop of the drain-source voltage v_{ds2} within 0 to $E/4$ according to the input voltage. The output voltage becomes $(E/4-v_{ds2})$ in this operating mode. In the same way, when $v_{\rm in}$ is within the region

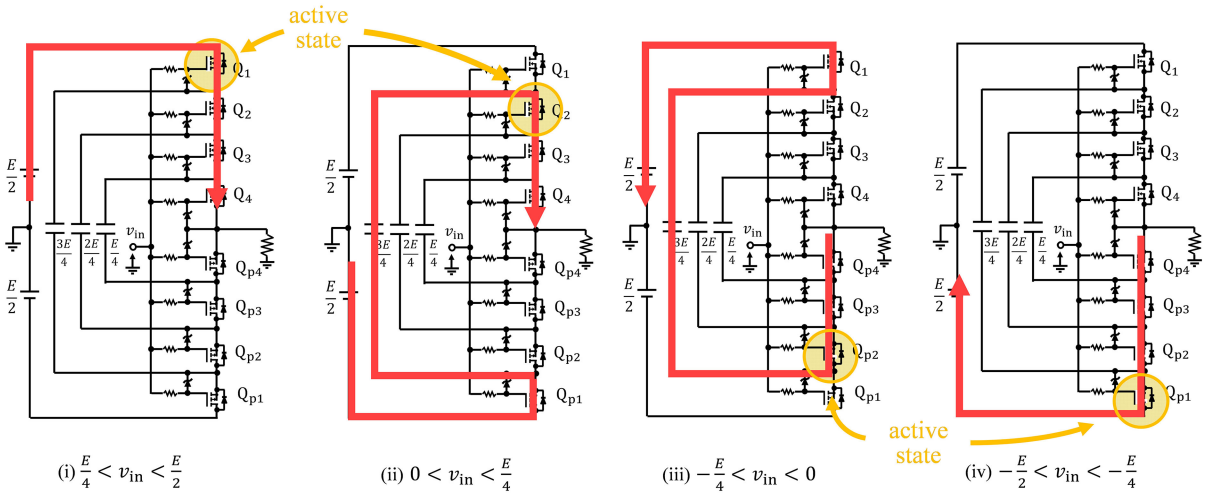

Fig. 2. Operating modes in 4-series FCLA. (a) $\frac{E}{4} < v_{\rm in} < \frac{E}{2}$. (b) $0 < v_{\rm in} \frac{E}{4}$. (c) $-\frac{E}{4} < v_{\rm in} < 0$. (d) $-\frac{E}{2} < v_{\rm in} < -\frac{E}{4}$.

(c) $-E/4<v_{\rm in}<0$ and (d) $-E/2<v_{\rm in}<-E/4$, the output voltage is expressed $(-E/4 + v_{dsp2})$ and $(-E/2 + v_{dsp1})$ by the drain-source voltages v_{dsp2} and v_{dsp1} of Q_{p2} and Q_{p1}, respectively.

The applied voltage and power loss in the active-state MOSFET can be reduced compared with that of the class-B amplifier. Therefore, the 4-series FCLA can realize higher efficiency than that of the conventional class-B amplifier. Generally, in the n-series FCLA, when the input voltage $v_{\rm in}$ is within the region of $(n-2k)E/2n < v_{\rm in} < (n-2k+2)E/2n$, the MOSFET Q_k operates in the active state, and the other MOSFETs are in the on-state or off-state. In each operating mode, the drain terminal voltage of the active-state MOSFET Q_k becomes $(n-2k+2)E/2n$ and the drain-source voltage of Q_k is always within E/n. It causes that the power loss generated in the active-state MOSFET can be reduced by increasing the number n of the series-connected MOSFETs.

However, the flying capacitors C_1, C_2, and C_3 do not charge by the load current in any operation modes. The voltage balance cannot be realized without an auxiliary circuit in this common gate circuit configuration. A solution of this issue is discussed in Section IV.

III. Theoretical Analysis of FCLA Efficiency

When the output voltage $v_{\rm out}$ and current $i_{\rm out}$ are given by (1) and (2), the theoretical efficiency $\eta_{\rm FCLA}$ of the n-series FCLA and $\eta_{\rm DCLA}$ can be derived as (3) based on elaborate calculations of the input and output powers. In this regard, the calculation conditions are shown below.

1) The voltage of the flying-capacitor C_k in the FCLA is always kept at $(n\text{-}k)E/n$.
2) The gate threshold voltage of each MOSFET is 0 V.
3) Only an even number is available as the number n of the series MOSFETs.
4) The power loss of the gate circuit is not considered.

$$v_{\rm out} = \frac{E}{2}\sin\theta \tag{1}$$

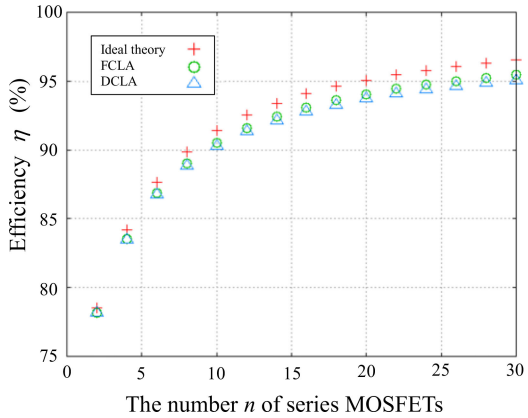

Fig. 3. Relationships between the number of series MOSFETs and efficiency.

$$i_{\rm out} = I_{\max}\sin\theta \tag{2}$$

$$\eta_{FCLA} = \frac{n^2\pi}{16\sum_{k=1}^{n/2}\sqrt{nk-k^2}}\left[1-\frac{2R_{on}I_{\max}(n-1)}{E} - \frac{4R_{ESR}I_{\max}}{\pi E}\left\{\theta_1 - \frac{2}{n^2}(n-2)\sqrt{n-1}\right\}\right] \tag{3}$$

Here, $\theta_k = \sin^{-1}\{(n\text{-}2k)/n\}$ denotes the boundary phase between the off-state and active-state. $I_{\max}$ is the amplitude of the output current, $R_{\rm on}$ is the on-state resistance of each MOSFET, $R_{\rm ESR}$ is the equivalent series resistance of each flying-capacitor, $V_{\rm F}$ is the forward voltage of each clamp diode.

Fig. 3 shows the relationship between the number n of the series MOSFETs and the efficiency η calculated by (3) and the equation of the efficiency in the DCLA [9]–[11]. The graph legend "Ideal theory" refers to the efficiency in consideration of only the power loss caused by the active-state MOSFET [9]. Furthermore, "FCLA" and "DCLA" stand for the efficiency with the conduction loss and power loss caused by the equivalent series resistance (ESR) of the flying-capacitors in

TABLE II
CIRCUIT PARAMETERS

Parameters	Symbol	Value
dc voltage	E [V]	100
Input voltage	v_{in} [V]	$50\sin\theta$
Maximum output current	$I_{\max}$ [A]	5
Diode forward voltage	V_{F} [V]	1.5
Capacitor equivalent series resistance	R_{ESR} [Ω]	0.025
MOSFET on-state resistance	R_{on} [Ω]	$0.1/n$

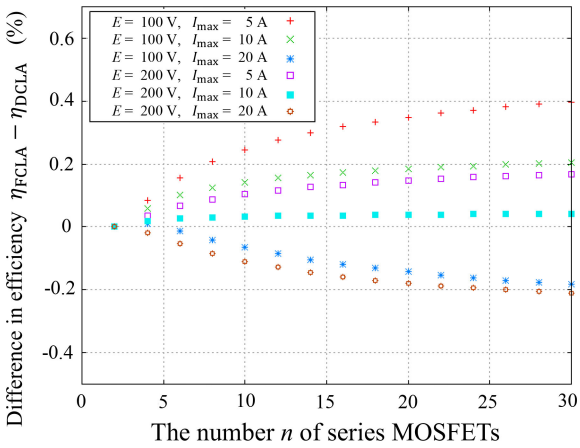

Fig. 4. Differences between the efficiencies of FCLA and DCLA.

FCLA, and the power loss caused by the forward voltage of the clamp-diodes in DCLA. Table II lists the circuit parameters. The on-state resistance R_{on} of each MOSFET is defined as $0.1/n$, as listed in Table II because as the number n of the series-connected MOSFETs increases, the rated voltage and on-state resistance of the MOSFETs can be lower in proportion to $1/n$.

From Fig. 3, it can be confirmed that the efficiency of FCLA can be improved by increasing the number of series MOSFETs. However, as the number of series MOSFETs increases, the progress of the efficiency is gradually saturated. Moreover, the efficiency of the FCLA is slightly higher than that of the DCLA in this calculation condition.

Fig. 4 shows the differences between the efficiencies of FCLA and DCLA. The positive number of the vertical axis indicates that the efficiency of the FCLA is higher than that of the DCLA, and vice versa. When E is changed from 100 V to 200 V, the calculation condition of the on-state resistance also changes from $0.1/n$ to $0.2/n$ because the on-state resistance is generally proportional to the rated voltage of the MOSFET.

In Fig. 4, when as $I_{\max}$ and E decrease, the difference between the efficiencies of FCLA and DCLA increases. Therefore, the FCLA has an advantage under lower voltage and smaller current compared with the DCLA under the investigated conditions listed in Table II. Furthermore, the efficiency of the FCLA can be improved by reducing the ESR with suitable selection of the capacitor, which means that the efficiency of the FCLA is able to become higher than that of the DCLA even under high-voltage and large-current conditions, because the relationship between the efficiency of FCLA and DCLA depends on the ESR of the capacitors and diode forward voltage according to (3) and the

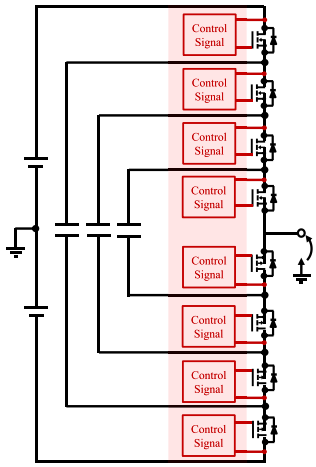

Fig. 5. Proposed circuit configuration of individual gate circuit in the FCLA.

equation of the DCLA efficiency. It is considered that suitable design and device selection expand the range of applications for FCLAs.

IV. VOLTAGE BALANCING CONTROL OF FLYING-CAPACITORS

A. Necessity of Capacitor Voltage Balancing

In the FCLA with the common gate circuit shown in Fig. 2, the flying-capacitors are only discharged by the load current, which causes the voltage variation and imbalance because the redundant operation states for the charge and discharge are insufficient. In this case, the capacitor voltage finally converges to a voltage that is not zero but lower than the regulated voltage, and the whole circuit operation becomes similar to that of the conventional class-B amplifier. Thus, any voltage balancing method without an additional circuit in the main circuit is needed for the satisfactory operation to realize the loss reduction. Moreover, by realizing self-voltage balancing, isolated dc power supplies for each flying capacitor are not required. In this work, voltage balancing control for flying capacitors by the appropriate changes in the charging and discharging currents is proposed without any auxiliary voltage balancing circuit.

B. Realization of Capacitor Voltage Balancing Control

Fig. 5 shows the proposed circuit configuration for the voltage balancing control of the flying capacitors. In the proposed method, individual linear gate drivers that can output an analog voltage are used, and they realize redundant operation modes for the charge and discharge of the flying capacitors. Fig. 6 shows the current paths of the 4-series FCLA with the proposed voltage balancing control when the output voltage region is within $0 < v_{\text{out}} < E/4$, and the load is purely resistive as a simple example. The current path of Fig. 6(a) is the same as that of Fig. 2(a), (ii), and C_1 becomes a discharging state. When the MOSFET Q_k becomes the off-state in Figs. 6(b)–(d), C_{k-1} becomes the charging state, and C_k becomes the discharging state. In these operation modes, the loss generated in the active-state MOSFET can be reduced in the same way as the common gate signal

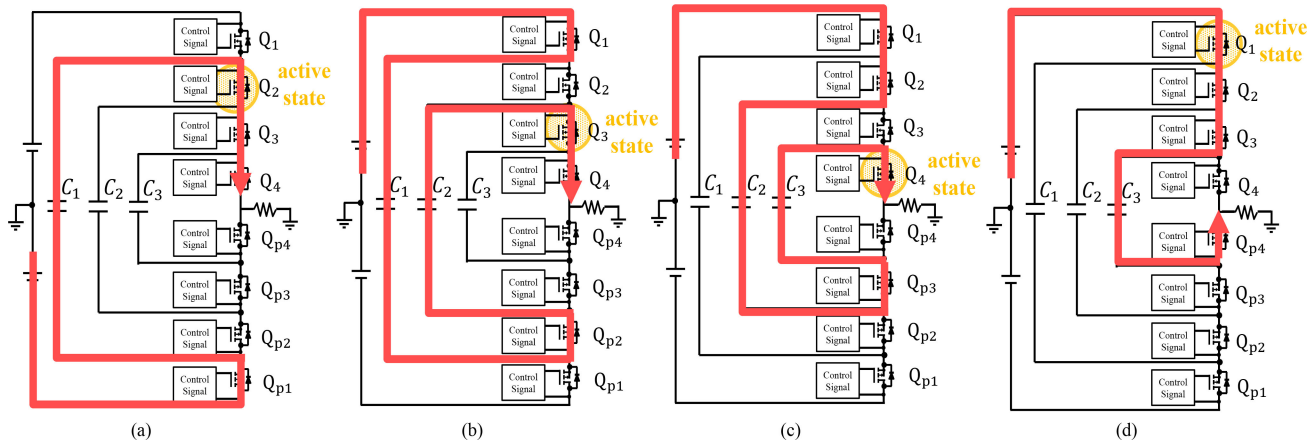

Fig. 6. Current paths of the 4-series FCLA with proposed control when the output voltage region is within $0<v_{\rm out}<E/4$. (a) Mode 2a (off-state: Q_1) (b) Mode 2b (off-state: Q_2) (c) Mode 2c (off-state: Q_3) (d) Mode 2d (off-state: Q_4).

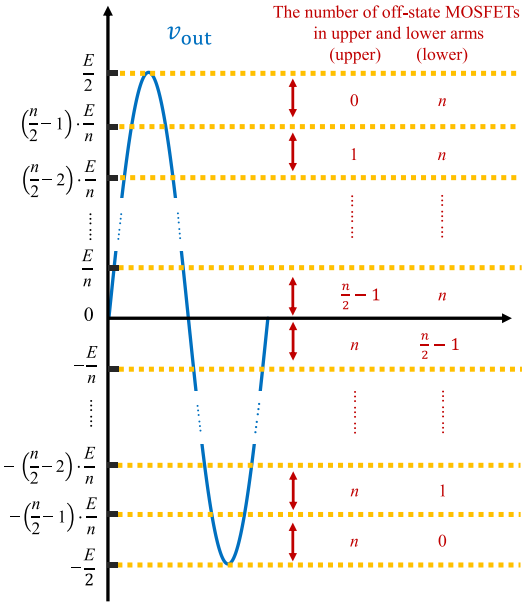

Fig. 7. Relationship between the output voltage region and the number of off-state MOSFETs.

TABLE III
POSSIBLE SWITCH COMBINATION AND CHARGING/DISCHARGING OF THE CAPACITORS IN 4-SERIES FCLA WITH THE PROPOSED VOLTAGE BALANCING CONTROL

v_{out}	#	Q_1	Q_2	Q_3	Q_4	Q_{p1}	Q_{p2}	Q_{p3}	Q_{p4}	C_1	C_2	C_3
$E/4<v_{out}<E/2$	1a	on	act.	on	on	off	off	off	off	-	-	-
	1b	on	on	act.	on	off	off	off	off	-	-	-
	1c	on	on	on	act.	off	off	off	off	-	-	-
	1d	act.	on	on	on	off	off	off	off	-	-	-
$0<v_{out}<E/4$	2a	off	act.	on	on	fwd	off	off	off	D	-	-
	2b	on	off	act.	on	off	fwd	off	off	C	D	-
	2c	on	on	off	act.	off	off	fwd	off	-	C	D
	2d	act.	on	on	off	off	off	off	fwd	-	-	C
$-E/4<v_{out}<0$	3a	fwd	off	off	off	off	act.	on	on	D	-	-
	3b	off	fwd	off	off	on	off	act.	on	C	D	-
	3c	off	off	fwd	off	on	on	off	act.	-	C	D
	3d	off	off	off	fwd	act.	on	on	off	-	-	C
$-E/2<v_{out}<-E/4$	4a	off	off	off	off	on	act.	on	on	-	-	-
	4b	off	off	off	off	on	on	act.	on	-	-	-
	4c	off	off	off	off	on	on	on	act.	-	-	-
	4d	off	off	off	off	act.	on	on	on	-	-	-

Note: act.: active state, fwd: on-state of FWD, D: discharge.

input. Moreover, in the n-series FCLA, the operation states of the flying-capacitors are determined according to the principle; C_{k-1} and C_k are in the charging and discharging states, respectively when the MOSFET Q_k is in the off-state. The number of off-state MOSFETs in the upper and lower arms is determined by the output voltage region, as shown in Fig. 7. For example, only one MOSFET is in the off-state when the output voltage region is within $0<v_{\rm out}<E/4$ in the 4-series FCLA, as shown in Fig. 6. Additionally, in the 12-series FCLA, the number of off-state MOSFETs is five when the output voltage region is within $0<v_{\rm out}<E/12$. The number of off-state MOSFETs increases as the output voltage decreases to reduce the loss generated in the active-state MOSFET.

Table III lists all the operation modes, and charge and discharge states of flying-capacitors in the 4-series FCLA with the proposed control. The redundant operation modes including charge and discharge states of all the flying-capacitors increase by the individual gate circuit compared with the case of the common gate circuit as shown in Table I. Fig. 8 shows the state transition diagram for an implementation of the proposed voltage balancing control in 4-series FCLA. Although the proposed control is expected to implement in various practical ways, this example is designed based on the control method on the flying-capacitor multi-level converters. The target flying-capacitor for charging is changed for each arbitrary output according to the scheme shown in Fig. 8. The constant value h is used to set the amplitude of the capacitor voltage ripple. This proposed control realizes the self-voltage balance of the flying-capacitors by changing the operation states in a similar way to the flying-capacitor multi-level converter with the carrier phase-shifted modulation [22]. In this regard, the switching speed of the change in the operating states is different between the FCLA and multi-level converter. In the FCLA, the linear operation of the MOSFETs is also used in the instance when the operation states change to prevent EMI. Moreover, the phase-shifted carrier

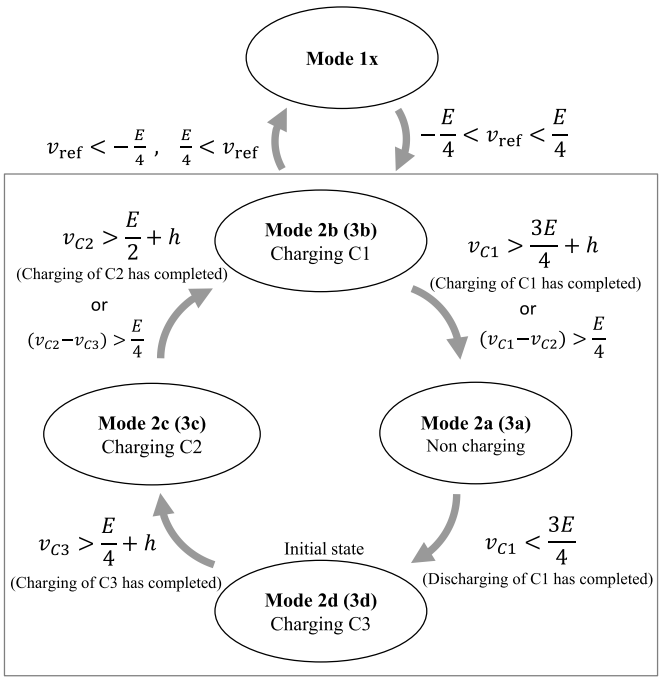

Fig. 8. State transition diagram for an implementation of the proposed voltage balancing control in 4-series FCLA.

frequency of the FCLA should be set as the lower frequency to avoid emitting EMI and reduce loss. Therefore, the phase-shifted frequency should be changed, considering the output waveform. In this study, voltage balancing control is realized based on the feedback values of all the flying-capacitor voltages. When the difference between the voltages of the charging and discharging states of the capacitors becomes larger than the summation of the regulated voltage value and the requirement of the flying-capacitor voltage variation, the current path is changed and the capacitor in the charging state also changes. Thus, the frequency for the charge and discharge of each flying-capacitor do not synchronize with the output waveform frequency and depends on the capacitance of the flying-capacitors, load current, and requirement of the capacitor voltage variation. The capacitor voltage balance can be realized by applying this proposed control scheme to each individual gate driver.

In a practical condition, the on-resistances of n-channel and p-channel MOSFETs are different in general. Since the charge and discharge currents of the flying-capacitors are almost determined by the output voltage and load impedance, the difference in the on-resistances between the n-channel and the p-channel MOSFETs has almost no effect on the voltage balancing of the flying capacitors.

C. Requirement and Operation of the Individual Gate Drivers

Fig. 9 shows the operation principle for changing the current path using each input gate-drain voltage by the individual gate drivers. In typical power converters, a gate driver is connected between the gate and source terminals of each MOSFET to charge and discharge the gate-source capacitance. In the FCLA, the gate-source voltage of the MOSFETs becomes almost zero

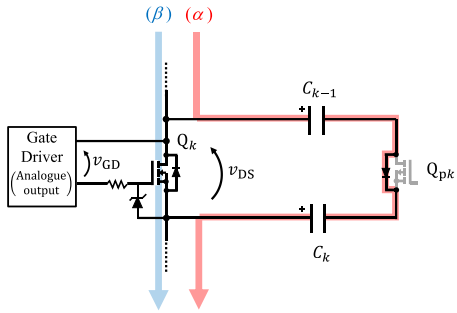

Fig. 9. Operation principle to change the current path using gate-drain connected gate driver.

for satisfying the well-known imaginary short because each MOSFET operates as the source follower operation. Moreover, not only the on and off-states, but also the active states must be controlled by the individual gate drivers in the proposed configuration of the FCLA. Therefore, the gate drivers with the analog voltage output are connected between the drain and gate terminals of each MOSFET and control their voltages by the linear operation.

The current path is selected, as shown in Fig. 9, based on the comparison of the gate-drain voltage $v_{\rm GD}$ and capacitor voltages. When the gate driver of the MOSFET Q_k outputs the voltage $v_{\rm GD}$, the gate-source voltage appears under the condition that the drain-source voltage $v_{\rm DS}$ is not equal to $v_{\rm GD}$. Subsequently, the source voltage follows the gate voltage because of the source follower operation; therefore, $v_{\rm DS}$ follows $v_{\rm GD}$. If the gate driver outputs a voltage higher than the difference between the capacitor voltages $v_{C(k-1)} - v_{Ck}$, $v_{\rm DS}$ also becomes higher than $v_{C(k-1)} - v_{Ck}$. Q_k is in the off-state and the current flow path (α) shown in Fig. 9 due to the body diode of the MOSFET Q_{pk} is in the on-state. However, if $v_{\rm DS}$ is lower than the difference $v_{C(k-1)} - v_{Ck}$, Q_k is in the on-state or active-state, and the current path is the path (β). Thus, the operation state of Q_k can be suitably controlled by the gate–drain input voltage.

D. Simulation Validation

Fig. 10 shows the simulation waveforms of the 4-series FCLA with the proposed control [19]. In the output voltage $v_{\rm out}$ and current $i_{\rm out}$ waveforms, a sinusoidal waveform can be obtained without an LC filter at the output terminal. When the time is within the region (a), as shown in Fig. 10, the operation mode becomes the same as that in Fig. 6(a). The output voltage region is within $0 < v_{\rm out} < E/4$, Q_1 changes to the off-state, Q_2 changes to the active state, and Q_3 and Q_4 change to the on-state. It can be confirmed that the discharging current i_{C1} flows in C_1, and v_{C1} decreases. When the time is within the region (b), as shown in Fig. 10, the operation mode becomes the same as that in Fig. 6(b). C_1 and C_2 change to the charging and discharging states in the same manner as in region (a). Similarly, when the time is within regions (c) and (d), the operation modes are shown in Figs. 6(c) and (d). As a result, the voltage of all the flying-capacitors can be kept at $(n\text{-}k)E/n$ [V], and all the drain-source voltages become lower than 30 V for the input dc voltage of 120 V. Thus,

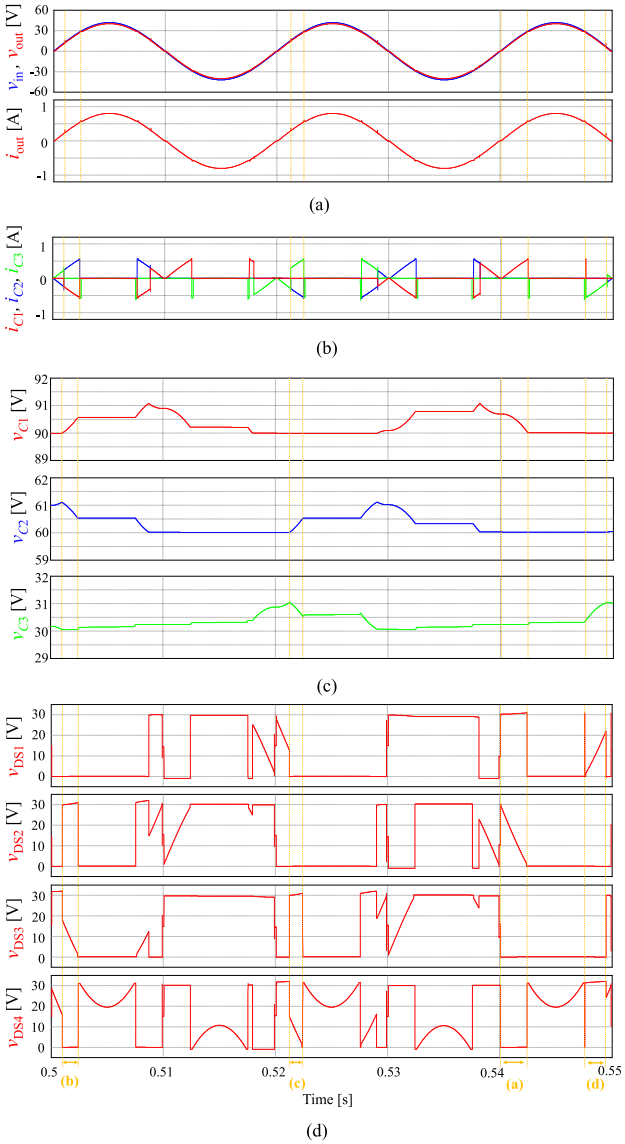

Fig. 10. Simulation waveforms of the 4-series FCLA with the capacitor voltage balancing control. (a) Input voltage $v_{\rm in}$, output voltage $v_{\rm out}$ and output current $i_{\rm out}$. (b) Flying capacitor currents i_k. (c) Voltages v_{Ck} of flying capacitor C_k. (d) Drain-source voltages $v_{\rm DS}k$ of MOSFET Q_k.

the capacitor voltage balance can be realized because of the proposed voltage balancing control.

V. Experimental Validation of the FCLA

A. Prototype Circuit

Fig. 11 shows the circuit schematic of the FCLA redrawn as a ladder circuit configuration. This circuit is divided into the dc voltage source part, series MOSFETs part, and load part. The series MOSFETs part consists of n-channel MOSFETs (Renesas: 2SK2926), p-channel MOSFETs (Renesas: 2SJ530), flying-capacitors, and gate circuits. Table IV lists the electrical characteristics of the MOSFETs used in the prototype circuit.

As a design policy of the MOSFETs and gate driving, both the operation characteristics of n-channel and p-channel MOSFETs

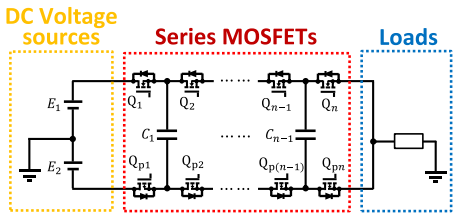

Fig. 11. Generalized topology of FCLA.

TABLE IV
Electrical Characteristics of MOSFETs

Parameters	Symbol	2SK2926 (n-channel)	2SJ530 (p-channel)
Drain to source maximum voltage	$V_{\rm DS}$ [V]	60	-60
Gate to source maximum voltage	$V_{\rm GS}$ [V]	±20	±20
Drain current	$I_{\rm D}$ [A]	15	-15
On-state resistance	$R_{\rm on}$ [Ω]	0.042	0.08
Gate to source threshold voltage	$V_{\rm th}$ [V]	1.5	-1.0
Input capacitance	$C_{\rm iss}$ [pF]	500	850

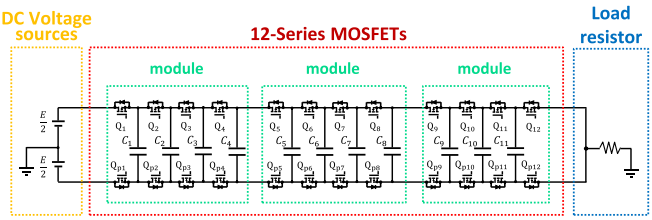

Fig. 12. Circuit configuration of FCLA when the number n of series MOSFETs is set as 12-series.

should be completely symmetric. However, the characteristics of the p-channel MOSFETs such as capacitances and gate threshold voltage are worse than that of the n-channel MOSFETs in general. To compensate the different characteristics, the gate resistances should be adjusted so that the product of the input capacitance and the gate resistance become close enough between the n-channel and p-channel MOSFETs. Although this design policy is similar to that of the class-B amplifiers, it is possible to decrease the voltage rating of each MOSFET as the number of the series devices increases in the case of the FCLA.

The frequency response of the FCLA is basically determined by the product of the input gate resistance and capacitance, so the response performance is considered to be almost the same as that of the class-B amplifier. The major benefit from the FCLA is in the possibility of high efficiency rather than improvement of the output response.

In FCLA topology, the number n of the series MOSFETs can be flexibly changed by combining modularized circuits of the series MOSFETs part. For example, a 12-series FCLA can be built using three 4-series FCLA modules, as shown in Fig. 12. The modularized structure tends to cause a longer commutation loop between the modules and increases the stray inductance in general. However, the increase in the stray inductance is not a

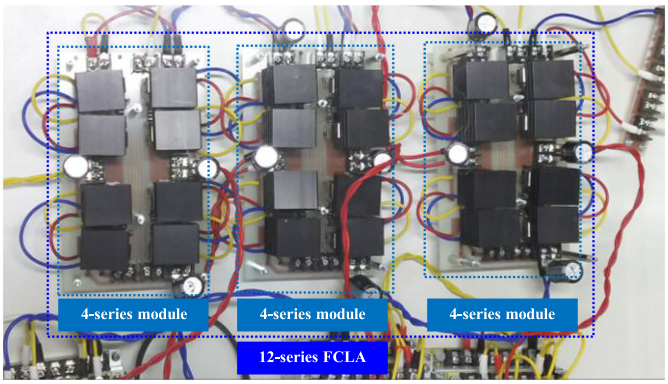

Fig. 13. Overview of the 12-series FCLA configured based on the 4-series modules.

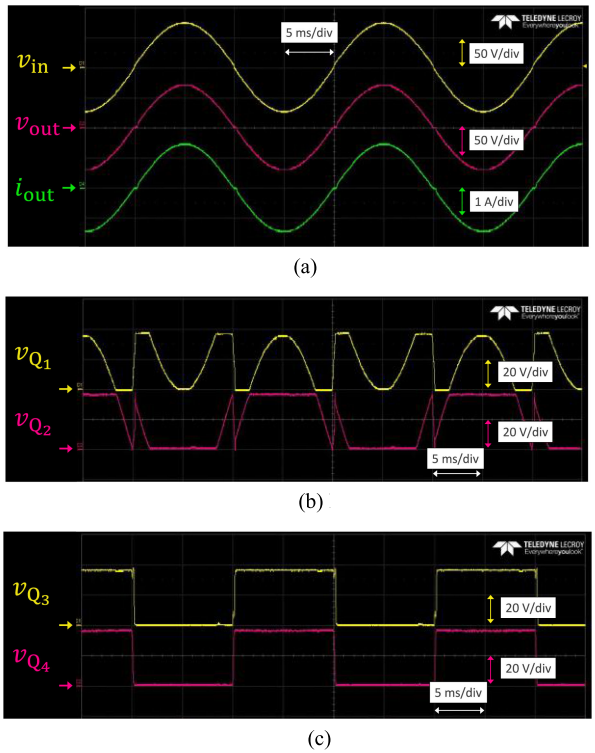

Fig. 14. Experimental waveforms of 4-series FCLA (Gate resistances: 100 kΩ (n-channel), 56 kΩ (p-channel), Load power factor: 1.0). (a) Input and output waveforms (b) Drain-source voltage waveforms of Q_1 and Q_2 (c) Drain-source voltage waveforms of Q_3 and Q_4.

critical issue because the MOSFETs in the FCLA do not operate as a switch with high dv/dt and di/dt. This feature is one of the attractive advantages of FCLAs. Fig. 13 shows an overview of the small-scale laboratory prototype of the FCLA when n is set as 12-series by combining three modules of the 4-series circuit.

B. Experimental Waveforms

The operating waveforms of the 4-series and 12-series FCLAs are shown in Figs. 14 to 17. Table V lists the experimental conditions. The dc voltage was 144 V, the AC output voltage was 144 V (peak-to-peak), the output frequency was 50 Hz in the sinusoidal waveform, and the loads were a purely resistive load of 47 Ω, and

TABLE V
EXPERIMENTAL CONDITION IN FIGS. 14 TO 17

Parameters	Symbol	Value
dc voltage	E	144 V
Output voltage	v_{out}	Sinusoidal, 144 V (peak to peak), 50 Hz
Zener voltage of zener diode	V_{zener}	13 V
Capacitance of flying capacitor	C_k	22 μF
Gate resistance of MOSFETs	R_{gate_n} (n-channel)	100 kΩ (Fig. 14)
		7 kΩ (Figs. 15-17)
	R_{gate_p} (p-channel)	56 kΩ (Fig. 14)
		4.125 kΩ (Figs. 15-17)
Loads	R_{load}	47 Ω (Figs. 14, 15, and 17)
	$R_{load} + L_{load}$	30 Ω + 120 mH (Fig. 16)

an inductive load of 30 Ω + 120 mH. In this experiment, a dc offset voltage was added to the sinusoidal input voltage to compensate for the well-known crossover distortion caused by the gate threshold voltage of the MOSFETs. This crossover distortion can be suppressed by adding an offset voltage to the input signal v_{in} to compensate the gate threshold voltage as the same way in the class-B linear amplifier. According to the operating modes of the FCLA shown in Fig. 2, the flying capacitors were not charged, and the voltage balance was not realized. Isolated dc power supplies were connected for each flying capacitor as the voltage balancing circuit to maintain the capacitor voltage at the regulated values, and to confirm the basic circuit operation and efficiency in the experiment. The capacitor voltage control is discussed in the next chapter.

Fig. 14 shows the experimental waveforms of the input voltage v_{in}, output voltage v_{out}, output current i_{out}, and drain-source voltage v_{Qk} of the MOSFET Q_k in the 4-series FCLA. It can be seen that the output voltage follows the input voltage. From this figure, it is confirmed that the FCLA operates as a current amplifier. In the drain-source voltage waveforms in Fig. 14(b), (c), it is confirmed that either the MOSFET Q_1 or Q_2 operates in the active state, and the other MOSFETs operate in the on or off-states when the input is positive. Moreover, each drain–source voltage of the MOSFETs in the off-state is a quarter of the dc input voltage. A slight distortion appears in the output voltage when the polarity of the output current is changed. Furthermore, a slight distortion also appeared in the waveform of v_{Q3} when MOSFET Q_2 turned to the active state as addressed above. However, when the gate resistance is high, the effect of the suppression reduces because of the restriction of the response bandwidth determined by the input capacitance and gate resistance of the MOSFET.

Fig. 15 shows the experimental waveforms when the gate resistances are changed from 100 kΩ to 7 kΩ (n-channel) and from 56 kΩ to 4.125 kΩ (p-channel), respectively. In the output waveforms, the distortion in Fig. 15 becomes relatively smaller than that in Fig. 14. Similarly, in the drain-source waveforms, there is almost no distortion in the waveform of $v_{Q3}$when MOSFET Q_2 turns to the active state. As the gate resistances are

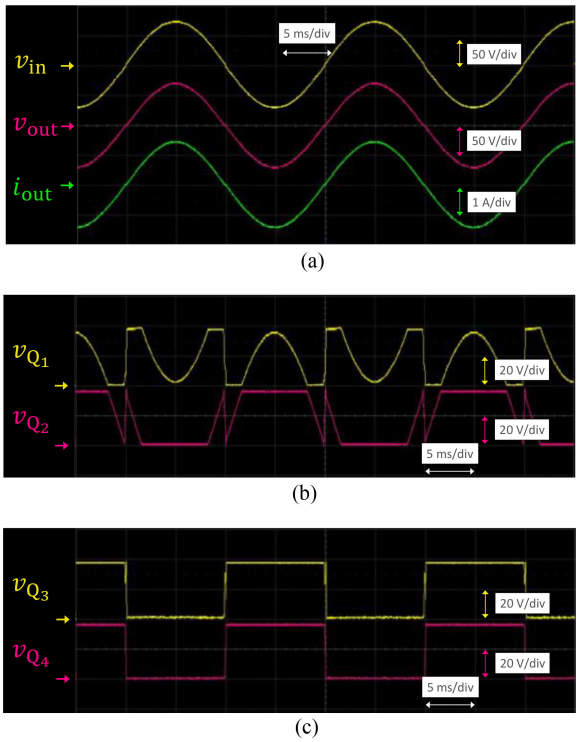

Fig. 15. Experimental waveforms of 4-series FCLA (Gate resistances: 7 kΩ (n-channel), 4.125 kΩ (p-channel), Load power factor: 1.0). (a) Input and output waveforms (b) Drain-source voltage waveforms of Q_1 and Q_2 (c) Drain-source voltage waveforms of Q_3 and Q_4.

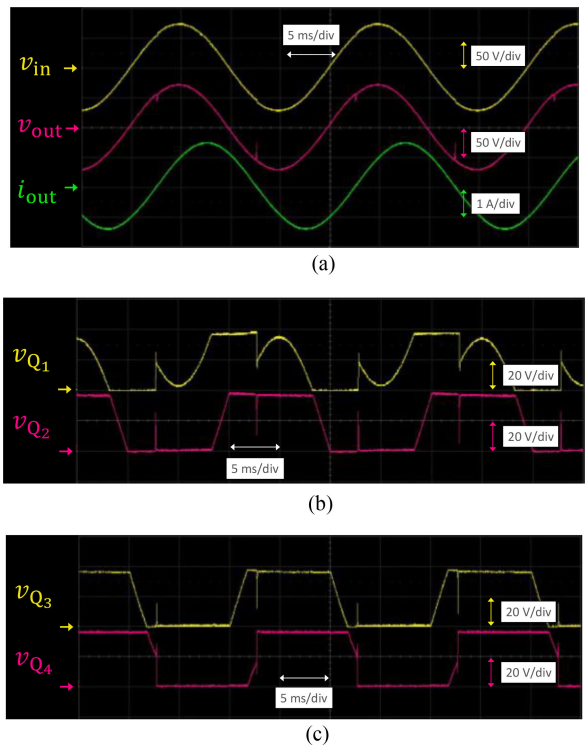

Fig. 16. Experimental waveforms of 4-series FCLA (Gate resistances: 7 kΩ (n-channel), 4.125 kΩ (p-channel), Load power factor: 0.62). (a) Input and output waveforms (b) Drain-source voltage waveforms of Q_1 and Q_2 (c) Drain-source voltage waveforms of Q_3 and Q_4.

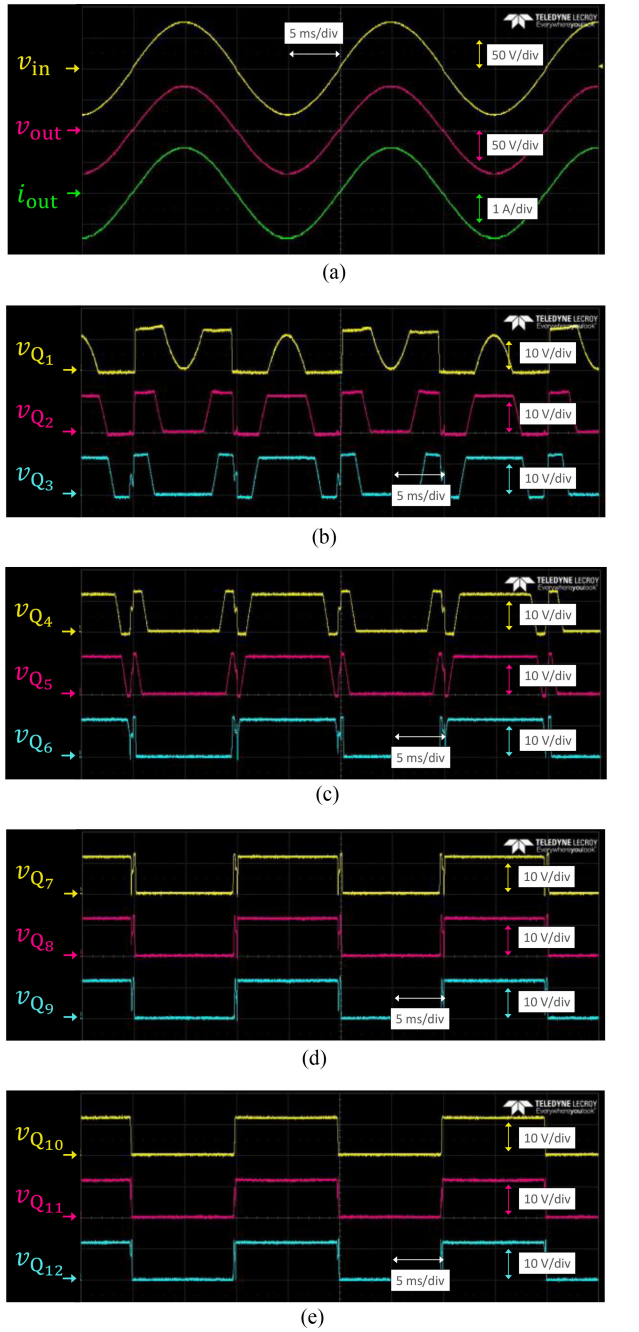

Fig. 17. Experimental waveforms of 12-series FCLA (Gate resistances: 7 kΩ (n-channel), 4.125 kΩ (p-channel), Load power factor: 1.0). (a) Input and output waveforms (b) Drain-source voltage waveforms of Q_1, Q_2, and Q_3 (c) Drain-source voltage waveforms of Q_4, Q_5, and Q_6 (d) Drain-source voltage waveforms of Q_7, Q_8, and Q_9 (e) Drain-source voltage waveforms of Q_{10}, Q_{11}, and Q_{12}.

smaller and output performance becomes faster, the crossover distortion is improved.

Fig. 16 shows the experimental waveforms when the load resistance R_{load} is 30 Ω, and inductance L_{load} is 120 mH. It can be confirmed that the FCLA operates as a current amplifier also when the load is inductive. However, a small surge voltage appears when the polarity of the output current is changed. This phenomenon occurs by the same mechanism of the cross-over

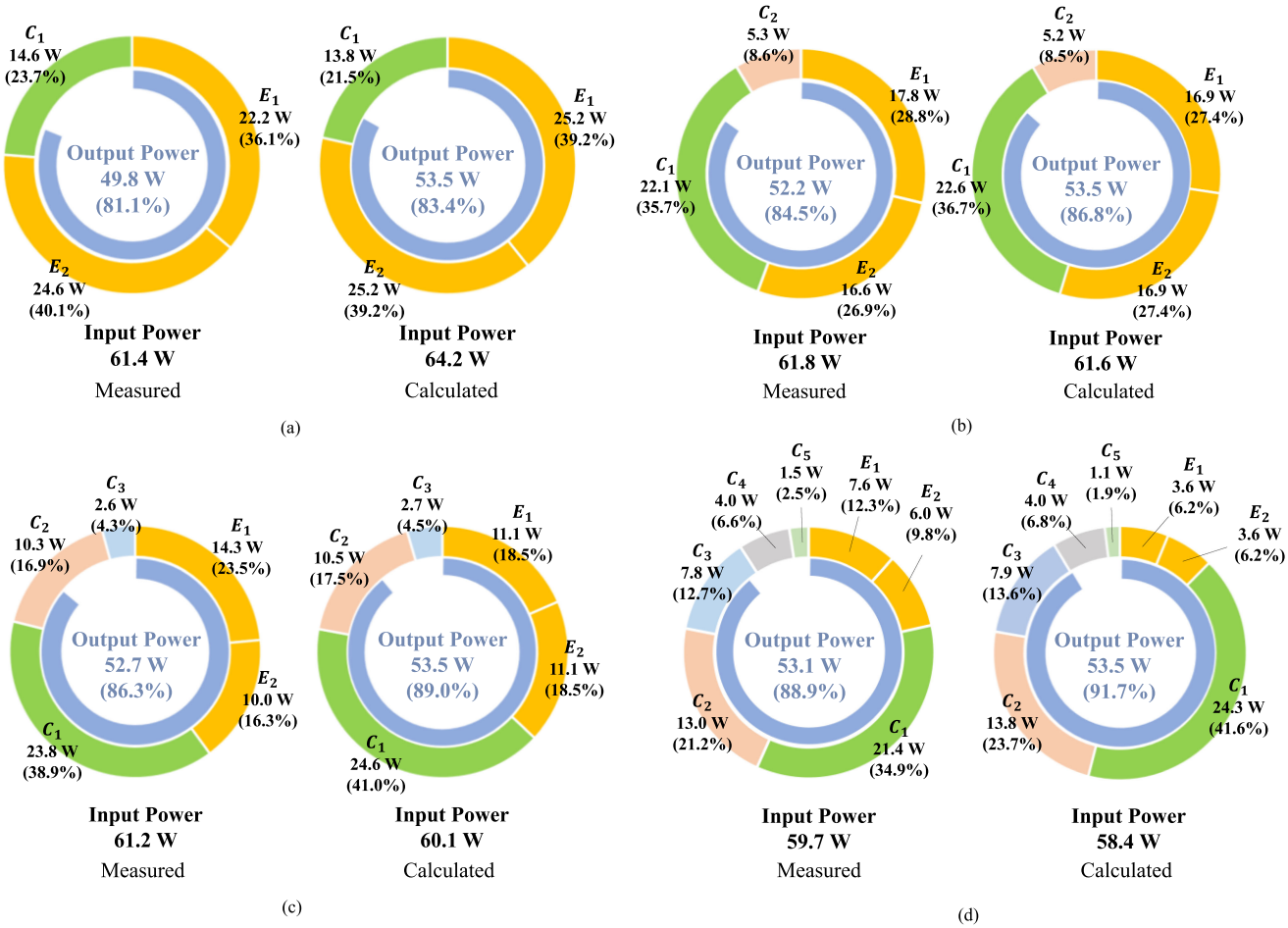

Fig. 18. Measured and calculated efficiencies of prototype FCLA. (a) 4-series FCLA (Fig. 15). (b) 6-series FCLA. (c) 8-series FCLA. (d) 12-series FCLA (Fig. 17).

distortion discussed above, due to the difference in the response speed between n-channel and p-channel MOSFETs. Practically, it is not a critical issue because its peak-voltage is lower than the theoretical maximum applied voltage of the MOSFETs (E/n). Furthermore, it can be fully compensated by applying feedback control.

Fig. 17 shows the experimental waveforms of the 12-series FCLA. It is confirmed that the 12-series FCLA operates as a current amplifier, although the 12-series FCLA has 12 current paths. It is seen that each drain–source voltage of the MOSFETs is kept below $E/12$. From these experimental results, the fundamental operation of the FCLA can be verified.

C. Experimental Efficiencies of the FCLAs

Fig. 18 shows the breakdown of measured and calculated powers and efficiencies of the prototype 4-series, 6-series, 8-series, and 12-series FCLAs. In this regard, the input power P_{Ck} of the flying-capacitor C_k, where k is within $n/2 \leq k \leq n-1$, is zero in principle. From Fig. 18, it is verified that the efficiency is improved by increasing the number of series MOSFETs from 4 to 12. In the 12-series FCLA, an efficiency of 88.9% was measured, an improvement of 10 points compared to the conventional class-B amplifier. The differences between the measured and calculated efficiencies in Fig. 3 are mainly caused by the circulating current flowing through the dc voltage, Zener diodes, and gate resistors.

D. Experimental Verification of Voltage Balancing Control

A prototype of the FCLA with individual gate circuits is designed to confirm the validity of the proposed capacitor voltage balancing. Fig. 19 shows the block diagrams of the proposed system. In this system, the FPGA controller determines the operation mode according to the reference output voltage and feedback flying-capacitor voltages and outputs the digital signals $v_{\mathrm{in\_}k}$ and $v_{\mathrm{in\_p}k}$ to the linear gate drivers. In the linear gate driver, the digital input signals are insulated by the digital isolators and converted to analog signals by Digital to Analog (D/A) converters. Non-inverting amplifiers amplify the output analog signals of the D/A converters at the final stage of the linear gate driver. Finally, the analog voltages are output to the gate-drain terminals of each MOSFET. Each gate circuit requires an isolated power supply in the circuit configuration with the individual gate circuits shown in Fig. 5 unlike that with the common gate circuit in Fig. 1. However, since this circuit does not perform switching operation, the usual isolated power supply circuits such as the bootstrap and charge pump cannot be

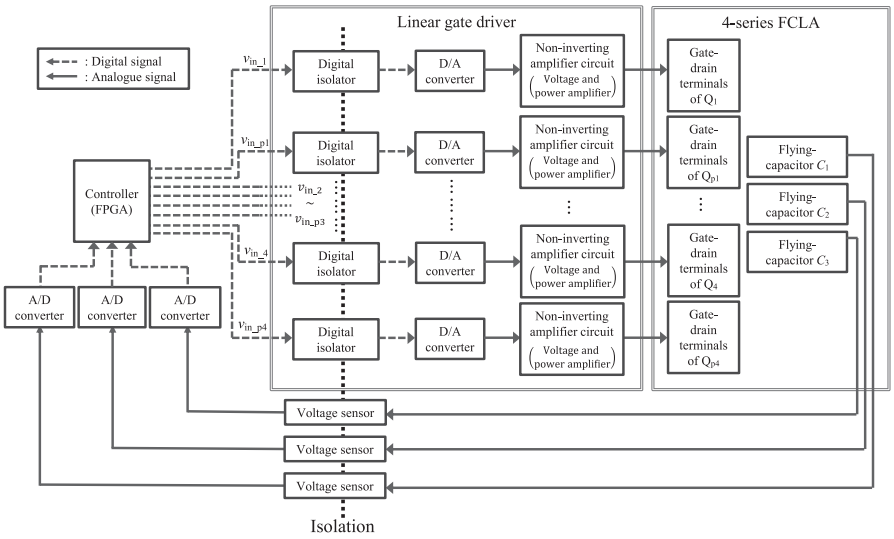

Fig. 19. Block diagrams of the FCLA with the proposed voltage balancing control of the flying capacitors.

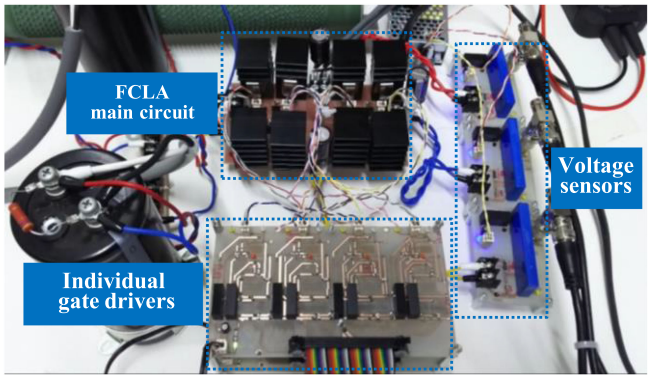

Fig. 20. Photo of 4-series FCLA applying voltage balancing control.

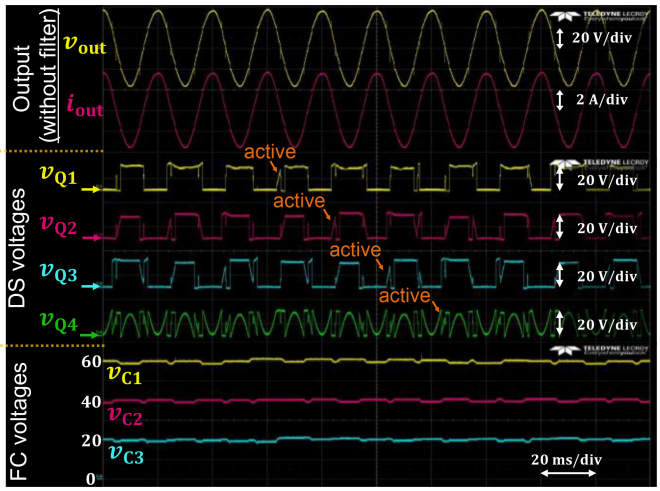

Fig. 21. Experimental waveforms using voltage balancing control for flying capacitors.

applied unlike the general PWM converter. This prototype circuit is designed using isolated dc-dc converter modules IH0524SH produced by XP Power. In this way, the state of each MOSFET can be controlled, and the proposed control can be practically realized.

Fig. 20 shows an overview of the laboratory prototype of the 4-series FCLA with the proposed gate drivers. Fig. 21 shows the experimental waveforms in the prototype circuit. In the output waveforms, a smooth sinusoidal waveform can be obtained, although the low-pass filter is not connected to the output terminal. From the waveforms of the drain-source and flying-capacitor voltages, it is confirmed that the active-state MOSFET changes according to the flying-capacitor voltages, and the flying-capacitor can be charged and discharged adequately. As a result, all the flying-capacitor voltages are maintained at the regulated values. Furthermore, the maximum drain-source voltage is maintained at approximately 20 V for the input dc voltage E of 80 V without surge voltage and EMI.

The efficiency of the prototype FCLA was measured as 80.6%, and the total harmonic distortion of the output voltage was 2.81%. As shown in Fig. 18(a), the efficiency of the 4-series FCLA with the common gate circuit was 81.1%. Thus, the efficiency degradation by introducing the capacitor voltage balancing control was approximately 0.5%, which means that the capacitor voltage balance can be achieved with a small loss. Thus, the 12-series FCLA with capacitor voltage balancing can achieve approximately 88% according to the experimental results shown in Fig. 18(d). A further increase in the number of the series MOSFETs enhances efficiency. From the results, the usefulness of the proposed capacitor voltage balancing control is verified.

VI. Discussion of Efficiency Considering Capacitor Voltage Balancing Control

Fig. 22 shows a summary of the relationship between the number of the series MOSFETs and the efficiency of the FCLA discussed above. The red plots show the calculation result using

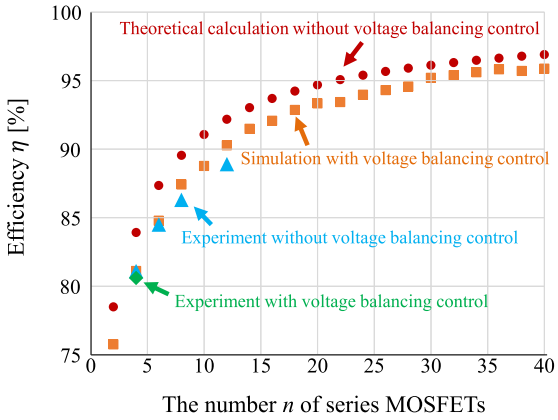

Fig. 22. Relationship between the number of series MOSFETs and efficiency of FCLA.

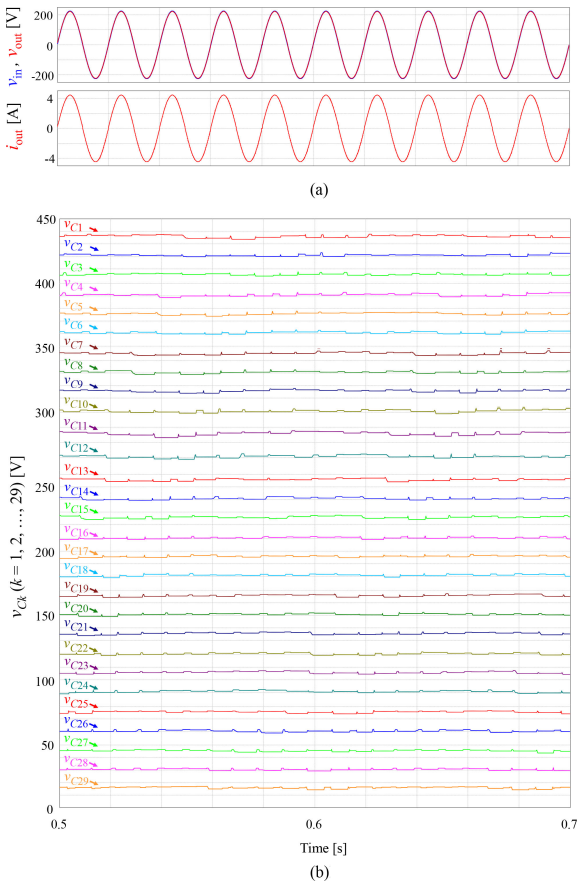

Fig. 23. Simulation waveforms of 30-series FCLA with the voltage balancing control. (a)Input voltage, output voltage and current. (b) Each flying capacitor voltage.

the theoretical formula (3). The orange plots are the results with individual input for the capacitor voltage balancing obtained by the simulations. Moreover, the experimental results are plotted as blue and green markers. From the result, it can be confirmed that the efficiency can be improved by increasing the number of series MOSFETs. Furthermore, it is clarified that the efficiency of the 30-series FCLA with the individual inputs exceeds 95%. The FCLA with over 95% efficiency can be used as a PWM inverter without harmonics and EMI. The gate loss is not considered in this efficiency calculation. It is considered that the gate loss has no significant effect on the total efficiency in the FCLA with sufficiently high power from the viewpoint of practical use.

Fig. 23 shows the simulation waveforms of the 30-series FCLA. The proposed capacitor voltage balancing control has the scalability for the number of series MOSFETs. Even in the 30-series circuit, it is observed that capacitor voltage balance is achieved by the proposed method. It is useful to increase the number of the series MOSFETs and contribute to realizing a power converter with the attractive performance of low harmonics, low EMI, and high efficiency by the FCLA.

VII. Conclusion

This paper presented a flying-capacitor linear amplifier (FCLA) to realize high-efficiency, low harmonic distortion, and low EMI. The characteristics of the FCLA were analyzed and evaluated. Its efficiency can be enhanced by increasing the number of series MOSFETs and by using a suitable design.

The proposed individual linear gate circuit balances the voltage of the flying-capacitors through appropriate changes in the charging and discharging currents. Furthermore, it was confirmed through a simulation that the efficiency of the FCLA with the individual gate circuit can also be improved by increasing the number of series MOSFETs. The prototype design and implementation of the linear gate circuit were shown, and the feasibility of the proposed method was verified. In this way, the proposed voltage balancing method enables a significant increase in the number of series MOSFETs in the FCLA because no additional voltage-balancing circuits are needed in the main circuit. Therefore, it contributes to realize an efficient and low-noise power converter using the FCLA with a high number of series MOSFETs. This paper demonstrated that the prototype 12-series FCLA achieves 89% efficiency as a first result.

The concern of the decrease in circuit reliability due to the high device count remains in the FCLA as in multi-level converters. However, the features of a low overshoot voltage and low EMI in the FCLA are expected to decrease the failure rate and circuit design cost compared to multi-level converters using the switching operation.

Appendix

In this appendix, the theoretical efficiency of the FCLA shown in (3) is derived.

In the n-series FCLA in Fig. 1, the currents i_{E1} and i_{E2} of the dc voltage sources E_1 and E_2, the current $i_{\mathrm{FCLAQ}k}$ and the drain-source voltage $v_{\mathrm{FCLAQ}k}$ of the MOSFETs Q_k, and the currents i_{Ck} of the flying-capacitors C_k, can be described as follows:

$$i_{E1} = \begin{cases} i_{\mathrm{out}} & \left(\begin{array}{c} \theta_1 < \theta < \pi - \theta_1, \\ \pi < \theta < \pi + \theta_1, \\ 2\pi - \theta_1 < \theta < 2\pi \end{array} \right) \\ 0 & (\text{otherwise}) \end{cases} \tag{4}$$

$$i_{E2} = \begin{cases} -i_{\text{out}} & \#\begin{pmatrix} 0<\theta<\theta_1, \\ \pi-\theta_1<\theta<\pi, \\ \pi+\theta_1<\theta<2\pi-\theta_1 \end{pmatrix} \\ 0 & \#(\text{otherwise}) \end{cases} \tag{5}$$

$$\begin{matrix} i_{\text{FCLAQ}k} \\ \left(k \le \frac{n}{2}\right) \end{matrix} = \begin{cases} i_{\text{out}} & \#\begin{pmatrix} \theta_k<\theta<\pi-\theta_k\,, \\ \pi<\theta<\pi+\theta_k\,, \\ 2\pi-\theta_k<\theta<2\pi \end{pmatrix} \\ 0 & \#\,(\text{otherwise}) \end{cases} \tag{6}$$

$$\begin{matrix} i_{\text{FCLAQ}k} \\ \left(\frac{n}{2}<k\right) \end{matrix} = \begin{cases} i_{\text{out}} & (0<\theta<\pi) \\ 0 & (\text{otherwise}) \end{cases} \tag{7}$$

$$\begin{matrix} i_{Ck} \\ \left(k<\frac{n}{2}\right) \end{matrix} = \begin{cases} i_{\text{out}}\begin{pmatrix} \theta_{k+1}<\theta<\theta_k, \\ \pi-\theta_k<\theta<\pi-\theta_{k+1} \end{pmatrix} \\ -i_{\text{out}}\begin{pmatrix} \pi+\theta_{k+1}<\theta<\pi+\theta_k, \\ 2\pi-\theta_k<\theta<2\pi-\theta_{k+1} \end{pmatrix} \\ 0 \quad (\text{otherwise}) \end{cases} \tag{8}$$

$$\begin{matrix} i_{Ck} \\ \left(\frac{n}{2}\le k\right) \end{matrix} = 0 \tag{9}$$

$$\begin{matrix} v_{\text{FCLAQ}k} \\ \left(k \le \frac{n}{2}\right) \end{matrix} =$$

$$\begin{cases} \frac{E}{n} - i_{\text{out}}\cdot R_{\text{on}} & \#\begin{pmatrix} 0<\theta<\theta_k, \\ \pi-\theta_k<\theta<\pi\,, \\ \pi+\theta_{k-1}<\theta<2\pi-\theta_{k-1} \end{pmatrix} \\ i_{\text{out}}\cdot R_{\text{on}} & \#\begin{pmatrix} \theta_{k-1}<\theta<\pi-\theta_{k-1}\,, \\ \pi<\theta<\pi+\theta_k, \\ 2\pi-\theta_k<\theta<2\pi \end{pmatrix} \\ \frac{E}{n}-\left\{v_{\text{out}}-\left(\frac{n}{2}-k\right)\frac{E}{n}\right\} & \#\begin{pmatrix} \theta_k<\theta<\theta_{k-1}\,, \\ \pi-\theta_{k-1}<\theta<\pi-\theta_k \end{pmatrix} \\ -v_{\text{out}}-\left(\frac{n}{2}-k\right)\frac{E}{n} & \#\begin{pmatrix} \pi+\theta_k<\theta<\pi+\theta_{k-1}\,, \\ 2\pi-\theta_{k-1}<\theta<2\pi-\theta_k \end{pmatrix} \end{cases} \tag{10}$$

$$\begin{matrix} v_{\text{FCLAQ}_k} \\ \left(\frac{n}{2}<k\right) \end{matrix} = \begin{cases} i_{\text{out}}\cdot R_{\text{on}} & \#\,(0<\theta<\pi) \\ \frac{E}{n}-i_{\text{out}}\cdot R_{\text{on}} & \#(\pi<\theta<2\pi) \end{cases}. \tag{11}$$

The input power P_{inFCLA} of the *n*-series FCLA can be calculated as follows:

$$\begin{aligned} P_{\text{inFCLA}} &= \frac{1}{2\pi}\int_0^{2\pi}\frac{E}{2}\cdot i_{E_1}d\theta + \frac{1}{2\pi}\int_0^{2\pi}\frac{E}{2}\cdot i_{E_2}d\theta \\ &+ \sum_{k\,=\,1}^{n-1}\left(\frac{1}{2\pi}\int_0^{2\pi}\frac{n-k}{n}E\cdot i_{Ck}d\theta\right) \\ &= \frac{EI_{\max}}{2n\pi}\left(4\sqrt{n-1}-n\right) + \frac{EI_{\max}}{2n\pi}\left(4\sqrt{n-1}-n\right) \\ &+ \frac{EI_{\max}}{n\pi}\left(n-4\sqrt{n-1}+\frac{4}{n}\sum_{k\,=\,1}^{\frac{n}{2}}\sqrt{nk-k^2}\right) \\ &= \frac{4EI_{\max}}{n^2\pi}\sum_{k\,=\,1}^{\frac{n}{2}}\sqrt{nk-k^2}. \end{aligned} \tag{12}$$

The loss P_{lossFCLA} generated in the FCLA can be calculated as follows:

$$\begin{aligned} P_{\text{lossFCLA}} &= 2\sum_{k=1}^{n}\left(\int_0^{2\pi} v_{\text{FCLAQ}k}\cdot i_{\text{FCLAQ}k}d\theta\right) \\ &+ \sum_{k=1}^{n-1}\left(\int_0^{2\pi} R_{\text{ESR}}\cdot i_{Ck}^2 d\theta\right) \\ &= \sum_{k=1}^{\frac{n}{2}}\left[\frac{EI_{\max}}{2\pi}\left\{\frac{\theta_k-\theta_{k-1}}{2} - \frac{\sin2\theta_k-\sin2\theta_{k-1}}{4}\right.\right. \\ &+ \left.\frac{n-2k+2}{n}\left(\cos\theta_k-\cos\theta_{k-1}\right)\right\} \\ &+ \left.\frac{R_{\text{on}}I_{\max}^2}{2\pi}\left\{\pi+2\left(\theta_k-\theta_{k-1}\right)-\left(\sin2\theta_k-\sin2\theta_{k-1}\right)\right\}\right] \\ &+ \frac{nR_{\text{on}}I_{\max}^2}{4} \\ &+ \sum_{k=1}^{n-1}\left[\frac{I_{\max}^2R_{\text{ESR}}}{2\pi}\left\{2\left(\theta_k-\theta_{k+1}\right)-\left(\sin2\theta_k-\sin2\theta_{k+1}\right)\right\}\right] \\ &= \frac{4EI_{\max}}{n^2\pi}\sum_{k=1}^{\frac{n}{2}}\sqrt{nk-k^2} - \frac{EI_{\max}}{4}\left[1-\frac{2R_{\text{on}}I_{\max}}{E}(n-1)\right. \\ &- \left.\frac{4R_{\text{ESR}}I_{\max}}{\pi E}\left\{\theta_1-\frac{2}{n^2}(n-2)\sqrt{n-1}\right\}\right]. \end{aligned} \tag{13}$$

From the above equations, the efficiency η_{FCLA} of the *n*-series FCLA can be calculated as follows:

$$\begin{aligned} \eta_{\text{FCLA}} &= \frac{P_{\text{inFCLA}}-P_{\text{lossFCLA}}}{P_{\text{inFCLA}}} \\ &= \frac{n^2\pi}{16\sum_{k=1}^{\frac{n}{2}}\sqrt{nk-k^2}}\left[1-\frac{2R_{\text{on}}I_{\max}}{E}(n-1)\right. \\ &- \left.\frac{4R_{\text{ESR}}I_{\max}}{\pi E}\left\{\theta_1-\frac{2}{n^2}(n-2)\sqrt{n-1}\right\}\right]. \end{aligned} \tag{14}$$

Similar to above, the theoretical efficiency of the DCLA can be derived with a loss by the diode forward voltage instead of that by the ESR of the flying-capacitors.

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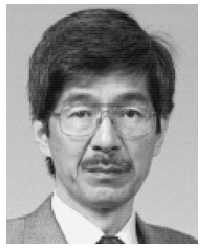

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