Variable Switching Frequency Control of Distributed Resources for Improved System Efficiency

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***Abstract*—This contribution explores the possibility of improving the global efficiency of three-phase inverter-based distributed resources (DR) embedded in low-voltage distribution feeders, by the adaptation of their switching frequency (SF) to the operation point of both the converter and local loads. The core of this proposal lies on the fact that in a good number of applications, in both service and residential sectors, the owner of the DR is also in charge of the losses caused in the local electric power system. This fact leaves room for a global optimization of the power losses, i.e., converter losses will be considered together with those losses caused by the current harmonics injected into the local grid. A dynamic adaptive SF frame of the DR is considered in this proposal to allow its operation beyond its rated frequency at light loads, subjected to the thermal constraints of the device. Simulation results obtained using PLECS software as well as an experimental validation of the method are included.**

***Index Terms*—Distributed resources (DR), efficiency, power losses, variable switching frequency (SF), voltage source converters (VSCs).**

I. Introduction

THE SOARING use of inverters in distributed generation and energy storage applications has increased the attention paid to the efficiency of these devices in recent years. The efficiency of power converters interconnected to the energy power system (EPS) is influenced by regulations, such as [1], which states limits for the harmonic current injection of these devices at the point of common coupling (PCC). In prevailing applications, such as solar and wind, power converters operate rarely at rated values, being the efficiency at light loads a source of great concern [2], [3]. According to [4], the tests to comply with [1], takes only into account the first 40 harmonics. This allows using relatively low switching frequencies (SFs), typically higher than 3 kHz, since the high-frequency harmonics induced by pulsewidth modulation (PWM) will be in this case over the stated limit.

The efficiency of the inverter as a separate unit is the only concern of the owner of the distributed resource (DR) when he is not responsible for the losses upstream. In this case, once verified that the selected SF complies with the harmonic emission limits, it can be maintained constant at any operating condition. In most cases, increasing the SF reduces the efficiency of the device due to the rise of the converter switching losses, while decreasing this parameter could make the device not conform with [4]. Notice that the tests must be conducted not just at 100% but also at 66% and 33% of the output rated current. Most of the efforts carried out in recent years by power electronics researchers in the quest for higher efficiency applications are founded on this concept that treats the DR as a separate unit. Thus, a good number of studies propose alternative power topologies for the grid-tie inverter or for the internal dc–dc stages of the DR, as a way of obtaining improved efficiency [5]–[7]. Other authors focus their approach in advance modulation schemes [8]–[10] or new power electronic devices [11], [12]. The improvement of the DR efficiency by optimizing the interaction between the grid-tie converter and the generation/storage stage is also a widely used approach, e.g., maximum power point tracking methods in wind turbines and photovoltaic (PV) solar systems [13], [14].

In a good number of common applications used in residential buildings and connected to the low-voltage (LV) grid, the owner of the DR is also responsible for the local losses caused by the inverter current harmonics both in line and local loads, up to the metering location at the distribution transformer (either on the LV or medium voltage (MV) side). In assessing the efficiency of the DR in this scenario, the inverter losses should be taken into account together with the distortion losses caused in the local grid [15]. The increasing penetration of DRs has driven power system researchers to deal with efficiency issues in their interconnection to the power grid. Thus, numerous studies can be found with the aim of optimizing the dispatch of these resources in the search of a coordinated behavior [16]–[19], and with the objective of optimizing their location in order to minimize power losses [20], [21]. However, the location of LV DRs is mostly driven by decentralized initiatives, so the assumption of a given site has to be considered in most of the scenarios. In the optimal dispatch approach, convenient active and reactive commands are provided to DRs based on a coordinated operation,

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but harmonic losses and, even less, internal operational features of the converters, such as the SF, are totally neglected. In this paper, the optimization of the efficiency of the DR within the local EPS, based on the adaptation of the SF used in the modulation scheme of the grid-tie converter, is analyzed. This is proposed as a convenient approach for LV applications in which the large impedance of the transformer at high frequencies allows to assume that most of the power losses are under the responsibility of the DR owner. This new approach has the potential to exist together with high-level controllers at the system level, or to be applied to standard converters just relying on local intelligence. Even if by design, a thermal constraint in the increment of the SF at rated power is likely to exist, the possibility of operating the device at higher frequencies when working at light loads is still there. Increasing the SF rises the converter switching losses but reduces the distortion losses in the local grid at the same time. This fact, together with the great advances carried out in recent years in the field of grid impedance estimation techniques [22]–[27], opens the door for a dynamic optimization of the SF capable of achieving an improved overall efficiency.

In Section II, a study of the effect of the SF on the harmonic emission in three-phase voltage source converters (VSCs) is carried out. Two-level inverters with first-order inductive filters are considered, as one of the preferred technologies in LV applications. The evaluation of inverter losses, considering thermal constraints, is presented in Section III. Section IV deals with the estimation of the distortion losses caused by the inverter in the local grid. The proposed method for the online optimization of the SF is described in Section V. Section VI presents a case study to demonstrate the validity of the proposal and experimental results are given in Section VII. Finally, the conclusions of the study are drawn in Section VIII.

II. SF and Current Harmonics

As a general rule, increasing the SF leads to a displacement of the harmonic spectrum of the voltage at the converter terminals to a higher frequency range. Consequently, the inductive behavior of the filter and grid upstream yields to a reduction in the induced current harmonics due to the higher impedance of these inductances at the new frequencies. However, it is important to note that the dead-time of the IGBTs limits the validity of the said statement, leading to the emergence of low-frequency harmonics (mainly 5th and 7th order) [28], [29] with a growing impact at higher SFs. Nevertheless, this effect can be mitigated by current regulators, whose bandwidth use to fall within these values. Fig. 1 shows the current distortion of an inverter given by the parameters shown in Table I as a function of the SF. According to the standard, [1], this value has been reported as the total rated-current distortion (*TRD*), where

$$TRD = \frac{\sqrt{\sum I_i^2}}{I_n} \tag{1}$$

which can be defined as the total root sum square of the current harmonics injected by the DR unit I_i, divided by the rated current capacity of that unit, I_n. In Fig. 1, the *TRD* has been split in two terms, TRD_{lf} and TRD_{hf} using the 40th harmonic included in [4] as a limit between low and high frequencies. Thus, those parameters can be related as

$$TRD = \sqrt{TRD_{lf}^2 + TRD_{hf}^2} \tag{2}$$

which allows us to show the different behavior of the theoretical PWM harmonics and the nonidealities induced by the dead-time. As it is shown in Fig. 1, the effect of the dead-time reaches such an importance in *TRD* that increasing the SF over a certain limit becomes counterproductive. The use of dead-time compensation techniques [30], [31] could potentially raise this limit. It is also interesting to point out that the results shown in Fig. 1 are independent of the load of the converter, as only the fundamental component varies on a significant scale with the SF. On the contrary, and especially in weak grids, the values shown in this graph can be affected to some extent by the impedance of the system upstream from the converter terminals, which is referred to as *system impedance* throughout this paper. This suggests that an online measurement of harmonic distortion will provide better results than a theoretical estimation. Nonetheless, the simplicity of this estimation can be valuable in most cases.

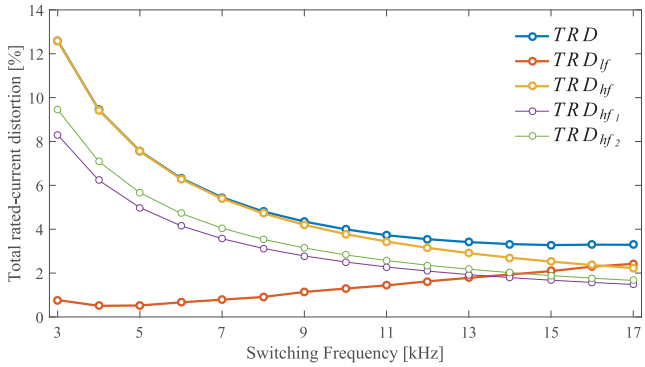

Fig. 1. Current *TRD* as a function of the SF for different frequency bands. Effect of the dead-time in low-frequency harmonics.

TABLE I
Converter Parameters

Hardware	
Grid voltage	$V_{rms} = 400$ V, $f = 50$ Hz
Rated power/current	$S = 30$ kVA, $I_n = 43.3$ A
System impedance	Direct coupling to an ideal grid
Coupling inductor	$L_{filter} = 1.0$ mH, $R_{filter} = 0.16$ mΩ
DC link	$v_{dc} = 800$ V, $C = 350$ μF
IGBT modules	2MBI200HH-120-50
Dead-time	$t_d = 1$ μs
Control	
PWM Type	Sym. regular sampled w/ 3^{rd} harm. injection
SF at rated power	$f_{sw} = 3$ kHz
PLL	Dual 2nd Order Generalized Integrator (SOGI)
Anti-aliasing filter	Butterworth 2nd order, $f_c = f_{sw}/2$
Current reg. bandwidth	300 Hz
Power factor	1

III. Converter Losses and Thermal Limits

Converter losses, P_{VSC}, are mainly determined by switching losses, P_{sw}, and conduction losses, P_{cd} [11], [32], [33]. Other issues should be considered when assessing the efficiency of

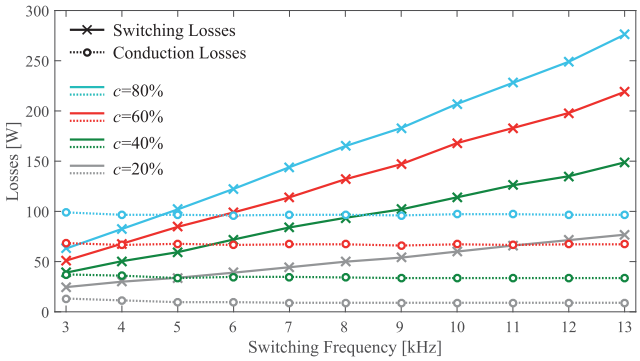

Fig. 2. Converter switching and conduction losses as a function of the SF.

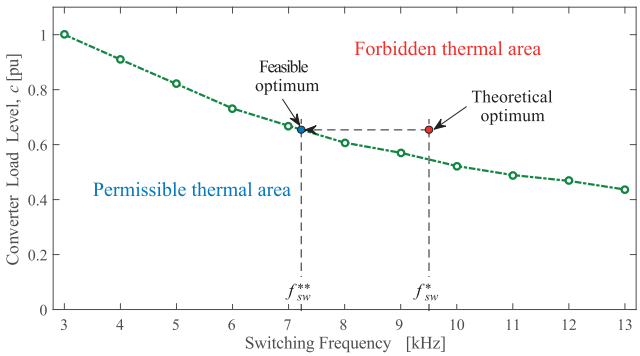

Fig. 3. Thermal constraints for variable SF operation.

these devices, such as cooling power; however, as they are not normally affected by the SF, they will not be considered in this paper. Switching losses are strongly influenced by the SF, f_{sw}, as well as by the load level of the converter c, defined as the ratio between the actual and rated current. Even if the power factor of the converter also affects this parameter due to variations in the commutation phenomenon, this effect is hardly noticeable and can be neglected with little error for the aim of this study. As increasing the SF results in a proportional rise of switching events, the relationship between the SF and switching losses is almost lineal. Conduction losses, for its part, are mainly affected by the load of the converter, and in a more subtle way, by the SF due to the increased current distortion that arises at lower frequencies. Taking these facts into consideration, an approach to the converter losses, with c and f_{sw} as parameters, can be obtained by using

$$P_{VSC}(c, f_{sw}) = P_{sw}(c, f_{sw}) + P_{cd}(c, f_{sw}). \quad (3)$$

The assessment of the aforementioned power losses for the specific IGBT power modules mounted in the converter used for the experimental validation included in Section VII is shown in Fig. 2. To obtain the graph, a PLECS model of the converter was implemented [34]. This model includes the thermal performance of the IGBT power modules, which allows to depict the operational constraints of the converter in terms of SF. Thus, the imperative derating of the device is shown in Fig. 3. This figure was calculated for each SF by assessing the load level of the converter at which the junction temperature of the solid

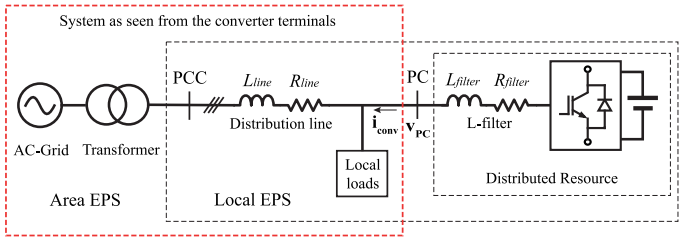

Fig. 4. Local EPS with embedded DRs.

state devices equals the temperature reached at rated values. The inclusion of these data in a two-dimensional (2-D) look-up table (LUT), together with the use of interpolation, is enough to obtain a good estimation of converter losses as a function of c and f_{sw} in the optimization scheme proposed in this paper. The exploitation of this table for control purposes by operating the converter at variable SF is analyzed in Section V. In any case, it is clear from Fig. 3 that, if the SF command f_{sw}^{*} lies on the forbidden area of the graph, it has to be reduced to the nearest feasible value, f_{sw}^{**}.

IV. Distortion Losses in the Local Grid

Even if limited by regulations, the injection of current harmonics into the distribution grid can cause significant power losses that are classified in the following two categories: First, copper losses in the distribution line and distribution transformer, and second, power losses in local loads. Notice that additional losses could exist upstream from the distribution transformer that are not on the local EPS owner's responsibility. However, this term can be neglected, not only because of the low value of the resistive contribution from the MV level when compared with the LV side, but also because of the low capability of high-order current harmonics to travel deep into the EPS. Fig. 4 shows a layout of the benchmark system considered in this paper. The local EPS, with embedded DRs, is connected to the area EPS through a distribution transformer, being the metering devices connected either in the MV or LV side according to the ownership of this piece of equipment. Both the DRs and the local loads are connected to the distribution line. Those local loads located close to the power converters are more prone to suffer from distortion losses. In Fig. 4, a local load is connected directly to the DR point of coupling (PC) to highlight this phenomenon. The effect of the distortion power in local loads is different according to the type of device (motor, lighting, heating, etc.) and its nature (linear/nonlinear). In any case, distortion power can be, as a general rule, considered undesirable [35]. Different types of penalization criteria could be considered in order to take into account the harmful effects of higher levels of injected current distortion in particular loads, e.g., cost associated to the loss of life. However, in this paper, only the cost associated with the power transmitted at the non-fundamental frequency is taken into account. A pure resistive load is considered in this paper as the easiest way to underline the benefits of the proposal.

A precise calculation of the power transmitted by the converter at harmonic frequencies can be done by assessing the

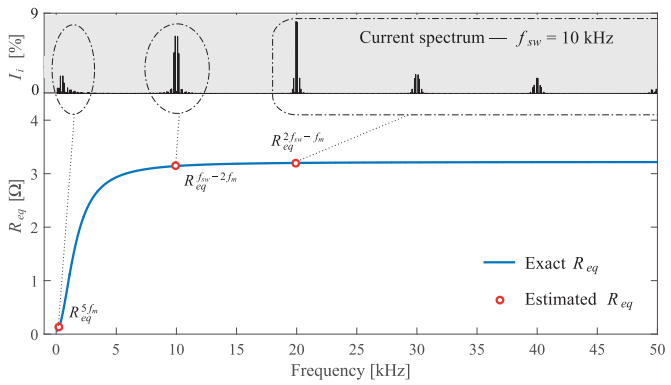

Fig. 5. Estimation of the resistive component of system impedance at the PC as a function of frequency.

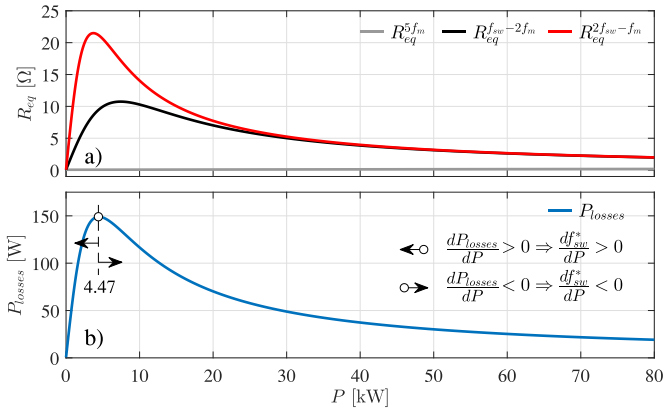

Fig. 6. Effect of the power demand of local loads in harmonic power losses. (a) Resistive component for the frequencies of interest (f_{sw} = 10 kHz, f_m = 50 Hz). (b) Harmonic power losses.

TABLE II
INSTALLATION PARAMETERS

Transformer	
Rated power	$S_n = 100$ kVA
Short-circuit impedance & resistance	$Z_{pu} = 0.06$, $R_{pu} = 0.01$
Distribution Line	
Lenght	$l = 200$ m
Resistance	$R_{line} = 0.2$ mΩ/m
X/R ratio	0.32
Local Loads	
Power factor	1
Active power	$P = 50$ kW

expression

$$P_{losses} = Re\left\{\sum_{i=2}^{N} \mathbf{v_{PC}}_i \cdot \mathbf{i}^*_{\mathbf{conv}\,i}\right\} \tag{4}$$

where $\mathbf{i_{conv}}_i$ and $\mathbf{v_{PC}}_i$ are the power invariant space vector harmonic components of the converter current and voltage at its PC, obtained by applying the direct Fourier transform (DFT). For the practical implementation of (4), natural sampling of voltages and currents at SF is not enough due to Nyquist limit, but oversampling can help in complying with these requirements. In any case, other simplified methods, such as Goertzel algorithm [36], are better suited for online applications [37], [38]. In this numerically efficient method, just a selected set of harmonics are identified, which can be enough to calculate the resistive component of system impedance, R_{eq}, at the most relevant bands of the spectrum. This reduced set of values can be used, together with the expected injection of current harmonics given in Fig. 1, to formulate a good estimation of the aforementioned power losses. Fig. 5 shows the value of R_{eq} for the installation depicted in Fig. 4 considering the parameters shown in Table II. The identification of just three impedance values, one at the low-frequency range (5th or 7th) and two at the two lowest PWM frequency bands (e.g., $f_{sw} - 2f_m$ and $2f_{sw} - f_m$, f_m being the modulation frequency), can be enough to estimate distortion losses by using

$$P_{losses} \approx 3I_n^2 \cdot \left(R_{eq}^{5f_m} \cdot TRD_{lf}^2 + R_{eq}^{f_{sw}-2f_m} \cdot TRD_{hf_1}^2 + R_{eq}^{2f_{sw}-f_m} \cdot TRD_{hf_2}^2\right). \tag{5}$$

Notice that with this aim, TRD_{hf} has been segregated in two components: TRD_{hf_1}, for the harmonic band around the SF and TRD_{hf_2}, for the rest of higher frequency values. The specific contribution of each of these components can be observed in Fig. 1.

It is important to highlight that the effect of a variation in the power demand, P, of the loads connected to the local EPS, on the harmonic power losses at the line and local loads, P_{losses}, is not obvious. As a consequence, neither is the effect of this variation on the resulting optimum SF. The value of the resistive components of system impedance for the benchmark system shown in Fig. 4 are the result of the parallel equivalent represented by the RL branch of the line and transformer and the resistive branch represented by the local loads. For the data shown in Table II, the value of these resistive components for the frequencies of interest is depicted in Fig. 6 as a function of P. At low power demand levels, the connection of new loads increases harmonic power losses. On the contrary, beyond a certain power demand, 4.47 kW in the present case, the connection of new loads decreases the resistive value of system impedance, and thus, harmonic power losses. For this reason, if the DR is working at a fixed load level, c, with a low power demand of local loads, the connection of new loads drives the optimum SF to higher values in search for a lower level of harmonic losses. Conversely, up from the stated power demand value, the connection of new loads leads to a reduction of the optimum SF value, as higher harmonic losses can be admitted in the search for a global optimum.

V. ONLINE OPTIMIZATION OF THE SF

The fundamentals of the online optimization of the SF proposed in this paper are schematically summarized in Fig. 7. The inputs for the algorithm are as follows: first, the space vector of the converter current, which is already available as calculated from current samples for the operation of its inner controller, and second, the resistive component of system impedance for the different frequency bands considered in Section IV. The application of a set of LUTs together with a SF sweep allows the

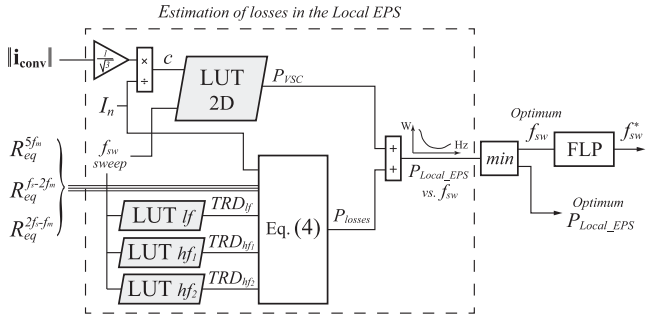

Fig. 7. Online method for the optimization of the SF.

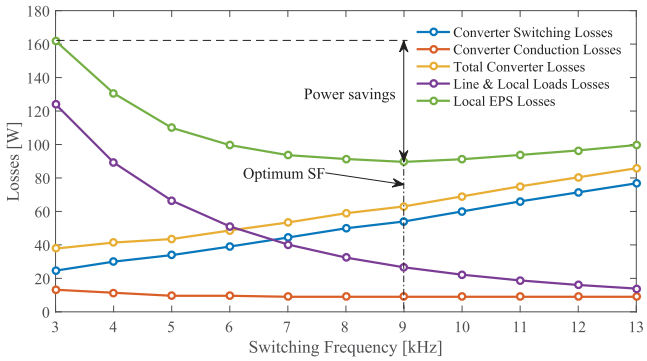

Fig. 8. Local EPS losses as a function of SF – $c = 20\%$.

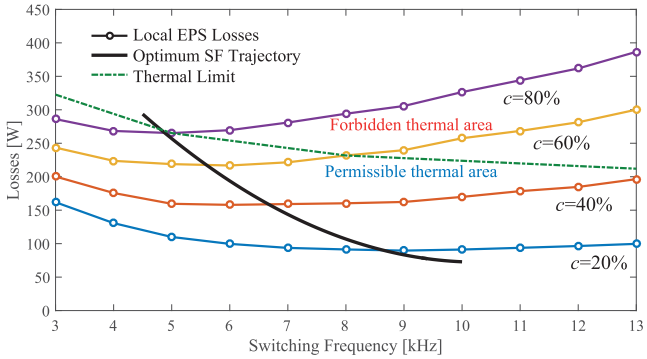

Fig. 9. Optimum trajectory of the SF as a function of converter load.

online calculation of a curve, relating the losses at the local EPS, $P_{\text{Local\_EPS}}$, with the SF, f_{sw}, for the present operating point. With this aim, the converter losses, P_{VSC}, are obtained from a 2-D-LUT built by adding the conduction and switching losses of the specific converter according to (3). A set of three 1-D-LUTs, built from the distortion data depicted in Fig. 1, provides the *TRD* of the converter at the different frequency bands for each SF used in the sweep. From these results, the losses at the line and local loads, P_{losses}, are obtained by using (5). The addition of both converter losses and line and local load losses at each SF leads to the desired curve. Then, the minimum of this curve is identified, which gives the optimum losses at the local EPS and, even more important, the optimum SF for the current operating point. Notice that the bandwidth of the SF command, f^*_{sw}, must be much lower than the one used in the inner controllers of the inverter not to interfere with its dynamic performance. As a consequence, a low update rate of this command is acceptable and the required computational burden can be assumed by the controller without a significant effort either in a synchronous or asynchronous scheme. In order to avoid the effect of noise in the sampled parameters, as well as steep frequency variations due to sudden changes in the inverter load level or in the system impedance—due to the connection/disconnection of local loads, a first-order low-pass (FLP) filter is used to smooth the frequency command.

Although not depicted in Fig. 7 for the sake of clarity, the frequency command, f^*_{sw}, should pass a final limitation stage in order to make the control compatible with the thermal constraints shown in Fig. 3. As already stated in Section III, if the pair (f^*_{sw}, c) lies in the forbidden area of this graph, the SF command is reduced to the maximum SF compatible with the present converter load level, f^{**}_{sw}.

VI. Case Study

In this section, a case study is used to illustrate the advantages of using an overall efficiency optimization of the DR within its local EPS. With this aim, the LV distribution feeder and the distributed generator (DG) depicted in Fig. 4 are considered. The parameters of the grid infrastructure are shown in Table II while those from the inverter-based DG are given in Table I (except for the system impedance, that for this case study is derived from Table II). Fig. 8 shows the total losses in the local EPS, together with its different components, i.e., converter losses and grid and local loads losses for a DR working at 20% of its rated power with unity power factor. It is concluded from this drawing that increasing the SF from the design parameter, 3 to 9 kHz, reduces the local EPS losses in a 44.6%, and improves the overall efficiency at this load level (i.e., the ratio between the local EPS losses and the power delivered by the converter) in 1.20%.

Fig. 9 expands the analysis to different load levels of the DR. As it is depicted in this figure, connecting the values of the minimum local EPS losses at each converter load level, c, leads to the optimum trajectory of the inverter SF. Furthermore, the thermal limit of the device is also given in Fig. 9. This limit is established by calculating the maximum acceptable SF at each load level, which is determined by the frequency that leads to the design temperature (i.e., the one obtained at 3 kHz and rated power). From the aforementioned graph, it can be concluded that for the device under test, a variable SF mode with optimization of losses is only feasible for loads lighter that 80% of rated power. Moreover, it is also observed that the benefit of the proposal is much more relevant at light loads: e.g., the saved power is higher at 20% than at 80% on both relative and absolute terms (72 W versus 21 W and 1.20% versus 0.09%).

Fig. 10 shows simulation results of the application of the online optimization method proposed in Section V to the present case study. An update rate of 10 ms was used for the SF command and a bandwidth of 0.6 Hz was selected for the FLP filter. The SF sweep included in the algorithm is conducted with a resolution of 100 Hz in order to limit the computational burden.

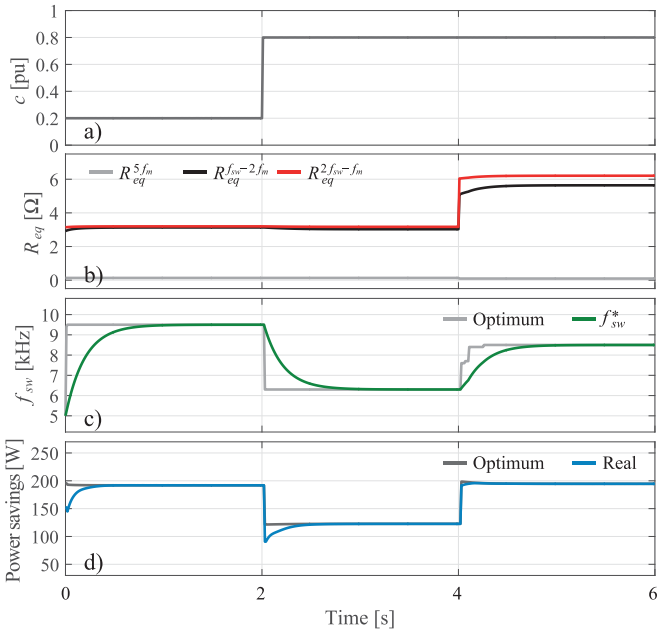

Fig. 10. Application of the optimization method to the proposed case study. (a) Converter load profile. (b) System impedance. (c) SF command. (d) Power savings.

As it is shown in Fig. 10(a), the converter load level is started at $c = 20\%$ and increased to $c = 80\%$ after 2 s, always with unity power factor. Moreover, the local loads stay at rated power according to Table II and are reduced to 50% of this value, i.e., 25 kW at 4 s. Fig. 10(b) shows the effect of the steep variation on the resistive components of system impedance induced by the local load reduction. After the load variation, slight modifications can be still observed on these values, which are caused by the SF drift along the process, due to the influence of reactive components on the resistive equivalent. The optimum SF value obtained by the algorithm along with the final SF command, i.e., after the FLP, is depicted in Fig. 10(c). The converter is started with a conservative SF value of 5 kHz and, from this instant, the algorithm competently tracks the optimum SF increasing the efficiency of the installation. As predicted in Fig. 6, the reduction of the power demand of local loads from 50 to 25 kW at 4 s leads to a rise of the optimum SF. In Fig. 10(d), the optimum and real power savings, compared to a traditional operation of the DR at constant SF, are depicted. As expected, greater power savings are obtained with the converter working at light loads as well as with an increased value of the resistive component of system impedance.

VII. Experimental Results

Two sets of experimental tests were carried out in this paper: the first one is aimed to prove the power saving potential of the stated proposal, and the second, to demonstrate the validity of the online SF optimization method described in Section V.

A. Test 1

The test setup used in this case is shown in Fig. 11. A four-quadrant grid simulator, TC.ACS by Regatron, is used to

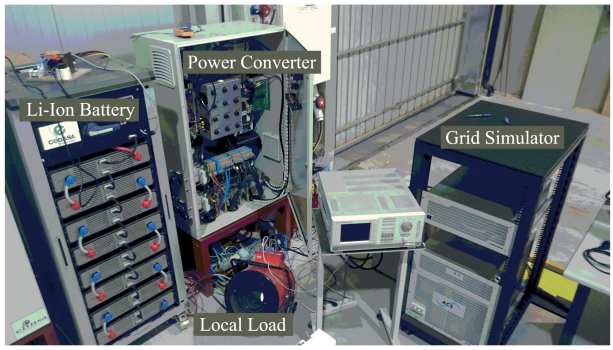

Fig. 11. Test setup.

emulate the electric system, 400 V –50 Hz, and a 0.32 mH inductor, L_1, is used to emulate the LV line and transformer according to Fig. 4. An almost purely resistive air-heating system with a rated power of 9 kW is used to emulate the local loads according to the figure. Finally, a custom-made three-phase two-level VSC, with a rated power of 30 kVA and a design SF of 6 kHz, is coupled to the grid through a 0.88 mH inductor, L_2, to play the role of the DR.

During this test the converter is operated in STATCOM mode at a light load, 10 kVA (i.e., $c = 33\%$), delivering reactive power to the LV grid. Similar results are expected from other operation modes, due to the small influence of the power factor in converter losses, as it was stated in Section II. The three-phase voltages and currents at the PC of the DR, PC in Fig. 4, were registered in steady state for different SFs within the range 6 –16 kHz. An offline handling of these measurements were carried out to calculate their DFT, and subsequently, the losses at harmonic frequencies at the line and local loads (i.e., those caused by the air-heating system and parasitic resistance of L_1) were calculated by the application of (4). For the particular case of the STATCOM operation mode, including the term at the fundamental frequency in (4) leads directly to the converter losses, so finally, the losses at the local EPS can be computed in a simple way as

$$\begin{aligned} P_{Local\_\mathrm{EPS}} &= Re\left\{\sum_{i=2}^{N} \mathbf{v_{PC}}_i \cdot \mathbf{i}^*_{\mathbf{conv}\,i}\right\} \\ &\quad - Re\left\{\sum_{i=1}^{N} \mathbf{v_{PC}}_i \cdot \mathbf{i}^*_{\mathbf{conv}\,i}\right\} \\ &= -Re\left\{\mathbf{v_{PC}}_1 \cdot \mathbf{i}^*_{\mathbf{conv}\,1}\right\}. \end{aligned} \tag{6}$$

Notice that this is just a particular result valid only for STATCOM operation mode. As stated in Section III, in a more general scheme in which the DR participates in the active power flow (inverter/rectifier mode), a LUT, with and estimation of converter losses as a function of the SF and the converter load level, ought to be used.

The results of the test are presented in Table III and Fig. 12. Thus, the spectra of the power invariant space vectors of voltage and current, at the PC of the DR, are shown in Fig. 12 for selected key SFs, such as 8, 12, and 16 kHz. Both the positive and negative sequence components are displayed in this image.

TABLE III
EXPERIMENTAL RESULTS – $c = 33\%$

SF	Losses			Pwr. savings
	Converter	*Line&Loads*	*Local EPS*	
6 kHz	781.2 W	253.8 W	1035.0 W	0.0 W
8 kHz	790.5 W	178.4 W	968.9 W	66.1 W
10 kHz	814.0 W	139.8 W	953.8 W	81.1 W
12 kHz	836.3 W	111.2 W	947.6 W	87.5 W
14 kHz	868.1 W	91.6 W	959.7 W	75.3 W
16 kHz	896.9 W	76.9 W	973.8 W	61.2 W

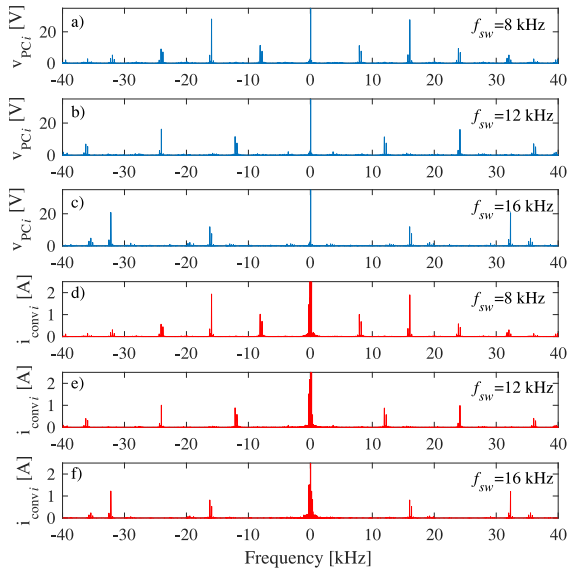

Fig. 12. Spectrum of signals measured at the PC for different SFs. (a), (b), and (c): Voltage space vector for 8, 12, and 16 kHz, respectively. (d), (e), and (f): Current space vector for 8, 12, and 16 kHz, respectively. Note: Fundamental components are truncated for the sake of clarity.

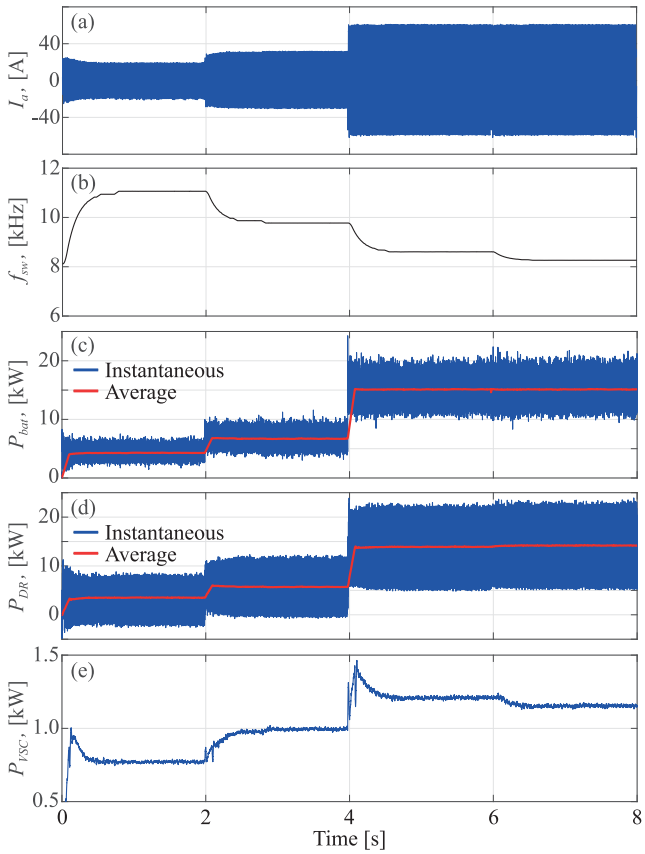

Fig. 13. Online SF optimization test. (a) Converter ac current—phase a. (b) Converter SF. (c) Power supplied by the Li-Ion battery—dc–dc converter output side. (d) Power supplied to the grid. (e) Converter losses.

The most significant harmonics, located in bands around one and two times f_{sw}, are shifted to higher frequencies as the SF increases. Also, a clear reduction in the injection of harmonic currents can be observed at higher SFs. In Table III, the computed values for converter losses, line and load losses, and local EPS losses for each of the analyzed SFs are displayed, together with the resulting power savings. Specifically, harmonic power losses at the line and loads are calculated by using (4), while the application of (6) allows the computation of the local EPS losses. Both equations take the voltage and current harmonics of Fig. 12 as an input. Finally, the difference between the results from (6) and (4) gives the value of converter losses. As expected, an optimum SF is obtained, capable of achieving the minimization of system losses. As it is highlighted in Table III, the operation at 12 kHz reduces the overall system losses in 87.5 W when compared with the operation at the design value. This means a reduction of around 8.4% of the losses at this operation point ($c = 33\%$), and thus, an improvement of the local EPS efficiency, which increases from 89.65% to 90.52%.

B. Test 2

Slight changes are introduced in the test setup for this case. The 30 kVA converter is now operated in inverter mode to effectively replicate the performance of a DR. With this aim, the dc bus of the converter is fed from the Li-Ion battery shown in Fig. 11 through a dc–dc stage. Furthermore, the converter is now coupled to the utility grid, 400 V –50 Hz, through a dedicated distribution line and transformer according to the values shown in Table II. Three separate air-heating systems, each with a rated power of 9 kW, are used to emulate the local loads. The connection/disconnection of these systems allows to test the effect of a sudden change in system impedance.

The custom-made converter is operated through a controller using a TI C2000 Delfino TMS320F28335 MCU. The algorithm described in Section V was included in the firmware with the LUT system embedded in nonvolatile RAM memory. Moreover, a variable SF inner current controller for the converter was specifically designed for this test, including an adaptive tuning of the associated regulators.

During the test, the dc–dc converter is commanded with different power steps, as shown in Fig. 13(d), while the VSC fixes a constant dc-bus voltage value of 800 V and a constant power factor of 0.6. The test is started at a light load, 7.5 kVA (i.e., $c = 25\%$), thus delivering 4.5 kW to the grid, while two of the 9-kW air-heating devices stay connected to emulate the local loads. After 2 s, the converter load level increases to 12 kVA (i.e., $c = 40\%$) and then to 27 kVA (i.e., $c = 90\%$) at time 4 s, so that up to 16.2 kW are injected into the local grid. Fig. 13 shows the phase current of the VSC during these variations together

with the performance of the SF in reaction to those load step changes. Finally, at time 6 s, one air-heating system is added to the two devices already connected to the local grid, thus shifting the local demand from 18 to 27 kW. As predicted in Fig. 6, the consequent change in system impedance at the converter PC causes a reduction of harmonic power losses that leads to a fall in the optimum value of the SF.

Fig. 13 shows the measurements of the power supplied by the Li-Ion battery along the test, together with the power supplied by the VSC to the local grid. Thus, in Fig. 13(e), the VSC losses are obtained. The value of line and local load losses are calculated from voltage and current measurements for each step (considering steady state intervals) through fast Fourier transform analysis, being 92.5, 137.6, 192.0, and 180.6 W, respectively. As expected, during the first three steps, the decreasing SFs lead to increasing line and local load losses. In the fourth step, even if the SF is further reduced, the decline of the Thevenin impedance of the system at the converter PC, due to the connection of a new load, overcomes this effect.

A comparison of the losses at the first step of the test, i.e., the one conducted with a lighter load, $c = 25\%$, with those obtained for the same conditions in a fix SF scheme of 6 kHz, reveals that up to 132 W can be saved using the proposed operating mode. This means increasing the efficiency in 1.7% at the present operating point and in 0.4% if referred to the rated power of the converter.

VIII. Conclusion

This paper presents an operation strategy for DRs based on the use of an adaptive SF framework in the grid-tie converter with the aim of achieving an overall improvement of the efficiency within the local EPS. The contribution demonstrates the interest of considering the converter losses together with the induced harmonic losses in the local line and loads when the ownership/operation of both assets is held by the same entity. The proposed method can be applied to DRs relying only on local intelligence but also to those in charge of system-level controllers. The thermal limits of the power modules used in the inverter are taken as a constraint in order to assure a safe operation of the device beyond its design SF when working at light loads. A LUT-based system, valid for an online implementation, was designed to provide the DR with a smart regulation of its SF. The results demonstrate that an improvement of the overall efficiency of the system at light converter loads by about 1% is readily achieved with the proposed method. This improvement is especially important for applications in which the grid-tie converter works often under rated power. This is the usual case of widespread technologies, such as PV systems and small wind turbines.

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