

# Temperature-Controlled Power Semiconductor Characterization Using Thermoelectric Coolers

Georges Engelmann<sup>1</sup>, Michael Laumen<sup>1</sup>, Jan Gottschlich, Karl Oberdieck, and Rik W. De Doncker

**Abstract**—Accurate characterization of power semiconductors over wide operating ranges is a necessity to accomplish better electrical and thermal designs of power converters. Especially, switching losses of power devices are rarely given sufficiently detailed in their datasheets, since they also depend strongly on the driving circuitry and design of the power converter itself. A means to extract the switching losses are double pulse measurements where the desired operating points can be freely chosen. This paper introduces a temperature conditioning unit that allows the adjustment of the junction temperature between  $-40\text{ }^{\circ}\text{C}$  and  $200\text{ }^{\circ}\text{C}$  using thermoelectric coolers (TECs). The unit is for an automated double pulse test bench with dc-link voltages of up to 1 kV and switching currents of up to 1 kA. Up to 1 kW of electrical power is required to power the TECs. The design of the power converter is shown as well as the control scheme. An algorithm, which automatically extracts the switching losses of the measured double pulse waveforms is presented. An exemplary characterization of an *Infinite EconoDual* power module is conducted and the results are presented.

**Index Terms**—Control systems, power semiconductor devices, semiconductor device measurements, temperature control, test equipment.

## I. INTRODUCTION

**M**OST DESIGN processes of power electronic converters are based on simulation models. The more accurate these simulation models are, the more optimized designs can be developed, which are required for electric vehicles or in general future power electronics applications to enable compact solutions with a high integration level [1]–[4]. Various models are usually used in several chained simulations [5] that allow a optimization on the system level. Finding accurate models of

different components is the challenge to which this study will contribute.

Besides the electrical design of the converters, the thermal aspect cannot be neglected. For the accurate thermal simulation of power modules, as, e.g., presented in [6], good thermal models for the different components, e.g., heat sinks and power semiconductors, are needed. However, such models are rarely given in the datasheets

A solution to this is to extract thermal models from measurements. In this study, the power semiconductor losses are of interest. Therefore, it is shown how to extract semiconductor switching losses from measurements over wide operating ranges of dc-link voltage  $U_{\text{DC}} = 0\text{ kV} \dots 1\text{ kV}$ , load current  $I_{\text{DC}} = 0\text{ kA} \dots 1\text{ kA}$ , and junction temperatures  $\vartheta_j = -40\text{ }^{\circ}\text{C}$  to  $200\text{ }^{\circ}\text{C}$ . Further measurement dimensions can be imagined, e.g., a variation of the gate resistance using a programmable gate driver [7], but this would go beyond the scope of this paper. A special focus is given on the temperature control unit.

First of all, the semiconductor switching losses are measured using a double pulse test bench [8]. As the switching behavior is temperature dependent [9], [10], a temperature control unit is necessary to set the junction temperature  $\vartheta_j$  to the desired value. Three different temperature control systems are commonly used with power semiconductor modules: compressor based, liquid nitrogen, or thermoelectric cooler (TEC) modules. Full automatic controllability including positive to negative temperatures are a requirement for the temperature control unit. A flexible exchange of the device under test (DUT) with different packages is required. Thus, liquid nitrogen cooling is not considered, because its handling requires too much effort and a separate setup for heating would be necessary. Several compressor-based liquid cooling systems are available that fulfill the required features, however, there is always the risk of a leakage and contamination of the test bench and the expensive equipment with cooling liquid.

Finally, only a TEC remains as a possible solution. The TEC allows cooling and heating with the same setup by simply reversing the current. TECs are already widely employed in electrical applications due to the aforementioned properties, for example, in high-frequency applications [11], [12], for the laser diode cooling [13], superconducting magnets [14], or integrated inside chips [15] to improve the accuracy of on-chip reference elements. TECs are used to build calorimeters [16] or to measure the heat flow out of a DUT as shown in [17]. A temperature control unit based on TECs, which are operating on the Peltier effect [18], got developed and presented in [19]. This study

Manuscript received September 8, 2017; accepted December 19, 2017. Date of publication January 22, 2018; date of current version May 18, 2018. Paper 2017-PEDCC-1082, presented at the 2016 IEEE International Power Electronics and Motion Control Conference, Varna, Bulgaria, Sep. 25–30, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Power Electronic Devices and Components Committee of the IEEE Industry Applications Society. This work was supported in part by the Research Project InSeL, funded by the German Federal Ministry of Education and Research (BMBF) under Grant 16EMO0035, and in part by Deutsche Forschungsgemeinschaft (DFG) under Grant GRK 1856. (Corresponding author: Georges Engelmann.)

The authors are with the Institute for Power Electronics and Electrical Drives, RWTH Aachen University, 52066 Aachen, Germany (e-mail: post@isea.rwth-aachen.de).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TIA.2018.2796574

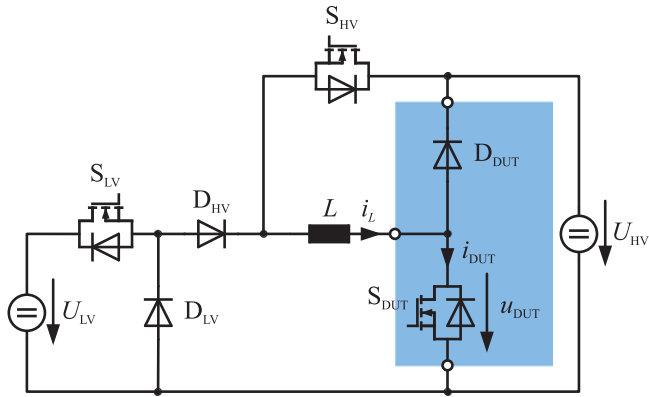


Fig. 1. Double pulse test bench topology.

uses the same hardware, although with an updated control algorithm to achieve improved heat-up and cool-down sequences. A good control algorithm is crucial to achieve short settling times without overshoot. The extracted switching losses of an *Infineon EconoDual FF600R12ME4C\_B11* insulated-gate bipolar transistor (IGBT) power module over a temperature range of  $\vartheta_j = -10\text{ }^\circ\text{C} \dots 125\text{ }^\circ\text{C}$ , dc-link voltage  $U_{DC} = 0\text{ V} \dots 800\text{ V}$  and an emitter current  $I_E = 0\text{ A} \dots 600\text{ A}$  is given as an application example. Further work using the presented hardware has already been published [10], [20].

## II. DOUBLE PULSE TEST BENCH

Fig. 1 depicts a simplified schematic of the modular double pulse test bench topology, which has also been presented in [8]. Contrary to the traditional double pulse test setups [21], [22], the generation of the test voltage and the test current are separated. Thus, the energy stored in capacitors can be significantly reduced and an independent adjustment of the test current and the test voltage for the DUT ( $S_{DUT}$  and  $D_{DUT}$ ) over the full current and voltage range of the test bench is possible without any modifications to the test setup. Particularly, the voltage source or capacitor bank  $U_{HV}$  does not need to be capable of supplying the energy required to establish the test current. The test voltage is provided by the voltage source  $U_{HV}$ , while the test current is generated by the low voltage source  $U_{LV}$ , the auxiliary switch  $S_{LV}$ , and the inductor  $L$ . Fig. 2 depicts the timing of the test procedure. First,  $S_{LV}$  and  $S_{DUT}$  are turned ON and the current in  $L$  increases to the required value during the interval denoted by  $t_1$ . For measurement of the turn-off losses,  $S_{DUT}$  is turned OFF (hard turn-off) after  $t_2$ , and the current commutates to  $D_{DUT}$ . After  $t_3$ , the auxiliary switch  $S_{HV}$  is turned ON to provide a freewheeling path for  $i_L$ . Before the turn-on switching loss measurement,  $S_{HV}$  is switched OFF after  $t_4$  and  $i_L$  flows through  $D_{DUT}$  again. When  $S_{DUT}$  is turned ON after  $t_5$ , the turn-on losses can be measured. Losses are measured by sampling the voltage  $u_{DUT}$  across  $S_{DUT}$  and the current  $i_{DUT}$ . The test bench that was used for the measurement presented in this paper can supply test currents of up to 1 kA and test voltages of up to 1 kV.

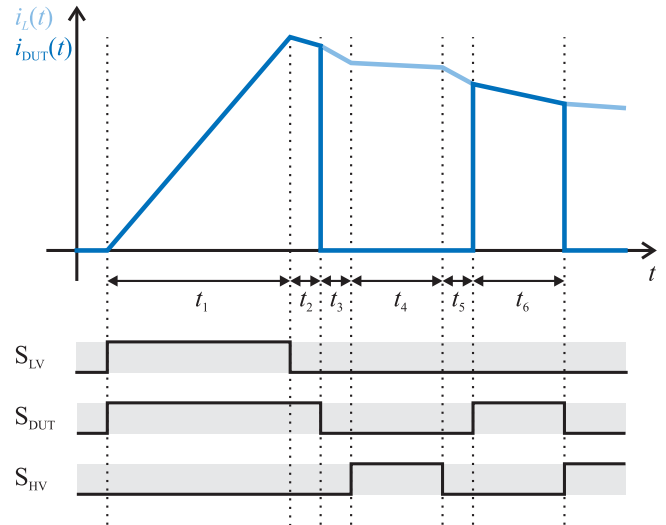


Fig. 2. Signal timing of the double pulse test.

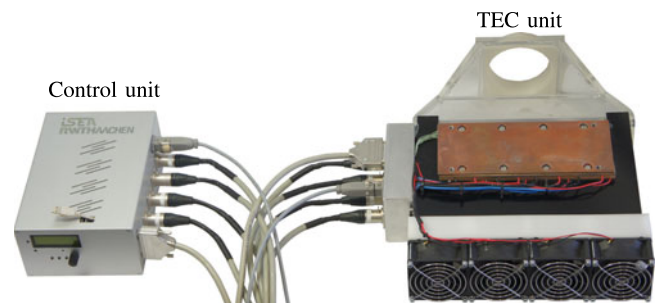


Fig. 3. Photograph of the control unit connected to the TEC unit.

## III. THERMAL CONTROL HARDWARE

A photograph of the temperature control system used to set the case and junction temperature of the power semiconductor, is shown in Fig. 3. The system consists of a control unit and the TEC unit. A modular concept is chosen so that the TEC unit can be exchanged easily to allow the use of different TEC units that are adapted to various power packages. The presented TEC unit is designed for power modules of the size of an Infineon HybridPACK 2.

The achievable temperature range of the presented TEC unit is  $-40\text{ }^\circ\text{C} \dots 200\text{ }^\circ\text{C}$ , which allows for characterization of devices for automotive traction applications as well as wide band gap devices that can exhibit junction temperatures of up to  $200\text{ }^\circ\text{C}$ . The following sections show the overall functionality of the different units. The detailed design is described in detail in [19].

### A. TEC Unit

In the thermal steady state, a certain thermal power is required as the DUT is not packed in an hermetically closed enclosure as physical accessibility is required (e.g., for wiring or measuring probes). As the heating power of the TEC is usually around one decade higher than the cooling power, the design is carried out for the minimum temperature of  $-40\text{ }^\circ\text{C}$ . The required thermal cooling power  $\dot{Q}_{cool}$  of the temperature unit including an

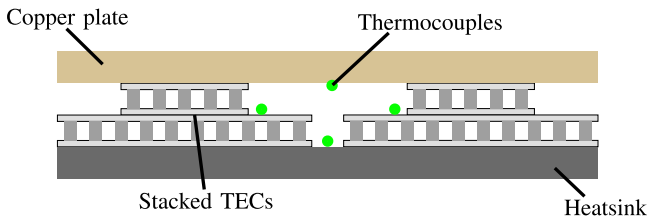


Fig. 4. Lateral cross section of the TEC stack [19].

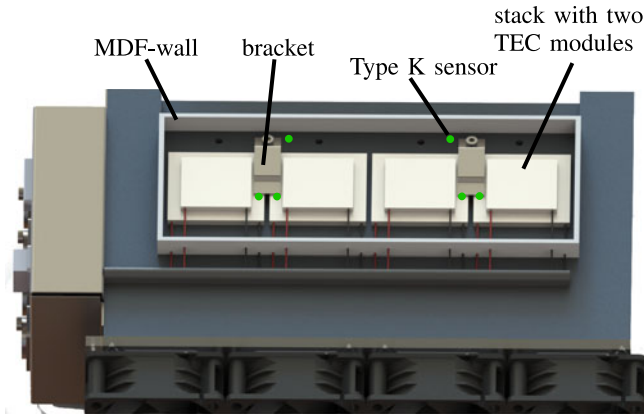


Fig. 5. Heat sink with four TEC stacks [19].

additional safety margin of 30% is determined experimentally to  $\dot{Q}_{cool} = 58.5 \text{ W}$  [19].

Taking into account the minimum temperature of  $-40 \text{ }^\circ\text{C}$  and a maximum heat sink temperature of about  $45 \text{ }^\circ\text{C}$ , a total temperature difference of  $\Delta\vartheta = 85 \text{ }^\circ\text{C}$  has to be created by the stack. The literature shows that when using a temperature difference of around 90 K, at least two modules in series should be used [23]. Using three stacked modules could result in a higher efficiency, however a drawback of thermally connecting several modules in series is the additional thermal resistance at the contacting surfaces. Therefore, two stacked TECs ( $n_s = 2$ ) are chosen to avoid a fourth thermal junction.

A lateral cross section of the heat sink and two stacked TECs is shown in Fig. 4. It shows the locations of the Type-K thermocouple sensors that are used for the temperature control. Each TEC requires individual control to achieve the maximum performance, which makes it necessary to measure the temperature in the middle of the TEC stack.

As the total geometric dimension is given by the base plate area of the HybridPACK 2 of around  $210 \text{ mm} \times 100 \text{ mm}$  and the TECs generally have a quadratic shape, a total of four stacks in parallel is used ( $n_p = 4$ ). A Computer-aided design drawing of the setup is shown in Fig. 5. The bottom TEC (*TEC1-24116T200*), which is connected to the heat sink, is rated for a maximum hot-side temperature of  $180 \text{ }^\circ\text{C}$ , while the hot-side of the upper module (*QC-127-1.4-8.5MD*) is rated for a temperature up to  $200 \text{ }^\circ\text{C}$ . Considering the given efficiencies of the TEC, a total loss power of  $\dot{Q}_{stack} = 188 \text{ W}$  is generated by each stack.

A heat sink (*SK-441-200-SA*) with a thermal resistance of  $R_{th,ha} = 0.032 \text{ K/W}$  using a forced air cooling speed of

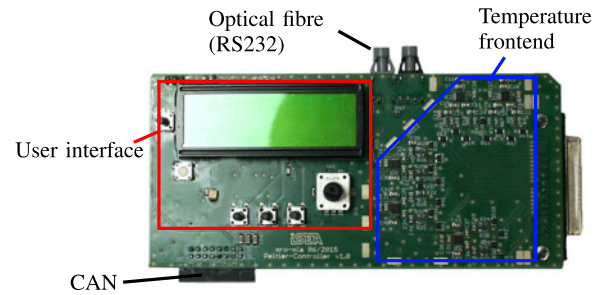


Fig. 6. Main control board [19].

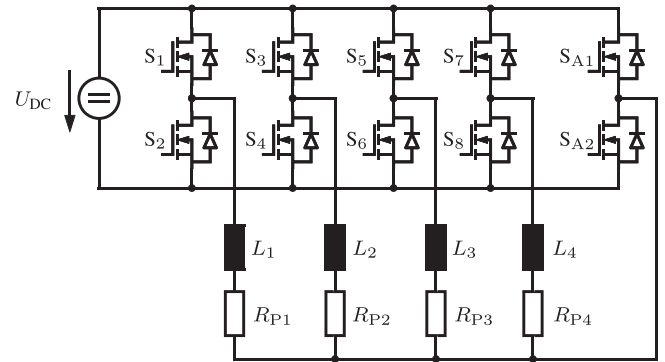


Fig. 7. DC-DC converter topology [19].

$v = 5 \text{ m/s}$  is chosen. This limits the maximum temperature increase of the heat sink with respect to 24 K to the ambient temperature.

### B. Control Unit

The control unit consists of a main control board and four dc-dc converter boards to individually control up to eight TECs. The TECs are powered using an external power supply  $U_{supply} = 30 \text{ V}$  with a current rating of  $I_{supply} = 35 \text{ A}$ .

The main control board is shown in Fig. 6. It includes the user interface, a controller area network (CAN) bus interface as well as the temperature front end. The user interface, which consists of a liquid crystal display (LCD) and several buttons, allows manual as well as remote configuration of the system. Remote controllability is enabled via a RS232 serial communication over fiber lines. This board acts as a master device on the CAN bus to control the remaining dc-dc converter boards. The analog front end implemented on this board consists of a ten channel Type-K thermocouple measurement circuit. To ensure accurate temperature measurements, a dedicated analog-to-digital converter *ADS1118*, which is optimized for K-type temperature measurements, is used. Although the *ADS1118* has an integrated temperature sensor for cold-junction compensation, an auxiliary cold junction compensation is required in this setup as the Type-K thermocouples are connected to copper wires at the TEC unit, which is at a different temperature than the *ADS1118*. A dedicated digital temperature sensor *DS18B20* is placed inside the connector that connects to the TEC unit.

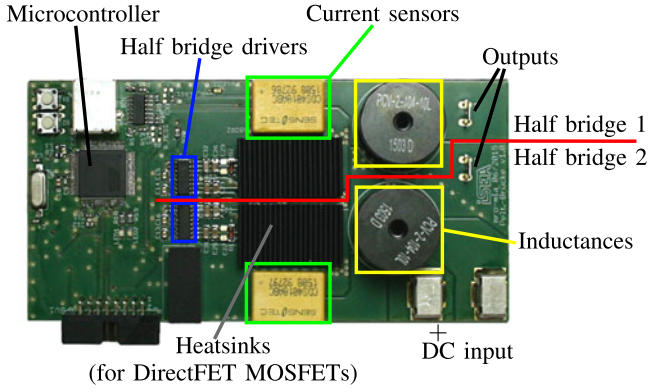


Fig. 8. PCB of the dc-dc converter [19].

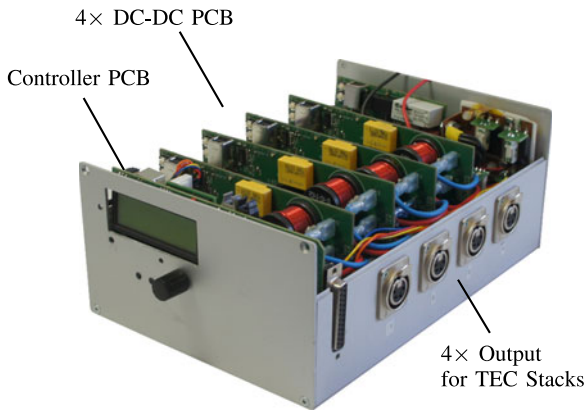


Fig. 9. Photograph of the control unit.

The TECs are powered using a buck converter topology as shown in Fig. 7. The switches  $S_1$ – $S_8$  are operated with a switching frequency  $f_{sw} = 200$  kHz, whereas the switches  $S_{A1}$  and  $S_{A2}$  have a constant state depending on the operation mode, i.e., heating or cooling. The smoothing inductances  $L_1$ – $L_4$  are mounted on the printed circuit board (PCB), the resistors  $R_{P1}$ – $R_{P4}$  represent the TECs. As there are eight TECs that have to be powered, the shown topology is implemented twice. The metal–oxide–semiconductor field-effect transistors  $S_1$ – $S_8$  are mounted on the PCB with a heat sink directly attached to their case using the double-sided gluing thermal interface material *Bond-Ply 100* [24]. One of these boards is shown in Fig. 8. Two half bridges are implemented on each PCB, which results in a total of four dc-dc converter PCB. A current sensor *Sensitec CDS4010* is installed for each half bridge. Each dc-dc converter PCB features a microcontroller that fulfills three main functions: generation of pulsewidth modulation signals for the switches, control of the output current, and communication to the main control board via a CAN bus. The static switches  $S_{A1}$  and  $S_{A2}$  are mounted directly on copper sheets to allow higher current and cooling capability. The control unit is shown in Fig. 9.

#### IV. CONTROL

An improved temperature control, compared to the previously implemented control in [19], is presented. For a fast control and

high stability, state-space decoupling based on [25] is used for the temperature controller. The current controller consists of a proportional-integral-differential controller [19]. The improved controller structure is shown in Fig. 10.

A precise model of the plant is of major importance for a precise control. Beneath the TEC, the thermal capacitance  $C_{th}$  of the copper base plate including the HybridPACK 2 and thermal resistances to ambient and heat sink are considered as the determining values of the plant.

The inner part of the temperature controller consists of a conventional proportional-integral (PI) controller that controls the thermal power (positive for heating, negative for cooling) of the thermoelectric elements, and thus, the temperature of the copper plate. To ensure that no wind-up will occur in the integrator, a trajectory filter is used to limit the input value to the PI controller.

The trajectory filter consists of a virtual model that represents the plant with its thermal capacitance and the resistances. As these values cannot be measured directly, estimated values for  $\hat{C}_{th}$ ,  $\hat{R}_{th,amb}$ , and  $\hat{R}_{th,hs}$  are used. In a first step, the difference between the temperature of the virtual model and the desired set point is scaled with  $K_p$  to get a value for the thermal power. As the TEC can only provide a certain maximum thermal power, the desired power has to be limited to the maximum possible value. Given the temperature difference  $\Delta\vartheta$  across the TEC and the cold-side temperature  $T_c$ , the maximum power can be calculated according to [26], with the maximum achievable cooling power  $\dot{Q}_c$ , the Seebeck coefficient  $S$ , the inner thermal resistance  $R_{th}$  of the TEC and the electrical resistance  $R$  as

$$\dot{Q}_c = S \cdot I \cdot T_c - R_{th}\Delta\vartheta - \frac{1}{2}I^2R. \quad (1)$$

The temperature  $\vartheta^*$  of the virtual model is obtained by integrating the thermal power and scaling the result with  $\hat{C}_{th}$ . This value is subsequently used as the set point for the PI controller. To increase the speed of the controller, a feed-forward of the thermal power to the input of the modulator is used to bypass the PI controller. Furthermore, the power required during the steady state to compensate for the losses to the ambient or to the heat sink are also fed directly into the modulator. The required power is calculated using the measured temperatures  $\vartheta_{Ambient}$ ,  $\vartheta_{Heat-sink}$ , and  $\vartheta_{Module}$  and estimations of the thermal resistance  $\hat{R}_{th,hs}$  between module and heat sink and  $\hat{R}_{th,amb}$  between module and ambient.

#### A. Modulator

As the TECs are controlled using a current signal, a modulator is used to calculate the current for each TEC based on the set point of the thermal power and the current temperature difference  $\Delta\vartheta$ . The total thermal power  $\dot{Q}_{tot}$  is equally distributed to each of the four stacks of the TEC

$$\dot{Q}_{stack} = \frac{\dot{Q}_{tot}}{4}.$$

The power for the upper TEC in the stack is equal to  $\dot{Q}_{stack}$ . The respective current  $I_{upper}$  can be calculated by solving (1) for  $I$

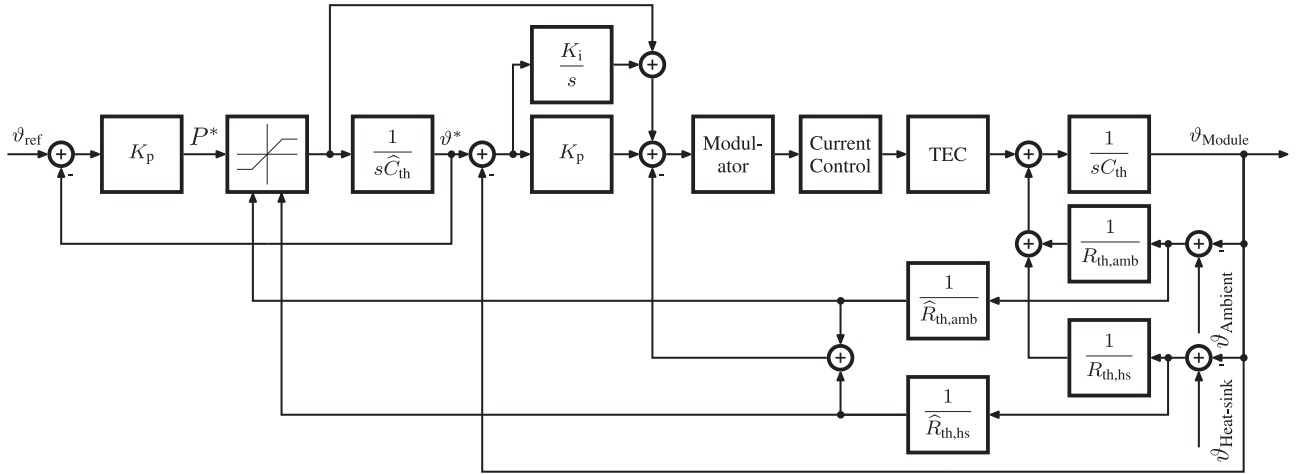


Fig. 10. Developed control structure of a single stack of two TECs.

as follows:

$$I = \frac{S}{R} \cdot T_c \pm \sqrt{\left(\frac{S}{R} \cdot T_c\right)^2 - \frac{2}{R} \cdot (R_{th}\Delta\vartheta + \dot{Q}_c)}. \quad (2)$$

The lower TEC does not only have to be able to transfer the thermal power  $\dot{Q}_{stack}$  at the upper side of the stack but also the additional ohmic losses  $P = I_{upper}^2 \cdot R_{upper}$  of the upper TEC. Given the total thermal power  $\dot{Q}_{lower} = \dot{Q}_{stack} + I_{upper}^2 \cdot R_{upper}$  of the lower TEC, its current  $I_{lower}$  can be calculated according to (2).

Due to the relation of current, thermal power, and temperature difference across a TEC given by (1), a positive feedback of, e.g., temperature difference and current exists. In practice, small errors in the current or temperature measurement as well as a nonuniform thermal power distribution will lead to small deviations of the temperature difference across each TEC. Due to the positive feedback of the modulator, this error is further increased. To counteract this behavior, a negative current feedback  $I_{feedback}$  is applied to the current set point of the TEC as

$$I_{feedback} = (\Delta\vartheta_{lower} - \Delta\vartheta_{upper}) \cdot K_{p,feedback}. \quad (3)$$

To achieve a good efficiency, the temperature  $\vartheta_{Midpoint}$  at the midpoint of the stack should be at around half of the total temperature difference across the whole stack.

## V. MEASUREMENT RESULTS

The correct operation of the implemented control structure is verified on conducting a heat-up and a cool-down process at an ambient temperature  $\vartheta_{Ambient} \approx 30^\circ\text{C}$ . The temperature values measured at the sensors are plotted in Figs. 11 and 12.

The measurement shows that the midpoints of the TECs are at slightly different temperatures. As the controller assumes the same thermal load for all four stacks, differences in thermal load, or production variations of the modules will lead to deviations in the midpoint temperatures.

The copper plate on which the DUT is mounted is isolated using polystyrene to increase resistance between copper plate and ambient. When a DUT is placed on the copper surface,

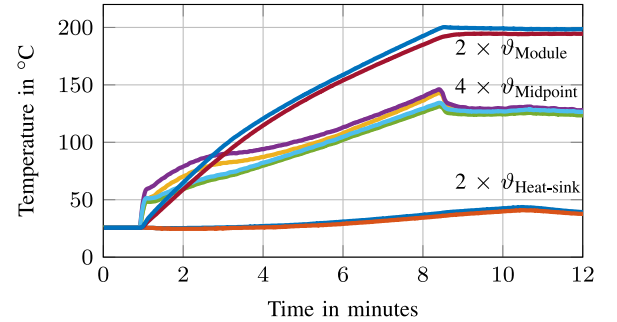


Fig. 11. Measured temperatures during a heat-up process.

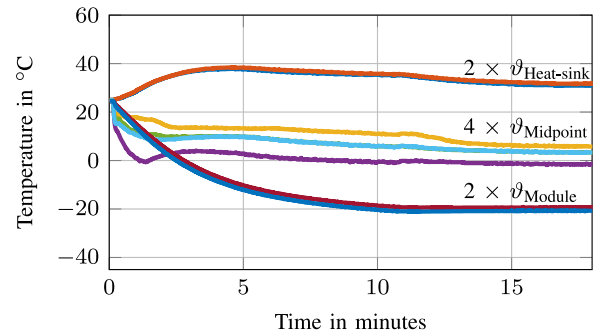


Fig. 12. Measured temperatures during a cool-down process.

the thermal isolation cannot be totally guaranteed as the power semiconductor needs various wiring and measuring probes to be connected. This includes the gate driver, power cables, current, and voltage measurements. Consequently, when a DUT is installed, more cooling power will be required to compensate for the additional power device to ambient thermal power flow.

## VI. ANALYSIS TOOL

Due to multiple parameters and high resolutions, the amount of a complete double pulse measurement for one DUT easily tends toward a few thousand recorded waveforms. Because such a high number of measured waveforms cannot be evaluated

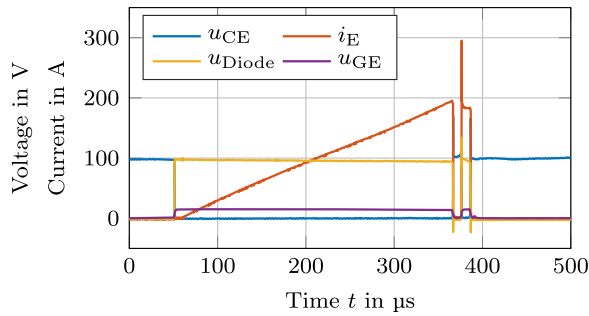


Fig. 13. Exemplary waveforms of a double pulse measurement.

manually, a MATLAB tool for automated evaluation has been developed. An overview of the individual operating steps is given in the following.

#### A. Waveform Consistency

At first, each double pulse measurement waveform is checked for erroneous measurements to provide the following stages with good measurements only. This mainly consists in checking if no measurement clipped due to higher peak voltages or currents than the measurement tool or the scope channel is specified for. This is mainly required for the reverse-recovery peak current, which, depending on the device used, can be several times higher than the nominal current.

#### B. Switching Events Detection

After basic validity checks are accomplished, the switching events are localized. A peak detection algorithm on the power losses  $p = u_{CE} \cdot i_E$  is carried out. An exemplary double pulse test waveform is shown in Fig. 13.

#### C. Switching Energy Calculation

Several algorithms on switching loss calculation are available and can be selected by the user. A first algorithm applies the switching loss definition according to the standard *IEC-60747*. A second possibility is to use the 5% borders of the peak power of a switching instant as shown in [20, Sec. II].

#### D. Post Analysis

After the extraction of the switching losses is completed, each measurement point can be analyzed individually to verify correct operation of the algorithm. The switching waveforms for the turn-on and the turn-off event are plotted by selecting a single result as exemplarily shown in Fig. 15.

#### E. Saving of the Results

The final results are stored in a MATLAB *.mat* file. Information about the nominal and the actual set points is included as well as a PLECS-compatible data field for the switching losses.

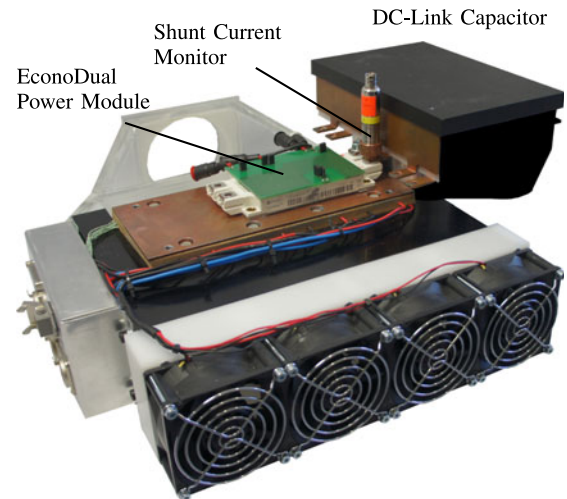


Fig. 14. Photograph of the power module mounted on the TEC unit.

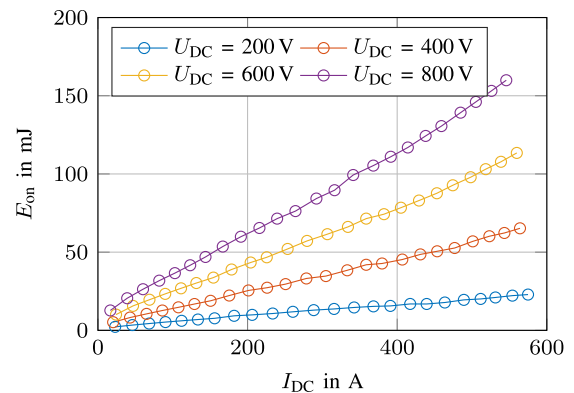


Fig. 15. Turn-on losses  $E_{on}$  at  $\vartheta_j = 80^\circ\text{C}$ .

## VII. APPLICATION EXAMPLE

An application example for the presented characterization methodology is shown for an Infineon EconoDual IGBT power module (*FF600R12ME4C\_B11*). The given power module is rated for a collector–emitter voltage  $U_{CE} = 1200\text{ V}$  and a nominal current  $I_C = 600\text{ A}$ . A turn-on gate resistance  $R_{g,on} = 1.5\ \Omega$  and a turn-off gate resistance  $R_{g,off} = 2.5\ \Omega$  are chosen. A *Power Integrations* gate driver *2SC0435T* with the respective turn-on and turn-off gate voltages  $U_{CC,on} = 15\text{ V}$  and  $U_{CC,off} = -10\text{ V}$  is used. A photograph of the power module mounted on the temperature control system is shown in Fig. 14.

Using the temperature control system in combination with the double pulse test bench introduced in Section II, the switching losses of the power module can be measured depending on the junction temperature. The measurement ranges with the corresponding step sizes are shown in Table I. A minimum temperature of  $\vartheta_j = -10^\circ\text{C}$  could be achieved. A further reduction of the temperature could not be achieved using this setup, because it was not possible to thermally isolate the DUT sufficiently from the ambient. A total thermal isolation is hardly possible as voltage and current sensing probes needs to be connected and placed close to the DUT. A total of  $8 \times 24 \times 10 = 1920$

TABLE I  
MEASUREMENT RANGES

Quantity	Range	Step	Measurements
$U_{DC}$	0 V... 800 V	100 V	8
$I_{DC}$	0 A... 600 A	25 A	24
$\vartheta_j$	-10 °C... 125 °C	15 °C	10

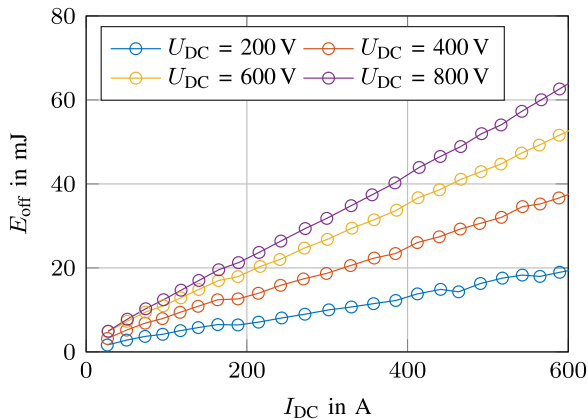


Fig. 16. Turn-off losses  $E_{off}$  at  $\vartheta_j = 80$  °C.

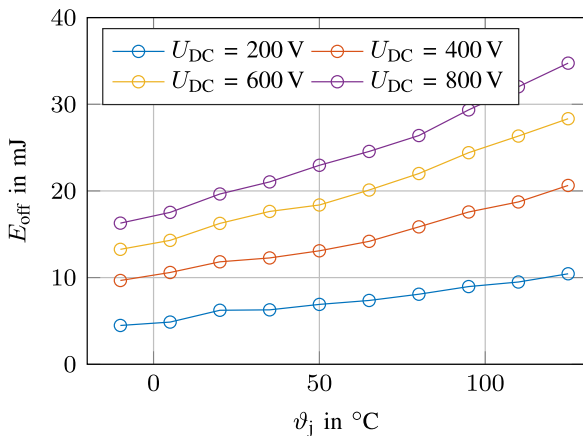


Fig. 17. Turn-off losses  $E_{off}$  over temperature at  $I_{DC} = 250$  A.

measurements have to be conducted. Knowing that the test bench achieves around 90 measurements per hour, a total time of 48 h is required to conduct all measurements.

The resulting switching losses for a junction temperature  $\vartheta_j = -10$  °C are plotted in Figs. 15 and 16. It is possible to create various plots to show temperature-dependent parameters, such as the switching losses as shown in Fig. 17.

## VIII. CONCLUSION

A modular temperature control system employing TECs that can be used in combination with a double pulse test bench has been presented. Automated sweeping through voltage, current, and temperature is possible by the given test setup. Besides the detailed hardware description of the TEC unit, a refined control

structure is presented and implemented. A heat-up process to the maximum temperature of 200 °C and a cool-down process to a temperature of -20 °C is shown. A minimum temperature of -10 °C could be reached for tests with a HybridPACK 2 IGBT module.

In combination with the automated double pulse test bench, an exemplary characterization of an Infineon EconoDual power module has been conducted and the temperature-dependent results have been shown.

## REFERENCES

- [1] H. van Hoek, M. Boesing, D. van Treek, T. Schoenen, and R. W. De Doncker, "Power electronic architectures for electric vehicles," in *Proc. Emobility—Elect. Power Train*, Nov. 2010, pp. 1–6.
- [2] R. W. De Doncker, C. Meyer, R. U. Lenke, and F. Mura, "Power electronics for future utility applications," in *Proc. Int. Conf. Power Electron. Drive Syst.*, Nov. 2007, pp. 1–8.
- [3] C. Neeb, L. Boettcher, M. Conrad, and R. W. De Doncker, "Innovative and reliable power modules: A future trend and evolution of technologies," *IEEE Ind. Electron. Mag.*, vol. 8, no. 3, pp. 6–16, Sep. 2014.
- [4] G. Engelmann, M. Kowal, and R. W. De Doncker, "A highly integrated drive inverter using directFETs and ceramic dc-link capacitors for open-end winding machines in electric vehicles," in *Proc. Appl. Power Electron. Conf. Expo.*, Mar. 2015, pp. 290–296.
- [5] K. Rigbers, S. Schroder, T. Durbaum, M. Wendt, and R. W. De Doncker, "Integrated method for optimization of power electronic circuits," in *Proc. Annu. Power Electron. Spec. Conf.*, vol. 6, Jun. 2004, pp. 4473–4478.
- [6] C. H. van der Broeck, L. A. Ruppert, A. Hinz, M. Conrad, and R. W. De Doncker, "Spatial electro-thermal modeling and simulation of power electronic modules," *IEEE Trans. Ind. Appl.*, vol. 54, no. 01, pp. 404–415, Jan./Feb. 2018.
- [7] J. Gottschlich and R. W. De Doncker, "A programmable gate driver for power semiconductor switching loss characterization," in *Proc. Int. Conf. Power Electron. Drive Syst.*, Jun. 2015, pp. 456–461.
- [8] J. Gottschlich, M. Kaymak, M. Christoph, and R. De Doncker, "A flexible test bench for power semiconductor switching loss measurements," in *Proc. Int. Conf. Power Electron. Drive Syst.*, Jun. 2015, pp. 442–448.
- [9] J. Lutz, *Halbleiter-Leistungsbaulemente: Physik, Eigenschaften, Zuverlässigkeit (German Edition)*. Berlin, Germany: Springer-Verlag, 2006.
- [10] C. van der Broeck, A. Gospodinov, and R. W. De Doncker, "IGBT junction temperature estimation via gate voltage plateau sensing," in *Proc. Energy Convers. Congr. Expo.*, 2017, pp. 5899–5906.
- [11] G. Festa and B. Neri, "Thermally regulated low-noise, wideband, I/V converter, using peltier heat pumps," *IEEE Trans. Instrum. Meas.*, vol. 43, no. 6, pp. 900–905, Dec. 1994.
- [12] S. Fernandez, A. Murk, and N. Kämpfer, "Design and characterization of a Peltier-cold calibration target for a 110-GHz radiometer," *IEEE Trans. Geosci. Remote Sens.*, vol. 53, no. 1, pp. 344–351, Jan. 2015.
- [13] S. Hava, R. Hunsperger, and H. Sequeira, "Monolithically Peltier-cooled laser diodes," *J. Lightw. Technol.*, vol. 2, no. 2, pp. 175–180, Apr. 1984.
- [14] T. Yamaguchi, H. Okumura, K. Nakamura, and S. Yamaguchi, "Multi-stage peltier current lead system for liquid helium free magnets," *IEEE Trans. Appl. Supercond.*, vol. 13, no. 2, pp. 1914–1917, Jun. 2003.
- [15] D. D. L. Wijngaards and R. F. Wolffenbuttel, "Study on temperature stability improvement of on-chip reference elements using integrated peltier coolers," *IEEE Trans. Instrum. Meas.*, vol. 52, no. 2, pp. 478–482, Apr. 2003.
- [16] D. F. Frost and D. A. Howey, "High-speed peltier calorimeter for the calibration of high-bandwidth power measurement equipment," *IEEE Trans. Instrum. Meas.*, vol. 65, no. 1, pp. 155–163, Jan. 2016.
- [17] Y. Zhang and T. M. Jahns, "Power electronics loss measurement using new heat flux sensor based on thermoelectric device with active control," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 4098–4106, Nov. 2014.
- [18] W. C. White, "Some experiments with Peltier effect," *Elect. Eng.*, vol. 70, no. 7, pp. 589–591, Jul. 1951.
- [19] G. Engelmann, M. Laumen, K. Oberdieck, and R. W. De Doncker, "Peltier module based temperature control system for power semiconductor characterization," in *Proc. Int. Power Electron. Motion Control Conf.*, Sep. 2016, pp. 957–962.

- [20] G. Engelmann *et al.*, “Experimental analysis of the switching behavior of an IGBT using a three-stage gate driver,” in *Proc. Int. Symp. Power Electron. Distrib. Gener. Syst.*, Apr. 2017, pp. 1–8.
- [21] Y. Shen, Y. Xiong, J. Jiang, Y. Deng, X. He, and Z. Zeng, “Switching loss analysis and modeling of power semiconductor devices base on an automatic measurement system,” in *Proc. Int. Symp. Ind. Electron.*, vol. 2, Jul. 2006, pp. 853–858.
- [22] V. Kumar, S. Reddy, and G. Narayanan, “Measurement of IGBT switching characteristics and loss using coaxial current transformer,” in *Proc. India Int. Conf. Power Electron.*, Dec. 2012, pp. 1–6.
- [23] H. J. Goldsmid, *Thermoelectric Refrigeration* (International Cryogenics Monograph Series). London, U.K.: Heywood, 1964.
- [24] G. Engelmann, T. Senoner, H. van Hoek, and R. W. De Doncker, “A systematic comparison of various thermal interface materials for applications with surface-mounted DirectFET MOSFETs,” in *Proc. Int. Conf. Power Electron. Drive Syst.*, Jun. 2015, pp. 112–117.
- [25] C. H. van der Broeck, R. W. De Doncker, S. A. Richter, and J. von Bloh, “Discrete time modeling, implementation and design of current controllers,” in *Proc. Proc. Energy Convers. Congr. Expo.*, Sep. 2014, pp. 540–547.
- [26] S. Lineykin and S. Ben-Yaakov, “Modeling and analysis of thermoelectric modules,” *IEEE Trans. Ind. Appl.*, vol. 43, no. 2, pp. 505–512, Mar. 2007.



**Georges Engelmann** was born in Wiltz, Luxembourg, in 1987. He received the diploma in electrical engineering from RWTH Aachen University, Aachen, Germany, in 2012.

Since 2013, he has been a Research Associate with the Institute for Power Electronics and Electrical Drives, RWTH Aachen University. His research interests include the field of power semiconductor switching characterization, as well as active gate drivers for wide-bandgap devices.



**Michael Laumen** was born in Heinsberg, Germany, in 1990. He received the M.Sc. degree in electrical engineering from RWTH Aachen University, Aachen, Germany, in 2015.

Since 2016, he has been a Research Associate with the Institute for Power Electronics and Electrical Drives, RWTH Aachen University. His research interests include the field of high-temperature gate drivers and measurement electronics, as well as converters for automotive applications.



**Jan Gottschlich** was born in Herford, Germany, in 1984. He received the diploma in electrical engineering from RWTH Aachen University, Aachen, Germany, in 2010.

Since 2011, he has been a Research Associate with the Institute for Power Electronics and Electrical Drives, RWTH Aachen University. His research interest includes measurement systems for power electronic applications and converter topologies for specialized applications.

Mr. Gottschlich is a member of the VDE Association for Electrical, Electronic, and Information Technologies.



**Karl Oberdieck** received the M.Sc. degree in electrical engineering from RWTH Aachen University, Aachen, Germany, in 2013.

Since 2014, he has been a Research Associate with the Institute for Power Electronics and Electrical Drives, RWTH Aachen University. His research interests include design and high-frequency modeling of converters, design of gate drivers for insulated gate bipolar transistors, as well as the development of high-frequency instruments for measurements of electromagnetic emissions for power electronic systems.

Mr. Oberdieck is a member of the VDE Association for Electrical, Electronic, and Information Technologies.



**Rik W. De Doncker** received the Ph.D. degree in electrical engineering from Katholieke Universiteit Leuven, Leuven, Belgium, in 1986.

In 1987, he joined the University of Wisconsin, Madison, WI, USA, as a Visiting Associate Professor. After a short stay as an Adjunct Researcher at the Interuniversity Microelectronics Centre, Leuven, he joined in 1989, the Corporate Research and Development Center, General Electric Company, Schenectady, NY, USA. In 1994, he joined Silicon Power Corporation, Malvern, PA, USA, a former division of General Electric Inc., as the Vice President of Technology. In 1996, he became a Professor with RWTH Aachen University, Aachen, Germany, where he currently leads the Institute for Power Electronics and Electrical Drives.

Since 2006, he has been the Director of the E.ON Energy Research Center, RWTH Aachen University.

Dr. De Doncker was the President of the IEEE Power Electronics Society (PELS) in 2005 and 2006. He was the founding Chairman of the German IEEE Industry Applications Society PELS Joint Chapter. In 2002, he received the IEEE Industry Applications Society Outstanding Achievement Award. In 2008, he received the IEEE Power and Energy Society Nari Hingorani Custom Power Award. In 2009, he led a Verband der Elektrotechnik, Elektronik, und Informationstechnik/Energietechnische Gesellschaft Task Force on electric vehicles. In 2010, he received an honorary doctor degree from TU Riga, Riga, Latvia. In 2013, he received the IEEE William E. Newell Power Electronics Award.