Optimized 9-Level Switched-Capacitor Inverter for Grid-Connected Photovoltaic Systems

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***Abstract*—This paper introduces a novel switched-capacitor-based 9-level inverter topology to meet IEEE standards for low total harmonic distortion (THD) in grid-connected inverters. The new design addresses the trade-off between increasing output voltage levels to reduce harmonics and the consequent rise in device count. The proposed topology is streamlined, consisting of 12 switches, 3 capacitors, 2 diodes, and a single DC source. Comparative analysis with similar topologies confirms the advantages of the new design. The experimental results show that the proposed inverter achieves a THD of 13.58% in its output voltage. The topology is validated through its application in a single-stage, three-phase photovoltaic system connected to the grid. Simulations are conducted using MATLAB/Simulink to test the system's performance. Furthermore, hardware-in-the-loop experiments are performed using OPAL-RT 5700 real-time simulators to further substantiate the efficacy of the proposed topology.**

***Index Terms*—Grid-Connected Inverters, Multilevel Inverters, Photovoltaic Systems, Switched-Capacitor, Total Harmonic Distortion.**

I. Introduction

Solar photovoltaic (PV) energy has become a viable alternative to conventional energy sources today. Power converters play an important role in the transformation of solar energy into electric energy [1], [2]. Among these, multilevel inverters (MLIs) are particularly favored for their superior output waveform quality, reduced total harmonic distortion (THD), minimal filtering needs, and lower voltage stress, among other advantages. This allows the use of devices of lower rating, thus reducing both the cost and size of MLIs [3]–[5]. MLIs are generally classified into neutral-point-clamp (NPC), flying-capacitor (FC), and cascade H-bridge (CHB) types. For MLIs connected to the grid, it is essential that the THD of the output voltage is in accordance with existing IEEE standards. To achieve this, an increase in voltage levels is often required, leading to a corresponding increase in the number of switches and devices. However, this increase in device count adds operational complexity, cost, and losses, particularly when higher voltage levels are targeted [6], [7].

To mitigate the challenges associated with traditional MLIs, the literature features various topologies designed to minimize the number of devices. Transformerless inverters (TI) have gained popularity in PV systems for their cost-effectiveness and compact size. However, they lack galvanic isolation and struggle with leakage current restriction, particularly in HERIC and H-6 configurations, due to switch-junction capacitance [8]. Moreover, these topologies are often bulky and expensive, necessitating the use of dual inductors for filtering and resulting in elevated conduction losses. In the case of NPC and FC topologies, a significant challenge lies in maintaining voltage balance across capacitors. The design process for these topologies is inherently cumbersome, and their output voltage levels are generally limited to five. Expanding beyond this five-level configuration for NPC and FC topologies introduces complexity due to increased device count [9]. CHB-MLIs typically employ multiple isolated DC sources to achieve elevated voltage levels [10], [11]. In PV systems, this often involves the use of several PV arrays, which introduces problems such as partial shading, array mismatches, and synchronization difficulties in Maximum Power Point Tracking (MPPT) algorithms. As a result, MLIs operating on a single DC source are generally preferred for PV applications [12], [13].

Switched-Capacitor Multilevel Inverters (SCMLIs) have shown promise for photovoltaic applications because of their ability to produce higher voltage levels while using minimal switch count and a single isolated DC source. In SCMLIs, capacitors are connected either in series or parallel during charging and discharging modes, and are specifically arranged in series during the discharging phase to achieve higher output voltage levels. Despite these advantages, SC-based Transformerless Inverters (TIs) designed for five-level output still suffer from high levels of harmonics in their output voltage [14]. As a result, these inverters require high-volume filters to effectively attenuate the harmonics. Further research into SC-based 7-level inverter topologies reveals challenges such as high voltage stress across switches [15], [16]. Additionally, some of these 7-level topologies have issues related to capacitor balancing [17]. In the context of PV-grid integration, a specific 7-level topology has been introduced that minimizes the number of switches and reduces the voltage stress [18]. Despite this, this design produces a THD of 16.66 % in its output voltage, making it necessary to employ larger filters to meet the IEEE 519-2022 standards for the 8 % THD below 1 kV bus voltage at PCC.

To achieve a balance between minimizing switch count and reducing the THD in the output voltage, a number of 9-level (9L) inverters have been explored in the literature. Various inverter topologies designed to produce the 9L output voltage are discussed in [19]–[22]. However, these designs subject the switches to high voltage stress. Conventional methods to create a 9L inverter, such as using cascade H-bridge units, require a minimum of four units with 12 switches and four isolated DC sources, making the system costly, bulky, and complex [23]. In PV applications, the use of multiple isolated

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DC sources introduces complications such as partial shading and mismatch of PV modules. Alternative 9L topologies that utilize 13 and 12 switches are presented in [24], [25]. These designs, although effective, increase the overall cost due to the high number of switches. In [26], a packed e-cell topology is proposed for 9L output, but it also relies on two isolated DC sources. Similarly, a t-type packed u-cell topology is described in [27], which also employs two isolated DC sources. Further developments in 9L inverters that focus on the use of a larger number of switches and DC sources are presented in [10], [28], [29]. This contrasts with the existing 13-level inverter design, which features 1.5 times voltage boosting and is based on two K-type units and 14 switches, including clamping transistors [30]. The primary objectives of this manuscript are as follows.

- To design a new 9L topology with reduced device count while achieving self-balanced capacitor voltage.
- To strike a balance between the output voltage %THD and the device count, addressing a current research gap.
- To implement a three-phase, single-stage solar PV system using the proposed 9L topology and integrate it with the grid.

Compared to the conference version [1], which proposed a 9L inverter using optimal devices, the manuscript further elaborates on and advances the work by:

- A pre-existing 7-level MLI [18] was successfully extended to a 9-level topology with reduced THD, utilizing only twelve switches and a single DC input source.
- A novel switching table was developed, achieving not only a 9-level output voltage, but also ensuring self-balanced floating capacitor voltages, thus enhancing the system's robustness and efficiency.
- The newly developed 9-level MLI topology was effectively implemented in a single-stage, three-phase solar PV system, demonstrating its real-world applicability and relevance to current energy demands.

By achieving these additional objectives and contributions, the manuscript provides a more comprehensive and in-depth study, distinguishing itself from the conference version. The construction and working principle of the proposed 9L-SCMLI topology are described in Section II. The theoretical analysis with PV-grid integration using the proposed 9L-SCMLI topology is also presented in Section II. The results and discussion are explained in Section III. Finally, the conclusion is drawn in Section IV.

II. Proposed 9L-SCMLI Inverter

A. Topology Description

The topology of the proposed 9L-SCMLI inverter is shown in Fig. 1. It is a single-phase configuration. It comprises nine active IGBT switches ($S_1, S_2, \ldots S_9$), two DC-link capacitors (C_1, C_2) and two floating capacitors (C_3, C_4). Switches S_7, S_8, and S_9 are bidirectional, and the remaining switches are unidirectional. Switches S_3 and S_4 are reverse blocking IGBTs. A half-bridge made of S_1 and S_2 is connected to the output side of the inverter. The midpoint of two floating capacitors (C_3 and C_4) and the other midpoint between the switches S_1 and S_2 are joined through a bidirectional switch S_9. The midpoint of two DC-link capacitors C_1 and C_2 is connected to one end of the bidirectional switches S_7 and S_8. The proposed inverter is fed from a single DC source with

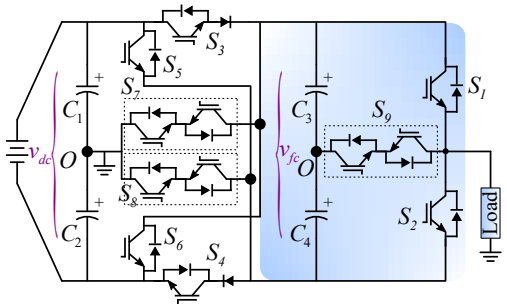


Fig. 1. $1-\varphi$ circuit structure for the proposed 9L-SCMLI.

TABLE I
Switching States of the Proposed 9L-SCMLI

Operating State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	v_o	V_{C3}	V_{C4}
1	0	1	1	0	0	0	0	1	0	0	c	c
2	0	0	1	0	0	0	0	1	1	$0.25x$	c	c
3	1	0	1	0	0	0	0	1	0	$0.5x$	c	c
4	0	0	0	0	1	0	0	0	1	$0.75x$	0	d
5	1	0	0	0	1	0	0	0	0	x	d	d
6	1	0	0	1	0	0	1	0	0	0	c	c
7	0	0	0	1	0	0	1	0	1	$-0.25x$	c	c
8	0	1	0	1	0	0	1	0	0	$-0.5x$	c	c
9	0	0	0	0	0	1	0	0	1	$-0.75x$	d	0
10	0	1	0	0	0	1	0	0	0	$-x$	d	d

Note: $x = V_{dc}$, c= charging ; d= discharging.

DC-link voltage V_{dc}. The magnitude of the input DC voltage is equally divided between C_1 and C_2. Therefore, the voltage across each of them is equal to (V_{dc}/2). Each floating capacitor C_3 and C_4 is charged to a voltage magnitude of V_{dc}/2. A load is applied to the output terminal. All switching states to generate the desired voltage levels are listed in Table I.

B. Operating Principle

Operating State-1 ($v_0 = 0$): During state 1, switch S_2, S_3, and S_8 are enabled. The positive load current flows through the path C_1-S_3-C_3-C_4-S_2-C_1 as indicated by the red line as shown in Fig. 2(a). The series connected DC-link capacitors C_1 and C_2 are charged to V_{dc}, so the voltage across each of them becomes equal to $V_{dc}/2$ and remains constant regardless of operating states. The strings of floating capacitors C_3 and C_4 are charged to V_{dc}/2 through a switch S_3 and S_8 as indicated by a blue dotted line. So, the voltage in both C_3 and C_4 becomes equal to $V_{dc}/4$. The charges of C_3 and C_4 are evenly distributed throughout the cycle, as shown in Table I. Hence, the voltage across them also remains constant during operation of the proposed 9L-SCMLI. The term v_o^1 denotes the output voltage corresponding to operating state 1. The voltage across C_1, C_2, C_3, C_4 (i.e., $\{V_{C1}, V_{C2}, V_{C3}, V_{C4}\}$, respectively), and v_o^1 can be mathematically represented as

$$\begin{cases} V_{C1} = V_{C2} = V_{dc}/2; \quad V_{C3} = V_{C4} = V_{dc}/4 \\ v_o^1 = V_{C1} - V_{C3} - V_{C4} = 0 \end{cases} \tag{1}$$

Operating State-2 ($v_o = 0.25V_{dc}$): During this state, switch S_3, S_8, and S_9 are ON. The positive load current flows through the path C_1-S_3-C_3- S_9-C_1 as indicated by the red line as shown in Fig. 2(b). The string of C_3 and C_4 is charged to V_{dc}/2 through a switch S_3 and S_8 as indicated by the blue dotted line. The output voltage during this state 2 v_o^2 can be expressed as

$$v_o^2 = (V_{C1} - V_{C3}) = 0.25V_{dc} \tag{2}$$

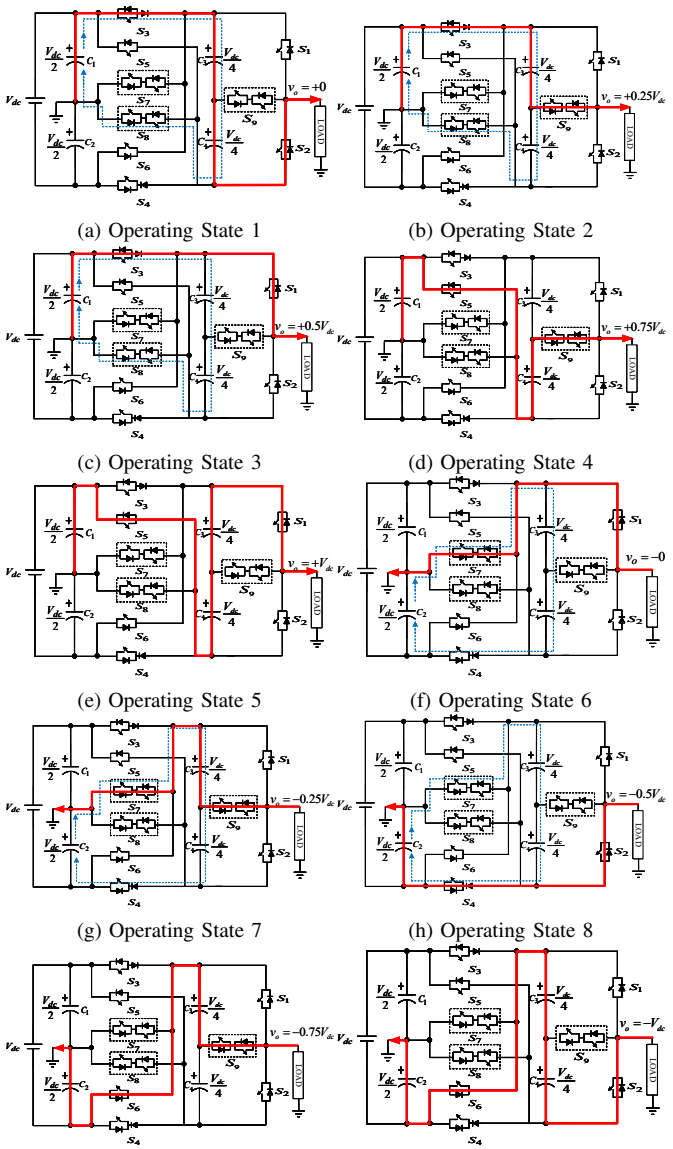


Fig. 2. Different operating states (a)-(j) of the proposed 9L-SCMLI in respect of the output voltage v_o.

Operating State-3 ($v_o = 0.5V_{dc}$): During state 3, the switch S_1, S_3, and S_8 are ON. The positive load current flows through the path C_1-S_3-S_1-C_1, which is shown by the red line. The charging of C_3 and C_4 takes place through the switch S_3 and S_8 as indicated by the blue dotted line as shown in Fig. 2(c). The output voltage (v_o^3) during state 3 can be represented as

$$v_o^3 = V_{C1} = 0.5V_{dc} \tag{3}$$

Operating State-4 ($v_o = 0.75V_{dc}$): During state 4, switch S_5 and S_9 are ON. The positive load current flows through the path C_1-S_5-C_4-S_9-C_1 as depicted in Fig. 2(d). The load current path is shown by the red line. No charge or discharge of C_3 occurs, although C_4 is discharged through the load. The output voltage during state 4 can be written as

$$v_o^4 = (V_{C1} + V_{C4}) = 0.75V_{dc} \tag{4}$$

Operating State-5 ($v_o = V_{dc}$): During state 5, switch S_1 and S_5 are ON. The positive load current flows through the path C_1-S_5-C_4-C_3-S_1-C_1 as indicated by the red line as shown in Fig. 2(e). Both C_3 and C_4 are discharged by load. The output voltage during state 5 can be written as

$$v_o^5 = (V_{C1} + V_{C3} + V_{C4}) = V_{dc} \tag{5}$$

For the remaining states, as indicated in Fig. 2(f) to Fig. 2(j). The analysis is the same as described for the above-mentioned states. As a result, nine different voltage levels are produced in the output voltage, including $\pm V_{dc}$, $\pm 0.75V_{dc}$, $\pm 0.5V_{dc}$, $\pm 0.25V_{dc}$, and ± 0.

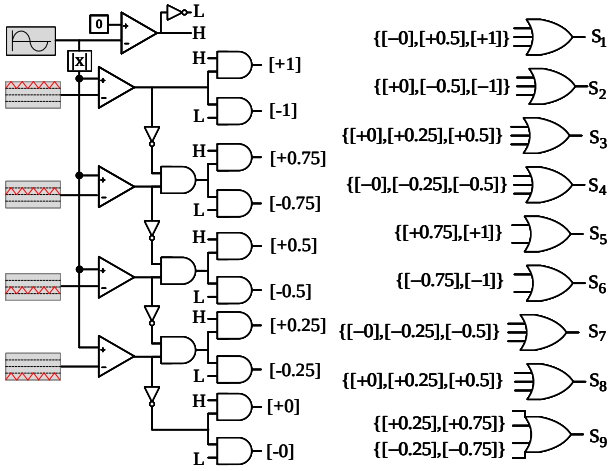


Fig. 3. PWM logic circuit for producing switching pulses for switch S_1 to S_9 of the proposed 9L-SCMLI.

C. PWM Control for Proposed 9L-SCMLI

The carrier-based sine PWM technique is considered to control the proposed 9L-SCMLI. One sinusoidal reference signal with an inverted negative half-cycle and four triangular carrier signals are used. The advantage of using such an inverted negative half-cycle reference signal is that the number of required carrier signals is half that of the noninverted reference signal. Hence, only four carrier signals instead of 8 are required to control a 9-level inverter. Each of the carrier signals has a $2.5kHz$ frequency. The carrier signals are level-shifted one above the other above the x-axis. Therefore, such a PWM is henceforth termed in this paper level-shifted PWM (LS-PWM). In addition to the reduced number of carrier signals, LS-PWM produces fewer harmonics in the output voltage. When the reference signal cuts the carrier signals, the gate pulses for all switches in the proposed 9L-SCMLI are produced according to the logic given in Fig. 3. In which the output of the AND gate ± 0 indicates zero voltage levels, ± 0.25 indicates $\pm 0.25V_{dc}$ voltage levels. Similarly, the voltage levels $\pm 0.5V_{dc}$, $\pm 0.75V_{dc}$, and $\pm V_{dc}$ are represented by the outputs ± 0.5, ± 0.75, ± 1, respectively. The carriers and reference signal arrangement, the gate pulse of each switch, and the 9-level output voltage waveform are illustrated in Fig. 4. The modulation index can be calculated as

$$m_a = \widehat{V}_{ref}/(4\widehat{V}_{cr}) \tag{6}$$

where m_a represents the modulation index, and $\widehat{V}_{ref}$ and $\widehat{V}_{cr}$ are the peak values of the reference signal and each carrier signal respectively.

D. Theoretical Analysis

Voltage and Current Stress on Switching Devices: Analyzing the operating states as demonstrated in Fig. 2, it is revealed that all the switches (S_1-S_9) are clamped across the capacitors during their turned OFF period. Therefore, the voltage across

TABLE II
VOLTAGE STRESS ACROSS THE PROPOSED 9L-SCMLI SWITCHES.

Operating State	S1	S2	S3	S4	S5	S6	S7	S8	S9	Vo $x = V_{dc}$
1	$0.25x$	0	0	$0.5x$	$0.5x$	x	$0.5x$	0	$0.25x$	0
2	$0.25x$	$0.25x$	0	$0.5x$	$0.5x$	x	$0.5x$	0	0	$0.25x$
3	0	$0.5x$	0	$0.5x$	$0.5x$	x	$0.5x$	0	$0.25x$	$0.5x$
4	$0.25x$	$0.25x$	$0.5x$	$0.5x$	0	$1.5x$	x	$0.5x$	0	$0.75x$
5	0	$0.5x$	$0.5x$	x	0	$1.5x$	x	$0.5x$	$0.25x$	x
6	0	$0.5x$	$0.5x$	0	x	$0.5x$	0	$0.5x$	$0.25x$	0
7	$0.25x$	$0.25x$	$0.5x$	0	x	$0.5x$	0	$0.5x$	0	-0.25
8	$0.5x$	0	$0.5x$	0	x	$0.5x$	0	$0.5x$	$0.25x$	-0.5
9	$0.25x$	$0.25x$	x	$0.5x$	$1.5x$	0	$0.5x$	x	0	-0.75
10	$0.5x$	0	x	$0.5x$	$1.5x$	0	$0.5x$	x	$0.25x$	-1

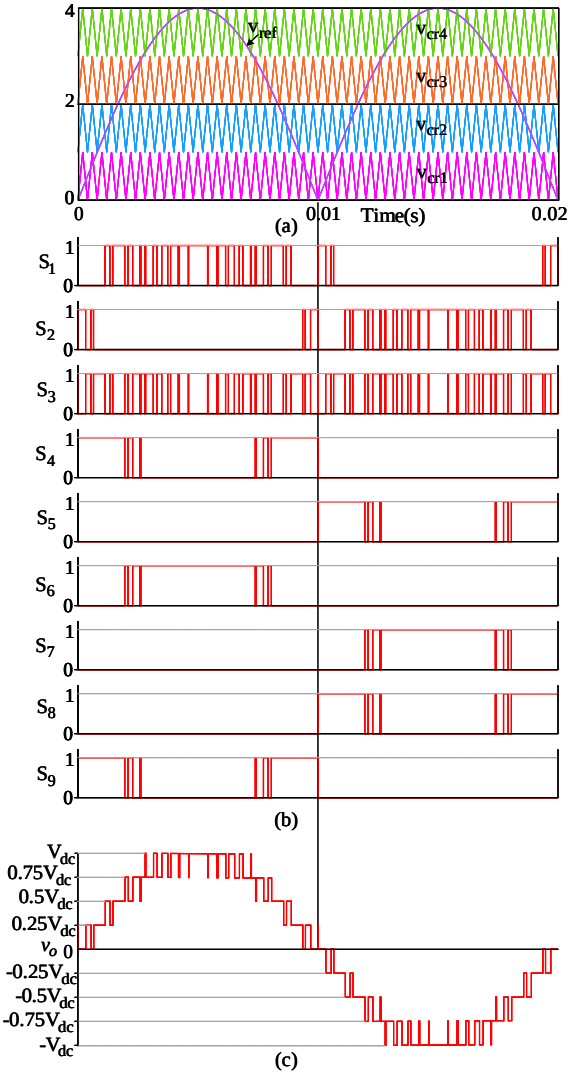


Fig. 4. Level-shifted sine PWM scheme for the proposed 9L-SCMLI.

each switch (V_{S1}- V_{S9}) for each output voltage level can be calculated as shown in Table II. From this table, the maximum voltage stress across the switches can be expressed as,

$$\begin{cases} V_{S1} = V_{S2} = V_{dc}/2; \quad V_{S5} = V_{S6} = 1.5V_{dc} \\ V_{S3} = V_{S4} = V_{S7} = V_{S8} = V_{dc}; \quad V_{S9} = V_{dc}/4 \end{cases} \tag{7}$$

It is evident that the highest voltage-stress occurs across switches S_5 and S_6 are $1.5V_{dc}$. For the SC-based inverter, some switches carry additional current due to capacitor charging. In the proposed topology, the charge current through the active capacitor (i_C) flows through the switches S_3, S_4, S_7 and S_8 only. Therefore, the current stresses across these switches are maximum. Other switches carry only the load current (i_L). The peak amplitude of the charging current passing through the switches is high, but its average value is lower. In the same way, the current stress on all switches can be calculated and tabulated in Table III. The maximum current stress on each switch on the proposed inverter can be mathematically represented as

TABLE III
CURRENT STRESS ON PROPOSED 9L-SCMLI SWITCHES.

Operating State	S1	S2	S3	S4	S5	S6	S7	S8	S9	Vo $x = V_{dc}$
1	0	i_L	i_L+i_C	0	0	0	0	i_L+i_C	0	0
2	0	0	i_L+i_C	0	0	0	0	i_C	i_L	$0.25x$
3	i_L	0	i_L+i_C	0	0	0	0	i_C	0	$0.5x$
4	0	0	0	0	i_L	0	0	0	i_L	$0.75x$
5	i_L	0	0	0	i_L	0	0	0	0	x
6	i_L	0	0	i_C	0	0	i_L+i_C	0	0	0
7	0	0	0	i_C	0	0	i_L+i_C	0	i_L	-0.25x
8	0	i_L	0	i_L+i_C	0	0	i_L	0	0	-0.5x
9	0	0	0	0	0	i_L	0	0	i_L	-0.75x
10	0	i_L	0	0	0	i_L	0	0	i_L	-x

$$\begin{aligned} i_{S1} &= i_{S2} = i_L \\ i_{S3} &= i_{S4} = i_{S7} = i_{S8} = (i_L + i_C) \\ i_{S5} &= i_{S6} = i_{S9} = i_L \end{aligned} \tag{8}$$

where $i_{S1}, i_{S1}, \ldots i_{S9}$ are the maximum current stress across switches $S_1, S_2, \ldots S_9$, respectively.

DC-link Capacitance Design: The semiconductor switches are selected considering voltage and current stress. The voltage between switches calculated in (7) is considered to decide the voltage rating of the switches. Average current ratings calculated in (8) are considered to determine the switching current rating. The switches S_3 and S_4 carry the capacitor charging current and the load current. Therefore, their current rating is high compared to other switches. The voltage rating of DC-link capacitors C_1, C_2 and the floating capacitors C_3, C_4 is determined on the basis of (1). The equivalent DC-link capacitance is calculated as

$$C_{dc-link} = \frac{P_o}{2\pi f_s V_{dc} \Delta V_{dc}}; \quad C_1 = C_2 = 2C_{dc-link} \tag{9}$$

where P_o and ΔV_{dc} represents the average power output of the inverter and ripple voltage (5-10% of V_{dc}) in C_1 and C_2 respectively. As C_1 and C_2 are connected in series. The capacitance of floating capacitors can be calculated as

$$C_F = \frac{I_{L,\max}}{\Delta V_C f_{sw}}; \quad C_3 = C_4 = 2C_F \tag{10}$$

where $I_{L,\max}$ is the amplitude of output current and ΔV_C is allowable ripple voltage (2-5% of V_{dc}/4 as per (1)) in the floating capacitors. As two floating capacitors C_3 and C_4 are connected in series.

Loss Analysis: The losses that occur in an SC-based power electronics converter are conduction losses, switching losses, and ripple losses in capacitors. In addition to those losses, conduction losses in the diode also occur where the diode is used. For the proposed 9L-SCMLI, a detailed loss analysis is given as follows

Conduction losses in switches and diodes: The IGBT with antiparallel diode is used as switches for the construction of the proposed 9L-SCMLI. In addition, two power diodes are also used. The conduction losses (P_{con}) and the diode losses (P_d) that occur on the switches and diodes, respectively, can

be calculated as follows [31].

$$P_{con} = [V_T + R_T i^{\beta}(t)]i(t)$$
$$P_d = [V_D + R_D i(t)]i(t) \quad (11)$$

For the switches, the on-state resistance, and on-state voltage are represented by R_T and V_T, respectively. Similarly, for the diode, these variables are denoted by R_D and V_D, respectively. The symbol β is the constant coefficient of the switch.

Switching losses: The switching losses (P_{sw}) occur in the switch during its transition from the ON state to the OFF state and vice versa. The energy losses during turn-on (E_{on}) and turn-off (E_{of}) of each switch can be calculated as follows [31]

$$E_{of} = \int_0^{t_{of}} \left[\left(\frac{v_{of}}{t_{of}} t \right) \left(-\frac{I_{of}}{t_{of}} (t - t_{of}) \right) \right] dt = \frac{1}{6} v_{of} I_{of} t_{of} \quad (12)$$

$$E_{on} = \int_0^{t_{on}} \left[\left(\frac{v_{on}}{t_{on}} t \right) \left(-\frac{I_{on}}{t_{on}} (t - t_{on}) \right) \right] dt = \frac{1}{6} v_{on} I_{on} t_{on} \quad (13)$$

where v_{of}, I_{of} and t_{of} are the turn-off voltage, current and time respectively of a switch. Similarly, v_{on}, I_{on} and t_{on} are the voltage, current, and time during the switch turn on, respectively. Thus, total switching losses in the inverter can be evaluated as

$$P_{sw} = f_s \left[\sum_{k=1}^{N_{sw}} \left(\sum_{i=1}^{N_{on}} E_{on} + \sum_{i=1}^{N_{of}} E_{of} \right) \right] \quad (14)$$

where N_{sw} is a number of switches, f_s is the fundamental frequency, and N_{on} and N_{of} are number of turning ON and OFF a switch during a complete cycle.

Ripple losses: The capacitors in an SC-based converter carry the charging and discharging current. Power losses occur in the capacitors because of their own internal resistance. The magnitude of the power loss (P_{cap}) depends on the magnitude of its voltage ripple and can be calculated as

$$P_{cap} = \frac{1}{2} C f_{sw} \Delta V_c^2 \quad (15)$$

where f_{sw} is the switching frequency, C is the capacitance of the capacitors $\{C_1, C_2, C_3, C_4\}$, and ΔV_c is the ripple voltage across respective capacitor. Therefore, the total losses that occur in the proposed 9L-SCMLI can be calculated as

$$P_{loss} = P_{con} + P_d + P_{sw} + P_{cap} \quad (16)$$

The total losses that take place in the switches, diodes, and capacitors of the proposed 9L-SCMLI are graphically presented in Fig. 5(a). It was calculated for a power output P_o=1000 W. The conduction losses in diodes (P_d) and ripple losses in capacitors (P_{cap}) together contribute 47% to the total losses. The rest of the losses (53%) take place in the switches (P_{con}, and P_{sw}). Among switches, S_3 and S_4 have a maximum amount of losses each of 12% as it carries the charging current in addition to the load current. In a practical implementation, these two switches could be strategically placed at one end of the power PCB near the entrance of the cooling mechanism. This could be forced air cooling or liquid cooling, depending on the specific application requirements. Such an arrangement would facilitate efficient heat dissipation from these switches, mitigating the impact of their higher loss contributions. The percentage of all four types of losses is shown in Fig. 5(b). which shows that the percentages of P_{con} and P_d are 44% and 22%, respectively. The contributions of P_{sw} and P_{cap} are 9% and 25%, respectively.

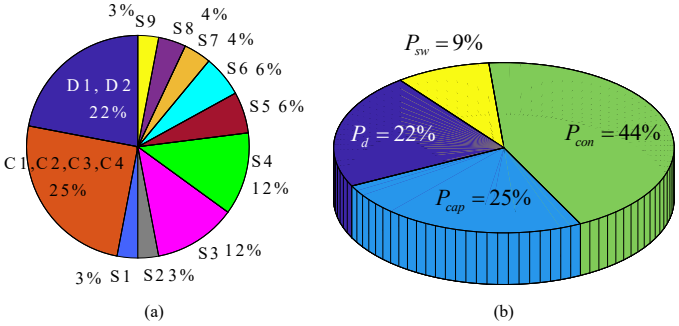


Fig. 5. (a) Power loss distribution among different devices and (b) Percentage of different types of losses of the proposed 9L-SCMLI.

E. Comparative Study

In order to prove the effectiveness of the proposed 9L-SCMLI, a fair comparison with similar typologies is illustrated in Table IV. To make such a comparison, the number of voltage levels (N), power electronics switches (N_{sw}), gate drives (N_{gd}), diodes (N_d), capacitors (N_c), and input DC source (N_{dc}) is taken into account. Furthermore, the switch-per-level ratio (N_{sw}/N) and the total standing voltage (TSV_{pu}) are added to the comparison to make it more reasonable. The term TSV_{pu} is calculated as follows;

$$TSV_{sw}(p.u) = \frac{1}{v_{o,\max}} \sum_{i=1}^{N_{sw}} V_{Si} \quad (17)$$

where V_{Si} is the voltage across i^{th} the switch, and $v_{o,\max}$ is the peak value of the output voltage. $TSV_{sw}(p.u)$ is evaluated after normalizing to $v_{o,\max}$.

All typologies with voltage gain equal to one are selected to achieve a greater degree of comparison. A five-level inverter is investigated in [32], which has a larger switch-per-level ratio and its TSV_{pu} value is quite high. In [16], a seven-level topology is proposed with 12 switches and 4 capacitors. The switch-per-level ratio is still high in such a topology. For a conventional Cascade H-Bride 9-level topology, 12 switches and 4 isolated input DC sources are required. The larger number of isolated DC sources is a drawback of the topology. In [23], a 9-level topology with 9 switches is proposed. Though it comprises a reasonable number of switches, it uses 4 isolated input sources. In another literature, a 9-level topology is described with 13 switches [24]. It consists of more switches and a higher N_{sw}/N ratio. In [25], a 9-level topology is invented with 12 switches, 3 capacitors, and a DC source. The drawback of such a topology is a higher number of switches. In [26], [27], the 9-level topology is investigated. However, the N_{sw}/N ratio, TSV_{pu}, and the number of switches are reasonable. However, both topologies use two isolated DC sources to achieve 9-level output. Using 12 switches, 12 gate drives, and 2 DC sources, a 9-level inverter is proposed in [10]. For such a topology, both the number of switches and the DC source are quite high. In [28], 17 switches and 4 capacitors are used to achieve a 9-level output. The number of switches is very large relative to the other topologies considered. Also, the value of TSV_{pu} is quite high. In [29], the 9-level output is achieved using 12 switches, 12 gate drives, and 2 DC sources. Such a topology also has the disadvantage of using more than one DC source. In contrast to the above, in this paper, a 9L-

TABLE IV
COMPARISON AMONG VARIOUS TOPOLOGIES ([P]: PROPOSED).

Topology	N	N_{sw}	N_{gd}	N_d	N_c	N_{dc}	N_{sw}/N	TSV_{pu}	VG	$\%\eta$	$\%THD\ v_o$	$\%THD\ i_a$
[32]-HIL	5	12	12	0	4	1	2.4	7.25	1	91.03%	21.91%	4.95%
[33]-HIL	5	6	6	0	0	2	1.2	7.84	0.5	90.73%	22.71%	4.83%
[16]-Exp	7	12	11	0	4	1	1.71	5	0.5	92.18%	17.85%	4.35%
[18]-HIL	7	10	8	2	3	1	1.42	5	1.5	96.21%	16.66%	3.84%
[34]-HIL	7	12	12	0	0	3	1.71	5.68	1	92.88%	17.69%	4.65%
[10]-Exp	9	12	12	0	2	2	1.33	4.5	1	96.91%	14.65%	3.67%
[11]-HIL	9	12	12	0	0	4	1.33	6.25	1	96.53%	16.78%	3.65%
[19]-Exp	9	10	10	2	3	1	1.11	5.5	1.5	97.01%	13.65%	3.75%
[23]-Exp	9	10	9	3	0	4	1	6	1	93.25%	14.95%	3.74%
[24]-Exp	9	13	13	0	2	1	1.44	7	1	92.15%	14.35%	3.69%
[25]-Exp	9	12	12	0	3	1	1.33	5	1	93.92%	14.21%	3.48%
[26]-Exp	9	8	8	0	2	2	0.88	4.5	1	93.01%	15.28%	3.61%
[27]-Exp	9	8	8	0	2	2	0.88	4.5	1	93.12%	15.01%	3.49%
[28]-Exp	9	17	17	0	4	1	1.88	7.25	1	91.49%	15.35%	3.53%
[29]-Exp	9	12	12	0	1	2	1.33	5	1	96.02%	14.81%	3.57%
[P]-HIL	9	12	9	2	4	1	1	5	1	97.25%	13.58%	3.27%
[35]-HIL	11	11	11	0	1	3	1	6.32	1.5	93.39%	12.81%	3.17%
[36]-HIL	13	10	10	0	4	2	0.76	5.85	1.5	92.38%	10.11%	2.26%
[30]-Exp	13	14	14	0	4	1	1.07	5.28	1.5	96.85%	9.11%	2.18%
[37]-HIL	23	12	12	0	2	2	0.52	6.29	1	92.73%	6.23%	1.84%

Note: $N/N_{sw}/N_{gd}/N_d/N_c$ = No. of voltage levels/switches/gate drivers/diodes/capacitors N_{dc}= No. of input DC source, VG=Voltage gain, η= efficiency at P_o=1000W. $\%THDv_o$= %THD in inverter voltage(v_o), $\%THDi_a$=THD in phase-a current at PCC.

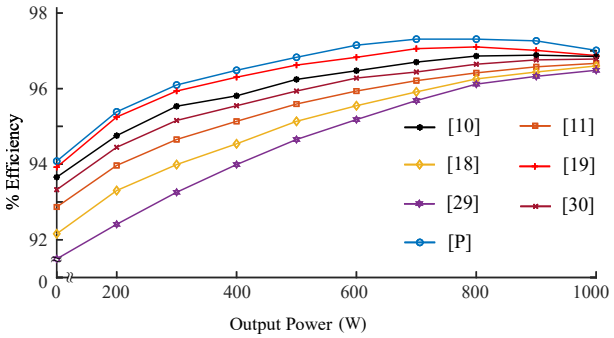


Fig. 6. HIL verified efficiency curves of different topologies in relation to output power.

SCMLI topology is proposed. It consists of 9 switches, 9 gate drives, 2 diodes, 4 capacitors, and only one DC source to produce 9-level output voltages. On the basis of the above discussion, it can be concluded that the 9L-SCMLI topology proposed in this paper is superior to other topologies taken into account.

The design of [33] comprises just 6 switches and 2 DC sources but requires an additional boost converter to achieve the required voltage boost. Likewise, the work in [34] generates a 7-level output using 12 switches; however, it requires a variable DC source, which is considered a drawback. On the contrary, a 7-level (7L) topology that achieves a voltage boost of 1.5 times is presented in [18]. Using 10 switches, its THD stands at an elevated 16.66%, indicating that there is room for improvement. The conventional 9-level cascaded H-Bridge (CHB) structure is described in [11]. While it serves as a foundational structure, it has the downside of requiring a high number of DC sources, rendering it impractical for some applications. A similar 9-level topology equipped with a voltage boost feature is reported in [19]. Although it also employs 10 switches, it is compromised by elevated voltage stress across those switches. An innovative 13-level output using 14 switches is demonstrated in [30], highlighting its extensibility through the addition of additional K-type units. Further multilevel inverter topologies for 11, 13, and 23 levels are explored in [35]–[37]. These designs employ 11, 10, and 12

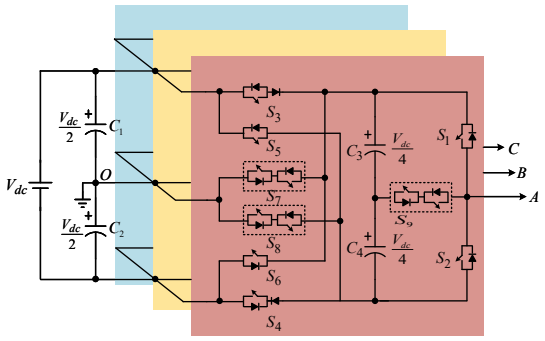


Fig. 7. $3-\varphi$ circuit structure of the proposed 9L-SCMLI.

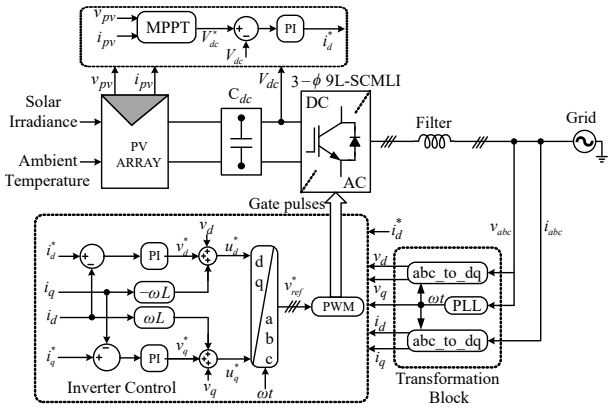


Fig. 8. Control block diagram of the $3-\varphi$ single-stage grid-connected PV system using the proposed 9L-SCMLI.

switches, respectively, but also suffer from high-voltage stress. In summary, each topology has its unique set of challenges, whether it is the number of DC sources, the high THD, the voltage stress or the complexity of the switch arrangements. Future research may focus on mitigating these issues to create more efficient and reliable systems.

The efficiency of an inverter topology is an important factor. It depends on the losses that occur in the topology. In a power electronics converter, three types of losses are mainly observed, such as conduction losses, switching losses, and capacitor ripple losses. The PLECS software is used to develop a thermal model of the inverter to evaluate losses. The efficiency of the inverter is estimated on the basis of the losses. The proposed 9L-SCMLI is correlated with recent MLIs in Table IV. This analogy is based on the number of switches, diodes, DC sources, capacitors, and gate drivers required for those topologies. It is obvious that among the single source MLI topologies, the proposed 9L-SCMLI needs the minimum number of switches and gate drivers. As a result, the cost and volume of the proposed inverter are significantly reduced. Furthermore, the voltage stress across the switches is lower and the maximum number of series connected switches is two to carry the load current. Therefore, both conduction losses and switching losses are significantly reduced. Fig. 6 shows the efficiency curves of different topologies considered in Table IV. The efficiency of the proposed topology is observed to be higher than that of the others. The other topologies have a comparatively lower efficiency than the proposed one, as a result of the higher number of switches. The maximum efficiency of the proposed topology is 97.25%, which corresponds to $300W$ output power. Compared to other

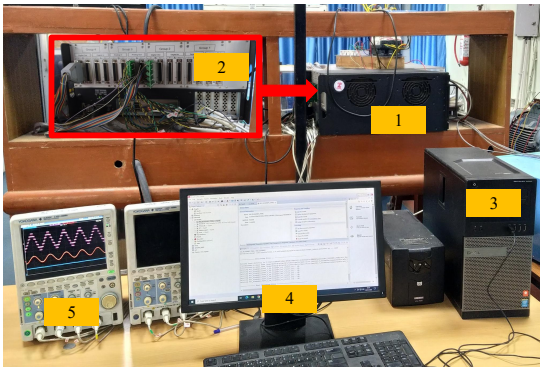


Fig. 9. HIL setup; 1: OPARL-RT 5700 RTU, 2: Signal i/o port of OPAL-RT, 3: Workstation, 4: Monitor, 5: Oscilloscope.

topologies, the efficiency of the proposed 9L-SCMLI is still high, 94.08% for $1000W$ output power, as shown in Table IV. The proposed 9L-SCMLI produces 13.58% THD, which is less than among the topologies considered for comparison.

F. PV-grid Integration with Proposed 9L-SCMLI

A single-stage PV-grid integration system is established using the $3-\varphi$ configuration of the proposed 9L-SCMLI. The $3-\varphi$ configuration of the proposed inverter, as shown in Fig. 7 is made up of three similar inverter legs. The $3-\varphi$ inverter is supplied by a single DC source through a common DC-link. The control block diagram of the system is shown in Fig. 8. The PV array is designed according to the specification in Table VI. The SunPower SPR-440NE-WHT-D photovoltaic module is selected in the PA array. The perturbation and observed (P&O) MPPT algorithm is used to extract the maximum power available from the photovoltaic array. The P&O is widely used for its precision and easy implementation. In each sample time, the MPPT calculates the delta change in the PV power and, based on the delta change, produces a reference value of V_{dc} that is termed V_{dc}^*. Then it is compared with the measure V_{dc}. The error signal is passed through a simple PI controller to produce a reference value of the current on the d-axis i_d^*. Three-phase PLL is used to convert the three-phase current (i_{abc}) and voltage (v_{abc}) at the point of common coupling (PCC) to the d- and q-axis current ($i_{d,}i_q$) and voltage ($v_{d,}v_q$) respectively. Then i_d^* and i_d are compared and passed through the PI controller to produce v_d^*. Similarly, i_q^* is externally given compared to i_q and passes through the PI controller to produce v_q^*. Next, v_d^*, v_d and the feedforward term $-\omega L i_q$ are added together to produce u_d^*, and v_q^*, v_q and feed-forward term $\omega L i_d$ are added together to produce u_q^*. Finally, three-phase reference signals (i_{abc}^*) for PWM are produced from u_d^* and u_q^* by converting them into the dq-abc transformation. The gate pulses for the inverter are generated by comparing four triangular carrier signals with the $3-\varphi$ sinusoidal reference signals V_{abc}^*. The inverter output is connected to a 400 V(rms) three-phase grid at the PCC point through a coupling inductor.

III. Results and Discussion

In proposed 9L-SCMLI, an Insulated-Gate Bipolar Transistor (IGBT) model was meticulously designed based on the datasheet specifications of the Semikron SKM100GB063D, a widely-used IGBT. This approach was taken to ensure that the simulation results are closely aligned with real-world applications. The initial modeling was performed in the Altair PSIM environment, known for its robust electrical simulation capabilities, and was subsequently accessed through the OPAL-RT 5700 Real-Time Emulator (RTE) feature integrated within the MATLAB/Simulink platform. This dual-platform strategy served as an additional layer of verification, improving the reliability and applicability of the model. Essential electrical and thermal characteristics were also incorporated to provide a comprehensive and realistic representation of the hardware component. The following assumptions are taken during validation, since real-time computational efficiency is often required for Hardware-In-Loop (HIL) simulations.

- Components like IGBTs are modeled based on ideal characteristics using datasheets, ignoring actual non-linear behaviors for computational feasibility.
- Simulation simplifies the complex switching dynamics of real-world components, focusing primarily on switched behaviors rather than intricate transients.
- Parasitic inductances and capacitance are averaged to make the model computationally less intensive.

TABLE V
Specifications for Testing Proposed 9L-SCMLI.

Description	Open-loop Parameters	Closed-loop Parameters
Input Voltage (V_{dc})	200 V	401.6 V
Peak Output Phase Voltage (V_o)	200 V	401.6 V
Output Power (P_o)	500 W	5 kW
Switching frequency (f_{sw})	2.5 kHz	2.5 kHz
Fundamental frequency (f_s)	50 Hz	50 Hz
DC-link capacitance (C_1, C_2)	470 μF, 250 V	2000 μF, 440 V
Floating capacitance (C_3, C_4)	2000 μF, 250 V	2000 μF, 440 V
Switches ($S_1 \ldots S_9$)	Semikron SKM100GB063D	

Note: $C_1 = C_2$ and $C_3 = C_4$ are calculated as per (9) and (10).

The experimental setup for the HIL test is shown in Fig. 9 and consists of the OPAL-RT 5700 RTE with sampling time of 10 μs, a high performance workstation, and YOKOGAWA-made oscilloscopes (model DLM2024). A $2\mu s$ dead time is provided for each gate pulse to control the proposed inverter through a level-shifted PWM.

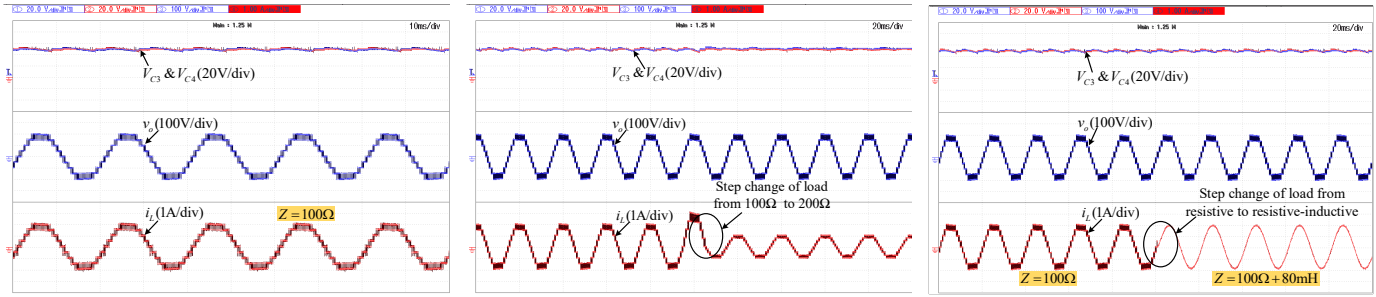
A. Single-Phase Open-loop HIL Validation

To test the single-phase 9L-SCMLI inverter in open-loop conditions, a series of Hardware-in-the-Loop (HIL) experiments are conducted in the laboratory. The inverter parameters utilized for these tests are detailed in Table V. The experiments proceed in the following sequence:

Initial Setup: The LS-PWM technique is initially used to generate all the switching pulses required for the inverter operation. The inverter specifications are tabulated in Table V.

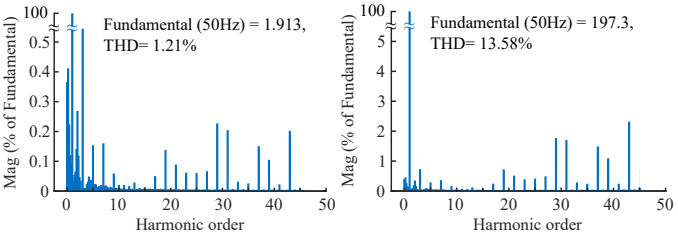
Resistive Load Test: A resistive load (R) with $Z = 100\Omega$ is first connected to the inverter output terminal. The resulting waveforms for the voltage across floating capacitors (V_{C3}, V_{C4}), output voltage (v_o) and output current (i_L) are shown in Fig. 10(a).The waveforms of V_{C3} and V_{C4} are balanced, each having a magnitude of $0.25V_{dc}$ or 50V. The peak of the output voltage (v_o) is 200V, consisting of 9 equal voltage levels. The output current (i_L) exhibits a staircase waveform with a peak magnitude of 2A.

Step Change to Higher Resistive Load: The resistive load is then changed from $Z = 100\Omega$ to $Z = 200\Omega$ and the corresponding waveforms are shown in Fig. 10(b). Despite the instant load change, the waveforms of V_{C3}, V_{C4}, and v_o



(a) Resistive load (b) Step change of load from 100Ω to 200Ω (c) Step change of load from resistive to resistive-inductive

Fig. 10. Open-loop HIL testing of the proposed 9L-SCMLI inverter under resistive load.



(a) (b)

Fig. 11. Harmonics spectrums of (a) output current, (b) output voltage of the proposed 9L-SCMLI inverter under RL load ((Z=100Ω + 80mH) under m_a=1.

remain constant. The only change is in the magnitude of i_L, which decreases to half.

Switching to Resistive-Inductive Load: Subsequently, the load is switched from a purely resistive load to a resistive inductive load (RL) characterized by $Z = 100\Omega + 80mH$. The updated waveforms are shown in Fig. 10(c). The output voltage (v_o) waveform remains unchanged. V_{C3} and V_{C4} are still balanced. The waveform of i_L transitions smoothly from a staircase shape to almost sinusoidal.

RL Load Connection: Initially, a Resistive-Inductive (RL) load characterized by $Z = 100\Omega + 80mH$ is connected to the inverter output terminal. The harmonic content in v_o and i_L is depicted in Fig. 11(a) and Fig. 11(b), respectively. %THD values for v_o and i_L are 13.58% and 1.21%, respectively. The corresponding observations can also be made from Fig. 12(a). Both V_{C3} and V_{C4} have balanced magnitudes of 50V. The output voltage (v_o) waveform remains unchanged from the previous tests. The output current (i_L) transitions to a nearly sinusoidal waveform.

DC Voltage Change: A sudden change in DC voltage is applied from $0.5V_{dc}$ to V_{dc} and the results are illustrated in Fig. 12(b). The magnitudes of V_{C3}, V_{C4}, v_o, and i_L instantly adjust to the new level V_{dc}.

Voltage Transient Conditions: Initially, V_{dc} is set to zero, leaving all waveform magnitudes zero. Upon application of a 200V DC input, the inverter starts to operate automatically. This initial condition is shown in Fig. 12(c).

Frequency Change: The inverter output frequency suddenly changes from $50Hz$ to $100Hz$, as shown in Fig. 12(d). v_o and i_L adapt to the new frequency. V_{C3} and V_{C4} remain unchanged.

Modulation Index Step Changes: Initial tests alter the modulation index from 1.0 to 0.7, as illustrated in Fig. 12(e) and then from 0.7 to 0.45, as illustrated in Fig. 12(f). The observations made from 12(e): V_{C3} and V_{C4} remain constant; the magnitude of i_L decreases proportionally; v_o changes to 9, 7, and 5 voltage levels for $m_a = 1.0$, $m_a = 0.7$, and $m_a = 0.45$, respectively; and further tests reverse the modulation index from 0.2 to 0.45, and then to 0.7. Similarly, observations made in Fig. 12(f): v_o and i_L adapt to the new modulation index; v_o manifests 3, 5, and 7 voltage levels; and i_L increases proportionally.

TABLE VI
SPECIFICATIONS OF THE PV ARRAY

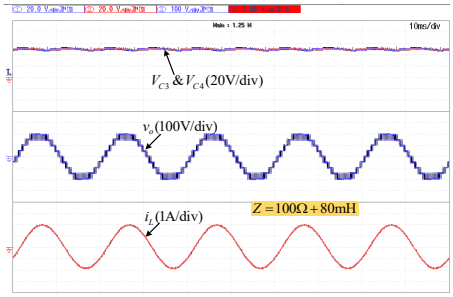
Parameters	Value
No. of parallel string (N_p)	2
No. of series connected modules per string (N_s)	6
Open-circuit voltage of each module (V_{oc})	86.5 V
Module voltage in MPP (V_{mpp})	72.9 V
Short-circuit current rating of each module (I_{sc})	6.5 A
Maximum module current at MPP (I_{mpp})	6.04 A
Maximum power of each module (P_{mpp})	440.3 W

The voltage stress across different switches is measured for a 200 V DC input. From Figs. 13 (a), (b), and (c), it is observed that the maximum voltage stress across switches S_1, S_2, and S_9 is 100V, 100V, and 50V, respectively. S_5 and S_6 exhibit a maximum voltage stress of 300V and the remaining switches show a voltage stress of 200V. The test results demonstrate that the proposed 9L-SCMLI performs smoothly under both steady-state and dynamic conditions.

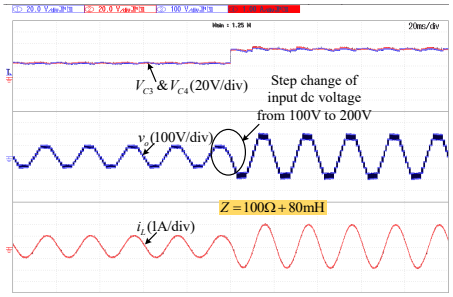
B. Three-Phase Closed Loop Test through PV-Grid Integration

1) Initial Experiment on 3-Phase Configuration: A 5 kW, single-stage, proposed $3-\varphi$ 9L-SCMLI based PV-grid system is tested in HIL experiment using OPAL-RT 5700 RTE under different load and environmental conditions. First, the experiment on the $3-\varphi$ configuration of the proposed 9L-SCMLI is carried out under open loop condition. The $3-\varphi$ inverter is supplied by a 400 V DC source and operates with a $2.5kHz$ switching frequency. A three-phase load of 5 kW with a 0.8 lag power factor is connected to the inverter output. The line-to-line output inverter voltage waveform ($v_{inv(L-L)}$), three-phase inverter currents (i_a, i_b, i_c), and the harmonic spectrum of i_a are shown in Fig. 14. It is observed that $v_{inv(L-L)}$ consists of 17 equal voltage levels and that the three-phase currents are nearly sinusoidal. The %THD in phase-a (i_a) current is only 0.89%.

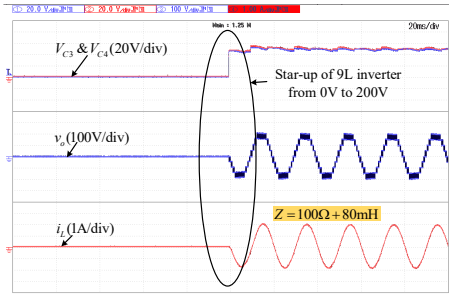
2) Testing under Various Power Factor Conditions: The proposed photovoltaic grid system is tested under the con-



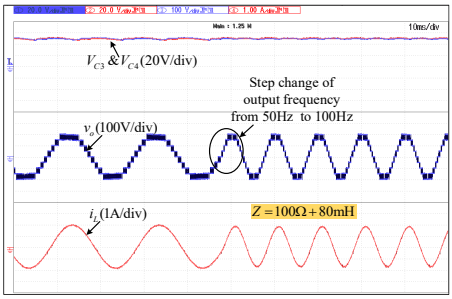
(a) Resistive-inductive load



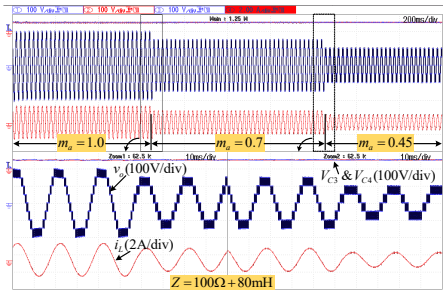
(b) Step change of input DC voltage from 100V to 200V



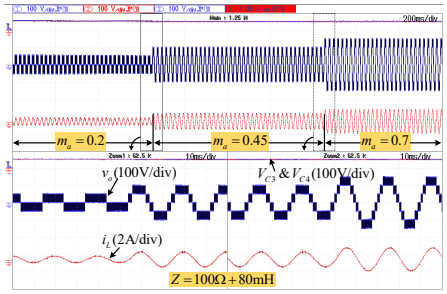
(c) Start-up condition of the inverter



(d) Step change of output frequency from 50Hz to 100Hz

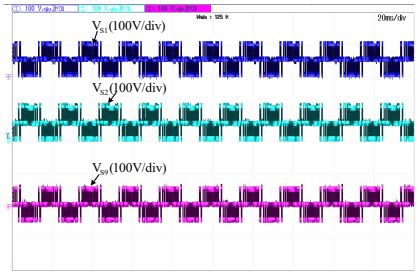


(e) Step change of modulation index (m_a) from 1.0 to 0.7, then 0.7 to 0.45

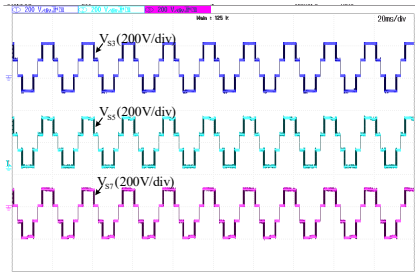


(f) Step change of modulation index (m_a) from 0.2 to 0.45, then 0.45 to 0.7

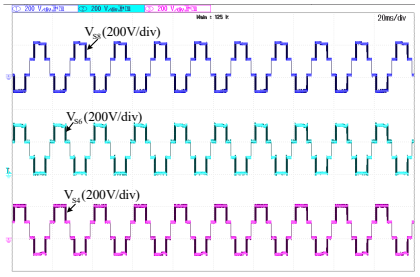
Fig. 12. Open-loop HIL results of the proposed 9L-SCMLI inverter under different conditions.



(a) Voltage stress across S_1, S_2, and S_9



(b) Voltage stress across S_3, S_5, and S_7



(c) Voltage stress across S_8, S_6, and S_4

Fig. 13. Voltage stress across switches of the proposed 9L-SCMLI for input DC voltage $V_{dc} = 200V$ during open-loop HIL test.

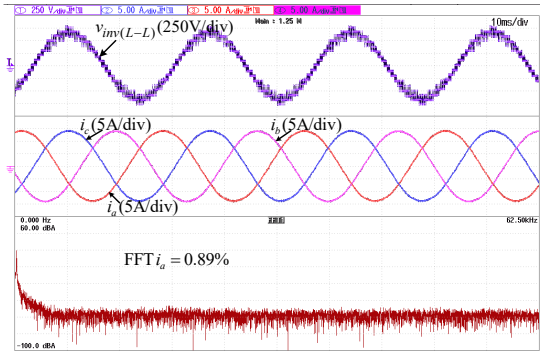
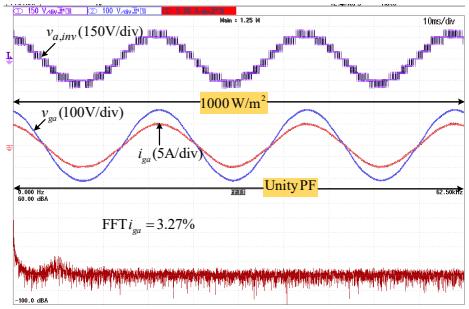


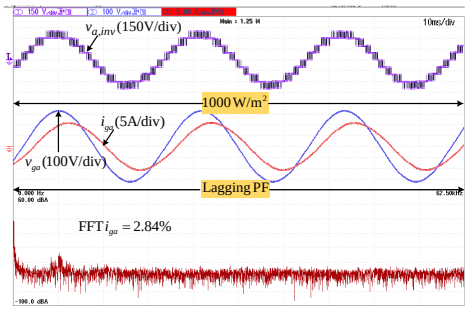
Fig. 14. HIL results of the $3-\varphi$ proposed 9L-SCMLI under 5 kW loads with 0.8 lagging power factor.

ditions of unity, lag, and leading power factor. The respective waveforms are plotted in Fig. 15. Solar irradiance is kept constant at 1000 $\mathrm{W/m^2}$ for all three cases. For the unity power factor, the phase-a voltage of the inverter ($v_{a,inv}$), phase-a grid voltage (v_{ga}), and injected grid current in phase-a (i_{ga}), and the harmonic spectrum of i_{ga} are shown in Fig. 15(a). The inverter operates at a modulation index of 0.8. It is observed that $v_{a,inv}$ consists of 9 equal voltage levels and the peaks of v_{ga} and i_{ga} reach 325 V and 9.667 A, respectively. v_{ga} and i_{ga} are in phase due to unity PF, and i_{ga} is nearly sinusoidal. The %THD in i_{ga} is 3.27 %, which is consistent with IEEE standards. Then, the PV system is operated under lagging PF, and the respective waveforms of $v_{a,inv}$, v_{ga}, i_{ga}, and the harmonic spectrum of i_{ga} are plotted in Fig. 15(b). It is observed that i_{ga} is close to sinusoidal and lags v_{ga} by 28.14° due to a lag PF operation. The peak of i_{ga} reaches 12.44 A and its content is 2.84% THD, which is in accordance with IEEE 519-2022 standards. The PV system is then run with the leading PF, and the corresponding waveforms of $v_{a,inv}$, v_{ga}, i_{ga}, and the harmonic spectrum of i_{ga} are illustrated in Fig. 15(c). The inverter runs at 0.88 leading PF. The i_{ga} leads to the v_{ga} by the 28.14° angle, which is the leading PF operation. The peak of i_{ga} reaches 12.32 A. The %THD in i_{ga} is 2. 92%, again complying with the IEEE 519-2022 standards.

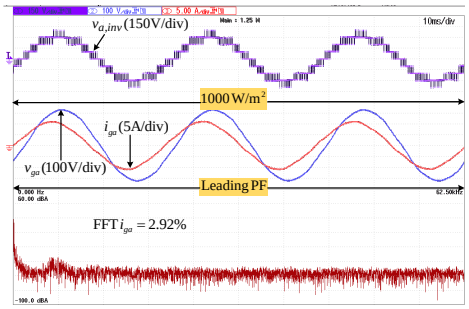
3) Experiments under Varying Irradiance: The experiment is carried out in the PV system under varying irradiance conditions, and the respective waveforms of the PV side under



(a) Unity power factor



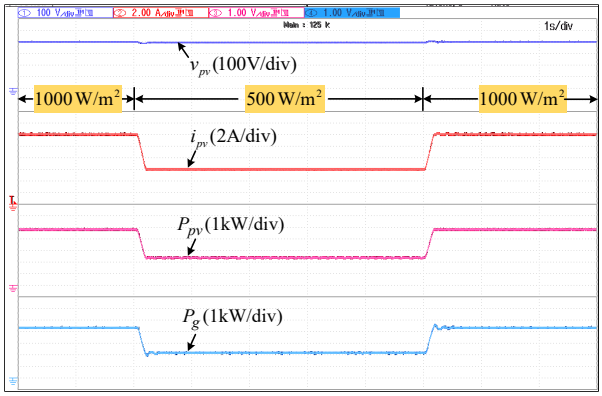
(b) Lagging power factor



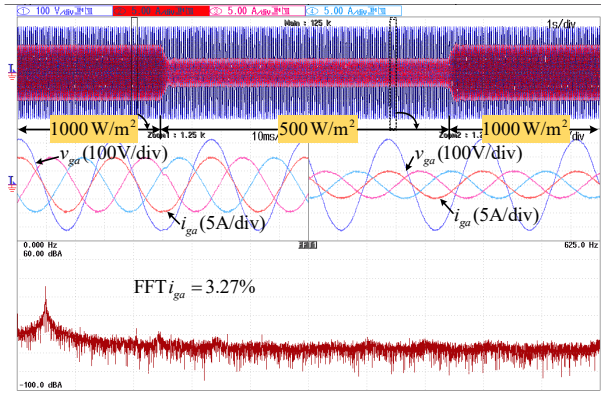
(c) Leading power factor

Fig. 15. HIL results of the PV-grid system using the proposed 9L-SCMLI under different power factor conditions.

varying irradiance such as PV voltage (v_{pv}), PV current (i_{pv}), PV output power (P_{pv}) and injected real power (P_g) to PCC are shown in Fig. 16(a). A step change in irradiance from 1000 W/m^2 to 500 W/m^2 is applied, and it is reversed after a certain period of time. The power factor of the photovoltaic system was kept in unity during this experiment. The magnitude of v_{pv} is 401.6 V for 1000 W/m^2 irradiances, and it is slightly reduced to 396.1 V during 500 W/m^2 irradiances. It can be said that the magnitude of v_{pv} remains almost constant despite such a variation in irradiance. The magnitude of i_{pv} decreases from 12.1 A to 6.04 A when the irradiance changes from 1000 W/m^2 to 500 W/m^2. The magnitude of P_{pv} is 4.8 kW and 2.4 kW for irradiance 1000 W/m^2 and 500 W/m^2, respectively. After achieving system losses, the PV system injects real power (P_g) into the PCC, which is 4.3 kW and 2.14 kW for irradiance 1000 W/m^2 and 500 W/m^2 respectively. The waveforms of the grid side parameters v_{ga}, i_{ga}, and the harmonic spectrum of i_{ga} under such varying irradiance are shown in Fig. 16(b). The peak magnitude of v_{ga} is observed to remain constant at 325 V despite the variation of irradiance. But the variation in the impact of irradiance on the magnitude of i_{ga}. The maximum magnitude of i_{ga} reduced from 9.667 A to 4.833 A when irradiance changed its step from 1000 W/m^2



(a) PV-side parameters

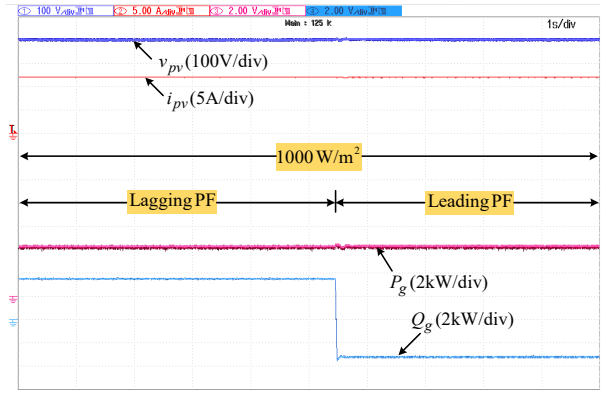


(b) Grid-side parameters

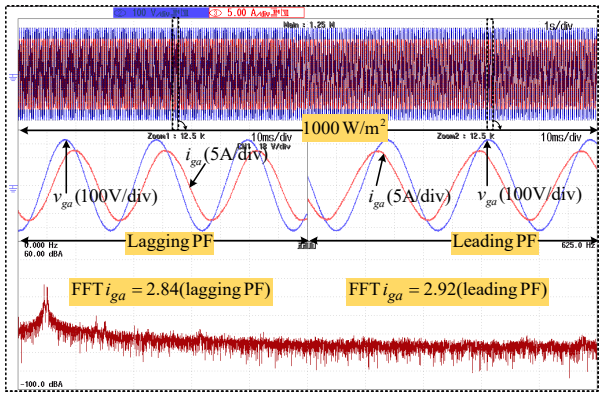
Fig. 16. HIL results of the PV-grid system using the proposed 9L-SCMLI under varying irradiance conditions.

to 500 W/m^2. The change in the maximum value of i_{ga} is smooth with the change in irradiance step. The %THD in i_{ga} is 3.27% corresponds to 1000 W/m^2 irradiance. However, the %THD increases to 4.79% during 500 W/m^2 irradiance. Both the value of %THD in i_{ga} comply with IEEE standards.

4) Dynamic Behavior Test: The dynamic behavior of the PV grid system is tested under a step change of the power factor from lagging to leading. During this dynamic test, the irradiance value is kept constant at 1000 W/m^2. The PV grid is initially run at 0.76 lag PF, then a command is applied to the control system to change the PF from 0.76 lag to 0.76 leading immediately. In this circumstance, the PV side parameters, such as v_{pv}, i_{pv}, and the real and reactive power P_g, Q_g injected into the PCC are illustrated in Fig. 17(a). It is evident that the magnitudes of v_{pv} and i_{pv} remain constant at 401.6 V and 12.1 A, respectively, due to constant irradiance. The magnitude of P_g is also constant at 4.3 kW. However, the sign of Q_g changes from positive (+3.5 kVAR) to negative (-3.5 kVAR) when the PF changes from lagging to leading. The grid side parameters under such a varying PF are plotted in Fig. 17(b). It is noticed that the magnitude of v_{ga} remains constant at 325 V, irrespective of the change in PF. The maximum value of i_{ga} is kept constant at 12.44 A for the lag PF and 12.32 A for leading PF, respectively. However, i_{ga} lags v_{ga} by the 39.11° angle during the lagging PF operation and advances v_{ga} by the same angle during the leading PF operation. The %THD in i_{ga} are 2.84% and 2.92% for 0.76 lagging PF and leading PF, respectively, which comply with IEEE standards. The angle change of i_{ga} from lagging to leading occurs



(a) PV-side parameters



(b) Grid-side parameters

Fig. 17. HIL results of the PV-grid system using the proposed 9L-SCMLI under step change of power factor from lagging to leading.

instantly. Therefore, it is concluded that the steady-state and dynamic behavior of the proposed photovoltaic grid system is satisfactory.

IV. Conclusion

In conclusion, this paper presents a new 9L-SCMLI topology that employs a single DC source while minimizing the switch count. The topology consists of 12 switches, 3 capacitors and 2 diodes and is capable of generating nine different output voltage levels with unity voltage gain. The output voltage has a low total harmonic distortion (THD) of 13.58%, attesting to its high-performance capability. This design leverages the switched-capacitor technique and has a self-voltage balancing feature. A comprehensive comparison with existing topologies based on criteria such as switch count, voltage stress, and the number of conducting switches demonstrates the superior effectiveness of the proposed design. The topology has shown satisfactory steady-state and dynamic performance under various test conditions. A single-stage three-phase photovoltaic (PV) system integrated with the grid has been successfully implemented using the proposed 9L-SCMLI. Experimental results under different conditions confirm the system's reliable performance and compliance with IEEE 512 standards for THD content in the injected grid current. This makes the proposed topology particularly well-suited for PV applications. Future work will explore the feasibility of scaling this topology for higher voltage and power applications.

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