Real-Time Lagrange-Polynomials Selective Harmonic Elimination for Unbalanced Five-Level Inverters

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Abstract—The effects of DC source voltage unbalance on the CHB inverter, if not properly managed, reduce the efficiency of the whole power system and generate unwanted harmonics in the output voltage with increased THD. In this paper, an SHE technique operating at the fundamental frequency has been proposed for unbalanced five-level CHB inverters to fix the amplitude of the fundamental harmonic, set the amplitude of the lower order harmonics to zero and achieve high efficiency performance. A preliminary off-line graphical approach was used to determine the switching angles at some modulation index values. Subsequently, a real-time interpolating Lagrange polynomial-based approach is proposed to obtain a continuous modulation index range. The study has been preliminarily analyzed in a simulation environment and subsequently validated experimentally.

Index Terms—Power quality, efficiency, total harmonic distortion, multilevel inverters.

I. INTRODUCTION

ULTILEVEL Power Inverters (MPIs) are an innovative and attractive solution for power conversion applications

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such as medium to high power motor drives, active power filters, reactive power compensation and renewable energy systems [1]. Compared to conventional two-stage voltage source inverters (VSIs), MPIs offer better harmonic behaviour with reduced total harmonic distortion (THD), reduced conduction and switching losses, reduced dv/dt stress, reduced electromagnetic interference (EMI) and fault tolerance. The performance of MPIs is strictly dependent on the modulation strategy adopted, which allows the switching angles to be determined. More specifically, switching and conduction losses are a very challenging issue due to the high blocking voltages and commuted currents in high power medium voltage (MV) applications where thermal constraints of semiconductor devices impose limits on total device losses. Therefore, low switching frequency modulation techniques are required to achieve high device utilization and higher converter efficiency [2]. In general, classical Selective Harmonic Elimination (SHE) and Selective Harmonic Mitigation (SHM) techniques operate at the fundamental switching frequency and are used in medium and high voltage applications where high-efficiency converter operation is required, such as drives [2], [3], [4], [5] and distributed generation [6], [7], [8], [9], [10]. This type of algorithm allows the elimination of lower order harmonics, the number of which is a function of the MLI hardware structure and, in the case of the CHB inverter structure, a function of the cascaded H-bridges. Although SHE PWM techniques can eliminate a greater number of harmonics [11], they operate at a higher switching frequency than the fundamental and are therefore not always suitable for high-efficiency operation. The challenging aspects of SHE algorithms are related to the problem formulations, the associated nonlinear transcendental equations can be solved by iterative approaches [12] and optimization methods or evolutionary algorithms [13].

When low-level topologies are considered, analytical solutions can be found [14]. The iterative approach, such as the Newton-Raphson (NR) algorithm, can be used to determine the switching angles, but the convergence of the method depends on the initial values, which are initially unknown, and the solution could be divergent. Artificial Intelligence (AI) based algorithms (Genetic and Particle Swarm Optimisation algorithms) are difficult to implement and have high computational costs [15], [16], [17]. Analytical methods can be computationally efficient: the transcendental equations can be approximated by polynomial equations and solved mathematically in closed form [18]. In this

© 2024 The Authors. This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/ article, a SHE approach operating at the fundamental frequency is proposed and applied to a three-phase, five-level cascaded Hbridge (CHB) inverter with unbalanced DC sources. Normally, the operation of CHB multilevel inverters with unbalanced DC sources generates unwanted harmonic components on the output voltage [19]. In this context, the main issues related to the application of SHE approaches are related to the choice of a method to solve the equations, its real-time applicability and its extension to a wider modulation index interval. In [20], the authors present an approach based on a hybrid Newton-Raphson method to solve the SHE equation without equal DC sources. The authors use the notch angles determined for equal DC sources also for unequal DC sources, then the content of lower order harmonics increases as well as the voltage THD. In [21], the authors use a generalized pattern search optimization method for harmonic elimination in 5- and 7-level inverters with equal and unequal DC sources. The performance of the proposed method is compared with that of a genetic algorithm. The main drawback is related to the complex implementation and its computational cost. In [22], the influence of the optimal DC source has been studied and its significant role in the effective harmonic elimination and the satisfaction of the desired fundamental harmonic value has been demonstrated. In order to address the main issues related to the computational burden of the SHE method and its harmonic cancellation effectiveness for unbalanced CHB inverters, a SHE technique operating at the fundamental switching frequency to reduce the power losses is proposed based on the following steps:

- 1) identification, by choosing some modulation indices, of the switching angles (solutions) depending on m, by graphical approach
- 2) constructing an analytical formula of the switching angles as a function of the modulation indices, based on the Lagrange polynomial, valid in the interval of m in which the solution exists.

The method can be extended to 7 and 9 level inverters; in fact, it is necessary to have a plane or a three-dimensional space of the switching angles, depending on the choice of *m*, which allows the identification of the solution values. For the 7-level inverters, an angle is expressed with respect to the other two, therefore the plane is identified. For the 9-level inverters, one angle is expressed with respect to the other three-dimensional space is identified. Since low-level multilevel inverters are adopted and proliferated in the main high-power MV industrial applications [23], such as electrical drives [3], [24] and distributed generation [7], the analysis focuses on a five-level configuration of CHB inverters. The main contribution is related to the high efficiency operation and the elimination of lower order harmonics resulting in a reduction of the filter size.

The advantage of the proposed method is that it avoids the use of a look-up table, saving memory and returning the values of the switching angles for any m within the interval in which the solution exists. If a look-up table is used, for a given m in the input not in the table, an error is made due to the approximation of the angles to the nearest m, with the possibility of not obtaining the performances of the method on the elimination of harmonics [25], [26], [27], [28]. A preliminary investigation of the effectiveness of the proposed graphical approach has been



Fig. 1. Three-phase 5-level CHB inverter.

carried out by the authors on the simulation environment for a wide choice of partitions of unequal dc voltage sources [29]. In this manuscript, the proposed SHE method has been deeply improved and its effectiveness has been experimentally validated for a three-phase five-level CHB inverter, considering the voltage partitions that allow to obtain the lowest values of THD%. This paper is structured as follows: Section II presents the mathematical framework of the proposed SHE approach.; Section III discusses the application of the proposed SHE technique with particular reference to the graphical analysis and the construction of Lagrange polynomials; Section IV discusses the simulation results obtained; Section V describes the test bench setup and the experimental results obtained for validation purposes. Finally, Section VI summarizes the main features of the proposed SHE approach and reports the conclusions of the study.

II. MATHEMATICAL FORMULATION OF THE PROPOSED SHE METHOD

In this paper, three-phase five-level CHB multilevel inverters are considered (Fig. 1), with two H-bridges fed by unequal DC voltage sources V_{dci} , i = 1, 2 and a modulation technique working at fundamental switching frequency (two switching angles), is proposed to reduce the switching losses.

The proposed technique calculates the switching angles α_i , i = 1, 2, which eliminate low order harmonics and return a fixed fundamental harmonic amplitude. It works in two steps:

- the first one is based on a graphical analysis of the implicit equations and finds the switching angles, for some modulation index values, as intersection points of the curves drawn;
- the second one uses the interpolation polynomials on the switching angles carried out in the previous step, to obtain the switching angles for any modulation index within the interest interval.

Given phase A, the Fourier series expansion, truncated to 2N - 1, of the inverter output phase voltage waveform is:

$$\nu_{AN}(\omega t) = \frac{4}{\pi} \sum_{k=1}^{N} H_{2k-1} \sin\left((2k-1)\,\omega t\right)$$
(1)

Partitions Depending on p					
per unit length (p.u.)					
p	p_1	p_2	$\frac{V_{dc1}}{V_{dc}} = \frac{p_1}{p}$	$\frac{V_{dc2}}{V_{dc}} = \frac{p_2}{p}$	
	1	p-1	$\frac{1}{p}$	$\frac{p-1}{p}$	
	2	p-2	$\frac{2}{p}$	$\frac{p-2}{p}$	
even	:	÷	:	:	
	$\frac{p}{2} - 1$	$\frac{p}{2} + 1$	$\frac{\frac{p}{2}-1}{p}$	$\frac{\frac{p}{2}+1}{p}$	
	1	p-1	$\frac{1}{p}$	$\frac{p-1}{p}$	
	2	p-2	$\frac{2}{p}$	$\frac{p-2}{p}$	
odd	:	:	:		
	$\frac{p-1}{2}$	$\frac{p+1}{2}$	$\frac{p-1}{2p}$	$\frac{p+1}{2p}$	

TABLE I

where H_{2k-1} is the amplitude of the harmonic of order 2k - 1, that can be expressed as:

$$H_{2k-1} = \frac{4}{\pi (2k-1)} \sum_{i=1}^{2} V_{dci} \cos\left((2k-1)\alpha_i\right)$$
(2)

The set of SHE equations to solve is:

$$\begin{cases} \frac{V_{dc1}}{V_{dc}}\cos\left(\alpha_{1}\right) + \frac{V_{dc2}}{V_{dc}}\cos\left(\alpha_{2}\right) - m = 0\\ \frac{V_{dc1}}{V_{dc}}\cos\left(5\alpha_{1}\right) + \frac{V_{dc2}}{V_{dc}}\cos\left(5\alpha_{2}\right) = 0 \end{cases}$$
(3)

Considering a real application with a storage system, in this work a battery cell with a nominal voltage of 4 V has been used as a case of study. The required voltage is $V_{dc} = \sum_{i=1}^{s} V_{dci} = 4p$ with p > 0, integer number equal to the number of the battery cell connected in series. Let $V_{dc1} = 4p_1$ and $V_{dc2} = 4p_2$, with $p = p_1 + p_2$ and $p_1 = 1, 2, \ldots, \frac{p}{2} - 1$ (if p is even) or $\frac{p-1}{2}$ (if p is odd) and $p_2 = p - 1, p - 2, \ldots, \frac{p}{2} + 1$ (if p is even) or $\frac{p+1}{2}$ (if p is odd), the possible partitions are shown in Table I. Table II summarizes, assuming p = 10, the switching angles obtained as a function of modulation index and unequal DC voltage sources, sorted with respect to the constraint $0 \le \alpha_1 < \alpha_2 < \frac{\pi}{2}$. In this way, a generic harmonic amplitude H_{2k-1} can be expressed as a function of the voltage partition p_1 and p_2 , respectively, and expressed in p.u. with respect to the V_{dc} . In fact, the amplitude of the fifth harmonic H_{2k-1}^{2} can be expressed as:

$$H_5^* = \frac{4}{5\pi} \left[\frac{p_1}{p} \cos(5\alpha_1) + \frac{p_2}{p} \cos(5\alpha_2) \right]$$
(4)

From equation (4), it is interesting to note that the amplitude of the fifth harmonic depends on the control angles, α_1 and α_2 , and on the voltage partition $\frac{p_1}{p}$ and $\frac{p_2}{p}$. According to the simulation analysis carried out in [29], the voltage partition considered in this study is $\frac{p_1}{p} = 0.6$, $\frac{p_2}{p} = 0.4$ because it provides solution for all considered modulation index and gives the best THD values evaluated as:

THD =
$$\left(\sqrt{\sum_{k=5,7...}^{49} H_k^2}\right) / H_1$$
 (5)

TABLE II SWITCHING ANGLES OBTAINED WITH p = 10

	~	~		
m	$\frac{p_1}{p}$	$\frac{p_2}{p}$	$\widetilde{\alpha_1}$ [rad]	$\widetilde{\alpha_2}$ [rad]
	0.9	0.1	0.3276	1.0718
	0.8	0.2	0.2898	0.8409
0.9	0.7	0.3	0.2413	0.7462
	0.6	0.4	0.1758	0.6871
	0.5	0.5	0.0149	0.6433
	0.8	0.2	0.3631	1.3070
	0.7	0.3	0.3635	1.0635
0.8	0.6	0.4	0.3227	0.9552
	0.4	0.6	0.1348	0.8329
	0.5	0.5	0.2572	0.8855
	0.2	0.8	0.0683	0.8948
	0.7	0.3	0.3785	1.4049
07	0.3	0.7	0.3045	0.9383
0.7	0.6	0.4	0.4425	1.1653
	0.4	0.6	0.3858	0.9896
	0.5	0.5	0.4295	1.0578
	0.1	0.9	0.5402	0.9626
	0.2	0.8	0.6179	0.9929
0.6	0.3	0.7	0.6429	1.0308
0.0	0.6	0.4	0.3855	1.4604
	0.4	0.6	0.6369	1.0882
	0.5	0.5	0.5739	1.2023

1) First Part of the Method: It is based on a graphical analysis and represents the system (3), written in implicit form and in p.u., as (6), in the plane $\alpha_1 \alpha_2$, and finds the solutions as the intersections of the curves $F_1(\alpha_1, \alpha_2) - m = 0$ and $F_2(\alpha_1, \alpha_2) = 0$.

$$\begin{cases} F_1(\alpha_1, \alpha_2) = \frac{p_1}{p} \cos(\alpha_1) + \frac{p_2}{p} \cos(\alpha_2) = m\\ F_2(\alpha_1, \alpha_2) = \frac{p_1}{p} \cos(5\alpha_1) + \frac{p_2}{p} \cos(5\alpha_2) = 0 \end{cases}$$
(6)

The constraint $0 \le \alpha_1 < \alpha_2 < \frac{\pi}{2}$ is imposed.

2) Second Part of the Method: After the application of the first part, based on the graphical analysis, the proposed method involves the identification of the control angles as a function of the modulation index. The idea is to construct two Lagrange polynomials $P_{v,k}(m)k = 1$, 2, associated to each angle, of degree v, where v + 1 is the number of modulation index values considered, in which the switching angles have been obtained graphically. It is well known that the Lagrange polynomials are expressed as:

$$P_{\nu,1}(m) = \sum_{i=0}^{\nu} l_i(m) \alpha_1(m_i)$$
(7)

$$P_{\nu,2}(m) = \sum_{i=0}^{\nu} l_i(m) \alpha_2(m_i)$$
(8)

$$l_i(m) = \frac{\prod_{j=0, j \neq i}^{v} (m - m_j)}{\prod_{j=0, j \neq i}^{v} (m_i - m_j)}, \ i = 0, \dots, v$$
(9)

where $m_0 < m_1 \cdots < m_v$ are the modulation index values at which the switching angles have been graphically obtained. The

BEST CASES IDENTIFIED IN [29] p_1 p_2 m $\alpha_1 [rad]$ $\alpha_2 [rad]$ THD [%] \mathcal{D} 0.9 0.6 0.4 0.1758 0.6871 9.86 0.8 0.6 0.4 0.3227 0.9552 11.80 0.7 0.4 0.6 0.3858 0.9896 12.99

1.0882

16.29

TABLE III

TABLE IV GRID CODES EN 50160 AND CIGRE WG 36-05

0.6369

	Odd harmonics				Even harmonics	
Not mu	Not multiple of 3		Multiple of 3			
n	l_n (%)	n	<i>l</i> _n (%)	n	l_n (%)	
5	6	3	5	2	2	
7	5	9	1.5	4	1	
11	3.5	15	0.5	610	0.5	
13	3	21	0.5	>10	0.2	
17	2	>21	0.2			
19-23-25	1.5					
>25	0.2+32.5/n					

switching angles as a function of m are:

$$\alpha_{v,1}(m) = P_{v,1}(m) + e_{v,1}(m) \tag{10}$$

$$\alpha_{\nu,2}(m) = P_{\nu,2}(m) + e_{\nu,2}(m) \tag{11}$$

where $e_{v,1}(m)$ and $e_{v,2}(m)$ are the errors of Lagrange polynomial, expressed as:

$$|e_{v,k}(m)| \le \frac{M}{(v+1)!} (m_v - m_0)^{v+1}$$
(12)

where M is a positive number. In the proposed application $\alpha_1(m)$ is approximated with $P_{v,1}(m)$ and $\alpha_2(m)$ is approximated by $P_{v,2}(m)$. Of course, due to these errors, the obtained resulting switching angles will be able to perform a significant attenuation of the 5th harmonic instead of eliminating it.

III. APPLICATION OF THE PROPOSED METHOD

As previously described, the proposed method focuses on the graphical analysis and the construction of the Lagrange polynomials. However, a proper choice of the stress partitions is necessary. In order to find proper values of the stress partitions, several case studies with different stress partitions have been addressed, as discussed in [29]. In detail, the graphical analysis showed that there are solutions only in the range of modulation index from 0.6 to 0.9. The authors also identified four best cases, which are summarized in Table III. For the purpose of investigation, the best cases summarized in Table III have been analyzed in the frequency domain and the harmonics have been compared with the limits of the EN 50160 and CIGRE WG 36-05 grid codes given in Table IV. In detail, the harmonic analysis of the best cases is shown in Fig. 2 for each case of Table III.

It is interesting to note that the proposed method makes it possible to eliminate the selected harmonic, in this case the fifth, and also to reduce other harmonics. Moreover, in all cases the



Fig. 2. Comparison of the voltage harmonics spectra and grid codes EN 50160 and CIGRE WG 36-05.



Fig. 3. Obtained solutions.

seventh harmonic is also lower than the limits given in the EN 50160 and CIGRE WG 36-05 grid codes. The voltage partitions chosen for this study are $\frac{p_1}{p} = 0.6$ and $\frac{p_2}{p} = 0.4$, which allow the lowest THD% values to be obtained, as shown in Table III. The graphical analysis is applied and the intersection points shown in Fig 3(a) and summarized in Table V are identified. In detail, Fig. 3(a) shows the valid solutions, marked with black dots, obtained when $\frac{p_1}{p} = 0.6$, $\frac{p_2}{p} = 0.4$ and m = 0.9, 0.8, 0.7, 0.6. The other points of intersection (green dots) give the solutions when $\frac{p_1}{p} = 0.4$, $\frac{p_2}{p} = 0.6$, therefore, they are not valid. Considering the values given in Table III, the Lagrange polynomials of the third order have been identified and expressed as:

$$\alpha_1 \simeq 24.95 \, m^3 - 61.235 \, m^2 + 48.489 \, m - 12.0525 \tag{13}$$

0.6

0.4

0.6

TABLE V SWITCHING ANGLES OBTAINED WITH $\frac{p_1}{p} = 0.6$, $\frac{p_2}{p} = 0.4$



Fig. 4. THD% vs. modulation index for $\frac{p_1}{p} = 0.6$, $\frac{p_2}{p} = 0.4$.

$$\alpha_2 \simeq -23.83 \, m^3 + 54.3 \, m^2 - 43.272 \, m + 13.024 \tag{14}$$

Fig. 3(b) shows the control angle trends obtained by the Lagrange approximation. In this way the control angles are defined in a continuous range of the modulation index from 0.6 to 0.9. However, the fifth harmonic cannot be eliminated in the whole range of the modulation index due to the approximation strategy used. In the next section, a detailed simulation analysis is reported where the results confirm the effectiveness of the proposed method.

IV. SIMULATION ANALYSIS

In order to validate the effectiveness of the proposed method, a detailed simulation analysis was carried out in MatLab/PLECS. Specifically, a circuit model of a three-phase five-level CHB inverter has been implemented and the simulation analysis was focused on the harmonic analysis of the output voltage waveforms. The simulation was performed considering p = 20 which results in a total voltage V_{dc} equal to 80 V. Therefore, the voltage levels were set at $V_{dc1} = 48$ V ($\frac{p_1}{p} = 0.6$) and $V_{dc2} = 32$ V ($\frac{p_2}{p} = 0.4$). Fig. 4 shows the THD% trend, expressed in percent, against the modulation index.

It should be noted that the lowest value of the THD%, lower then 10%, was recorded for modulation index equal to 0.9. Furthermore, the THD% values increase as the modulation index decreases, with the maximum value being 27% for a modulation index of 0.615. Fig. 5 shows the first voltage harmonic versus the modulation index. The first voltage harmonic shows a linear trend in the range of the modulation index considered. As is well known, this is an interesting feature from a control point of view, as it allows the use of common control strategies using PI regulators. Fig. 6 shows the amplitudes of the lower



Fig. 5. Fundamental voltage harmonic vs. modulation index.



Fig. 6. Comparison among low-order harmonics vs. modulation index: fifth (blue curve), seventh (orange curve), eleventh (yellow curve) and thirteenth (purple curve).

voltage harmonics, from the fifth to the thirteenth, versus the modulation index expressed as a percentage of the first voltage harmonic. As previously described, the proposed algorithm is set to eliminate the fifth harmonic. As shown in Fig. 6, the fifth harmonic (blue curve) is eliminated only in accordance with the modulation index values chosen for the construction of the Lagrange polynomials. In the other points, the fifth harmonic is significantly attenuated and can be considered negligible. Thus, this result confirms the effectiveness of the proposed algorithm, which shows a good attenuation of the selected harmonic in all ranges of the modulation index. For the other harmonics, only the seventh harmonic (orange curve) rises above 10% as the modulation index decreases. The seventh harmonic reaches the 23% when the modulation index is equal to 0.635. In order to demonstrate the effectiveness of the proposed method and its higher accuracy, a comparative analysis has also been carried out taking into account the linear interpolation. Fig. 7 shows the comparison between the control angles and fifth harmonic values obtained with the proposed Lagrange method (blue curve) and the linear interpolation method (red curve). It should be noted that the control angle trends show little difference between the two different approaches. However, the proposed method allows lower fifth harmonic values to be obtained, demonstrating its superiority over linear interpolation.



Fig. 7. Comparison between the proposed Lagrange interpolation method and linear interpolation method on the fifth harmonic elimination.

TABLE VI MAIN PARAMETERS OF THE DIGIPOWER CHB INVERTER EMPLOYING MOSFET IRFB4115PBF

Quantity	Symbol	Value
Voltage	$V_{\rm dss}$	150 V
Resistance	R_{DSon}	$9.3m\Omega$
Current	I_D	104 A
Turn on delay	T_{Don}	18 ns
Rise time	T_R	73 ns
Turn off delay	$T_{D \text{off}}$	41 ns
Fall time	T_F	39 ns
Reversal	<i>T</i>	0.0
recovery	T_{RR}	86 ns

 TABLE VII

 MAIN DATA OF DC POWER SUPPLY RSP-2400

Section	Quantity Value		
	dc Voltage	48 V	
Outmut	Rated Current	50 A	
Output	Rated Power	2400 W	
	Voltage rise time	80 ms (Max) at full load	
	Voltage range ac	$180-264~\mathrm{V}$	
Inout	Frequency range	47-63 Hz	
mput	Efficiency	91.5%	
	ac current	12 A/230 VAC	

V. EXPERIMENTAL VALIDATIONS

In order to experimentally validate the proposed SHE method, a test bench has been set up at the SDESLAB of the University of Palermo. It consists of:

- a three-phase, five-level CHB inverter obtained by assembling six H-bridges controlled by a control board using an Intel-Altera Cyclone III FPGA programmed in VHDL with 32-bit arithmetic. The whole system was designed by DigiPower. The power rating of each H-bridge, using power MOSFETs, is 5 kW, giving a total power rating of 30 kW. The main specifications are listed in Table VI;
- six RSP-2400 programmable DC power supplies, whose main specifications are listed in the Table VII;



Fig. 8. Schematic representation of the test bench.

- a passive electric load RL (constantan rheostats with $R = 20 \Omega$ and L = 3 mH);
- a Teledyne LeCroy MDA 8038HD oscilloscope equipped with Teledyne Lecroy HVD3106 A 1 kV, 120 MHz high voltage differential probes and Teledyne Lecroy CP030 A AC/DC, 30 A RMS, 50 MHz high sensitivity current probes;
- two Yokogawa power meters (WT 330 and WT 130).

Fig. 8 shows a schematic representation of the implemented system, including the measurement circuit. Experimental validation was carried out through a series of tests. In particular, no-load and load tests with the RL load have been carried out to validate the proposed approach by considering the phase voltage THD% as a comparative quantity. Furthermore, the FPGA hardware resources required by the proposed algorithm are compared with those obtained by using algorithms based on Look-Up Tables (LUTs) that store the switching angles.

A. Harmonic Analysis

In this subsection a detailed analysis of the voltage harmonics is reported. As shown in the simulation analysis, the THD% values and the amplitudes of the lower harmonics were used as comparison tools. As described in [29], several combinations of control angles and voltage partitions have been identified from the graphical analysis and the best cases are summarized in Table III for each value of the modulation index considered.

Fig. 9 shows the experimental phase voltages, referred to the star point voltage of the load, and the corresponding best-case harmonic spectra. The voltage scale has been set to 50 V/div with a time scale of 5 ms/div, while the harmonic spectrum has been set with a voltage and frequency scale of 20 V/div and 200 Hz/div respectively.



Fig. 9. Best case experimental results: phase voltages (green, red and blue curves) and corresponding voltage harmonic spectra (blue bar graph) for $\frac{p_1}{p} = 0.6$, $\frac{p_2}{p} = 0.4$.



Fig. 10. Comparison of simulation and experimental harmonics spectra for $\frac{p_1}{p} = 0.6$, $\frac{p_2}{p} = 0.4$ and m = 0.6.

It should be noted that the fifth harmonic is eliminated in all the cases considered, confirming the effectiveness of the proposed method. Figs. 10 and 11 show the comparison of simulation and experimental harmonic spectra; the red line represents the harmonic limits of the grid codes (EN 50160 and CIGRE WG 36-05). The effectiveness of the proposed method is confirmed. It is also interesting to note that the seventh harmonic is lower in all cases with respect to the grid code limits, while the eleventh harmonic is lower for modulation index values equal to 0.7 and 0.9. In terms of THD%, the experimental results confirm the effectiveness of the proposed method, as shown in Fig 12. In the second part of the harmonic analysis, the effectiveness of the control angle evaluation with Lagrange polynomial approximations was validated. Specifically, the third-order polynomial



Fig. 11. Comparison of simulation and experimental harmonics spectra for $\frac{p_1}{p} = 0.6$, $\frac{p_2}{p} = 0.4$ and m = 0.8.



Fig. 12. Comparison of simulation and experimental THD% values of the best cases summarised in Table III.



Fig. 13. Comparison between simulation and experimental results of THD% and fundamental voltage harmonics both versus modulation index.



Fig. 14. Comparison between simulation and experimental results of low order harmonics and harmonic limits (grid codes EN 50160 and CIGRE WG 36-05) vs. modulation index.

approximation (7), (8), to evaluate α_1 and α_2 in real time has been implemented in an FPGA-based control board. Thus, the experimental validation has been carried out by considering several values of the modulation index in the range [0.6, 0.9]and by considering three values of the fundamental frequency: 50 Hz, 100 Hz and 150 Hz, respectively. Fig. 13 shows the comparison between the simulation (blue curve) and the experimental results (crosses) in terms of THD% vs. modulation index and fundamental voltage harmonic vs. modulation index. The effectiveness of the proposed method in the considered modulation index range and for each fundamental frequency is confirmed. Fig. 14 shows the comparison between simulation (blue curves) and experimental results (crosses) of the low order harmonics, from fifth to thirteenth, vs. modulation index and for each considered value of the fundamental frequency. It should be noted that the experimental results show the same trend as the simulated values. As expected, the fifth harmonic is significantly mitigated and the relative value is below the grid code limit (red line) in all ranges of the modulation index and for each value of the fundamental frequency. It is also interesting to note that other harmonics are also below the grid code limit only for certain values of the modulation index. Again, the differences are mainly due to the numerical approximation of the control angles. Furthermore, the experimental analysis has been extended to validate the comparison of the proposed Lagrange method with linear interpolation. Fig. 15 shows the comparison between the



Fig. 15. Comparison of simulation and experimental results of the fifth harmonic vs. modulation index.

simulation and the experimental results of the fifth harmonic values obtained experimentally. It is interesting to note that the experimental tests confirm the superiority of the proposed method observed in the simulation analysis. In order to demonstrate the effectiveness of the proposed method also for different voltage inputs, additional experimental tests were carried out. In detail, three sets of voltage inputs were considered, keeping the same voltage partitions $(\frac{p_1}{p} = 0.6, \frac{p_2}{p} = 0.4)$: $V_{dc1} = 36$ V and $V_{dc2} = 24$ V, $V_{dc1} = 48$ V and $V_{dc2} = 32$ V, and $V_{dc1} = 54$ V and $V_{dc2} = 36$ V. Fig. 16 shows the experimental phase voltages and corresponding harmonic spectra, obtained with the scope for a modulation index value equal to 0.75, for different dc input voltages. As shown in Fig. 16, the proposed method is applicable for different values of the voltage input, obviously, it is necessary to keep the voltage distribution $\frac{p_1}{p} = 0.6$, $\frac{p_2}{p} = 0.4$.

B. Efficiency Analysis

As previously discussed, the purpose of the proposed algorithm is to eliminate the fifth voltage harmonic. However, the conversion efficiency plays an important role in high power applications. Using a passive load, the input DC power and output AC power have been measured and the conversion efficiency has been evaluated for different values of the modulation index and for each value of the fundamental frequency considered. Fig. 17 shows the trend of the conversion efficiency versus the modulation index for each value of the fundamental frequency. It is interesting to note that the conversion efficiency shows a constant trend in all ranges of the modulation index and for each value of the fundamental frequency. This is an interesting result in all applications where a variable modulation index is required, such as variable load/speed electrical drive applications, and confirms the high efficiency inverter operation of the proposed SHE method.

C. Dynamic Analysis

The dynamic analysis is concerned with measuring the total execution time to obtain the desired output voltage by calculating the control angles in real time. The control algorithm, properly designed for experimental validation, was implemented in the DigiPower FPGA-based control board using the VHDL



(c) $V_{dc1} = 54$ V and $V_{dc2} = 36$ V

Fig. 16. Experimental phase voltages and corresponding harmonic spectra for different input voltages.



Fig. 17. Conversion efficiency vs. modulation index for each of the fundamental frequencies taken into account.



Fig. 18. Block diagram of the control algorithm implemented in Quartus II environment.

programming language. The FPGA is an ALTERA Cyclone III and the control algorithm was developed in the Quartus II environment. Fig. 18 shows a simplified block diagram of the implemented control algorithm.

The Lagrange Polynomials block, clocked at 1 MHz, allows the solution of the polynomial equations to calculate the control angles α_1 and α_2 . This task is performed every 2 μ s using 32-bit signed integer variables, where the modulation index m is the input variable and α_1 and α_2 are the output variables, which are computed in the same time. The *Carrier Generator* block returns the reference gate signals in almost the same time, so, both blocks are executed simultaneously. Note that their execution times were estimated at an early stage by simulation analysis using the



Fig. 19. Experimental dynamic analysis to change the modulation index from 0.6 to 0.9: (a) voltage (blue curve), current (purple curve) and trigger (cyan curve) signal dynamic behaviour, (b) zoomed view.

ModelSim Altera environment, and then adopted in the actual system. Finally, the Comparator and Dead-time block allows the gate signals for the converter to be generated by adding a dead time of 500 ns. The total execution time, measured when imposing a step change of m from 0.6 to 0.9 is 5 μ s. Fig. 19(a) shows the load phase voltage (blue curve), load phase current (purple curve) and the trigger signal (cyan curve) which has been used to locate the modulation index step change event in time. Note that when the trigger signal changes state, the voltage also appears to change abruptly at the same time. In fact, on this time scale, the delay due to the execution time cannot be appreciated and it is necessary to zoom in on the scope recording. In fact, Fig. 19(b) shows the zoomed version of the same event in order to evaluate with accuracy the delay between the trigger signal and the effect of the modulation index change on the voltage. This change coincides with the execution time of the algorithm that has been evaluated by means of the vertical cursors and is equal to 5.24 μ s, confirming the correctness of the value estimated in ModelSim-Altera. In order to validate the stability of the proposed method in the case of sudden load changes, an additional dynamic load change test was carried out, capturing the transient of the voltages and currents. Fig. 20 shows the voltage and current transients for a modulation index m equal to 0.75 and a sudden load change. It should be noted that the system shows the same voltage trends with the frequency spectrum, as shown in the corresponding harmonic spectra before and after the load change transient. The same result was obtained for the other modulation index values.

D. Hardware Resources Comparative Analysis

In order to demonstrate the superiority of the proposed approach, an experimental comparison has been carried out in terms of hardware resource requirements of the FPGA-based control board (Cyclone III - EP3C40Q240C8). In detail, the comparative analysis is carried out by considering the proposed algorithm, based on the resolution of Lagrange polynomials in real time operation, and four different algorithms in which the control angles are precalculated and allocated in a read only memory (ROM), as shown in Fig. 21. In Fig. 21, the control angles are precalculated with a resolution of 32 bits and four different cases have been considered in terms of the number of ROM addresses. In fact, the number of ROM addresses represents the discretization of the modulation index range, which includes 4, 8, 16 and 32 values respectively. When comparing Fig. 18 and Fig. 21, it should be noted that only the evaluation of the control angles is different. The hardware requirements are summarized in Table VIII for all cases considered. It is interesting to note that although the proposed algorithm has higher hardware requirements in terms of total logic elements, total combinational functions and dedicated logic registers, the total memory bit required are 0. This result confirms the superiority of the proposed algorithm because the control angles can be evaluated within the modulation index range where the solutions exist, without using preallocated memory. Although the reported memory values are not high compared to the available memory, it should be noticed that for topologies with a higher number



Fig. 20. Experimental dynamic load change and corresponding voltage harmonic spectra for m = 0.75.



Fig. 21. Block diagram of the control algorithm implemented in Quartus II environment based on ROM.

TABLE VIII HARDWARE REQUIREMENTS COMPARISON

	Total logic	Total combi-	Dedicated	Total
	Flamanta	national	logic	memory
	Elements	functions	registers	bits [bit]
ROM 4 x	662 /	662 / 20600	258 /	512 /
32 bit	39600	002 / 39000	39600	1161216
ROM 8 x	662 /	((2) 1 20(00	258 /	1024 /
32 bit	39600	002 / 39000	39600	1161216
ROM 16	662 /	((2))20(00	258 /	2048 /
x 32 bit	39600	662 / 39600	39600	1161216
ROM 32	662 /	((2))20(00)	258 /	4096 /
x 32 bit	39600	002 / 39000	39600	1161216
Proposed	1474 /	1472 / 20600	328 /	0/11/1010
algorithm	39600	14737 39000	39600	0 / 1101210

of levels, the LUT dimension increases significantly due to the increase in the number of switching angles.

VI. CONCLUSION

A new SHE technique has been proposed for 5-level CHB inverters supplied by unbalanced DC sources. The graphical analysis has allowed us to find the switching angles for fixed modulation indeces and, a third-order interpolating Lagrange polynomial has been used to extend the proposed approach to any modulation index within the interesting interval. The performance of the proposed SHE technique has been analyzed in simulation and several experimental investigations have been carried out to show the effectiveness of the proposed approach. A detailed dynamic analysis has been carried out by demonstrating the optimal real-time operation of the proposed algorithm.

REFERENCES

- B. Singh, R. Kumar, and P. Kant, "Adjustable speed induction motor drive fed by 13-Level cascaded inverter and 54-Pulse converter," *IEEE Trans. Ind. Appl.*, vol. 58, no. 1, pp. 890–900, Jan./Feb. 2022.
- [2] A. Edpuganti and A. K. Rathore, "A survey of low switching frequency modulation techniques for medium-voltage multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 5, pp. 4212–4228, Sep./Oct. 2015.
- [3] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of modulation and control techniques for multilevel inverters in traction applications," *IEEE Access*, vol. 9, pp. 24187–24204, 2021.
- [4] A. F. Abouzeid et al., "Control strategies for induction motors in railway traction applications," *Energies*, vol. 13, 2020, Art. no. 700.
- [5] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.
- [6] R. P. Aguilera et al., "Selective harmonic elimination model predictive control for multilevel power converters," *IEEE Trans. Pow. Electron.*, vol. 32, no. 3, pp. 2416–2426, Mar. 2017.

- [7] C. Buccella, C. Cecati, M. G. Cimoroni, G. Kulothungan, A. Edpuganti, and A. Kumar Rathore, "A selective harmonic elimination method for five-level converters for distributed generation," *IEEE J. Emerg. Select. Topic Power Electron.*, vol. 5, no. 2, pp. 775–783, Jun. 2017.
- [8] G. Schettino, A. O. Di Tommaso, R. Miceli, C. Nevoloso, G. Scaglione, and F. Viola, "Dead-time impact on the harmonic distortion and conversion efficiency in a three-phase five-level cascaded H-bridge inverter: Mathematical formulation and experimental analysis," *IEEE Access*, vol. 11, pp. 32399–32426, 2023.
- [9] G. S. Kulothungan, A. K. Rathore, J. Rodriguez, and D. Srinivasan, "Fundamental device switching frequency control of current-fed nine-level inverter for solar application," *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1839–1849, Mar./Apr. 2020.
- [10] Y. Zhang, Y. W. Li, N. R. Zargari, and Z. Cheng, "Improved selective harmonics elimination scheme with online harmonic compensation for high-power PWM converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3508–3517, Jul. 2015.
- [11] M. S. A. Dahidah, G. Konstantinou, and V. G. Agelidis, "A review of multilevel selective harmonic elimination PWM: Formulations, solving algorithms, implementation and applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4091–4106, Aug. 2015.
- [12] M. Ahmed, A. Sheir, and M. Orabi, "Real-time solution and implementation of selective harmonic elimination of seven-level multilevel inverter," *IEEE J. Emerg. Select. Topics Power Electron.*, vol. 5, no. 4, pp. 1700–1709, Dec. 2017.
- [13] M. A. Memon, S. Mekhilef, and M. Mubin, "Selective harmonic elimination in multilevel inverter using hybrid APSO algorithm," *IET Power Electron.*, vol. 11, no. 10, pp. 1673–1680, Aug. 2018.
- [14] M. Ahmed et al., "General mathematical solution for selective harmonic elimination," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4440–4456, Dec. 2020.
- [15] A. Kavousi, B. Vahidi, R. Salehi, M. K. Bakhshizadeh, N. Farokhnia, and S. H. Fathi, "Application of the bee algorithm for selective harmonic elimination strategy in multilevel inverters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1689–1696, Apr. 2012.
- [16] S. Padmanaban, C. Dhanamjayulu, and B. Khan, "Artificial neural network and Newton Raphson (ANN-NR) algorithm based selective harmonic elimination in cascaded multilevel inverter for PV applications," *IEEE Access*, vol. 9, pp. 75058–75070, 2021.
- [17] M. Sadoughi, A. Pourdadashnia, M. Farhadi-Kangarlu, and S. Galvani, "PSO-Optimized SHE-PWM technique in a cascaded H-bridge multilevel inverter for variable output voltage applications," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8065–8075, Jul. 2022.
- [18] C. Buccella et al., "Recursive selective harmonic elimination for multilevel inverters: Mathematical formulation and experimental validation," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 2, pp. 2178–2189, Apr. 2023.
- [19] Z. Ye et al., "New inter- and inner-phase power control method for cascaded H-bridge based on simplified PWM strategy," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8607–8623, Aug. 2020.
- [20] A. Kumar, D. Chatterjee, and A. Dasgupta, "Harmonic mitigation of cascaded multilevel inverter with non equal DC sources using Hybrid Newton Raphson Method," in *Proc. IEEE 4th Int. Conf. Power, Control & Embedded Syst.*, 2017, pp. 1–5.
- [21] K. Haghdar and H. A. Shayanfar, "Selective harmonic elimination with optimal DC sources in multilevel inverters using generalized pattern search," *IEEE Trans. Ind. Informat.*, vol. 14, no. 7, pp. 3124–3131, Jul. 2018.
- [22] K. Haghdar, "Optimal DC source influence on selective harmonic elimination in multilevel inverters using teaching–learning-based optimization," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 942–949, Feb. 2020.
- [23] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010.
- [24] A. Marzoughi, R. Burgos, and D. Boroyevich, "Investigating impact of emerging medium-voltage SiC MOSFETs on medium-voltage high-power industrial motor drives," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1371–1387, Jun. 2019.
- [25] C. Buccella, M. G. Cimoroni, H. Latafat, G. Graditi, and R. Yang, "Selective harmonic elimination in a seven level cascaded multilevel inverter based on graphical analysis," in *Proc. IEEE 42nd Annu. Conf. Ind. Electron. Soc.*, 2016, pp. 2563–2568.

- [26] P. Kalkal and A. V. Ravi Teja, "An approach in selective harmonic mitigation technique for reduction of multiple harmonics with only two switchings per quarter," in *Proc. IEEE 48th Annu. Conf. Ind. Electron. Soc.*, 2022 pp. 1–6.
- [27] A. Kumar, P. Kalkal, and A. V. R. Teja, "A graphical approach in selective harmonic elimination for simultaneous reduction of multiple harmonics and overall THD," in *Proc. IEEE 48th Annu. Conf. Ind. Electron. Soc.*, 2022 pp. 1–6.
- [28] C. Wang, Q. Zhang, W. Yu, and K. Yang, "A comprehensive review of solving selective harmonic elimination problem with algebraic algorithms," *IEEE Trans. Power Electron.*, vol. 39, no. 1, pp. 850–868, Jan. 2024.
- [29] C. Buccella et al., "Investigation about selective harmonic elimination in unbalanced multilevel inverters," in *Proc. IEEE 21st Mediterranean Electrotechnical Conf.*, 2022, pp. 1235–1240.
- [30] CENELEC EN 50160, "Voltage characteristics of electricity supplied by public distribution systems," 2001.
- [31] CIGRE WG 36-05, "Harmonics, characteristic parameters, methods of study, estimates of existing values in the network," *Electra*, vol. 77, pp. 35–54, 1981.



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