A Partial Active Gate Control for Improvement of a Trade-Off Relation Between Surge Voltage and Efficiency in a Three-Phase Inverter

Van-Long Pham, *Member, IEEE*, Hidemine Obara, *Member, IEEE*, and Katsuhiro Hata, *Member, IEEE*

***Abstract*—This paper presents a control method of fully digital active gate drivers in a three-phase inverter to simultaneously realize surge voltage reduction and efficiency enhancement. Generally, the surge voltages of power devices occur at each switching, and they are determined depending on the operation mode including switching schemes and three-phase current directions. The active gate control technology can change the gate drive current and switching speed in detail in every gate control period which is usually quite shorter than the switching period, and it contributes to suppressing surge voltages. However, offline optimization of the active gate driving pattern considering operating conditions is usually complicated and takes a long time to find a better gate pattern. In this paper, a partial active gate control method without detailed pattern optimization is proposed. In the proposed method, the active gate driving patterns of fully six gate drivers are suitably changed according to the phase angle of the three-phase current to minimize the highest surge voltage and the switching loss in a fundamental period without any optimization. A prototype of the three-phase inverter using a 6-in-1 SiC power module and six digital active gate driver ICs was developed to verify the improvement effect of the proposed active gate control. Based on an analysis result of operation modes and surge voltages in the three-phase inverter, a suitable active gate control method was clarified considering each operating region in one ac cycle. It has been verified that the proposed partial active gate control contributes to reducing the highest surge voltage, fixing a high efficiency.**

***Index Terms*—Active gate driver, digital control, efficiency, SiC-mosfet, surge voltage, three-phase inverter.**

I. Introduction

WIDEBAND-GAP power devices such as Silicon carbide (SiC) and Gallium Nitride (GaN) devices are widely used in high-efficiency and high-power-density applications [1], [2], [3]. However, a faster switching capability causes high surge voltage and switching loss due to the effect of stray capacitances and inductances, especially in motor drive applications [4], [5]. Adjusting the switching speed and the gate driving technique is essential to improve the performance of the power circuit [6]. An active gate drive (AGD) technology is one of the key innovations to improve the trade-off relation between the surge voltage and switching loss of power devices [7], [8], [9], [10], [11], [12], [13], [14], [15]. A fully digital AGD shows the advantage compared with an analog active gate drive in a programmable function and finding suitable gate patterns after implementation [8], [9], [10], [11]. So far, there are some researches regarding fully digital AGD to improve the performance of power converters. The digital AGD was applied to a chopper circuit and half-bridge inverter in [10], [11]. The single-phase full-bridge inverter with only two of four (2/4) digital AGDs was discussed in [12], [13]. A three-phase inverter with only two of six (2/6) digital AGDs was verified in [14]. In a fully digital active gate driver, there is a high degree of freedom to determine even one switching waveform. The active gate driver with 63-level variable drivability has been reported and has to be selected one gate pattern from 63^n patterns when the number of the control slots (time resolution of the gate control) is n. To find an optimal gate pattern, a lot of offline switching tests and optimization algorithms such as simulated annealing (SA) [10], particle swarm optimization (PSO) [12], [13], [14], recurrent neural network (RNN) [15], and genetic algorithm (GA) [16] are needed. Recent developments of various active gate drivers including the optimization methods have been summarized in [17]. In a practical implementation, the requirement of such complex offline optimization may become a bottleneck. In addition, most of the studies on the active gate drive focus on one switching trajectory, and there are a few studies focusing on continuous operations such as ac fundamental period in power converters with active gate control [11], [12], [13], [14].

In this paper, six (6/6) fully digital AGD ICs are applied for a three-phase inverter in a motor drive application. The first step for the challenge of using individual gate patterns for all six AGD ICs to overcome the high complexity is started. When six AGD ICs are used individually, a further advanced gate control method utilizing a higher degree of freedom can be applied. In this study, the gate driving patterns are suitably changed considering the three-phase currents to improve the

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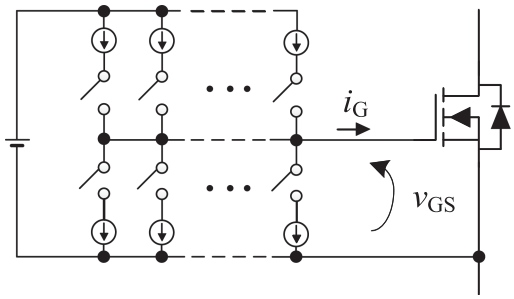


Fig. 1. Simple model of the digital active gate driver.

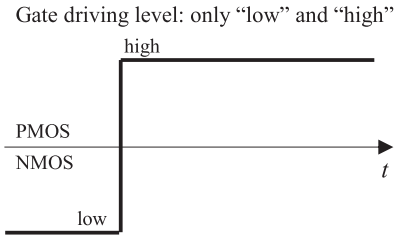


Fig. 2. Normal gate drive.

highest surge voltage and efficiency in an ac fundamental period without any gate pattern optimization. In this article, based on the conference paper [18], a detailed analysis of operation modes in the three-phase inverter and surge voltages is discussed, and its result reflects to the proposed active gate control method. The design and implementation of the proposed control in a prototype three-phase inverter with the six fully digital AGDs are presented, and the validity has been confirmed in experiments.

II. Fully Digital Active Gate Driver

In this work, laboratory-developed fully digital active gate driver ICs with parallel connected 63 CMOS drivers are used, and they can be digitally controlled to change the number of on-state CMOS, as shown in Fig. 1. In the proposed fully digital AGD IC, the input signals are six bits to control 63 PMOSs and six bits to control 63 NMOSs. The PMOSs and NMOSs are used for turn-on and -off, respectively, and the number of the on-state PMOSs and NMOSs are expressed by positive and negative numbers, respectively. Therefore, the gate drivability can be controlled between -63-level to 63-level in every clock period using the FPGA, and the number of time slots should be tuned considering the switching characteristics of power devices. This operation is equivalent to changing the gate resistance instantaneously in the general gate drivers. Figs. 2 and 3 show the conceptual drawings of the gate driving. Fig. 2 shows the general gate drive, which always uses low or high-level constant driving. This means that the general gate driver utilizes only one degree of freedom in turn-on and turn-off, and the gate drivability can be changed by only a change in the gate resistance before circuit implementation. On the other hand, the fully digital AGD has multiple CMOS drivers connected in parallel, and it can finely change the gate drivability during switching transients by changing the number of the on-state CMOSs as shown in Fig. 3.

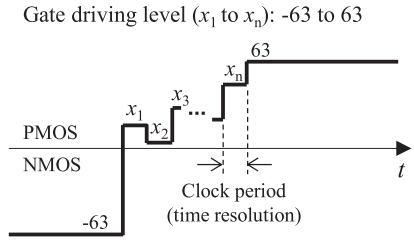


Fig. 3. Active gate drive (AGD).

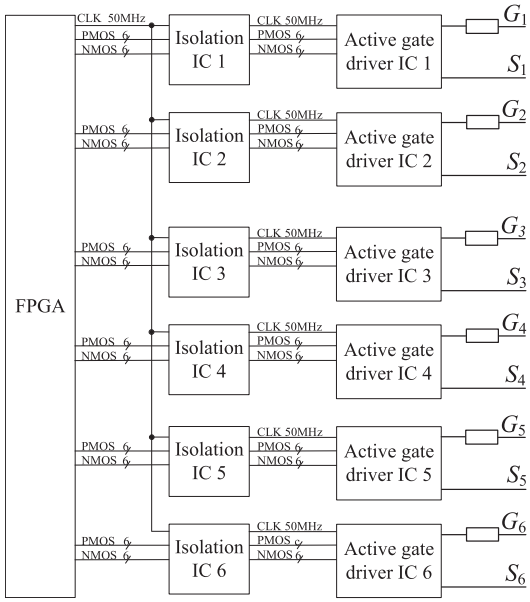


Fig. 4. Block diagram of proposed (6/6) fully digital AGD control in the three-phase inverter.

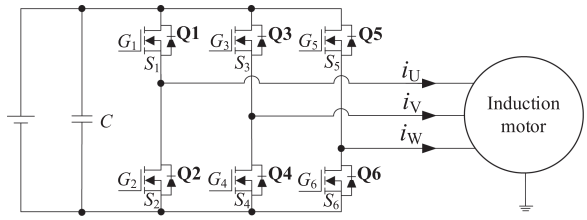


Fig. 5. Three-phase inverter for motor control.

III. Design of the Active Gate Driver for Three-Phase Inverter in Motor Drive Application

A. 6/6 Fully Digital AGD for Three-Phase Inverter

Fig. 4 shows the configuration of the fully digital AGDs and controllers where six (6/6) fully digital AGD ICs are used to control six gate voltage in the prototype of the three-phase PWM inverter. In the FPGA, six parallel digital signals control PMOSs and NMOSs, respectively for each AGD ICs. The digital signal isolation ICs are used between FPGA and AGD ICs. The 50 MHz clock signal is used to synchronize FPGA signals with the AGD ICs. The clock period of the slot (time resolution) for each driving pattern shown in Fig. 3 can be set as 20 ns at the shortest. Fig. 5 shows the circuit diagram of a three-phase inverter for motor drive application. In this study, an induction

TABLE I
COMPONENTS

AGD IC	Laboratory developed
Signal isolation IC	IL260-1E
FPGA	Cyclone V
SiC power module	FS55MR12W1M1H
PCB	Laboratory developed

TABLE II
EXPERIMENTAL PARAMETERS

Input DC voltage	282 V
Output AC voltage	200 V
Carrier frequency	2 kHz
Fundamental frequency	50 Hz
Dead time	800 ns

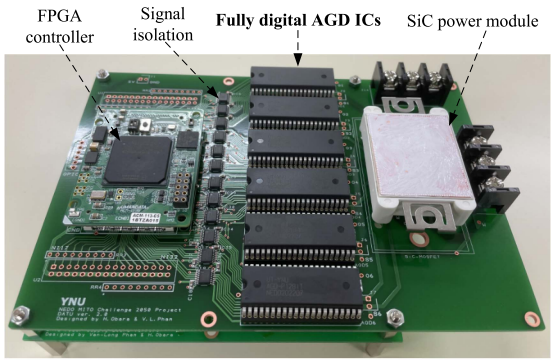


Fig. 6. Developed three-phase inverter with the fully digital active gate drive control.

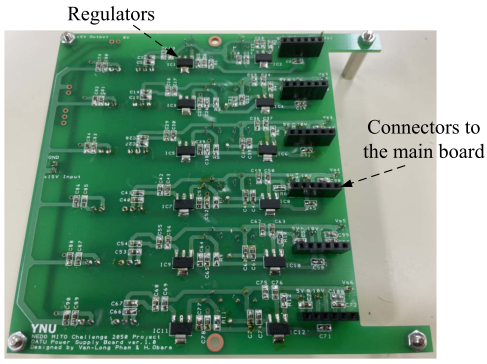


Fig. 7. Developed power supply board for the gate drivers.

motor is used as a load. The G_1 to G_6 and S_1 to S_6 in Fig. 4 are connected to the gate and source terminals of six power devices Q1 to Q6 in a power module in Fig. 5.

B. Design of the Experimental System

The components are listed in Table I. The experimental parameters are listed in Table II. Figs. 6 and 7 show the photograph of the prototype inverter. The 6-in-1 SiC power module FS55MR12W1M1H is used (In Fig. 6, a heatsink for the SiC module is removed to show the position of the

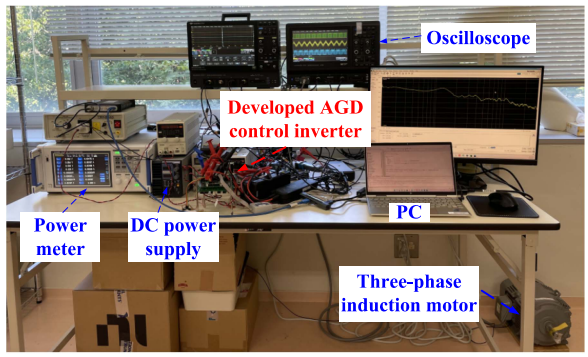


Fig. 8. Experimental system.

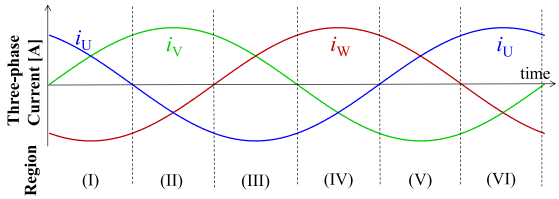


Fig. 9. Six regions based on the current directions in the three-phase inverter.

devices clearly.). Fig. 8 shows the overview of the experimental setup. The power meter Hioki PW6001 with the measurement accuracy of ±0.02%rdg.±0.03%f.s and the current sensor Hioki CT6862-05 with the measurement accuracy of ±0.03%rdg.±0.002%f.s are used. The total accuracy for measuring power is ±0.05%rdg.±0.032%f.s in this measurement. The oscilloscopes WaveSurfer 4024HD and HD4096 are used to measure the waveforms.

IV. BEHAVIOR OF SURGE VOLTAGES IN THE THREE-PHASE INVERTER

In this part, the behavior of surge voltages generated in the three-phase inverter is analyzed to clarify how the active gate control should be operated. Firstly, operation regions are divided into six regions with different three-phase current directions as shown in Fig. 9 because the behaviors of the surge voltages change depending on each current direction. For example, the region (I) has positive i_u and i_v, and negative i_w. The region (II) has positive i_v, and negative i_u and i_w. Because the direction and amplitude of the three-phase current affect to the operation modes, the behavior of surge voltages changes. Thus, it is considered that the active gate control pattern should be suitably selected according to the operation region.

Fig. 10 shows an example of all the drain-source voltage in the motor-fed three-phase inverter in one ac cycle. These waveforms were experimentally measured under no-load motor condition with a low power factor as shown in the Section III. From Fig. 10, it can be seen that the surge voltage changes depending on the region. For example, Fig. 10(a) shows that v_{DS1} has higher surge voltages in the regions (II), (IV) and (VI), and lower surge voltages in the other regions. By focusing on each surge voltage waveform, it is observed that there are two types of surge voltage as shown in Fig. 11. As the first one, the surge voltages

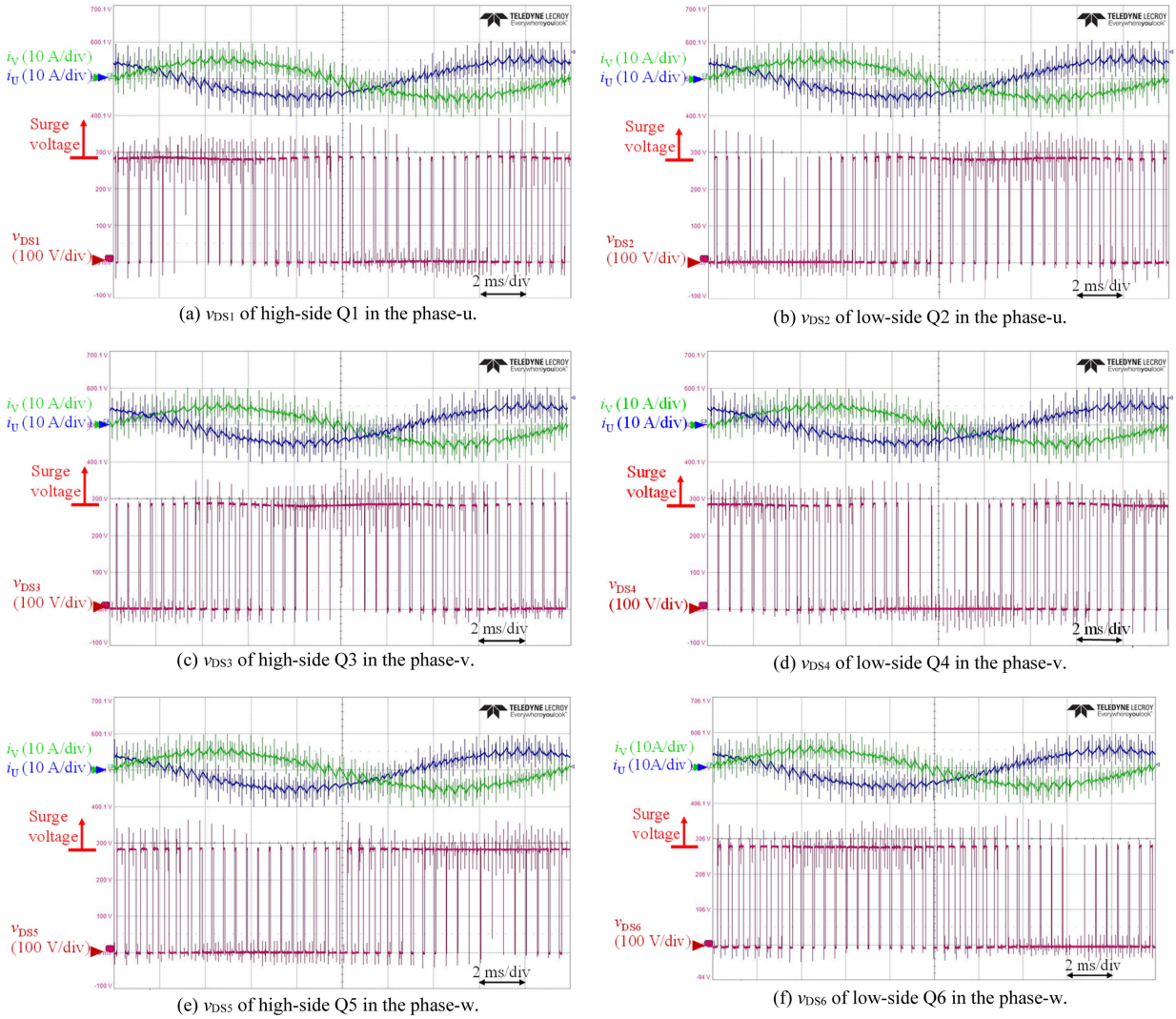


Fig. 10. Measured waveforms of each drain-source voltage in one AC cycle on three-phase inverter.

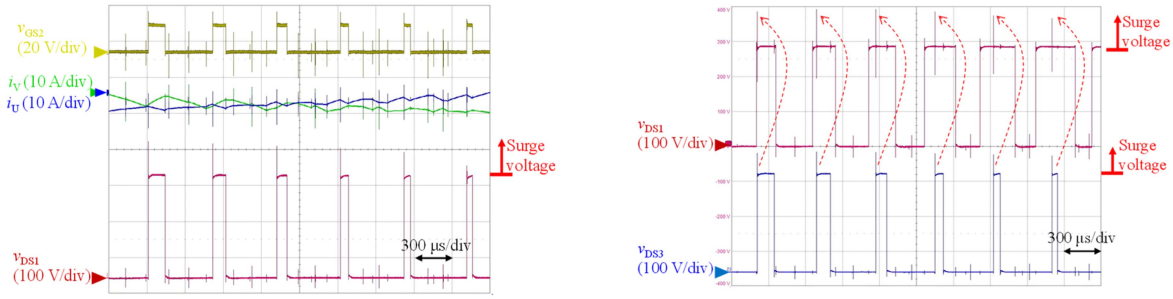


Fig. 11. Waveform of v_{DS1} in high-surge voltage regions.

occur at the current commutation instants in the phase itself. For example, in the phase-u, the surge voltage occurs in the v_{DS1} when the Q2 switches as shown in Fig. 11(a). These surge voltages tend to become higher during one ac cycle as shown in the region (IV) of Fig. 10. On the other hand, as the second type of surge voltages, they occur under the constant drain-source voltage without switching operation in the phase leg as shown in Fig. 11(b). This means that the surge voltages happen in the other phase leg, and they interact with the phase itself. For example, the surge voltages happened in the phase-v interact to the v_{DS1} as

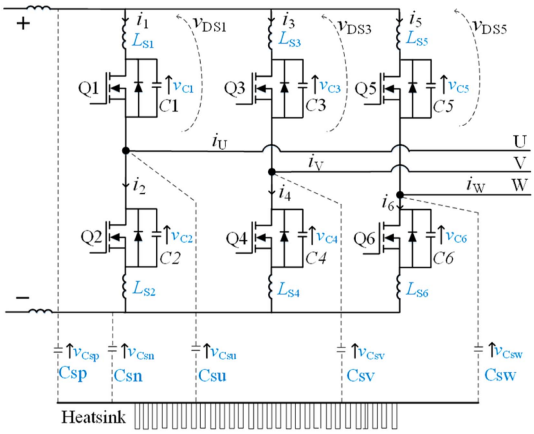


Fig. 12. Equivalent circuit model of the three-phase inverter included leakage capacitances.

shown in Fig. 11(b). From Fig. 10, these surge voltages also tend to highly affect to the whole drain-source voltage waveforms. The high-surge voltages on v_{DS3} and v_{DS5} occurred by the switching operations on each phase-v and phase-w, and they interact to the v_{DS1} in the phase-u in the regions (VI) and (II) as shown in Fig. 10(c) and (e), respectively. Detailed mechanisms of the surge voltage considering the current loops are analyzed in the next section.

V. Analysis of Surge Voltages in the Three-Phase Inverter

The general mechanism of the surge voltage generation in the inverter may be well-known. However, a detailed analysis of the surge and switching operation considering each phase leg has not been so important because gate driving and switching transient have not been able to be actively controlled so far even if it is clear. From the viewpoint of a design of the active gate control considering the detailed operation, a further detailed mechanism of the surge generation is analyzed in this paper. Particularly, the mechanism of the surge voltage generated in one phase leg is well known. For example, high surges happen in the drain-source voltage of the low-side MOSFET Q2 under the positive output current ($i_{out}>0$) and of the high-side MOSFET Q1 under the negative output current ($i_{out}<0$) due to the reverse recovery currents, as reported in some previous papers [11], [14]. However, even in the papers focusing on the active gate control technologies, it lacks a detailed analysis of the surge generation mechanism in the three-phase inverter. The surge voltages in the three-phase inverter with six individual active gate drivers depend on the direction, amplitude, and phase angle among three-phase currents as mentioned in the previous section.

Fig. 12 shows an equivalent circuit model of the three-phase inverter considering leakage capacitances between each MOSFET in a 6-in-1 power module and the heatsink. C_{su}, C_{sv}, and C_{sw} express leakage capacitances between each phase and the heatsink. C_{sp} is the leakage capacitance between the drain-pads of Q1, Q2, and Q_3 to the heatsink. C_{sn} is the leakage capacitance between the source-pads of Q1, Q2, and Q3 to the heatsink. The relationship among the output capacitances ($C1$–$C6$) of the MOSFETs, leakage capacitances, and stray inductances (L_{S1}–L_{S6}) can be simply expressed in the following equations.

The equations of the phase-u:

$$v_{Csp} = v_{C1} + L_{S1}\frac{di_1}{dt} + v_{Csu} \tag{1}$$

$$v_{Csp} = v_{C1} + L_{S1}\frac{di_1}{dt} + v_{C2} + L_{S2}\frac{di_2}{dt} + v_{Csn} \tag{2}$$

The equations of the phase-v:

$$v_{Csp} = v_{C3} + L_{S3}\frac{di_3}{dt} + v_{Csv} \tag{3}$$

$$v_{Csp} = v_{C3} + L_{S3}\frac{di_3}{dt} + v_{C5} + L_{S4}\frac{di_4}{dt} + v_{Csn} \tag{4}$$

The equations of the phase-w:

$$v_{Csp} = v_{C5} + L_{S5}\frac{di_5}{dt} + v_{Csw} \tag{5}$$

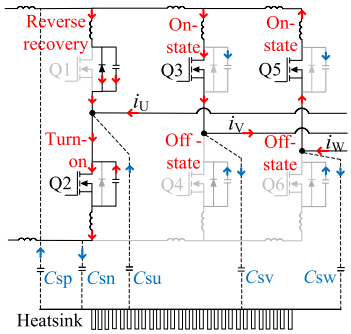
$$v_{Csp} = v_{C5} + L_{S5}\frac{di_5}{dt} + v_{C6} + L_{S6}\frac{di_6}{dt} + v_{Csn} \tag{6}$$

Firstly, the switching operation in the phase-u is analyzed. Then it can be expanded to the other MOSFETs Q3 and Q5 with phase shift conditions of the three-phase inverter. The low-side MOSFETs (Q2, Q4, Q6) have reverse conditions with high-side MOSFETs in the half of the ac cycle (shifted 180 degrees).

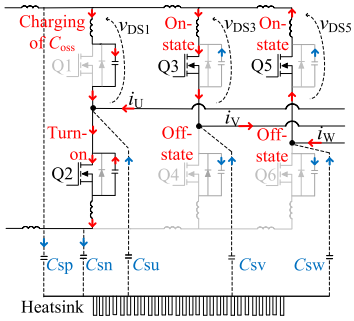
Figs. 13, 14, and 15 show the current paths in the three-phase inverter considering the leakage capacitances between the phase legs and heatsink potential during the regions (II), (III), and (IV) with higher surge voltages of Q1. In the schematics shown in Figs. 13, 14, and 15(a) and (b), the interaction currents between the three legs flowing through the leakage capacitances are shown by the blue arrows. The other currents such as the load currents and charge/discharge currents of the output capacitances in the MOSFETs are drawn in the red arrows. Figs. 13, 14, and 15(c) show examples of experimental waveforms in each switching transient under gate driving with 63-level constant gate pattern.

In the surge voltage waveforms shown in Fig. 10, it is seen that the regions (II), (III) and (IV) have a negative load current in phase-u, and the surge that occurs when Q2 switches is large. This surge voltage occurs inside the phase leg and is defined as a "phase surge" in this analysis. On the other hand, in the regions (I), (V), and (VI), the load current in the phase-u is positive, and the surge generated in the phase-v or phase-w interferes with the phase-u is large. This type of surge voltage is interacted from the other phase leg and is defined as an "interaction surge" in this analysis.

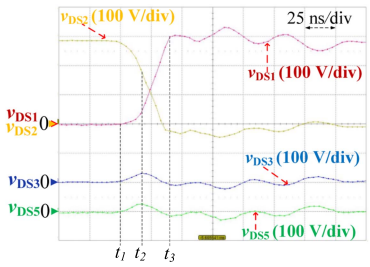
Figs. 13, 14, and 15 show the operation modes for the phase surges in the regions (II), (III) and (IV). In all three modes, the turn-on of Q2 results in charging the output capacitance C_{oss} of Q1, causing current to circulate to the other phase leg through the leakage capacitances and stray inductances around Q1. As the result, high-frequency surge voltages on v_{DS1} occur. In more detail, the region (IV) has the highest surge voltages, the region (III) has the second highest surges, and surge voltages in the region (II) are the smallest among the three regions. As



(a) The reverse recovery condition in Q1 by the turn-on of Q2.

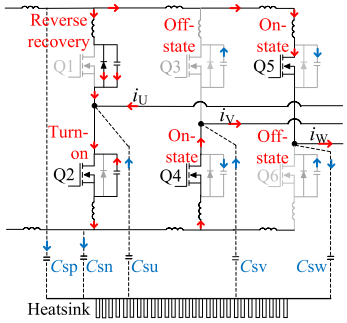


(b) Surge voltages in the phase-u interacts to the other phase legs with a small effect.

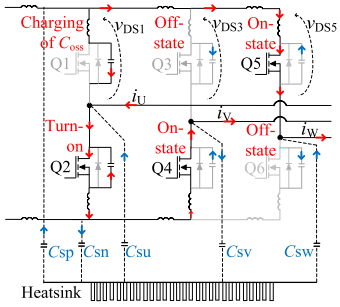


(c) Experimental waveforms of drain-source voltages in each MOSFET.

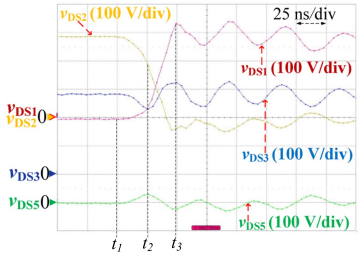
Fig. 13. Mechanism of the phase surge voltage on v_{DS1} in region (II).



(a) The reverse recovery condition in Q1 by the turn-on of Q2.



(b) Surge voltages in the phase-u interacts to the other phase legs with a middle effect.



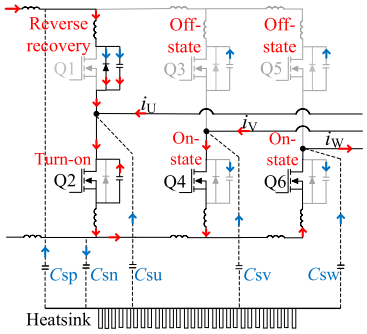
(c) Experimental waveforms of drain-source voltages in each MOSFET.

Fig. 14. Mechanism of the phase surge voltage on v_{DS1} in region (III).

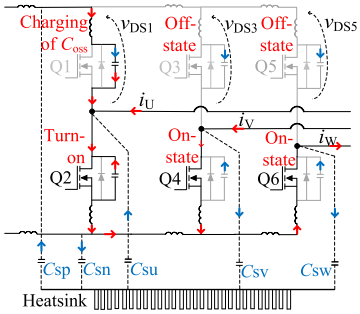
a result of the analysis, it is considered that these differences come from impedance differences of the surge current path including the leakage capacitances. In these modes, when the low-side MOSFET in the phase-v and/or phase-w is on-state, the impedance of the current path becomes smaller, and the surge current becomes larger. In the region (II) of Fig. 13, Q4 and Q6 are off-state, and the impedance of the surge current path is the largest among the three operating modes. In the region (III) of Fig. 14, Q6 is off-state but Q4 is on-state. Thus, a surge current happens in the phase-u flows to phase-v through the leakage capacitances, and a larger surge in v_{DS1} occurs than that in the region (II). From another point of view, this is an interaction surge in which phase-u switching affects v_{DS3} of Q3, and is the surge seen in the region (III) of v_{DS3} in Fig. 10(c). In the region (IV) of Fig. 15, both Q4 and Q6 are on-state, and it can be seen that the surge current flows from phase-u to phase-v and phase-w. As a result, the highest surge voltage occurs in the whole ac cycle. Since this is also an interaction surge to v_{DS3} and v_{DS5}, it can be seen that the surge voltages in the region (IV) of v_{DS3} and v_{DS5} in Fig. 10(c) and (e) become larger.

On the other hand, Figs. 16, 17, and 18 show the operation modes of regions (I), (V) and (VI) that affect v_{DS1} due to interaction surges. Fig. 16 shows the interaction surge to v_{DS1} due to the turn-on of Q6 in the phase-w. In this mode, Q2 is on-state, Q4 is off-state, and the surge current flows almost only in the phase-u. Thus, the surge itself becomes relatively lower. Fig. 17 shows also an interaction surge to v_{DS1} due to the turn-on of Q5. In this regard, Q1 is on-state for a long time, and most of the surge voltages occur as an undershoot during the period when Q1 is on-state, unlike the case of region (I) in Fig. 16. Fig. 18 shows the interaction surge to v_{DS1} due to the turn-on of Q4 in the phase-v. Since both Q2 and Q6 are on-state, the effect on v_{DS1} is the highest, and a larger surge occurs. From another point of view, this is the period when the phase surge in Q3 is the highest.

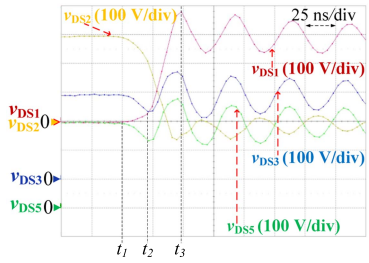
As can be seen from the above, the difference of the surge generation modes between the three-phase and half-bridge



(a) The reverse recovery condition in Q1 by the turn-on of Q2.

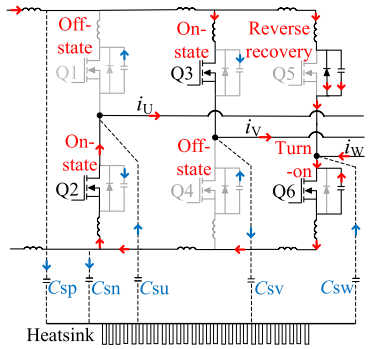


(b) Surge voltages in the phase-u interacts to the other phase legs with a large effect.

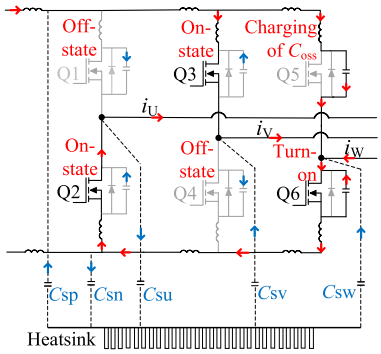


(c) Experimental waveforms of drain-source voltages in each MOSFET.

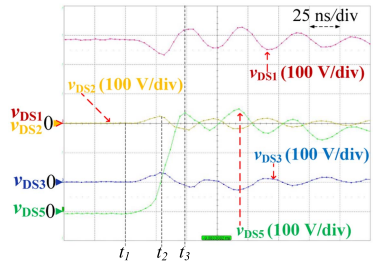
Fig. 15. Mechanism of the phase surge voltage on v_{DS1} in region (IV).



(a) The reverse recovery condition in Q5 by the turn-on of Q6.



(b) Surge voltages in the phase-w interacts to v_{DS1} in the phase-u with a middle effect.



(c) Experimental waveforms of drain-source voltages in each MOSFET.

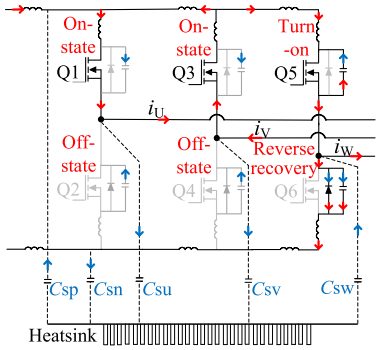
Fig. 16. Mechanism of the interaction surge voltage on v_{DS1} in region (I).

inverters is that there is an interaction surge between phase legs. Moreover, the main trigger for the interaction surges is the phase surge. Therefore, it can be considered that an interaction surge voltage can be reduced by suppressing the phase surge voltage that occurs inside each phase leg. Based on the above analysis of the surge generation mechanisms in the three-phase inverter, an effective control method of active gate drive for each region will be proposed and investigated in the next chapter.

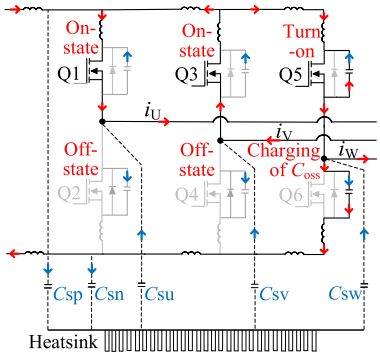
VI. Proposed Partial Active Gate Driving Control Methods and Experimental Results

A. Suppression of Surge Voltage by Using Active Gate Drive

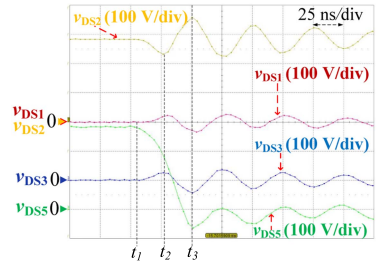
Fig. 19 shows three kinds of gate patterns used in the experiments in this paper. The 63-level constant pattern in Fig. 19(a) shows that the number of on-state CMOS drivers is 63, which is like the general gate drive using a fixed gate resistor and the maximum drivability of the gate driver. Fig. 19(b) shows the 5-level constant pattern, which uses 5-level gate drivability only in the first 260 ns. After that, the number of the on-state CMOSs becomes 63-level to decrease the on-state resistance of the power device. Fig. 19(c) shows the example of the AGD pattern that uses the 5-level in the first 40 ns, then the 40-level in the next 40 ns to make the gate charge and discharge faster. After that, it returns to the 5-level for 180 ns before changing to the 63-level. The durations of the gate patterns have been determined manually based on offline measurements in this paper. To optimize the durations of the gate pattern, for example, an offline switching test with an optimization algorithm is effective as reported in [10] and [13]. However, such an optimization method needs a long time to find just one gate pattern. The target in this paper is to abbreviate such optimization. The authors have manually searched for a suitable gate pattern to reduce the surge voltages without any optimization program. The found gate pattern is not an optimal pattern to solve the tradeoff relation between



(a) The reverse recovery condition in Q6 by the turn-on of Q5.

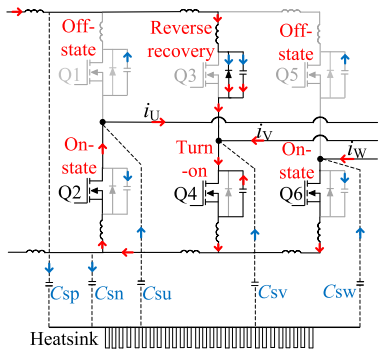


(b) Surge voltages in the phase-w interacts to v_{DS1} in the phase-u with a small effect.

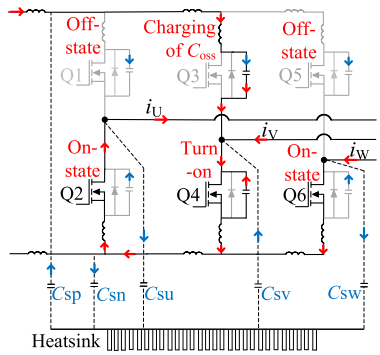


(c) Experimental waveforms of drain-source voltages in each MOSFET.

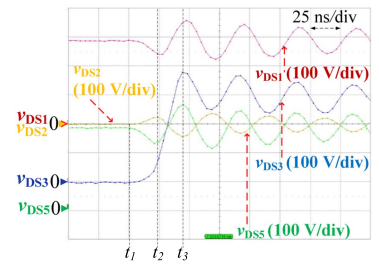
Fig. 17. Mechanism of the interaction surge voltage on v_{DS1} in region (V).



(a) The reverse recovery condition in Q3 by the turn-on of Q4.



(b) Surge voltages in the phase-v interacts to v_{DS1} in the phase-u with a large effect.



(c) Experimental waveforms of drain-source voltages in each MOSFET.

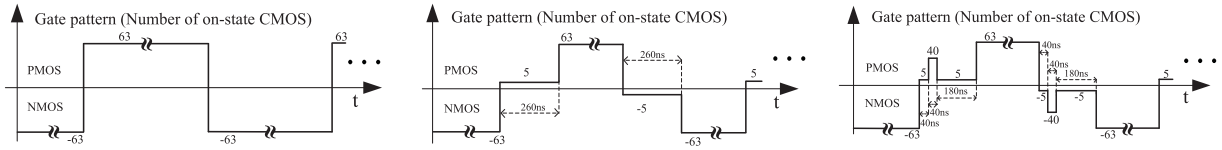
Fig. 18. Mechanism of the interaction surge voltage on v_{DS1} in region (VI).

switching loss and surge voltage, but a better pattern to reduce the surge voltage. If we apply this pattern only for the switching with high surge voltage, increasing the switching loss does not become a big issue because the high surge switching counts are not many. These three types of AGD control methods are investigated in this experiment.

Figs. 20 and 21 show the experimental waveforms by the conventional AGD method using the 63-level constant pattern and 5-level constant patterns, respectively. The gate patterns utilized in a load current cycle are shown in Figs. 20(a) and 21(a). From the overall waveform in Fig. 20(b), the highest surge of v_{DS1} happens when the i_v starts to change from positive to negative in the region (IV), while the surge is lower in the region (II). The waveforms in regions (II) and (IV) are shown in detail in Fig. 20(c) and Fig. 20(d), respectively. When using the 5-level constant pattern contributes to suppressing the first overshoot of the surge voltage as shown in Fig. 21(b). The surge in the region (II) and region (IV) are both suppressed to 322 V by slowly increasing the gate charge, as shown in Fig. 21(c) and (d), respectively. However, the efficiency of the inverter decreased from 95.58% under 63-level constant pattern to 95.01% under 5-level constant pattern because of the slow switching speed at all the time in all the power devices.

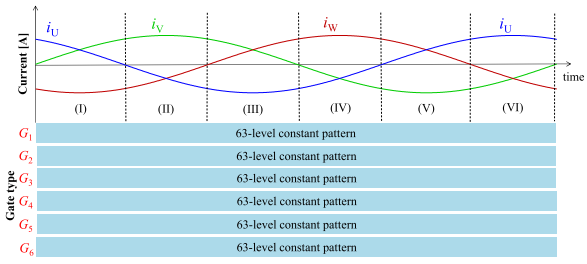
B. A Proposed Active Gate Control Method to Improve the Surge Voltage and Efficiency

Figs. 22 and 23 show the experimental waveforms by using the proposed partial AGD method to suppress surge voltage and improve the overall efficiency. In the proposed method, a gate drive pattern with a slow gate charge and discharge is used for gate G_1 in only the region (I) where i_U and i_V are both positive for suppressing the surge voltage. On the other hand, the 63-level constant pattern is used for G_1 in the other regions for fast

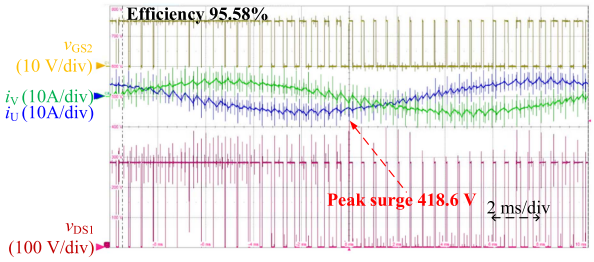


(a) 63-level constant pattern. (b) 5-level constant pattern. (c) AGD pattern.

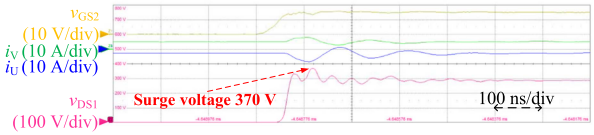
Fig. 19. Gate patterns using in the experiments shown in Figs. 20, 21, 22, and 23.



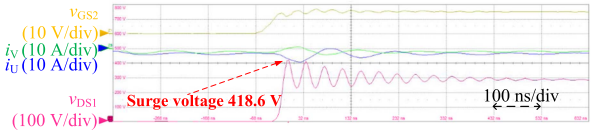
(a) Applied gate patterns in a cycle of load current.



(b) Overall waveform.

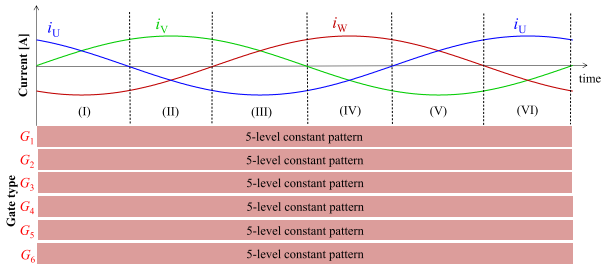


(c) Waveforms in the lower surge voltage region of region (II).

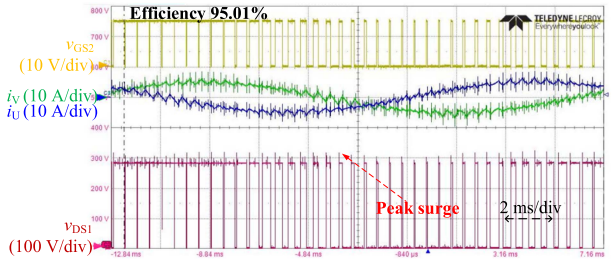


(d) Waveforms in the highest surge voltage region of region (IV).

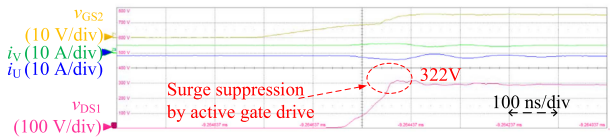
Fig. 20. Experimental waveforms under always 63-level constant pattern gate drive.



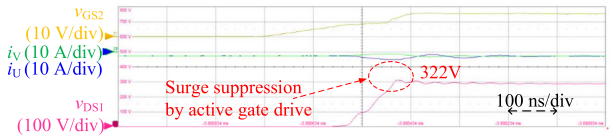
(a) Applied gate patterns in a cycle of load current.



(b) Overall waveform.



(c) Waveforms in the lower surge voltage region of region (II).



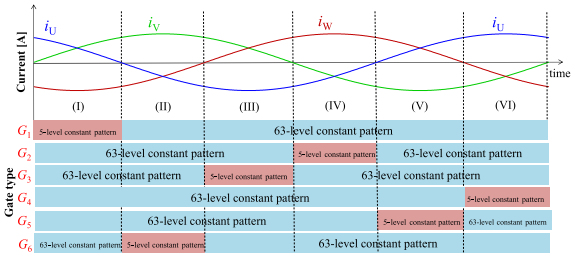
(d) Waveforms in the highest surge voltage region of region (IV).

Fig. 21. Experimental waveforms under always 5-level constant pattern gate drive.

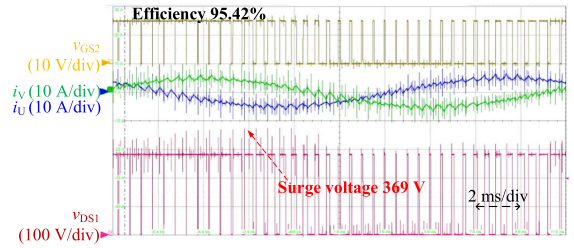
switching and reducing switching loss. For the low-side power device, a gate drive pattern with a slow gate charge and discharge is used for gate G_2 in only the region (IV) where i_U and i_V are both negative. The 63-level constant pattern is used for G_2 in the other regions. As the same with the phase-v and phase-w, it is shifted 120° for G_3 and G_4, and 240° for G_5 and G_6, respectively, due to the different phases among the three-phase currents.

In Fig. 22, the 5-level constant pattern is used as a gate pattern with a slow gate charge. Fig. 22(c) shows that the surge voltage remained at 369 V in the region (II), which is the same as Fig. 20(c) due to using the 63-level constant pattern in this region. However, the highest surge 418.6 V shown in Fig. 20(c) is suppressed to 322 V by using a 5-level constant pattern for only G_2 in only the region (IV). Due to slow switching in only one region, and fast switching in the remaining five regions of each phase, the efficiency increases from 95.01 to 95.42%.

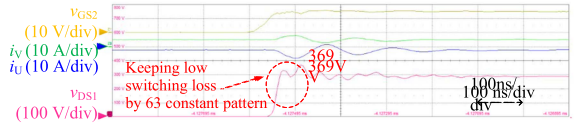
Fig. 23 shows the experimental result using a partial AGD pattern partially. In the turn-off transient, a weak turn-off using the gate pattern of 5-level in 40 ns contributes to suppressing the first overshoot as the surge voltage initially. It shows that the surge voltage could be reduced from 418.6 V to 343 V by using this AGD pattern in the region (IV), as shown in Fig. 23(d). The surge of 394.6 V in the region (II) is remained due to using the 63-level constant pattern in this region. Applying the AGD pattern



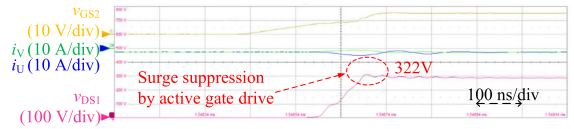
(a) Applied gate patterns in a cycle of load current.



(b) Overall waveform.

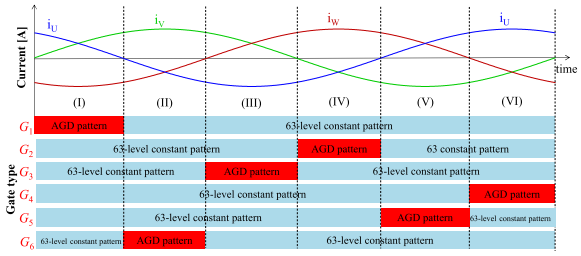


(c) Waveforms in the lower surge voltage region of region (II).

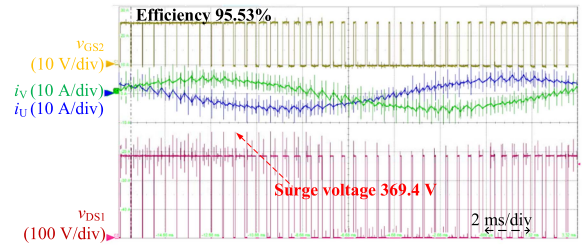


(d) Waveforms in the highest surge voltage region of region (IV).

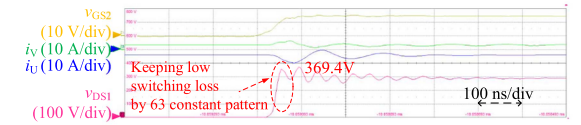
Fig. 22. Experimental waveforms under the proposed partial active gate drive method utilizing 5-level constant gate pattern shown in Fig. 19(b).



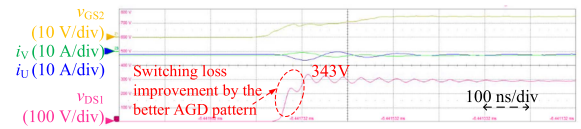
(a) Applied gate patterns in a cycle of load current.



(b) Overall waveform.



(c) Waveforms in the lower surge voltage region of region (II).



(d) Waveforms in the highest surge voltage region of region (IV).

Fig. 23. Experimental waveforms under the proposed partial active gate drive method utilizing AGD pattern shown in Fig. 19(c).

increases the efficiency to 95.53%, which is a high efficiency while keeping the surge voltage at 369.4 V.

C. Comparison of the Proposed and Conventional Active Gate Drive

Fig. 24 shows the surge voltage and efficiency comparison based on the results shown in Figs. 20, 22, and 23. The blue plots show the results under the always same gate pattern shown in Figs. 20 and 21. It is seen that there is a trade-off relation between the switching loss and surge voltage reductions under the constant gate patterns and the always same pattern. This is the well-known limitation of the general gate drivers with the gate resistance adjustment. The AGD control with the always same pattern can improve the efficiency from 95.01% to 95.15% by changing from a 5-level constant pattern to the AGD pattern. However, the surge voltage also increases to 370 V. On the other hand, the red color plots are the results of using the proposed partial AGD method. It can be seen that the proposed partial AGD method achieves higher efficiency than the above conventional AGD method while keeping the surge voltage at 369.4 V. In comparison with the always 63-level gate pattern, the surge voltage could be reduced from 418.6 V to 369.4 V

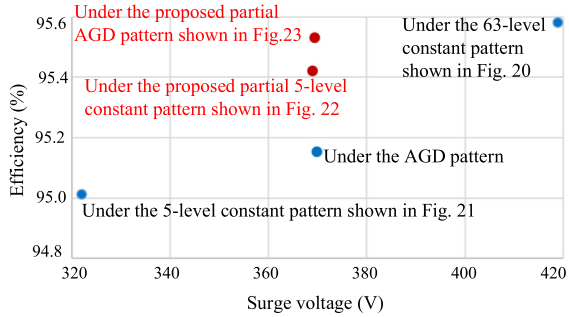


Fig. 24. Comparison of surge voltage and efficiency when using proposed partial AGD control, conventional AGD control, and normal gate drive (f_{sw} = 2 kHz).

fixing the efficiency of 95.53% by using the proposed partial AGD method.

From the result, the effectiveness of the proposed partial AGD control has been verified in the motor-fed three-phase inverter. A further suitable active gate pattern than that in Fig. 19(c) is expected to improve the trade-off relationship. Moreover, it is expected to be improved by further flexible active gate patterns controlled considering the operation states of the three-phase inverter.

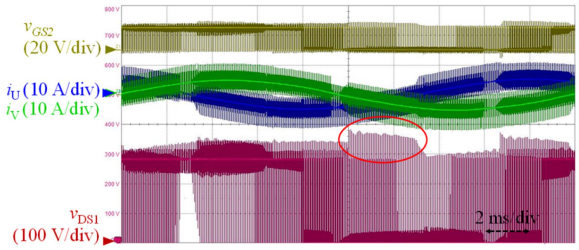


Fig. 25. Experimental waveform under always 63-level constant pattern gate drive ($f_{sw} = 20$ kHz).

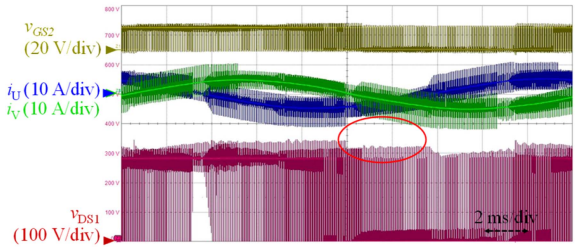


Fig. 26. Experimental waveform under proposed partial active gate drive method utilizing AGD pattern ($f_{sw} = 20$ kHz).

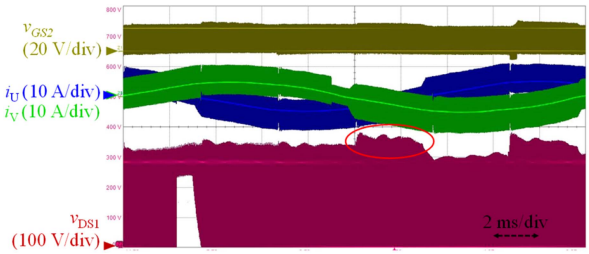


Fig. 27. Experimental waveform under always 63-level constant pattern gate drive ($f_{sw} = 50$ kHz).

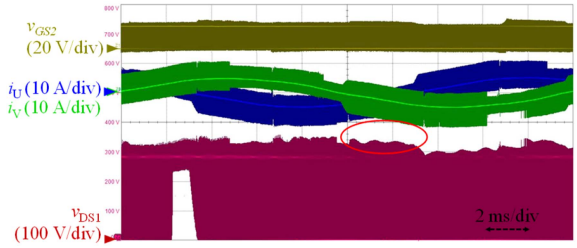


Fig. 28. Experimental waveform under proposed partial active gate drive method utilizing AGD pattern ($f_{sw} = 50$ kHz).

D. Comparison of the Effectiveness in the Different Switching Frequencies

Figs. 25 to 28 show the experimental waveforms under the carrier frequencies of 20 kHz and 50 kHz with the same format as Figs. 20(b) and 23(b) for the comparison with 2 kHz. The experimental waveforms show that the proposed partial active gate drive method effectively reduces the surge voltage only in the higher surge region (IV) even under the conditions of the higher switching frequencies of 20 kHz and 50 kHz.

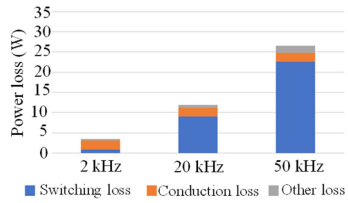


Fig. 29. Power loss breakdown under always 63-level constant pattern gate drive.

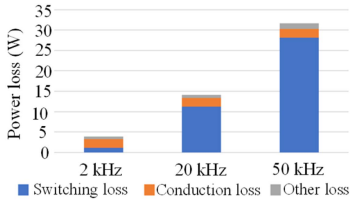


Fig. 30. Power loss breakdown under always AGD pattern gate drive.

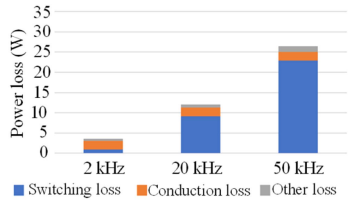


Fig. 31. Power loss breakdown under the proposed partial active gate drive method utilizing AGD pattern.

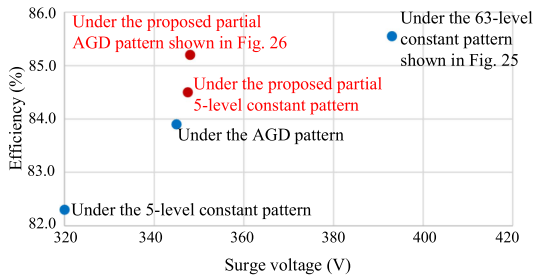


Fig. 32. Comparison of surge voltage and efficiency when using proposed partial AGD control, conventional AGD control, and normal gate drive ($f_{sw} = 20$ kHz).

The switching losses based on the experimental waveforms are also analyzed, and the summary of the power loss breakdowns in the different switching frequencies is shown in Figs. 29 to 31. It is shown that the switching losses significantly increase as the switching frequency increases, and the switching loss becomes dominant in the condition of the higher switching frequency of 20 kHz and 50 kHz compared with the condition of 2 kHz. Fig. 32 shows the comparison of surge voltage and efficiency under the switching frequency of 20 kHz under these gate driving conditions. By applying the proposed partial active gate drive method utilizing the AGD pattern, the efficiency is improved by 0.4% at the switching frequency of 2 kHz, 1.2% at 20 kHz, and 3.2% at 50 kHz in comparison to the always AGD pattern. The proposed partial active gate drive can realize lower surge voltage and lower power loss, and the effectiveness becomes larger as the switching frequency increases.

VII. Conclusion

This paper presented a partial active gate driving method using all six AGD ICs with 63-divided gate drive levels in the three-phase inverter. From the analysis of the operation modes and surge voltages, it has been clarified that there are two types of surge voltages in the drain-source voltage in each MOSFET. The phase surge happens in the switching phase leg, and it affects the drain-source voltage of the opposite MOSFET. The interaction surge occurs in the other phase leg and interferes to the phase leg that the surge voltage observed. As a result, it was seen that the phase surge is the trigger and higher than the interaction surge from the principle of the circuit connection. Based on the analytical result, a partial AGD control method for the three-phase inverter was proposed. It was demonstrated in the prototype three-phase inverter that the proposed partial AGD control reduces the surge voltage from 418.6 V to 369.4 V while keeping the efficiency under high-speed gate driving. This proposed partial AGD control method is expected to realize a high-performance on the efficiency and electromagnetic interference even in common main power devices and circuits. The advantage of the proposed partial AGD control method is to abbreviate the gate pattern optimization unlike the simpler AGD. Moreover, the proposed method can adjust the effectiveness for the surge suppression after circuit implementation and during continuous operation by a software-oriented approach unlike the conventional hardware countermeasures such as snubber capacitor and suitable layout design.

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