Adjustable Current Limiting Function With a Monolithically Integrated SiC Circuit Breaker Device

Taro Takamori, *Graduate Student Member, IEEE*, Keiji Wada, *Senior Member, IEEE*, Norman Boettcher, Tobias Erlbacher, Wataru Saito, *Senior Member, IEEE*, and Shin-ichi Nishizawa, *Member, IEEE*

***Abstract*—This article proposes a current limiting function for a self-sensing and self-triggering monolithically integrated SiC circuit breaker device. The proposed function provides the device not only with a fast-response current breaking operation but also with the current limiting operation, including supplying a constant current to the load and preventing the detection of inrush currents. This function is suitable for replacing mechanical conductors in initial charging circuits within rectifiers and safety equipment in case of overcurrent phenomena. The proposed method achieves certain constant currents through a simple variation of the gate-drive circuit with the adjustable parameters of an additional MOSFET. The mechanism of the current limiting function is verified using TCAD simulations based on certain conditions. Consequently, experimental results verified that the circuit breaker device with the current limiting function reduces the inrush current by up to 76.9% using a 500 VDC distribution circuit system.**

***Index Terms*—Current limiter, JFET, monolithic integration, self-triggered, silicon carbide, solid-state circuit breaker.**

I. Introduction

DC power distribution systems are an important part of technology related to supporting future power transmission systems. One of the most important issues to be overcome in DC distribution systems is ensuring safety against non-zero crossing direct currents [1], [2], [3]. Circuit breakers and current limiters are essential for preventing equipment damage from high $\mathrm{d}i/\mathrm{d}t$ events, such as short circuits and inrush currents in DC power distribution systems. Furthermore, high inrush currents may be introduced into DC applications with high inductive load energy, resulting in failures and safety concerns.

However, mechanical circuit breakers are plagued by potential problems owing to their bulky bodies and their inability to address accidents that exhibit fast transient responses. Moreover, the initial charging circuit used when applying power to the DC coupling capacitor for rectifiers suffers from a bottleneck with the mechanical conductor, although it is not used during the steady-state period [4], [5].

Thus, a protection technology using semiconductor devices is a strong candidate for supporting high safety in DC power distribution systems [6], [7]. Semiconductor-based circuit breakers and current limiters have been offered as system-level solutions that combine intelligent technologies [8], [9], [10], [11], [12], [13], [14], [15]. Silicon carbide (SiC) material provides the power semiconductor devices fully demonstrated compared to existing silicon (Si) power devices [16], [17]. In particular, these characteristics provide excellent performance in circuit breakers and current limiters against fast turn-off speeds, low resistance, and higher operating temperature owing to cutoff and current limiting operations, rendering them suitable for the applications.

A monolithically integrated SiC circuit breaker device has been developed as a promising candidate for fast-response protection against DC system accidents [18], [19], [20], [21], [22]. The solid-state circuit breaker device comprises technologies that function on a self-sensing, self-triggering basis based on "thyristor dual" functionality with a pJFET and nJFET [23], [24], [25]. Sensing components for operating solid-state circuit breakers are plagued by several challenges related to conduction loss and delays owing to auxiliary circuits. Therefore, the removal of the auxiliary circuits is an important technique for reducing the detection time and number of components. Based on these perspectives, the structure can provide even faster interruption speeds than conventional solid-state circuit breakers, thereby contributing to the suppression of accidental currents.

The circuit breaker device has been analyzed using the technology computer-aided design (TCAD) simulations based on the basic design methodology [18] and fabricated [19]. In addition, the fabricated circuit breaker device has been verified to evaluate

Manuscript received 28 December 2022; revised 14 April 2023; accepted 5 June 2023. Date of publication 23 June 2023; date of current version 20 September 2023. Paper 2022-PEDCC-1688.R1, presented at the 2022 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, May 26–28, and approved for publication in the IEEE Transactions on Industry Applications by the Power Electronic Devices and Components Committee of the IEEE Industry Applications Society [DOI: 10.1109/ECCE50734.2022.9948054]. This work was supported in part by the Federal Ministry of Education and Research (BMBF) through SiC-DCBreaker under Grant 03INT501BC and in part by the Japan Science and Technology Agency (JST), Support for Pioneering Research Initiated by the Next Generation (SPRING) under Grant JPMJSP2156. *(Corresponding author: Taro Takamori.)*

Taro Takamori and Keiji Wada are with the Department of Electrical Engineering and Computer Science, Tokyo Metropolitan University, Tokyo 192–0397, Japan (e-mail: takamori-taro@ed.tmu.ac.jp; kj-wada@tmu.ac.jp).

Norman Boettcher and Tobias Erlbacher are with the Fraunhofer Institute for Integrated Systems and Device Technology IISB, 91058 Erlangen, Germany (e-mail: norman.boettcher@iisb.fraunhofer.de; tobias.erlbacher@iisb.fraunhofer.de).

Wataru Saito and Shin-ichi Nishizawa are with the Research Institute for Applied Mechanics, Kyushu University, Fukuoka 816–8580, Japan (e-mail: wataru3.saito@riam.kyushu-u.ac.jp; s.nishizawa@riam.kyushu-u.ac.jp).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TIA.2023.3288856.

Digital Object Identifier 10.1109/TIA.2023.3288856

the blocking performances up to 800 VDC [20], [21]. In general, the circuit breaker represents a two-pole device. However, a third pin (source) is provided that accepts an external control signal to extend the current limiting capability [22]. This function is useful as an alternative method for the initial charging circuit to mitigate the inrush current to the DC coupling capacitor for the rectifiers. Moreover, this principle can be applied to drive circuit technology to provide multifunctional solutions.

Recently, several proposals have been developed for current limiting functions of solid-state circuit breakers. For example, circuit breakers [12], [13], [14] consist of a current sensor, a latch circuit for determining the time constant, a gate drive circuit for use in the current limiting function, and a circuit breaker [15] is adapted a microcontroller contributes to short circuit, over current protection, and inrush current suppression with pulse width modulation (PWM). On the other hand, the circuit breaker device with the "thyristor dual" concept provides these functions in a monolithic integration. Therefore, it has the advantage over the current limiting function with the circuit breakers in that the device operates without the need for additional components.

This article proposes a current limiting function that enhances the monolithically integrated SiC circuit breaker device. The function is realized through the modulation of a current bypass through the aforementioned source pin. The function can control the limiting current value using a MOSFET and a gate-drive circuit with adjustable parameters externally connected to the source terminal of the circuit breaker device. Moreover, the proposed function allows for the extension of the current limiting operation, including providing a constant current to the load and preventing the triggering of inrush currents. The experimental results are demonstrated using a 500 VDC distribution system. Moreover, the previous report [22] has never discussed the mechanism of the current limiting function inside the device in detail. The simulation results show that the proposed method [22] contributes to the formation of a current bypass in the circuit breaker device owing to the low resistance of the source side.

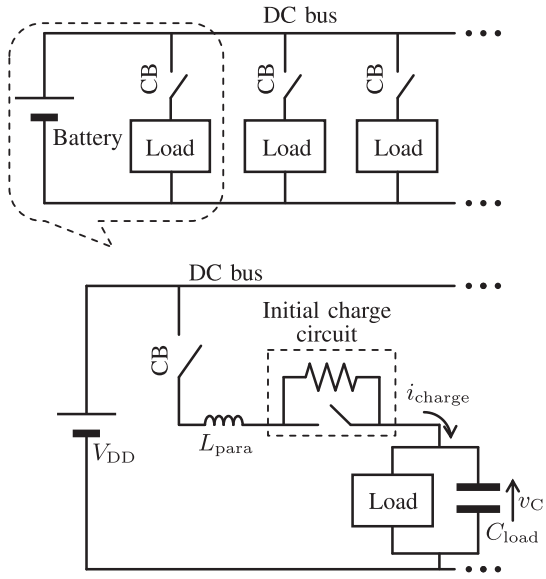

Fig. 1. Circuit configuration of the DC system including parasitic parameters.

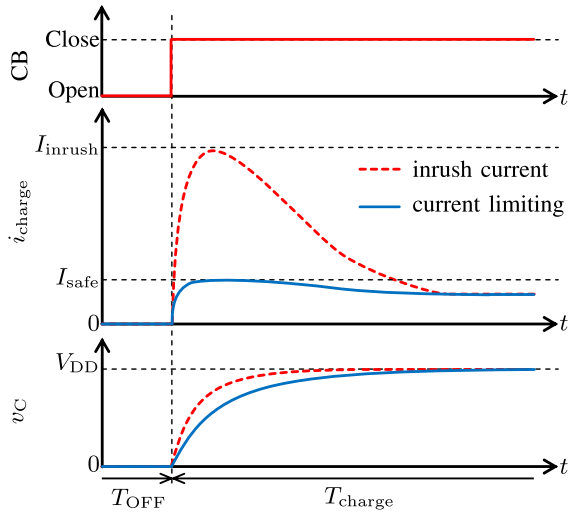

Fig. 2. Waveforms of the inrush current in the DC system.

II. Protection Function of Direct Current Applications

Fig. 1 shows the equivalent circuit diagram of the DC power distribution system, and Fig. 2 shows the waveforms of the inrush current in the DC system. In DC systems, a power source is supplied to the loads through a DC bus. Furthermore, a decoupling capacitor C_{load} is connected in parallel to the load to stabilize the input voltage V_{DD}. A current limiting resistance and mechanical conductor are incorporated to limit the inrush current for application as the initial charge circuit. The mechanical conductor is connected only for its switching function between current limiting and steady-state operations. However, the mechanical conductor is one of the factors that makes power converters bulky and degrades the contact, even though they are only used for a very short time during initial start-up operations.

Moreover, circuit breakers should serve from accidents. As shown in Fig. 1, the DC power distribution system comprises multiple loads connected to a single bus. However, the configuration is not flexible under fault conditions. To protect other loads from accidents, circuit breakers (CB) are connected separately at the front ends of the loads [1].

During an accident, the energy stored in the wiring inductance L_{para} generates accident energy E_{fault}, which is calculated as

$$E_{\text{fault}} = \frac{1}{2} L_{\text{para}} I_{\text{charge}}^2. \tag{1}$$

Therefore, limiting the charging current I_{charge} and carefully designing the inrush current I_{inrush} to not exceed the safety level I_{safe}, even in case of the connection with the DC bus, is desirable. This function facilitates fast interruption in the short circuit events, and reduction of the accident energy E_{fault}.

Thus, replacing the initial charge circuit and the circuit breakers connected with the DC bus with the multifunctional

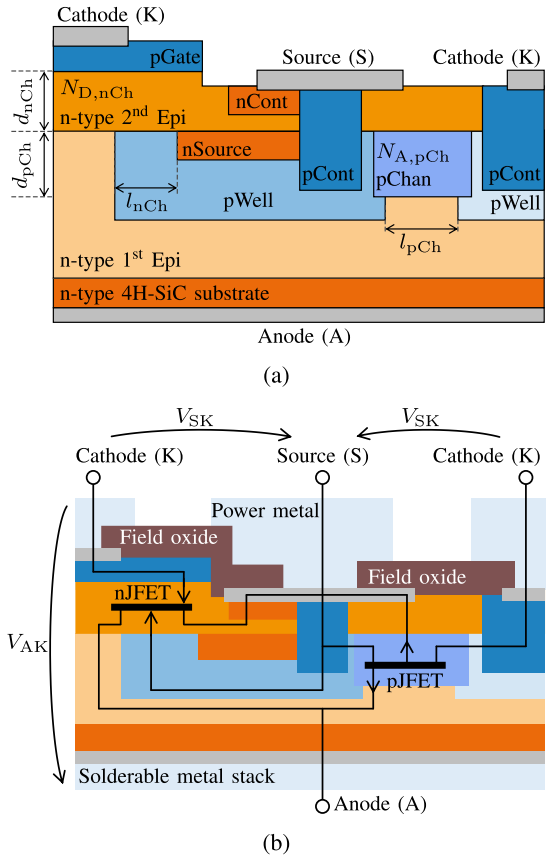

Fig. 3. Schematic cross-section of the circuit breaker topology. (a) Ohmic contact formation and (b) back-end processing.

solid-state circuit breaker can solve the problems encountered by the mechanical conductors.

III. Monolithically Integrated SiC Circuit Breaker Device

A. Structure of the Circuit Breaker Device

Fig. 3 shows the structures of the monolithically integrated SiC circuit breaker device. Fig. 3(a) shows a schematic half-cell cross-section of the circuit breaker device. The circuit breaker device is based on a 4H-SiC technology and adopts a "thyristor dual" structure consisting of an nJFET and a pJFET connected in series [23], [24]. The design methodology for the circuit breaker device parameters is defined by the channel length $l_{\mathrm{nCh/pCh}}$, channel depth $d_{\mathrm{nCh/pCh}}$, and channel doping concentration $N_{\mathrm{D,nCh/A,pCh}}$. Fig. 3(b) shows the back-end processing of the circuit breaker device. A voltage equivalent to the power source should be expected at the gate of JFETs after the circuit breaker enters the blocking state in DC systems. Moreover, the device topology is specifically designed to provide sufficient voltage sustainability for the pJFET gate structure.

Fig. 4 shows a manufactured circuit breaker device board and the equivalent circuit configuration. The manufactured circuit breaker device is mounted on direct bonded copper (DBC) boards and applied to card edge connectors. The structure interacts with the drain-source and gate-source voltages of the nJFET and pJFET to determine the operation of each JFET. This realizes current sensor-less detection based on the trigger current I_{trig} designed for the circuit breaker device. In addition, the source pin always floats during the circuit breaker operation.

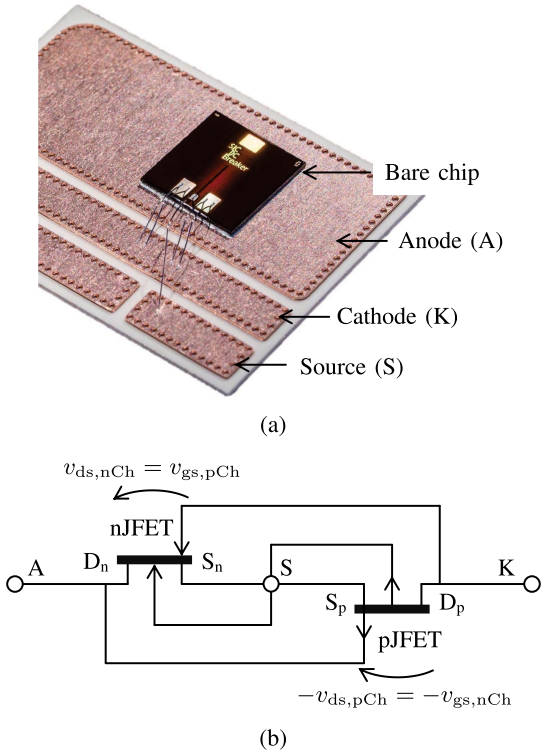

Fig. 4. Monolithically integrated circuit breaker device. (a) Manufactured circuit breaker device board and (b) equivalent circuit configuration of the circuit breaker device.

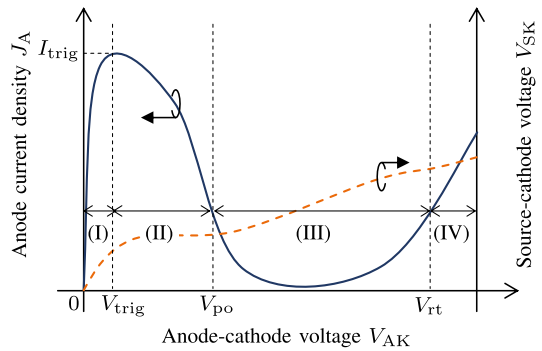

Fig. 5. Concept waveforms of the electrical characteristics of the circuit breaker device.

B. Basic Design Concept of the Circuit Breaker Device

Fig. 5 shows concept waveforms of the circuit breaker device characteristics of anode-cathode voltage V_{AK}, anode current density J_{A}, and source-cathode voltage V_{SK} of the circuit breaker device. The circuit breaker device is classified into four

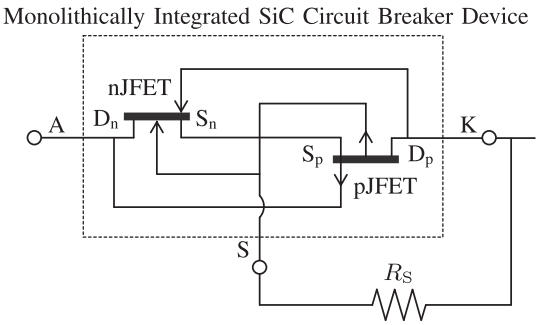

Fig. 6. Circuit configuration of the proposed current limiting function with the circuit breaker device.

periods of electrical characteristics as follows: (I) linear, (II) transit, (III) blocking, and (IV) reach-through. In the conduction state, the anode current I_A operates in the period (I). A specific on-resistance $R_{on,sp}$ is defined as $\Delta V_{AK}/\Delta J_A$ in the period (I). When the anode current I_A reaches the trigger current I_{trig}, the transition from the period (I) to (II) and the current interruption by the blocking period (III) function in the range of a pinch-off voltage V_{po} and a reach-through voltage V_{rt} to ensure protection during the DC application. Furthermore, the blocking period (III) should correspond to the input voltage of the DC system to ensure a low leakage current and to maintain the blocking voltage.

C. Current Limiting Function

Fig. 6 shows the circuit configuration used for the proposed current limiting function. To realize the current limiting operation, a source resistance R_S is connected in parallel with the pJFET between the source and cathode terminals of the circuit breaker device. Consequently, the drain-source voltage of the pJFET $-v_{ds,pch} = -v_{gs,nch}$ is controlled based on the value of the resistance R_S to ensure its relaxation. Consequently, rather than turning to the blocking state, the circuit breaker limits the anode current I_A to the saturation current level of the JFET. The extension of the trigger current function should be used to prevent the circuit breaker device from making incorrect overcurrent decisions. Conversely, when short circuit events occur, the circuit breaker device can perform a cutoff operation at a high speed by removing the external trigger.

IV. TCAD Simulation

To investigate the influence of source resistance R_S, simulations were performed using a device model with Sentaurus TCAD. The model design of the circuit breaker device was based on the structure used in [18]. The parameters of the source resistance R_S were set to 0, 5×10^{-2}, and $1 \times 10^{9}\,\Omega$ for the short condition, current limiting function, and floating condition, respectively.

A. Quasi-Static Electrical Characteristic

Fig. 7 shows the simulation results of the electrical characteristics of the circuit breaker device under certain R_S conditions. Fig. 7(a) shows the overall output characteristics of anode current density J_A and source-cathode voltage V_{SK}. The basic concept of the circuit breaker device design is the minimization of the leakage current within the blocking region upon the application of a DC voltage V_{DD}. However, the leakage current during the blocking period is released by lowering the resistance R_S. Thus, the leakage current is responsible for generating a constant current as the current limiting function in the case of low R_S. Essentially, the output characteristics of the nJFET were determined by the $v_{gs,nCh} = v_{ds,pCh}$. Moreover, the addition of R_S to the pJFET connected in parallel provided the role of bypassing the current to the source side. Thus, the output characteristics of the nJFET can be indirectly modified by the resistance R_S.

Fig. 7(b) shows the output characteristics of reaching the trigger current I_{trig}. Adjustments to the resistance R_S contributed to the extension of the trigger current I_{trig}. When the resistance R_S was significantly low, the trigger produces a constant current

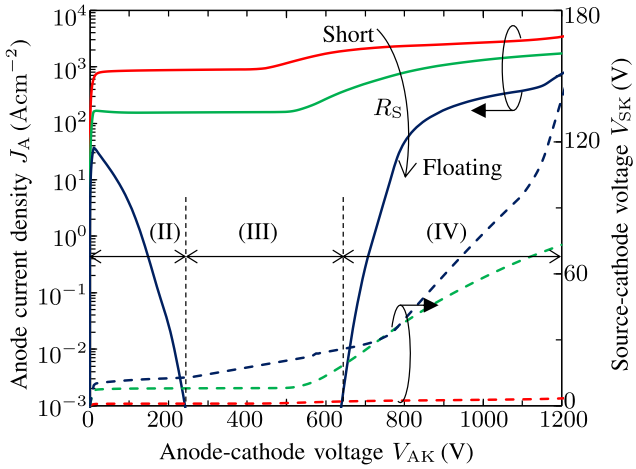

Fig. 7. Simulation results of anode current density J_A and source-cathode voltage V_{SK} with certain R_S conditions, (a) overall output characteristics and (b) reaching the trigger current I_{trig}.

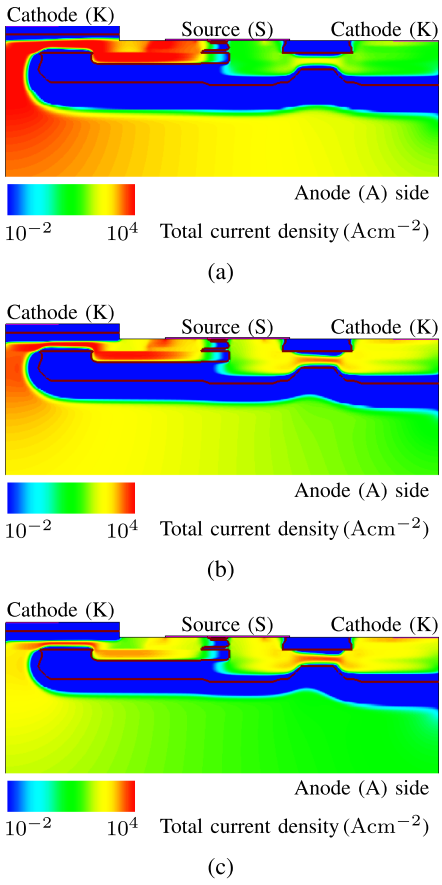

Fig. 8. Simulation results of the total current density with reached trigger current I_{trig} at $V_{\mathrm{AK}} = 10\,\mathrm{V}$, (a) short condition, (b) current limiting operation, and (c) floating condition.

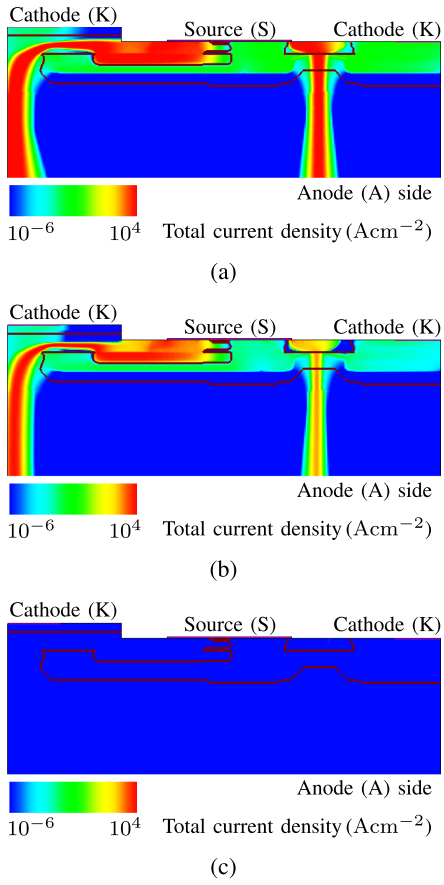

Fig. 9. Simulation results of the total current density with blocking operation region at $V_{\mathrm{AK}} = 500\,\mathrm{V}$, (a) short condition, (b) current limiting operation, and (c) floating condition.

without a cutoff operation. Thus, the extension of the temporary trigger current avoids false trigger operations.

B. Current Flow Inside the Circuit Breaker Device

Fig. 8 shows the simulation results of the total current density when the current reached the trigger current I_{trig} at $V_{\mathrm{AK}} = 10\,\mathrm{V}$. The results indicate that the resistance R_{S} affects the anode current I_{A} conducted through the nJFET. Typically, the pJFET drain-source interface acts as a conduction path for the anode current (see Fig. 8(c)). However, almost all the current from the anode side flowed to the source side when the resistance R_{S} was set to a low value.

Fig. 9 shows the simulation results of the total current density in the blocking voltage region at $V_{\mathrm{AK}} = 500\,\mathrm{V}$. When the resistance R_{S} was set to a high value, current flowed through the circuit breaker device and was blocked by the circuit breaker operation. However, a lower R_{s} provides the current paths created on both the pJFET and nJFET toward the source terminal. Furthermore, the current bypass between the source and cathode via resistance R_{S} reduces $v_{\mathrm{gs,nCh}} = v_{\mathrm{ds,pCh}}$, and the output characteristics of the nJFET are affected. This phenomenon is supported by the V_{AK}–V_{SK} characteristics shown in Fig. 7(a). In addition, a high current density was observed in the 1st Epi

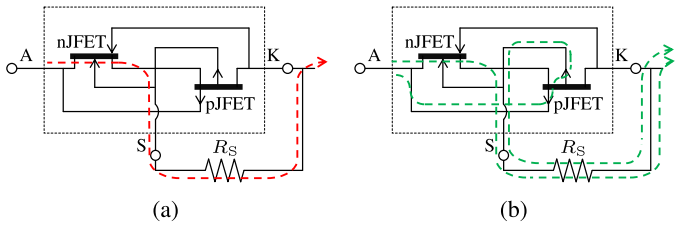

Fig. 10. Current flows within the circuit breaker device, (a) short condition, (b) current limiting operation.

and pJFET channels. This result indicates that the reach-through phenomenon occurs only in the bulk and gate of the pJFET. This phenomenon occurs owing to the blocking operation of the anode-cathode voltage v_{AK} because the source terminal is connected to the cathode side.

Fig. 10 shows the current paths within the circuit breaker device with each operation. In the case of a short condition between the source and cathode, the current path leads to the source terminal from the drain-source of the nJFET. However, in the case of the current limiting function, two different current paths are generated through nJFET and pJFET. The results indicate that the current limiting operation creates current bypass routes, resulting in different current paths inside the circuit breaker

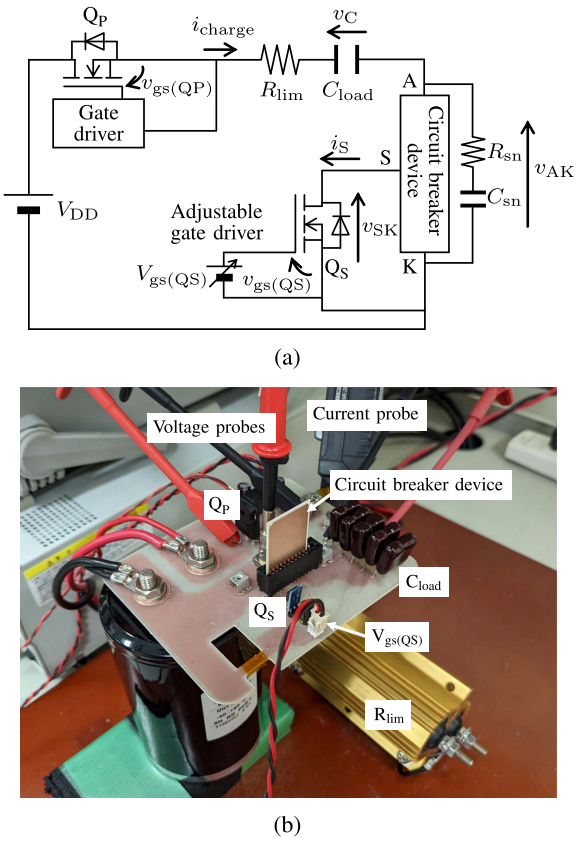

Fig. 11. Experimental setup. (a) Circuit configuration and (b) picture of the circuit board.

TABLE I
PARAMETERS OF THE EXPERIMENTAL CIRCUIT

Parameter		Value
Input voltage	V_{DD}	500 V
Capacitive load	C_{load}	50 nF
Limiting resistance	R_{lim}	150 Ω
Snubber circuit	R_{sn}, C_{sn}	4.7 Ω, 220 pF
Circuit breaker device	I_{trig}, V_{po}, V_{rt}	0.45 A, 145 V, 700 V
MOSFET	$\mathrm{Q_S}$	60 V, 7.7 A rated

device compared with the cases of circuit breaker operation and reach-through phenomenon [18], [19], [20].

V. Experimental Results

To verify that the circuit breaker device functions in the current limiting operations, the proposed method was demonstrated using a DC distribution circuit system with a capacitive load.

Fig. 11 shows the experimental circuit configuration and a picture of the setup. Table I lists the parameters of the experimental circuit. The experimental circuit has the same configuration as the circuit branch connected to a DC bus. A MOSFET $\mathrm{Q_P}$ is connected between a DC voltage V_{DD} and capacitive load C_{load}. When the MOSFET $\mathrm{Q_P}$ is turned on, the power supply to the load is activated. The resistance R_{lim} is added to regulate the current charge relative to the rating of the circuit breaker device used in the experiment. Thus, the current is suppressed to a low value

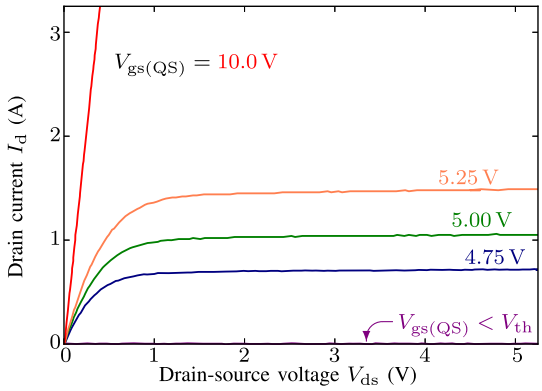

Fig. 12. Measurement result of the I_{d}–V_{ds} output characteristics of a MOSFET $\mathrm{Q_S}$.

relative to the input voltage V_{DD}. The R_{sn}–C_{sn} snubber circuit is connected in parallel to the circuit breaker device to suppress malfunctions. The designed parameters of the circuit breaker device are the pinch-off voltage $V_{\mathrm{po}} = 145\,\mathrm{V}$, reach-through voltage $V_{\mathrm{rt}} = 700\,\mathrm{V}$, and the trigger current $I_{\mathrm{trig}} = 0.45\,\mathrm{A}$. These parameters are suitable for the input voltage $V_{\mathrm{DD}} = 500\,\mathrm{V}$. The specific on-resistance $R_{\mathrm{on,sp}}$ was measured as $1.56\,\Omega\mathrm{cm}^2$.

Fig. 12 shows the measurement result of the I_{d}–V_{ds} output characteristics of a MOSFET $\mathrm{Q_S}$ (Vishay IRFR014, 60 V, 7.7 A, on-resistance $R_{\mathrm{ds(on)}} = 200\,\mathrm{m}\Omega$) by a semiconductor curve tracer (Iwatsu CS-3200). The MOSFET $\mathrm{Q_S}$ was connected between the source and cathode pins of the circuit breaker device and acted in the same manner as the variable resistor R_{S}. The MOSFET $\mathrm{Q_S}$ functioned according to a voltage power supply (TEXIO PAR36-3A) that supported a variable gate-source voltage $V_{\mathrm{gs(QS)}}$ as an adjustable gate driver. The MOSFET $\mathrm{Q_S}$ acts as a resistor instead of the resistance R_{S} by changing the gate voltage $V_{\mathrm{gs(QS)}}$. This function is useful for adaptation to various applications because the MOSFET $\mathrm{Q_S}$ allows for more flexible control of the circuit breaker device operation in response to the circuit conditions. In addition, the gate voltage level can be used as a multifunction controller, that combines the ability to adjust the current limiting and reset functions after being triggered by an external control signal [21]. The demonstration provides the on-resistance $R_{\mathrm{ds(on)}}$ of the MOSFET $\mathrm{Q_S}$ down to $200\,\mathrm{m}\Omega$ by changing the gate-source voltage $V_{\mathrm{gs(QS)}}$ to 0 V, 4.75 V, 5.00 V, 5.25 V, and 10 V.

Fig. 13 shows the schematic waveforms of the current limiting operation. The resistance on the source side is determined by the gate voltage $V_{\mathrm{gs(QS)}}$ and the circuit breaker device acts as a current limiting operation. As long as the anode-cathode voltage v_{AK} converges to zero, the circuit breaker continues to supply a constant current to the capacitance load C_{load}.

Figs. 14 and 15 show the experimental results of the current limiting function with the circuit breaker device. Fig. 14 shows the observed waveforms of the extension of the trigger current I_{trig} with the current limiting function. When the MOSFET $\mathrm{Q_P}$ turned on, the current i_{charge} began to flow in the load C_{load}. When the bypass current path of the source-cathode is set to narrow down, $V_{\mathrm{gs(QS)}}$ must be set to 0 V. Thus, the

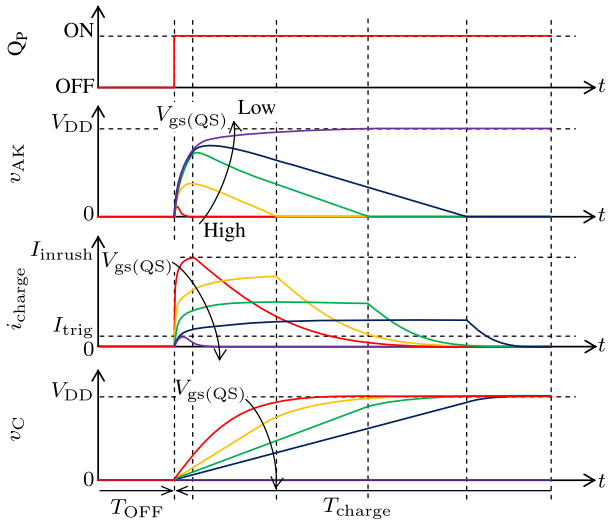

Fig. 13. Waveforms of the current limiting operation.

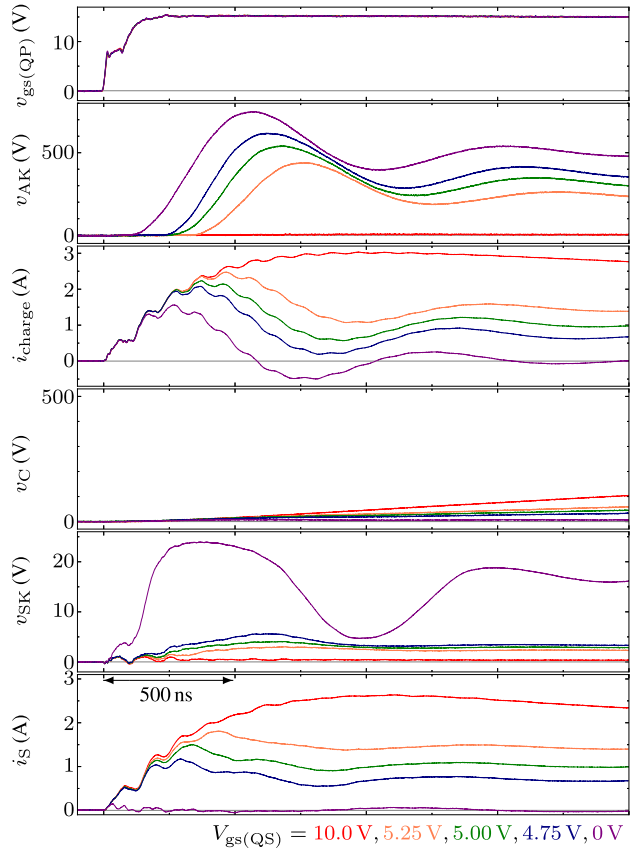

Fig. 14. Experimental results of the current limiting function during the extension of the trigger current I_{trig}.

circuit breaker started the self-triggering operation at the trigger current I_{trig}. In case of $V_{gs(QS)} = 0$ V, the circuit breaker device performed the interrupting operation to suppress up to the inrush current i_{charge} value of 1.56 A. The source-cathode voltage V_{SK} was used to determine the output characteristics of the nJFET. Therefore, the gate-source voltage was transferred to the nJFET for shutdown operation immediately after the self-triggering

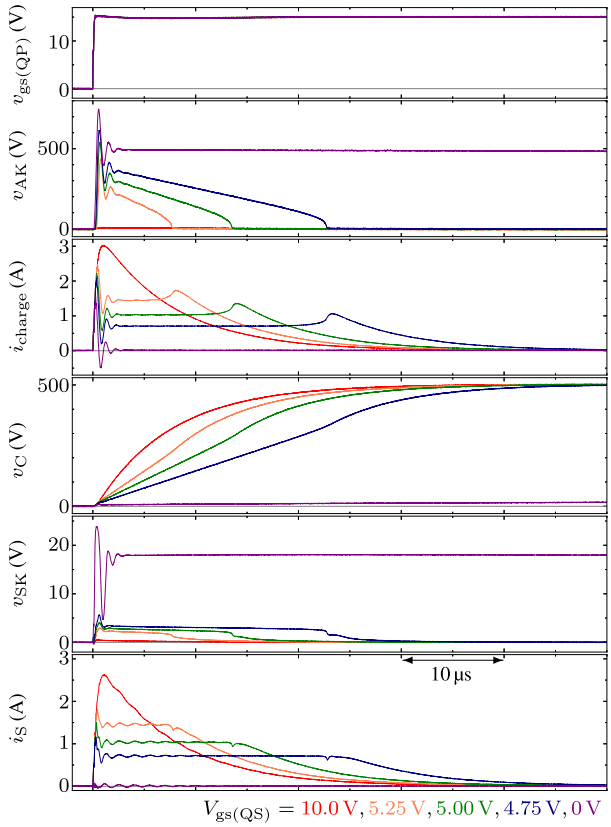

Fig. 15. Experimental results of the current limiting function during the supply of constant current.

operation begins. As the source side maintains a high resistance state, the source current i_S remained zero.

In contrast, for the bypass current path of the source-cathode, $V_{gs(QS)}$ should be adjusted to 10 V. Thus, the circuit breaker does not work under current limiting operations. The source-cathode voltage V_{SK} was limited to a small voltage drop because a current path bypassing the pJFET was formed between the source and cathode terminals. Consequently, the nJFET does not perform self-triggering operations. In addition, the source current i_S is responsible for most of the anode current i_{charge}. The peak value of i_{charge} was observed to be 3.03 A. Thus, the circuit breaker device prevented false current detection by expanding the trigger current. As supported by the simulation results, the connection of R_S facilitates the current flow into the bypass route to the source terminal. The source-cathode voltage v_{SK} remains lower than that required for circuit breaker operation, which results in the trigger current I_{trig} being extended.

Fig. 15 shows the observed waveforms of the supply of constant current with the current limiting function. By adjusting to the gate-source voltage $V_{gs(QS)}$ in the range of 4.75 V to 5.25 V, Q_S maintained an arbitrary on-resistance and the circuit breaker worked under the current limiting operation. In this operation, the current limiting function controls the current supplied to the load to a constant value of up to 1.43 A at $V_{gs(QS)} = 5.25$ V and at least 0.70 A at $V_{gs(QS)} = 4.75$ V, which is up to 76.9% lower than that when working in the conduction state. In addition, it

generated the constant current corresponding to the gate-source voltage $V_{\mathrm{gs(QS)}}$ and controlled the supply current for the capacitive load C_{load}. While current limiting is in progress, the nJFET operates with part of the input voltage V_{DD} clamped by the drain-source voltage of the nJFET $v_{\mathrm{ds,nch}}$ $(= v_{\mathrm{AK}} - v_{\mathrm{SK}})$. Therefore, the current limiting function is performed, while most of the energy dissipation is received by the nJFET. In contrast, the voltage drop in MOSFET $\mathrm{Q_S}$ occurs because of the source current i_{S}. After the transient state, it converges to zero and v_{AK} begins the blocking operation at a voltage equal to V_{DD}.

VI. Conclusion

This article proposed a current limiting function for a monolithically integrated SiC circuit breaker device. The proposed function performs the circuit breaker as a current limiting operation, maintaining a constant current supplied to the load. In addition, this function effectively prevents inrush currents from being executed as a breaking operation. The simulation results indicate that the resistance connected to the source side affects the current bypass paths on the circuit breaker device. The method adjusts the source-cathode voltage of the circuit breaker device using the MOSFET as a variable resistor to regulate the current limiting value. Furthermore, the experimental results indicated that the inrush current was reduced to up to 76.9% based on the 500 VDC circuit system. The current limiting function is a useful operation to prevent false detection of the self-triggering circuit breaker device and is a good candidate as an alternative component to the mechanical conductor in the initial charge circuits.

References

[1] D. Kumar, F. Zare, and A. Ghosh, "DC microgrid technology: System architectures, AC grid interfaces, grounding schemes, power quality, communication networks, applications, and standardizations aspects," *IEEE Access*, vol. 5, pp. 12230–12256, 2017.

[2] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC microgrids—Part II: A review of power architectures, applications, and standardization issues," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3528–3549, May 2016.

[3] M. Okamura and T. Takaoka, "The evolution of electric components in prius," *IEEJ J. Ind. Appl.*, vol. 11, no. 1, pp. 1–6, 2022.

[4] Y. Gu, X. Xiang, W. Li, and X. He, "Mode-adaptive decentralized control for renewable DC microgrid with enhanced reliability and flexibility," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 5072–5080, Sep. 2014.

[5] T. Mannen and K. Wada, "Control method for overvoltage suppression across the DC capacitor in a grid-connection converter using leg short circuit of power MOSFETs during the initial charge," *IEEE Trans. Ind. Appli.*, vol. 55, no. 4, pp. 4012–4019, Jul./Aug. 2019.

[6] R. Rodrigues, Y. Du, A. Antoniazzi, and P. Cairoli, "A review of solid-state circuit breakers," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 364–377, Jan. 2021.

[7] Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, F. Wang, and B. J. Blalock, "Design and performance evaluation of overcurrent protection schemes for silicon carbide (SiC) power MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5570–5581, Oct. 2014.

[8] T. Takamori, K. Wada, W. Saito, and S.-I. Nishizawa, "Gate drive circuit for current balancing of parallel-connected SiC-JFETs under avalanche mode," *Microelectron. Rel.*, vol. 114, 2020, Art. no. 113776.

[9] T. Takamori, K. Wada, W. Saito, and S.-I. Nishizawa, "Paralleled SiC MOSFETs DC circuit breaker with SiC MPS diode as avalanche voltage clamping," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2022, pp. 225–229.

[10] K. Palaniappan, W. Sedano, M. Vygoder, N. Hoeft, R. Cuzner, and Z. J. Shen, "Short-circuit fault discrimination using SiC JFET-based self-powered solid-state circuit breakers in a residential DC community microgrid," *IEEE Trans. Ind. Appl.*, vol. 56, no. 4, pp. 3466–3476, Jul./Aug. 2020.

[11] Y. Sato, Y. Tanaka, A. Fukui, M. Yamasaki, and H. Ohashi, "SiC-SIT circuit breakers with controllable interruption voltage for 400-V DC distribution systems," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2597–2605, May 2014.

[12] D. Marroqui, A. Garrigós, and J. M. Blanes, "LVDC SiC MOSFET analog electronic fuse with self-adjusting tripping time depending on overcurrent condition," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 8472–8480, Aug. 2022.

[13] D. Marroquí, J. M. Blanes, A. Garrigós, and R. Gutiérrez, "Self-powered 380 V DC SiC solid-state circuit breaker and fault current limiter," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9600–9608, Oct. 2019.

[14] A. Garrigós, D. Marroquí, C. Orts, C. Torres, and J. M. Blanes, "Latching current limiter for space platform power distribution using a low-voltage p-MOSFET and a Normally-ON SiC JFET," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5464–5473, Oct. 2022.

[15] D. He, Z. Shuai, Z. Lei, W. Wang, X. Yang, and Z. J. Shen, "A SiC JFET-based solid state circuit breaker with digitally controlled current-time profiles," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1556–1565, Sep. 2019.

[16] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[17] Y. Funaki and K. Wada, "Gate drive circuit implementation for parallel connection of power devices considering parasitic inductance," *IEEJ J. Ind. Appl.*, vol. 12, no. 2, pp. 176–182, Mar. 2023.

[18] N. Boettcher and T. Erlbacher, "Design considerations on a monolithically integrated, self controlled and regenerative 900 V SiC circuit breaker," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, 2020, pp. 1–6.

[19] N. Boettcher and T. Erlbacher, "A monolithically integrated SiC circuit breaker," *IEEE Electron Device Lett.*, vol. 42, no. 10, pp. 1516–1519, Oct. 2021.

[20] N. Boettcher, T. Takamori, K. Wada, W. Saito, S.-I. Nishizawa, and T. Erlbacher, "Fabrication aspects and switching performance of a self-sensing 800 V SiC circuit breaker device," in *Proc. IEEE 34th Int. Symp. Power Semicond. Devices ICs*, 2022, pp. 261–264.

[21] N. Boettcher, T. Takamori, K. Wada, W. Saito, S.-I. Nishizawa, and T. Erlbacher, "Short circuit performance and current limiting mode of a monolithically integrated SiC circuit breaker for DC applications up to 800 V," in *Proc. 24th Eur. Conf. Power Electron. Appl.*, 2022, pp. P.1–P.9.

[22] T. Takamori, K. Wada, N. Boettcher, T. Erlbacher, W. Saito, and S.-I. Nishizawa, "Adjustable current limit feature with a self-sensing and self-triggering monolithically integrated SiC circuit breaker device," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2022, pp. 1–6.

[23] J.-L. Sanchez et al., "A new high-voltage integrated switch: The 'thyristor dual' function," in *Proc. 11th Int. Symp. Power Semicond. Devices ICs*, 1999, pp. 157–160.

[24] J.-P. Laur et al., "A new circuit-breaker integrated device for protection applications," in *Proc. 11th Int. Symp. Power Semicond. Devices ICs*, 1999, pp. 315–318.

[25] A. Würfel, J. Adler, A. Mauder, and N. Kaminski, "Over current breaker based on the dual thyristor principle," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs*, 2016, pp. 143–146.

Taro Takamori (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from the Tokyo University of Science, Tokyo, Japan, in 2019, and the M.S. degree in electrical engineering in 2021 from Tokyo Metropolitan University, Tokyo, where he is currently working toward the Ph.D. degree in electrical engineering. From 2022 to 2023, he was with the Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, Germany, as a Visiting Researcher. His current research interests include characterization and reliability of power semiconductor devices for solid-state circuit breakers.

Keiji Wada (Senior Member, IEEE) was born in Hokkaido, Japan. He received the Ph.D. degree in electrical engineering from Okayama University, Okayama, Japan, in 2000. From 2000 to 2006, he was an Assistant Professor with Tokyo Metropolitan University and the Tokyo Institute of Technology. He became an Associate Professor in 2006 and a Professor in 2021 with Tokyo Metropolitan University. His research interests include gate-drive circuits, electromagnetic interference filters, and power converter circuits. He is a senior member of IEEJ.

Norman Boettcher received the Bachelor of Engineering degree in mechatronics from the Beuth University of Applied Sciences, Berlin, Germany, in 2013, and the Master of Science degree in power- and micro electronics from Reutlingen University, Reutlingen, Germany, in 2016. He is currently working towards the Ph.D. degree in a monolithically integrated circuit breaker device based on a 4H-SiC JFET technology with Friedrich-Alexander University Erlangen-Nuremberg, Erlangen, Germany. Since 2017, he has been with the Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, working on the development of novel semiconductor devices. His research interests include concepting, simulation, fabrication, and characterisation of power electronics.

Tobias Erlbacher received the Diploma in electrical engineering (microelectronics) from the University of Erlangen-Nuremberg, Erlangen, Germany, in 2004, and the Ph.D. degree in 2008. Since 2009, he has been with the Fraunhofer Institute of Integrated Systems and Device Technology IISB, Erlangen, where he is heading the "Devices" Group. He is currently working on design and development of silicon carbide devices for power applications, and high-temperature integrated circuits and sensors. He has authored a book on lateral power transistors in integrated circuits. He has authored or coauthored more than 130 papers in scientific journals and contributed to 16 patents. His research activities focuses on device modeling, design and integration and technology development for power electronics. This includes the monolithic integration of passive networks and the optimization of power semiconductor devices in silicon integrated circuits.

Wataru Saito (Senior Member, IEEE) received the B.Eng., M.Eng., and Dr.Eng. degrees in electrical and electronics engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 1994, 1996, and 1999, respectively. In 1999, he joined the Toshiba Corporation, Kawasaki, Japan, where he engaged in the development of power semiconductor devices. Since 2019, he has been with Kyushu University, Fukuoka, Japan. His research interests include basic research on next-generation power semiconductor devices and related application technologies. He is the Editor of IEEE TRANSACTIONS ON ELECTRON DEVICES. He formerly served on the committee member of Power Devices & ICs Committee in IEEE Electron Device Society from 2015 to 2020. He is a member of the technical program committee of IEEE Electron Devices Technology and Manufacturing Conference. He formerly served on the technical program committees of IEEE International Electron Devices Meeting from 2020 to 2021 and IEEE International Symposium on Power Semiconductor Devices and ICs from 2016 to 2020. He was the recipient of the conference prize paper award in 2008 IEEE Power Electronics Specialists Conference.

Shin-ichi Nishizawa (Member, IEEE) received the B.Eng., M.Eng., and Dr.Eng. degrees in chemical engineering from Waseda University, Tokyo, Japan, in 1989, 1991, and 1994, respectively. Then, he joined Waseda University, Tokyo, Japan, as a Research Associate. In 1996, he joined the Electrotechnical Laboratory, Japan (since 2001, the National Institute of Advanced Industrial Science and Technology). Since 2017, he has been a Professor with Kyushu University, Japan. His research interests include semiconductor wafer and process technologies for power devices and power electronics components and systems.