Studies on Alternative Schemes for the MMC-Based Acceleration Grid Power Supply of DEMO Neutral Beam Injector

Francesco Santoro, Alberto Ferro, Marco De Nardi, and Elena Gaio

***Abstract*— The European DEMO will make use of a significant additional heating power, which could be partly provided by neutral beam injectors (NBIs), which accelerate negative ions by means of grids placed at increasing potentials. These grids will be fed by the acceleration grid power supply (AGPS), divided in a number of stages, which has to provide an overall dc voltage down to −1 MV and currents in the order of tens of Amperes. The AGPS will have to satisfy a set of static and dynamic requirements, mainly in terms of ripple, accuracy, and rise time. In addition, during the NBI operation, frequent losses of insulation between the grids, called breakdowns (BDs), are expected. The AGPS will be able to handle such events by nullifying the output currents as fast as possible in order to limit the energy discharged onto the grids. Adopting the modular multilevel converter (MMC) technology for the AGPS of DEMO and future tokamaks seems promising, due to its intrinsic properties of modularity, high efficiency, fast dynamic response and small energy transferred to the arc in case of BD. Since the converter will be air-insulated, one of the main drawbacks is the large volume occupied. This can be partly reduced by adopting alternative MMC schemes, to minimize the number of components and optimize the counter-voltage applied by the converter at BD. In this article, alternative topologies for the MMC submodules (SMs) or combinations of different schemes [full-bridge (FB), half-bridge (HB)] are investigated. After a preliminary design of the converter, the results of numerical simulations carried out with circuit models are shown, with control schemes customized for the NBI operation. The performance of the different solutions in steady-state, dynamic and anomalous conditions are discussed, with particular focus on BD events. Finally, thermal analyses on the converter are carried out, to verify whether natural convection of air can be a suitable cooling method for the power components.**

***Index Terms*— Power conversion, power supplies.**

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I. Introduction

THE European DEMO project has entered the Conceptual Design Phase in 2021 [1]. During this phase, will be analyzed and then defined the most suitable technologies for the plant electrical system (PES), that includes all subsystems involved in the supply of electrical power for DEMO loads, as outlined in [2]. The heating and current drive mix that will be installed in DEMO is still under evaluation and, until a final decision, neutral beam injection is a possible option [3].

The pre-conceptual design of the neutral beam injector (NBI) currently foresees, as in ITER, to accelerate negative ions of Hydrogen isotopes at −1 MeV in five stages, each with an acceleration grid placed at increasing potentials from −1 MV to 0 kV with steps of 200 kV [4]. The grids are fed by a dedicated power supply, the acceleration grid power supply (AGPS), which is composed of five stages of 200 kV and 60 A each, in series. During the NBI operation, the breakdown (BD) between the grids, will be a frequent event. A BD, from the point of view of the AGPS, is basically a short circuit at its output. The power supply has to be able to handle such events by stopping the rise of the current and bringing it to zero as fast as possible, then resume the operation once the arc is extinguished. It is also important to limit the energy delivered to the arc to avoid damaging the grids. The main preliminary electrical requirements, reported in Table I, have been assumed equal to the ones for ITER NBI AGPS [5].

A solution for DEMO NBI AGPS, based on the AGPS for ITER and its full scale prototype, MITICA, under construction in Padua, consists of a two-stage conversion system that makes use of HV diode rectifiers and HV dc-filters insulated in SF_6; the system is presented in detail in [6] and [7], and a simplified scheme is presented in Fig. 1(a). Another solution is based on the modular multilevel converter (MMC) technology, whose theoretical feasibility of being adopted as AGPS for DEMO has been proven in [8]. The MMC-based AGPS, shown in Fig. 1(b), would allow a modular structure, a single conversion stage, a direct control over the output voltage, a reduced dc-filter, from which derives also a low energy discharged at the BD and the insulation of the components in air. Air-insulation is the only reasonable choice for such an extremely large number of components, as dielectric gases or liquids, or vacuum, would require to enclose the converter in a huge vessel, making also difficult the maintenance. MMCs are widely employed in commercial applications such as HVDC

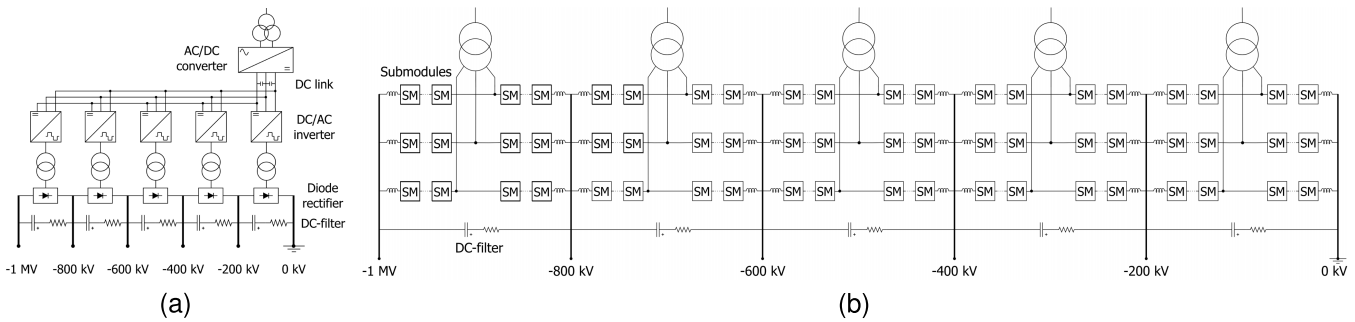

Fig. 1. Simplified schemes of the possible DEMO AGPS solutions. (a) ITER/MITICA-like solution. (b) MMC-based solution.

TABLE I
MAIN ELECTRICAL REQUIREMENTS OF DEMO NBI AGPS

Parameter	Value
Rated voltage	-1 MV
Number of stages	5×200 kV
Voltage accuracy (referred to full voltage)	$\pm 2\%$
Max voltage ripple, referred to set voltage	$\pm 5\%$
Max rise time of the output voltage	80 ms
Max voltage undershoot at beam on	15%
Voltage regulation range	20–100%
Rated current	~ 60 A
Switch-off delay in case of BD	$\sim$ tens of μs
Maximum charge transferred to the arc	~ 100 mC per stage
Time to be ready for restart after a BD	20 ms

transmission, but, for the AGPS application, the converter would have unique requisites, like the handling of BDs with subsequent restart, a wide output voltage regulation range, and a limited ripple for the whole voltage range. A drawback of this technology applied to the AGPS is the volume occupied, much larger than the ITER/MITICA-like solution, since most components are air-insulated. To mitigate this issue, in this article have been studied alternative MMC schemes to the one in [8], with the aim of reducing the clearances required for the insulation and the number of components.

II. MODULAR MULTILEVEL CONVERTER

The converter has a modular structure: the constitutive element of the MMC, the submodule (SM), is composed of IGBTs with antiparallel diodes and a capacitor. The SMs can be controlled to produce a variable voltage. A string of SMs in series with an inductor forms an arm. There are two arms per phase, six in total, and are named upper and lower arms to be easily identifiable. The arm inductor has the role of limiting the dc-faults current and reducing the high-frequency harmonics of the current in the arm. A general scheme of a three-phase MMC is depicted in Fig. 2.

The MMC, from a three phase ac input (with line voltage v_{ac}), can produce a dc output voltage V_{dc}. For each phase, neglecting the voltage drops on the arm inductors, are valid the following relations of instantaneous voltages:

$$V_{dc} = v_l + v_u \tag{1a}$$

$$v_{ac} = \frac{v_l - v_u}{2} \tag{1b}$$

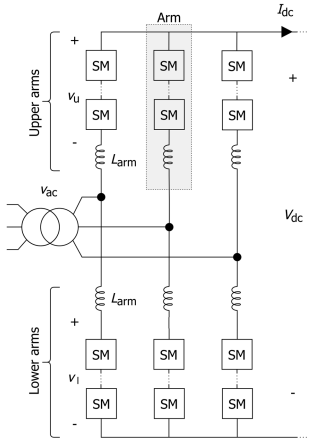

Fig. 2. General scheme of a three-phase MMC.

where v_l and v_u are, respectively, the voltages on the lower and upper arm (not including the arm inductors, as in Fig. 2), which are directly controllable by inserting or bypassing SMs. Besides the ac component from the input and the dc from the output, in the arms is flowing also the circulating current, which is a current component present only in the six arms that does not affect the input and output of the converter.

The main types of SMs are the half-bridge (HB) and the full-bridge (FB), whose scheme are depicted in Fig. 3(a) and (c). As presented in Fig. 3(b) and (d), the SMs can produce a voltage at the output by inserting the capacitor: for the HB the output voltage is unipolar, instead for the FB is bipolar. The FB SM has also the inherent feature of blocking dc-fault currents by switching off its IGBTs.

Typically, MMC are composed of only HB or FB SMs. In [8] it has been used as reference a FB-based MMC, opportunely designed. The FB-based MMC would provide the maximum operational flexibility since its voltage could be adjusted from the nominal value to its opposite. In addition, it could handle grid BDs by switching off the IGBTs: the SM capacitors will result inserted with opposite voltage to the ac voltages so that the currents are driven to zero. At the BD it will result a voltage on the arm inductors approximately equal to the sum of the capacitor voltages of the switched-off SMs in each arm since in that moment is formed a loop with just the inductors and the capacitors of those SMs. Part of the SMs, instead of being switched off, could be switched to the

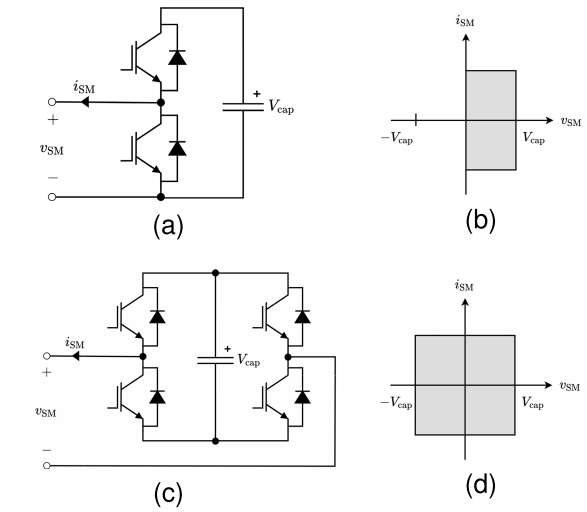

Fig. 3. Schemes of the main MMC SMs. (a) HB SM scheme. (b) HB operating region. (c) FB SM scheme. (d) FB operating region.

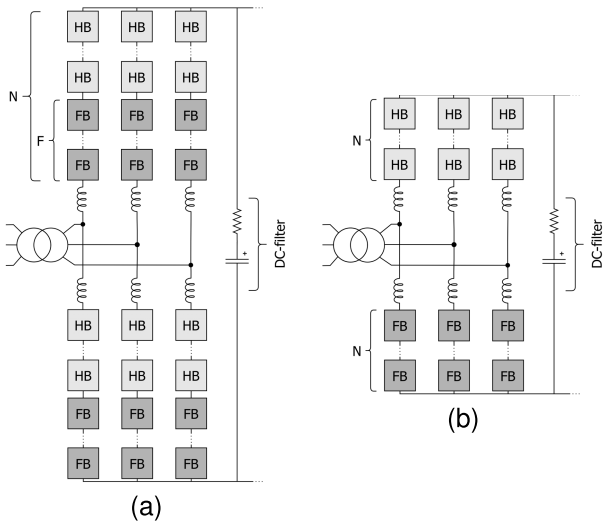

Fig. 4. Scheme of Hybrid MMCs. (a) HS-MMC. (b) HA-MMC.

bypass state so that the voltage applied on the arm inductors is reduced and, as a consequence, also the necessary insulation clearance. However, the number of power semiconductors is extremely large.

On the other hand, the HB-based MMC is not able to bring to zero the BD current and it allows a too limited adjustability of the output voltage, as described in [9] in Chapter 1, thus it is not considered suitable for this application.

In the following will be presented MMC topologies with a reduced number of components, making a mixed use of HB and FB SMs, hence called Hybrid MMCs. Hybrid MMCs require specific control techniques, which will be briefly introduced.

A. Hybrid Symmetric MMC (HS-MMC)

The HS-MMC has the same number of HB and FB SMs in the lower and upper arms, hence the attribute "symmetric." Its scheme is depicted in Fig. 4(a), where N and F indicate, respectively, the number of SMs per arm and of FB SMs per arm. This topology has been extensively reviewed in [10].

The voltage on the capacitors of the HB SMs is balanced (i.e., close to their reference value) only if the current becomes positive and negative in each cycle, while for the FB SMs the balance can be achieved also with just positive or negative current. Thus, in the HS-MMC, to maintain the balance between the HB and FB SMs, the dc voltage cannot go lower than the peak ac voltage $\hat{v}_{ac}$ [10]. This makes the HS-MMC somewhat limited in their dc output voltage range, but $\hat{v}_{ac}$ can be chosen in order to allow to obtain the lowest dc voltage required $V_{dc,min}$, which is 20% of the nominal dc voltage $V_{dc,nom}$ ($V_{dc,min} \leq V_{dc} \leq V_{dc,nom}$). The minimum number of FB SMs that allows to produce this voltage range is $F = (N/3)$, derived from the indications in [10]. The components of the arm reference voltages can be expressed explicitly with the following vectorial (containing the values for the three phases) equations:

$$\boldsymbol{v}_{u,ref} = \frac{V_{dc,ref}}{2} - \boldsymbol{v}_{s,ref} - \boldsymbol{v}_{c,ref} \tag{2a}$$

$$\boldsymbol{v}_{l,ref} = \frac{V_{dc,ref}}{2} + \boldsymbol{v}_{s,ref} - \boldsymbol{v}_{c,ref} \tag{2b}$$

where $V_{dc,ref}$ is the set dc voltage, $\boldsymbol{v}_{s,ref}$ are the reference values of the ac component of the arm voltages and $\boldsymbol{v}_{c,ref}$ are the reference values of the voltages that drive the circulating currents. The quantities $\boldsymbol{v}_{s,ref}$ and $\boldsymbol{v}_{c,ref}$ are computed by the control system. From the equations in (2), the sum of the upper and lower arm voltages is equal to $V_{dc,ref}$ plus the voltage applied on the arm inductors, which is $2 \cdot \boldsymbol{v}_{c,ref}$.

The HS-MMC is capable of driving the BD current to zero and limiting the voltage resulting on the arm inductors by bypassing the HB SMs instead of switching them off. The voltage across the arm inductors, with this strategy, would be about proportional to the number of FB SMs per arm that result inserted, instead to the number of all SMs.

B. Hybrid Asymmetric MMC (HA-MMC)

The HA-MMC has the upper arms composed of only HB, while the lower arms by FB SMs; its scheme is depicted in Fig. 4(b). This topology has been proposed by Jung for HVDC transmission systems [11].

Differently from the HS-MMC, the HA-MMC does not require that the current in the lower arms becomes positive and negative in every cycle due to the presence of only FB SMs, as explained in Section II-A. The dc component of the upper arm voltage v_u is the same for every value of V_{dc} and set to half the nominal dc voltage, while it is adjusted accordingly to V_{dc} the dc component of the lower arm voltage v_l. The components of the arm voltages can be expressed explicitly with the following vectorial equations:

$$\boldsymbol{v}_{u,ref} = \frac{V_{dc,nom}}{2} - \boldsymbol{v}_{s,ref} - \boldsymbol{v}_{c,ref} \tag{3a}$$

$$\boldsymbol{v}_{l,ref} = \left(V_{dc,ref} - \frac{V_{dc,nom}}{2}\right) + \boldsymbol{v}_{s,ref} - \boldsymbol{v}_{c,ref} \tag{3b}$$

where $V_{dc,nom}$ is the maximum value that V_{dc} can reach.

The HA-MMC is also able of bringing the BD current to zero, but since the HB SMs insert their capacitor only if i_{SM}

from Fig. 3(a) is negative, with positive arm current any upper arm would be short-circuited. Among the loops in which the ac current flows, some include an upper arm and a lower arm or another upper arm. In those, at the BD, the upper arm with positive arm current will be completely bypassed and the other arm, to provide enough voltage to oppose the one on the ac side, must have a number of SMs resulting inserted double than the HS-MMC to compensate for the bypassed arm and have a similar behavior. Thus, at least a number of SMs per arm double than the HS-MMC needs to be turned-off instead of bypassed, which means the voltage on the arm inductors can be two times larger than in the HS-MMC at the BD.

Preliminary simulations showed that, differently from the HS-MMC, for the HA-MMC the circulating current control is needed, to maintain the capacitor voltage balanced between the arms, resulting in a dc voltage ripple about five times larger (this side effect of the circulating current control is explained in the following section). For these reasons, the HS-MMC has been selected for further investigations.

For comparison, the total number of IGBTs required per stage would be 2400 for a FB-based MMC, 1800 for a HA-MMC and 1596 for a HS-MMC (as will be defined in Section IV).

III. Control Scheme

The control scheme of a MMC is composed of multiple stages to control different quantities. A simplified diagram of the control that has been implemented for the HS-MMC is presented in Fig. 5(a). The main quantities controlled are the dc voltage V_{dc}, the upper and lower arm currents, respectively, the vectors $\boldsymbol{i}_{\mathrm{u}}$ and $\boldsymbol{i}_{\mathrm{l}}$, and the SM capacitors voltage.

The dc voltage and the ac current are regulated through proportional integral (PI) controllers which use as reference, respectively, the set dc voltage and the output of the "dc-bus control," which regulates the dc voltage.

The fundamental frequency of the circulating current, which is double the line frequency, can be suppressed to reduce power losses by implementing appropriate control methods, such as proportional resonant (PR) controllers [12]. This kind of control has a downside: its output appears as high-frequency ripple at the dc side of the converter. Due to this reason, to prioritize a lower output ripple than the removal of the double line frequency harmonic, the control is only active during the ramp-up of the voltage (during which the ripple is not a concern). Then the control is switched-off and the ac component of the circulating current starts flowing.

After the voltage reference for the arm is computed as in (2), is determined the number of SMs which needs to be inserted with the phase-shifted pulsewidth modulation (PS-PWM). It compares the insertion index of each arm with as many triangular carriers as the number of SMs which are phase shifted one another by an angle φ^i, defined as follows:

$$\varphi^i = \frac{2\pi}{N}(i-1) \quad \text{for } i = 1, \ldots, N. \tag{4}$$

To further minimize the dc voltage ripple it has been added a variable shift, indicated as θ, between the lower and upper arm carriers. Defining the relative voltage level as

$$m_{\mathrm{dc}} = \frac{V_{\mathrm{dc,ref}}}{V_{\mathrm{dc,nom}}} \tag{5}$$

for even values of $m_{\mathrm{dc}} \cdot N$ the shift is $\theta = 0$, while for odd values is $\theta = (\pi/N)$.

The SMs inserted are chosen by a sorting algorithm, based on the one proposed in [12] and adapted specifically for the HS-MMC, which adds or removes SMs only when the number of SMs to be inserted N_{new} changes, thus when $N_{\mathrm{new}} \neq N_{\mathrm{old}}$. The sign of variation on the number of SMs, $\Delta N = N_{\mathrm{new}} - N_{\mathrm{old}}$, indicates whether insert or bypass $|\Delta N|$ SMs. The complete diagram of the algorithm is presented in Fig. 5(b).

IV. Preliminary Design

The higher the ac voltages, the lower are the currents flowing in the arms, but due to the characteristics of the HS-MMC, the maximum ac peak voltage that guarantees the balance between HB and FB SM capacitors during the operation at the minimum dc voltage is $\hat{v}_{\mathrm{s}} = 30$ kV. The highest voltage, and thus the lowest current, is preferred as it minimizes the current ratings of the components (inductors, IGBTs and capacitors).

From the power balance of the ac input and dc output of the converter, it is possible to calculate the expected ac peak currents at nominal conditions as follows:

$$\hat{\imath}_{\mathrm{s,nom}} = \frac{2 \cdot V_{\mathrm{dc,nom}}\, I_{\mathrm{dc,nom}}}{3 \cdot \hat{v}_{\mathrm{s,nom}}} = \frac{2 \cdot 200\ \mathrm{kV} \cdot 60\ \mathrm{A}}{3 \cdot 30\ \mathrm{kV}} \approx 267\ \mathrm{A}. \tag{6}$$

The current flowing in the SMs is the combination of the dc, ac, and circulating currents, computed as follows:

$$\begin{aligned} I_{\mathrm{SM,nom}} &= \frac{I_{\mathrm{dc,nom}}}{3} + \frac{\hat{\imath}_{\mathrm{s,nom}}}{2} + \hat{\imath}_{\mathrm{c}} \\ &= \frac{60}{3} + \frac{267}{2} + 70\ \mathrm{A} \approx 223\ \mathrm{A} \end{aligned} \tag{7}$$

where the approximate value of $\hat{\imath}_{\mathrm{c}}$ has been obtained from the simulations. A commercial IGBT module, manufactured by ABB, has been selected to be used as reference for choosing the main parameters of the sub modules. It has been chosen a phase leg IGBT module rated for a collector-emitter voltage $V_{\mathrm{CES}} = 3.3$ kV and a continuous dc collector current $I_{\mathrm{C}} = 450$ A. It can sustain a peak forward current I_{FRM} of 900 A for up to 1 ms. The module is composed of the series of two IGBTs, each with its antiparallel diode, so HB SMs will require one and FB SMs will require two. The complete datasheet can be found in [13].

The sum of the voltages of the SM capacitor per arm is chosen equal to the maximum which needs to be produced, increased of 15% for margin, which gives

$$V_{\mathrm{cap,tot}} = 1.15 \cdot \left(\frac{V_{\mathrm{dc,nom}}}{2} + \hat{v}_{\mathrm{s,nom}} \right) \approx 150\ \mathrm{kV}. \tag{8}$$

The voltage of the single capacitor is determined by the collector-emitter voltage of the IGBT module V_{CES} divided by a safety factor of 2, as follows:

$$V_{\mathrm{cap,nom}} = \frac{V_{\mathrm{CES}}}{2} = \frac{3.3\ \mathrm{kV}}{2} \approx 1.5\ \mathrm{kV}. \tag{9}$$

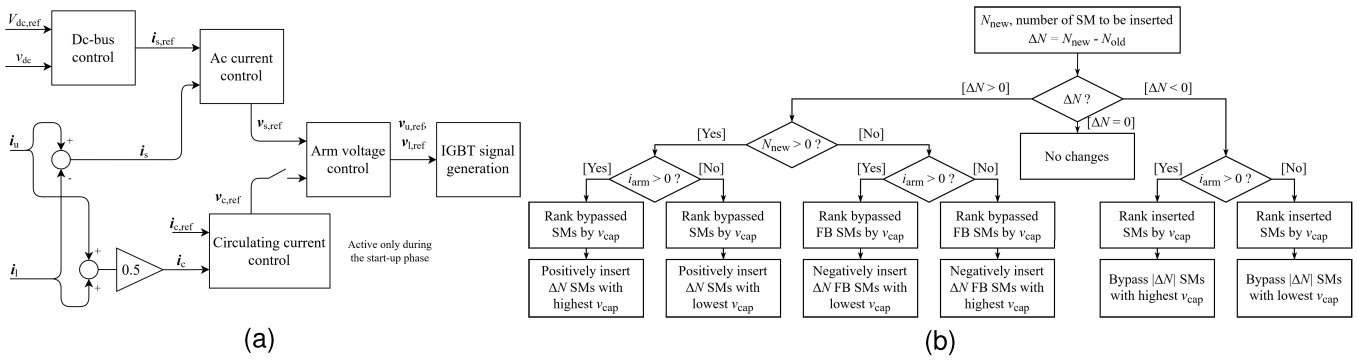

Fig. 5. (a) Simplified diagram of the control scheme implemented for the HS-MMC. (b) Diagram of the SM sorting algorithm.

The number of SMs per arm can now be computed as

$$N = \frac{V_{\text{cap,tot}}}{V_{\text{cap,nom}}} = \frac{150\ \text{kV}}{1.5\ \text{kV}} = 100 \tag{10}$$

of which $F = (N/3)$ are FB SMs and the remaining HB SMs.

The energy that each SM has to provide every period can be computed as follows:

$$\Delta E_{\text{SM}} = \frac{\Delta E_{\text{arm}}}{N} = \frac{2 \cdot P_{\text{dc,nom}}}{3 \cdot m_{\min}\, \omega\, N}\left(1 - \left(\frac{m_{\min}}{2}\right)^2\right)^{\frac{3}{2}} \tag{11}$$

where $m_{\min}$ is the minimum modulation index, defined as $m = (2 \cdot \hat{v}_{\text{s}}/V_{\text{dc}})$ and is minimum for $V_{\text{dc}} = V_{\text{dc,nom}}$. An initial estimate of the SM capacitance, for $V_{\text{cap,nom}} = 1.5$ kV, has been obtained from the following equation [14]:

$$C_{\text{SM}} = \frac{\Delta E_{\text{SM}}}{2 \cdot V_{\text{cap,nom}}^2\, \delta_{\text{cap,pp}}} \approx 2.5\ \text{mF} \tag{12}$$

where $\delta_{\text{cap,pp}}$ is the normalized peak to peak voltage ripple on the capacitor, chosen to be $\delta_{\text{cap,pp}} = 7.5\%$.

The equivalent switching frequency of the converter has been assumed equal to $f_{\text{eq}} = 20$ kHz: a high frequency can reduce the ripple at the output and then require a smaller filter but it may lead to excessive commutation losses on the power components. The resulting switching frequency of the single SM is

$$f_{\text{SM}} = \frac{f_{\text{eq}}}{2 \cdot N} = 100\ \text{Hz}. \tag{13}$$

The arm inductors have been sized to limit the current at BD below the maximum interruptable current by the IGBT module, I_{CM}. In the worst case, the voltage on the arm inductor can reach $(V_{\text{dc,nom}} + \hat{v}_{\text{ll}}/2)$, where $\hat{v}_{\text{ll}} = \sqrt{3} \cdot \hat{v}_{\text{s}}$ is the ac line to line voltage, for an estimated duration of $t_{\text{d}} = 10$ µs, which takes into account the BD detection time and the commutation delay of the IGBTs, with margin. In the SPIDER experiment [15], the delay between the BD and the actual turn-off of the IGBTs is about 5 µs, thus the assumed value t_d could be feasible. The inductance needed to limit the current from $I_{\text{SM,nom}}$ to I_{CM} in the time t_{d} is

$$L_{\text{arm}} = \frac{\left(V_{\text{dc,nom}} + \hat{v}_{\text{ll}}\right)t_{\text{d}}}{2\left(I_{\text{CM}} - I_{\text{SM,nom}}\right)} = \frac{(200 + 52\ \text{kV})10\ \mu\text{s}}{2(900 - 223\ \ \text{A})} \approx 2\ \text{mH}. \tag{14}$$

The choice of the dc-filter capacitance is a trade-off between a reduced voltage ripple and a limited amount of energy discharged at the BD. In the simulations, the best performances were obtained with a capacitance of $C_{\text{filter}} = 25$ nF. In ITER and MITICA, for comparison, for each 200 kV stage, the dc-filter capacitance is 300 nF [5]. In series, there is a resistor whose role is to limit the current peak of the discharge of the dc-filter at the BD to a maximum of $I_{\text{grids,max}} = 3$ kA. The resistance can be chosen as

$$R_{\text{filter}} = \frac{V_{\text{dc,nom}}}{I_{\text{grids,max}}} = 67\ \Omega. \tag{15}$$

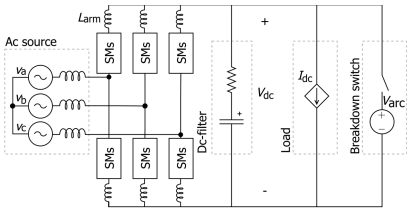

Fig. 6. Simplified schematic of the model used to simulate the converter.

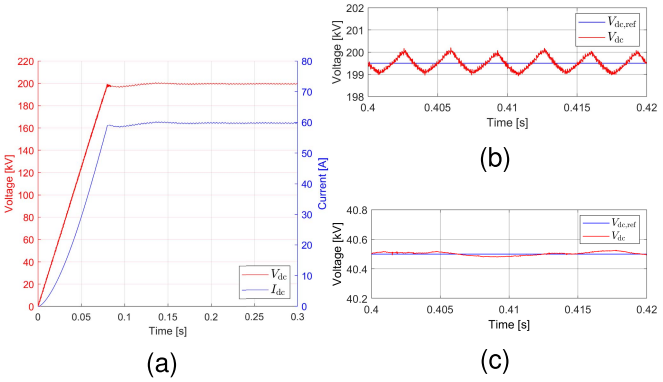

Fig. 7. Waveforms at the startup of the converter and steady state. (a) Voltage and current on the dc side at $V_{\text{dc,nom}}$. (b) Detail of the dc voltage at $V_{\text{dc,nom}}$. (c) Detail of the dc voltage at $0.2 \cdot V_{\text{dc,nom}}$.

V. Simulations With a Circuit Model

To verify the performance of this converter and its suitability as the AGPS for the DEMO NBI, a circuit model has been developed to perform numerical simulations, depicted in Fig. 6. The model does not take into account parasitic elements, which will be studied in future design stages since they may have a significant impact during transients and on the

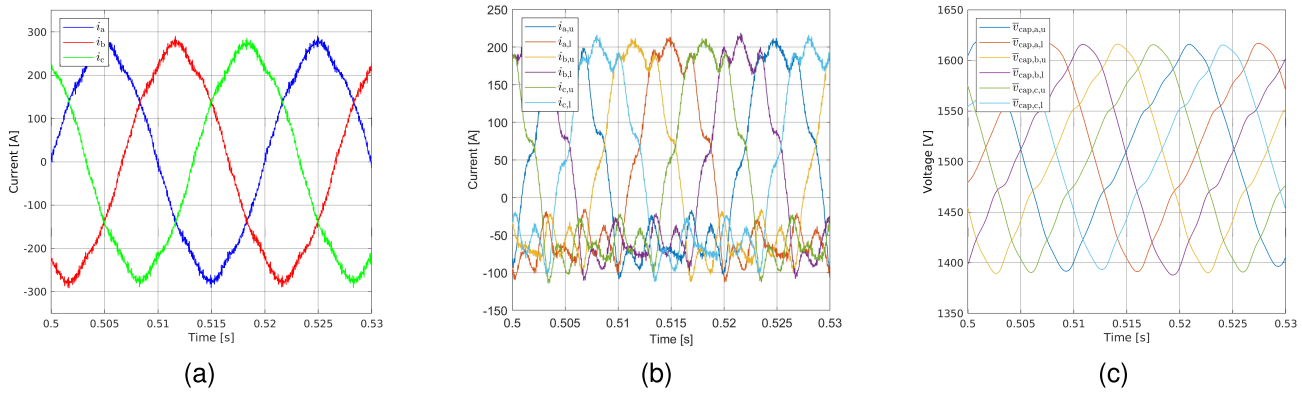

Fig. 8. Waveforms during steady state at $V_{\mathrm{dc,nom}}$. (a) AC currents. (b) Arm currents. (c) Average SM capacitor voltage per arm.

charge delivered to the arc. The load has been modeled as an ideal controlled current source, whose current depends on the accelerating voltage V_{dc} according to the perveance matching law, as follows:

$$I_{\mathrm{dc}} = p \cdot V_{\mathrm{dc}}^{\frac{3}{2}} \tag{16}$$

where p is the perveance constant, which depends on the physical characteristics of the grids and of the accelerated ions.

The startup, steady state, and BD conditions were simulated on the circuit model. The results are reported and analyzed in the following paragraphs.

A. Startup and Steady State

In Fig. 7(a) are presented the dc output voltage and current waveform at the startup of the converter. The voltage increases with a voltage ramp and reaches $0.9 \cdot V_{\mathrm{dc,nom}}$ within 80 ms, as the requisite in Table I. In Fig. 7(b) and (c) are, respectively, pictured a detail of the dc voltage to highlight the ripple, respectively, for $V_{\mathrm{dc}} = V_{\mathrm{dc,nom}}$ and $V_{\mathrm{dc}} = V_{\mathrm{dc,min}} = 0.2 \cdot V_{\mathrm{dc,nom}}$. As it can be seen, the ripple is always below 0.5% of the set output voltage in the whole voltage range.

In Fig. 8 are presented the waveforms during steady state at $V_{\mathrm{dc,nom}}$: in particular, in Fig. 8(a) is depicted the ac current, with a THD of about 4.5%, in Fig. 8(b) the arm current, which is not much sinusoidal due to the lack of the circulating current control, and in Fig. 8(c) the average voltage on the SM capacitors, which is stable within ±10% of the nominal capacitor voltage.

B. Thermal Model

In order to estimate the expected temperature on the SMs in case of different cooling techniques, the semiconductors have been modeled with a Foster network model [16] integrated in the circuit model. The scheme of the model is presented in Fig. 9.

The power losses are computed as the sum of the conduction losses and of the switching losses of the IGBT or the recovery losses of the diode, which are given in the manufacturer's datasheet in function of the flowing current in the component, along with the thermal parameters of the module.

The heatsink to ambient thermal resistance $R_{\mathrm{th,H-A}}$ assumed is based on the indications reported in [16] and on the

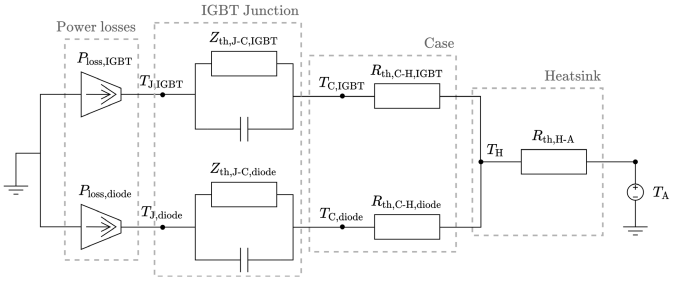

Fig. 9. Simplified scheme of the thermal model of an IGBT, where "J" stands for junction, "C" for case, "H" for heatsink and "A" for ambient.

datasheet of a heatsink, model P 3/120, manufactured by Semikron [17]. From the simulations resulted that the IGBT module would operate at an average junction temperature of:

1) 140 °C with natural air convection ($R_{\mathrm{th,H-A}} = 600$ K/kW);
2) 60 °C with forced air convection ($R_{\mathrm{th,H-A}} = 100$ K/kW);
3) 45 °C with water cooling ($R_{\mathrm{th,H-A}} = 10$ K/kW).

Since the first case would be too close to the maximum operating temperature, 150 °C, and a water cooling would be much more complex to implement, forced air convection may be an adequate solution.

C. Breakdown

The BD has been simulated with an ideal switch and a dc voltage source that represents the arc voltage (estimated as $V_{\mathrm{arc}} \approx 100$ V), in parallel to the load, as in Fig. 6. After a delay time of 10 µs, the IGBTs are all switched off in FB SMs, while the HB SMs are turned in bypass-state.

In Fig. 10 are presented the waveforms of the operation during a BD that take place at $t = 0.13$ s. Due to the sudden stop of operation after the detection of the BD, the SM capacitors remain charged at different voltages, as can be seen in Fig. 10(b). After a waiting time of 20 ms to ensure the arc is extinguished, the converter restarts the operation. The arm currents, in Fig. 10(c), do not exceed 900 A. As presented in Fig. 10(d), the total charge delivered at the arc after the BD, $\int i_{\mathrm{tot}}\,\mathrm{d}t$, computed as the integral of the current on the short circuit, resulted about 60 mC, of which 5 mC due to the dc-filter, noted as $\int i_{\mathrm{filter}}\,\mathrm{d}t$. The difference is the component of just the AGPS, $\int i_{\mathrm{AGPS}}\,\mathrm{d}t$. This value is below the requested

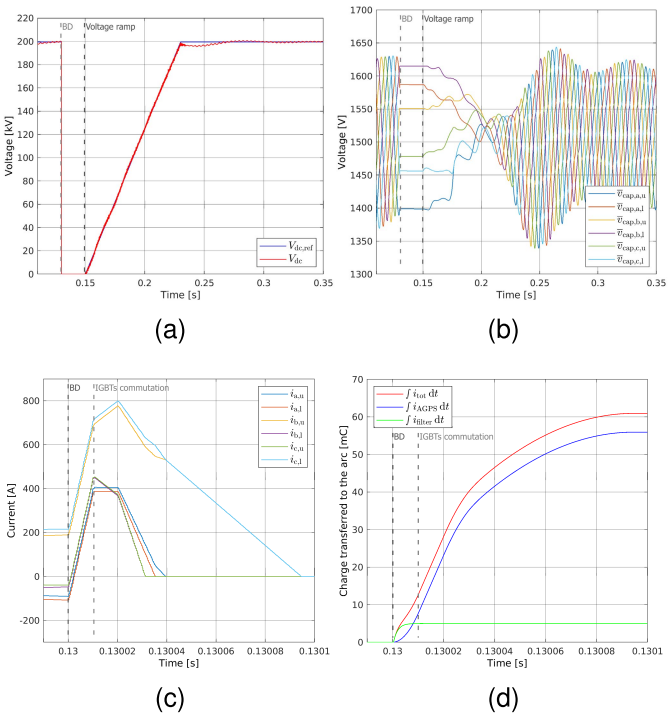

Fig. 10. Waveforms at the BD. (a) DC voltage. (b) Average SM capacitor voltage per arm. (c) Arm currents. (d) Charge transferred to the arc.

value in Table I, but it could be improved by optimizing the value of L_{arm}. The charge, in the case of the ITER/MITICA-like AGPS, has been estimated of about 95 mC, of which 60 mC due to the dc-filter [18].

VI. Conclusion

This article presents the studies to further optimize the conceptual design of a MMC-based AGPS for DEMO NBI. The use of the HS-MMC topology reduces the number of power semiconductors and at the same time satisfies the requirements indicated in Table I, in particular the current blocking capability, the output voltage range, and the maximum p.u. ripple allowed for any set voltage. The control methods have been modified in order to minimize the ripple at the output voltage and the number of commutations. After having selected the main parameters, it has been developed a model to perform numerical simulations. The model showed a very low voltage ripple and limited charge delivered to the arc after the BD. From the simulations, resulted that forced air cooling would be sufficient to keep the junction temperature of the IGBT modules below the maximum acceptable.

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