Prototype Inductive Adders With Extremely Flat-Top Output Pulses for the Compact Linear Collider at CERN

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***Abstract*— The compact linear collider (CLIC) study is exploring the scheme for an electron–positron collider with high luminosity and a nominal center-of-mass energy of 3 TeV. The CLIC predamping rings (DRs) and DRs will produce, through synchrotron radiation, ultralow emittance beam with high bunch charge, necessary for the luminosity performance of the collider. To limit the beam emittance blow-up due to oscillations, the pulse generators for the DR kickers must provide extremely flat, high voltage, pulses. The specifications for the DR extraction kickers call for a 160- or 900-ns duration flat-top pulse of ±12.5 kV, with a combined ripple and droop of not more than ±0.02% (±2.5 V) for each pulse: an inductive adder is a very promising approach to meet the specifications. Recently, the first 20 layer, 12.5 kV, full-scale prototype inductive adder has been assembled at CERN and testing has commenced. This paper presents flat-top stability and repeatability measurements of the output waveforms of this full-scale prototype inductive adder for CLIC DR kicker systems. The pulse waveforms have been recorded with an oscilloscope which has nominally 16-bit resolution and allows measurements of minimum and maximum envelope curves for a large number of consecutive output waveforms. Both passive and active modulation methods have been applied to improve the relative flat-top stability of the prototype inductive adder to meet the specification of ±0.02%.**

***Index Terms*— Analog modulation, compact linear collider (CLIC), droop compensation, inductive adder, pulse power modulator, ripple compensation.**

I. Introduction

THE compact linear collider (CLIC) would be a high-energy electron–positron collider [1]. It could provide very clean experimental environments and steady production of all particles within the accessible TeV energy range. To achieve high luminosity at the interaction point, it is essential that the beams have very low transverse emittance: the pre-damping ring (PDR) and damping ring (DR) damp the beam emittance to extremely low values in all three planes. Two different RF system frequencies were originally considered for the CLIC DR system, namely, 1 and 2 GHz [1]: the 1-GHz RF system is the current baseline.

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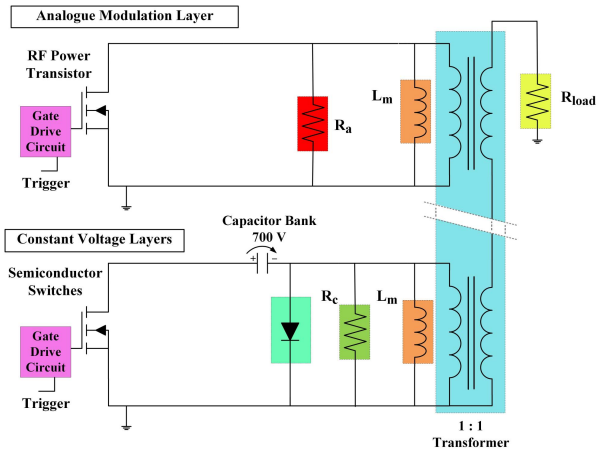

Fig. 1. Schematic of an inductive adder with a single constant voltage layer, with core loss resistance R_c and magnetizing inductance L_m.

Stripline kickers are required to inject beam into and extract beam from the PDRs and DRs [2]. Jitter in the magnitude of the kick waveform would cause beam jitter at the interaction point [3]. Hence, in particular, the DR extraction kicker must have a very small magnitude of jitter: the 2-GHz RF specifications called for 12.5-kV pulses of 160-ns duration flat-top, with a combined ripple and droop of not more than ±0.02% [1]. The 1-GHz specifications call for a burst of two 160-ns duration flat-top pulses with 580 ns between the end of the flat-top of the first pulse and the beginning of the flat-top of the second pulse, which can be fulfilled, e.g., with a 900 ns, continuous, flat-top duration. The requirements for the voltage and stability during these two 160-ns sections of the flat-top are the same as for the 2-GHz design, i.e., ±0.02% at 12.5 kV [1]. The flat-top repeatability requirements are also extremely tight, ±0.01%, for both RF system designs [1].

II. Inductive Adder

A review of the literature of existing pulse generators has been carried out and an inductive adder (Fig. 1) has been selected as the most promising means of achieving the specifications for the DR kickers [4]. The inductive adder is a solid-state modulator, which can provide relatively short and precise pulses. An early reference about design principles of an inductive adder is given in [5] and an extensive summary of previous development of inductive adders at the Lawrence

TABLE I
SPECIFICATIONS FOR THE INDUCTIVE ADDER FOR CLIC DR EXTRACTION KICKER

Output voltage (kV)	12.5
Nominal output impedance (Ω)	50
Output current (A)	309
Flat-top duration (ns)	160 or 900 (excl. settling time)
Desired pulse rise/fall time (ns)	100/100
Flat-top stability (%)	±0.02
Flat-top repeatability (%)	±0.01

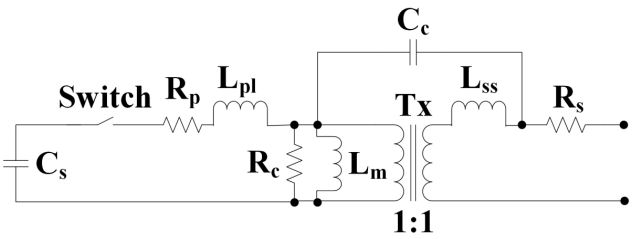

Fig. 2. Simplified equivalent circuit of a single layer of an inductive adder.

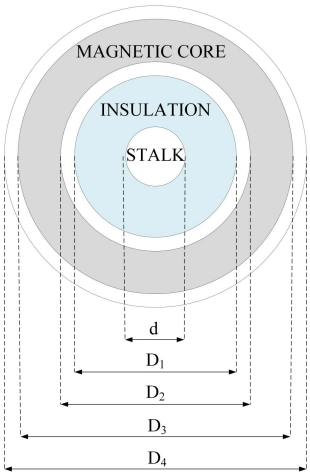

Fig. 3. Cross section of an inductive adder cell.

Livermore National Laboratory in [6], with examples of using modulation techniques for adjusting output waveforms. More recent research on inductive adders, also called inductive voltage adders or linear transformer drivers in the literature, have been carried out for Pockels cells divers for the National Ignition Facility [7], fast kicker systems at the Lawrence Berkeley National Laboratory [7], and industrial applications of pulsed power [9].

With a careful design of the inductive adder, it may be possible to directly meet the ripple and droop requirements of the PDR kicker and analog modulation may provide a means to meet the demanding specifications for the DR extraction kicker [10], [11]. The reasoning for choosing the main components of the inductive adder has been given in [11]. Two 5-layer, 3.5 kV, prototype inductive adders have been assembled and tested at CERN. The design parameters and the initial results for these pulse modulators were presented in [12] and [13]. The prototype inductive adders have been equipped with an analog modulation layer, which can be used to compensate the droop and ripple of the output waveform. Operation of the passive and active modulation layers has been verified with measurements and the results have been presented in detail in [14], [15], [16, pp. 189–207], and [17]. Evaluation of magnetic core material and custom-made magnetic cores for the full-scale, 12.5-kV, prototype inductive adders was presented in [17]. The detailed electrical design of the full-scale prototype inductive adder was presented in [18]. Holma *et al*. [17] and Holma and Barnes [18], [19] presented measurements on the first five layers of the full-scale prototype inductive adder. Holma and Barnes [18], [19] presented initial measurements on the first 20 layer, full-scale, prototype inductive adder with 10 or 17 constant voltage layers installed and one analog modulation layer in operation. This paper is a continuation of these studies.

III. DESIGN OF THE 12.5-kV PROTOTYPE INDUCTIVE ADDER

A. Specifications for the Prototype Inductive Adder

Table I shows the specifications for the 12.5-kV prototype inductive adder for the CLIC DR extraction kicker system. In this system, the inductive adder generates pulses for a stripline kicker, which has a characteristic odd-mode impedance of 40.5 Ω [2]. The stripline kicker has two electrodes and for odd-mode operation, during extraction, these electrodes are pulsed to equal magnitude but opposite polarity voltages. The stripline electrodes may be terminated with their odd-mode characteristic impedance, and therefore the nominal output current of the inductive adder, at 12.5 kV, would be 309 A. The even-mode characteristic impedance of the stripline kicker is seen by the passing beam when the kicker is not powered and this has been optimized to 50 Ω [2].

For the CLIC baseline option, which has a 1-GHz RF system for the DR, the flat-top duration for the output pulse is either 160 or 900 ns, depending on the RF system design of the DRs [1]: the 900 ns option could also be two pulses of 160-ns flat-top with 580-ns gap between flat-top sections. The full-scale prototype inductive adder has been designed to supply pulses with up to 1100-ns flat-top duration. The specified maximum allowable total pulse duration, including rise time, flat-top duration, and fall time, is approximately 2.2 μs [1]. However, to limit stress on the kicker system, the desired rise and fall times are in the range of 100 ns. The required pulse flat-top stability of ±0.02%, i.e., ±2.5 V for ±12.5 kV operation, defines the allowance for the combined droop and ripple for a single pulse. The pulse flat-top repeatability defines the allowed difference for any consecutive pulses and it is specified to be ±0.01%, which corresponds to ±1.25 V, for ±12.5-kV operation.

B. Electrical and Mechanical Design of the Prototype Inductive Adder

Fig. 2 shows a simplified equivalent circuit of a single layer of an inductive adder and Fig. 3 shows the cross section of an inductive adder cell. Table II shows the electrical parameters

TABLE II
DESIGN PARAMETERS FOR THE 12.5-kV INDUCTIVE ADDER FOR CLIC DR EXTRACTION KICKER

Electrical parameters	
Output voltage (kV)	±12.5
Nominal output impedance (Ω)	50
Flat-top duration (ns)	1100 (incl. settling time)
Insulation material	air ($\varepsilon_r = 1$)
L_{pl} (nH)	6.6
L_{ss} (nH)	7.1
C_c (pF)	5.7
R_c (Ω)	140
L_m (μH)	58
C_s (μF)	96
Physical dimensions (see Fig. 3)	
Height of a magnetic core (mm)	50 (2 x 25)
Height of a cell (mm)	60
d (mm)	60
D1 (mm)	108
D2 (mm)	142
D3 (mm)	286
D4 (mm)	334

and physical dimensions for the full-scale 12.5-kV prototype. The insulation material for the prototype inductive adder, between the stalk and housing of the magnetic cores, is air. The nominal output impedance of the prototype inductive adder is 50 Ω and the measurements shown in this paper have been carried out with a 50-Ω load. The output impedance has been chosen according to the availability of commercial coaxial cables and feedthroughs. According to simulation studies shown in [16, pp. 125–131], 110 ns is the maximum predicted settling time if the output impedance of the inductive adder is 50 ± 15 Ω, the pulse rise time is 50–150 ns, and the odd-mode impedance of the stripline kicker is 41 Ω. In this simulation, the total single way propagation delay of an inductive adder and a cable between the adder and the striplines was 13 ns and the single way delay of striplines was 7 ns [16, pp. 125–131]. The design value for the maximum flat-top duration of the prototype inductive adder is 1100 ns, to allow up to 200 ns for the settling time of the output voltage, and therefore there is enough margin for the required settling time which is caused by the mismatch of the odd-mode impedance of the striplines.

The electrical parameters, shown in Fig. 2 and Table II, are the following: L_{pl} is the primary loop inductance, R_c is the loss resistance of a magnetic core, L_m is the magnetizing inductance of a magnetic core, C_c is the parasitic coupling capacitance per cell between the primary and secondary windings of the coaxial transformer structure, and C_s is the total capacitance of the pulse capacitors per layer. R_p and R_s in Fig. 2 are the resistances of a primary and secondary, respectively, associated with a cell.

The main components for the prototype are shown in Table III. Both NWL T00216 capacitors [24] and custom-made Leclanché pulse capacitors [25] have been used in the primaries of the full-scale prototype adder. Design steps and evaluation of pulse capacitors, MOSFETs, and magnetic core material for the 12.5-kV prototype inductive adder were presented in detail in [16, pp. 52–78 and pp. 166–172]. For the final prototype design presented here, parameters in Table II have been revised to the latest values.

TABLE III
MAIN COMPONENTS FOR THE 12.5-kV CLIC DR EXTRACTION KICKER INDUCTIVE ADDER

Component	***Manufacturer***	***Type***
Gate driver	IXYS [22]	IXDD614SI
MOSFET	Microsemi [23]	APT12057LFLL
Pulse capacitor #1	NWL [24]	T00216
Pulse capacitor #2	Leclanché [25]	PPM-4 170-12.0 a
Transformer core	Hitachi-Metals [26]	Finemet FT-3L

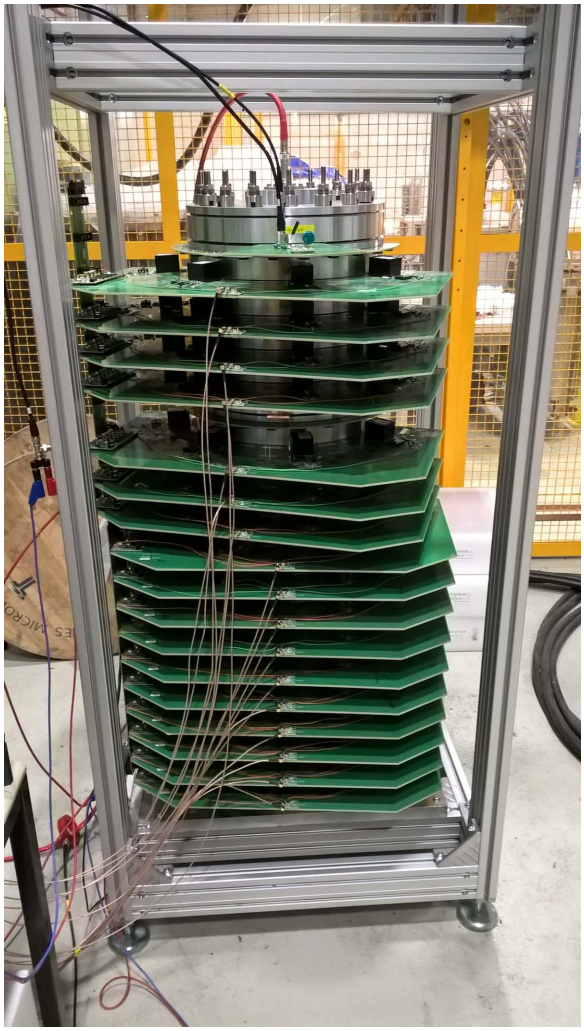

Fig. 4. Photograph of the first 20 layer, 12.5 kV, prototype inductive adder assembled at CERN, with 17 constant voltage layers and one analog modulation layer. Each layer is 6 cm high and the total height of the stack with output feedthroughs is approximately 1.5 m.

IV. MEASUREMENTS SETUP

Measurements were carried out with a 20 layer, full-scale, prototype inductive adder for the CLIC DR kicker systems (Fig. 4). For the tests and measurements reported here, the prototype inductive adder was equipped either with 14 or 17 constant voltage layers. In addition, in measurements with modulation, the adder was also equipped with one analog modulation layer, i.e., 15 or 18 layers in total. The remaining two or five layers out of 20 layers of the prototype inductive adder were short circuited on the primary side and the effect

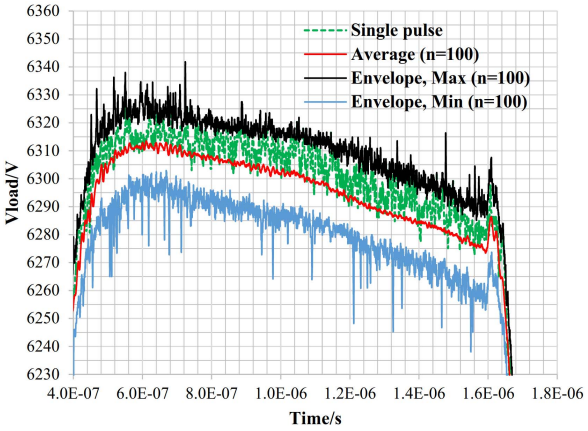

Fig. 5. Measured load voltage V_{load} of the 20 layer full-scale prototype for a single pulse and for an average of 100 pulses: the plot also shows a minimum and a maximum envelope for 100 pulses. The inductive adder was equipped with 17 constant voltage layers. The initial capacitor voltage was 386 V.

of the short circuits, on the output waveform, is considered to be negligible. The main reason for this configuration was availability of the printed circuit boards (PCBs) for the primary circuit at the time when the measurements for this paper were carried out. Four current branches were powered in each constant voltage layer: each current branch consisted of either a single NWL T00216, 12 μF, [24] or a Leclanché PPM-4 170-12 a, 12 μF [25], pulse capacitor, and an APT12057LFLL [23] MOSFET. The output voltages recorded in measurements were between 6.3 and 6.5 kV and the initial capacitor voltages of the constant voltage layer were 400 V per layer with 17 constant voltage layers and 494 V per layer with 14 constant voltage layers. The output waveforms were recorded with a Rohde & Schwarz RTO1004 oscilloscope [27], with a high-resolution option, which has a specified resolution of 14 effective bits in the required bandwidth of 100 MHz. The load used in the measurements shown in this paper was 50 Ω, which was built from a set of noninductive, high voltage, resistors manufactured by HVR [28].

V. Measurements Without Analog Modulation

Fig. 5 shows a measured output waveform of the 20 layer full-scale prototype with 17 constant voltage layers installed: the output pulse waveform was not modulated. In this measurement, the pulse capacitors of each layer were initially charged to 386 V. The peak output voltage was 6.31 kV, which corresponds approximately to a half of the nominal voltage of the CLIC DR extraction kicker systems. The pulse flat-top duration was 1150 ns and the total pulse duration approximately 1.4 μs. In Fig. 5, the single pulse is shown as a green curve, the average of 100 pulses as a red curve and the minimum and maximum envelopes of 100 pulses as a blue and a black curve, respectively. The measured droop of the output waveform is 32 V (0.5%) over 900 ns, which is the maximum required flat-top duration for the CLIC DR kicker systems, and 38 V (0.6%) over 1000 ns, from the maximum amplitude of the flat-top to the end of the flat-top. In Fig. 5, the measured minimum and maximum envelopes, for

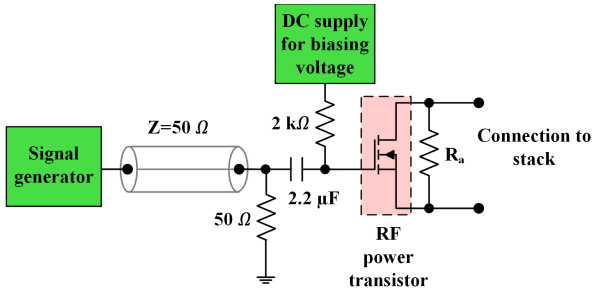

Fig. 6. Schematic of the analog modulation layer used in the measurements.

100 pulses, are mainly within ±20 V (±0.3%) in comparison with an ensemble average of 100 pulses; however, the largest single-sample variations are up to ±43 V (±0.7%).

The measured minimum and maximum envelopes were initially assumed to be dominated by the repeatability of the flat-top of the pulses of the prototype inductive adder. Hence, several measurements were also carried out in order to improve flat-top repeatability, i.e., by applying common-mode or differential-mode noise filters on: 1) the output of the high-voltage dc power supply, which was used to charge the pulse capacitors of the prototype inductive adder and 2) the low-voltage dc power supply, which feeds the gate drivers. Measurements were also carried out at different charging voltages of the capacitors of the constant voltage layers and pulse waveforms were recorded. The measurements were carried out with the first five assembled layers of the prototype inductive adder with capacitor voltages in the range of 100–500 V and were reported in [19]. To conclude, the filters did not improve the measured minimum and maximum envelopes and there was not a clear correlation between the output voltage and the measured flat-top minimum and maximum envelopes. However, it was observed that the envelopes, measured for 100 pulses, were approximately ±0.2% of the maximum range of the channel of the Rohde & Schwarz RTO1004 oscilloscope: this occurred for all three sensitivities selected. Therefore, it was assumed that the measured minimum and maximum envelopes, shown in Fig. 5, were actually determined by noise which was created in the measurement setup, e.g., by the oscilloscope and not by the inductive adder. Hence, the repeatability of the flat-top of the pulses was supposed to be better than the difference of the measured minimum and maximum envelopes for, e.g., 100 pulses. This is investigated further in Section VII.

VI. Measurements With Passive Analog Modulation

Measurements were also carried out by applying passive and active analog modulation. The operation principle of an analog modulation layer is described in detail in [29]. In the measurements shown here, the prototype inductive adder was equipped with 17 constant voltage layers and one analog modulation layer. The analog modulation layer consisted of a resistor R_a (Figs. 1 and 6), which was 2.4 Ω, and an RF power transistor type ARF463AP1G, manufactured by Microsemi [23]. The schematic and design of the analog modulation layer are

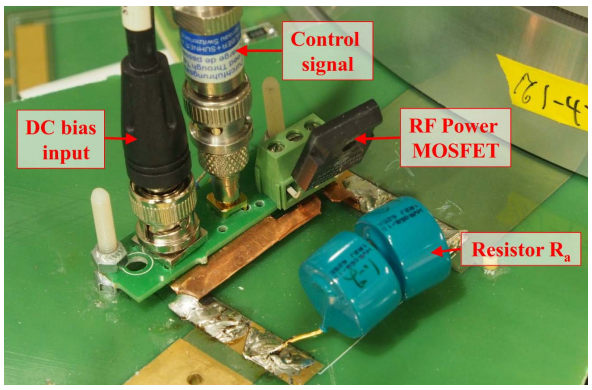

Fig. 7. Photograph of the analog modulation layer.

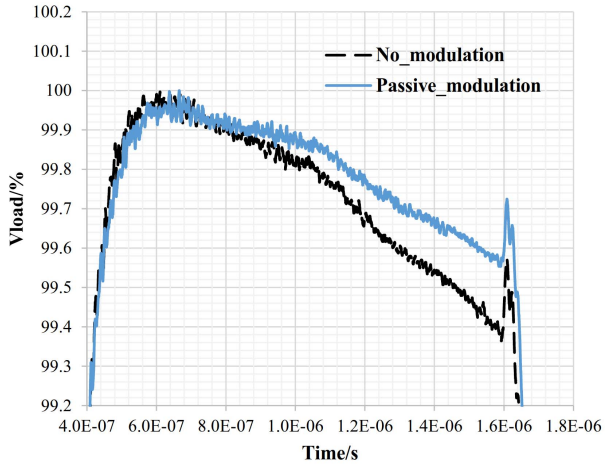

Fig. 8. Measured load voltage without modulation (black, dashed) and with passive modulation (blue curve). The inductive adder was equipped with 17 constant voltage layers and, in the case of passive modulation, with a single passive analog modulation layer with resistor $R_a = 2.4\ \Omega$. The initial capacitor voltage of each constant voltage layer was 386 V without modulation and 400 V in the case when passive modulation was applied.

described in detail in [16, pp. 176 and 178], the simplified schematic is shown in Fig. 6 and a photograph of the PCB is shown in Fig. 7. A point to note is that the resolution of the analog modulation, i.e., the minimum amplitude change of the output waveform of an inductive adder, is defined by the minimum change in the input signal to the analog modulation layer within the bandwidth of the analog modulation layer and the inductive adder stack. The modulation bandwidth is limited by the cutoff frequency of the stack: this can be estimated as the cutoff frequency of an inductor–resistor type low-pass filter, which is formed by the inductance of the stack and the load [29]. For the 20 layer prototype inductive adder this frequency is 56 MHz.

The blue curve in Fig. 8 shows the measured output voltage of the prototype inductive adder in the case where passive modulation ($R_a = 2.4\ \Omega$) was applied: the RF power MOSFET, shown in the schematic in Fig. 6, was not conducting. For comparison, the waveform without modulation is also shown, as a black dashed line, in Fig. 8. In both measurements, the maximum amplitude was approximately 6.3 kV. The curves are normalized to a 100% maximum amplitude. The droop of the output waveform was decreased from 0.6% to 0.4% by applying passive modulation. In the case in which modulation was applied, the flat-top stability corresponds to ±0.2% over 900 ns, for the flat-top duration, from an elapsed time of 700–1600 ns in Fig. 8.

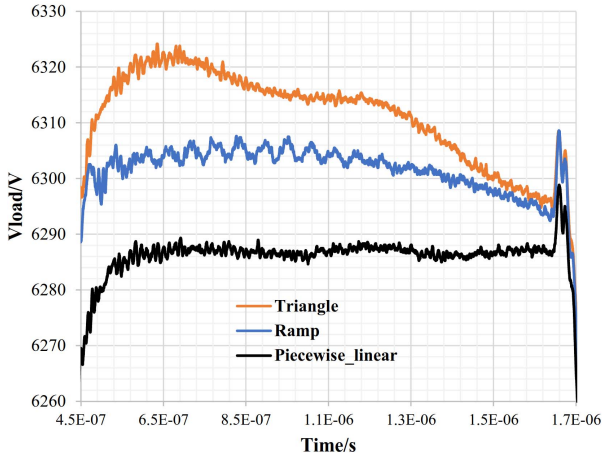

Fig. 9. Measured load voltage with active analog modulation. Three different control waveforms are used: triangle (orange, top), ramp (blue, middle), and piecewise linear (black, bottom). The curves are averages of 100 consecutive waveforms.

VII. Measurements With Active Analog Modulation

A. Measurements on a Stability of a Flat-Top Pulse

In the measurements shown in this section, the goal was to generate a flat-top pulse with the required flat-top stability and flat-top duration for the CLIC DR extraction kicker system. Active analog modulation was applied to improve the flat-top stability with respect to the curves shown in Fig. 8. Fig. 9 shows three intermediate steps to improve the flat-top stability with active analog modulation. The control signal waveform for the RF power transistor of the analog modulation layer (Fig. 6) was a triangle (orange, these top), a ramp (blue, middle), and a piecewise linear function (black, bottom) in these measurements. All curves in Fig. 9 are averages of 100 consecutive waveforms. In addition to the control signal, the RF power transistor was biased with a dc power supply, similar to that described in [13]. With the triangle waveform (orange, top), the flat-top of the pulse droops by approximately 27 V and the flat-top stability is in this case ±0.2% (±13.5 V) over 900 ns, from an elapsed time of 650–1550 ns. In the case where a ramp waveform was applied (blue, middle), the pulse flat-top is a rounded bump and the flat-top stability is ±0.1% (±7 V) over 900 ns. With a piecewise linear waveform (black, bottom), the flat-top stability is ±0.04% (±2.5 V) over 900 ns. This waveform was subsequently modified to improve the flat-top stability further.

Fig. 10 shows the best measured flat-top waveform for two different measurements. In Fig. 10, the orange curve (top) is an average of 1000 measured pulses and the blue curve (bottom) is an average of 100 measured pulses. The offset difference of the measurements was most probably caused by thermal drift

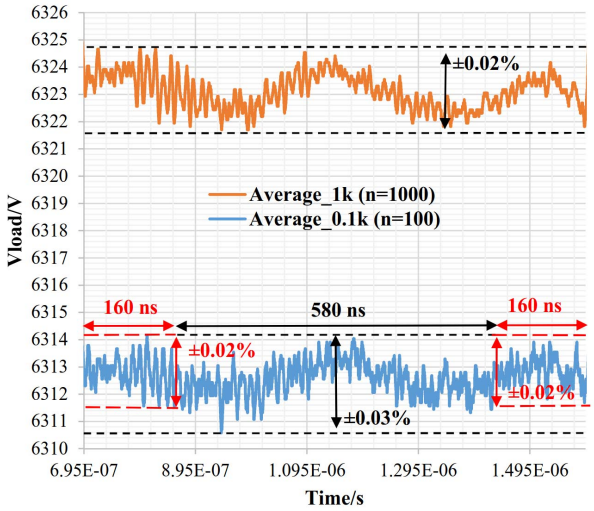

Fig. 10. Measured load voltage with active analog modulation. The orange curve (top) and blue curves (bottom) are an average of 1000 pulses and 100 pulses, respectively. The prototype inductive adder was equipped with 17 constant voltage layers and a single active analog modulation layer.

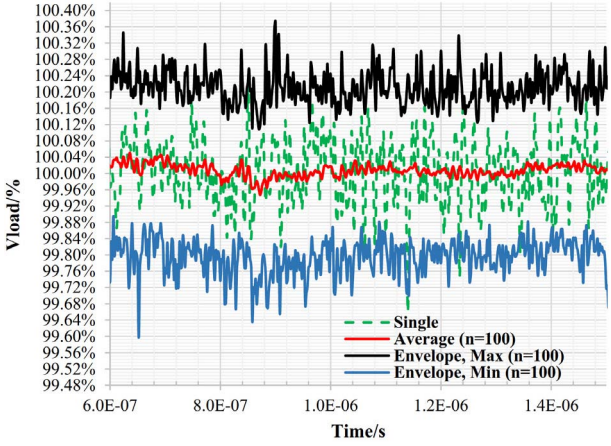

Fig. 11. Measured load voltage with active analog modulation. The red curve (middle) is an average of 100 pulses and the black (top) and blue (bottom) curves are maximum and minimum envelopes, respectively, of 100 pulses. The vertical sensitivity setting of the oscilloscope was 1 kV/div. The prototype inductive adder was equipped with 14 constant voltage layers, and a single active analog modulation layer.

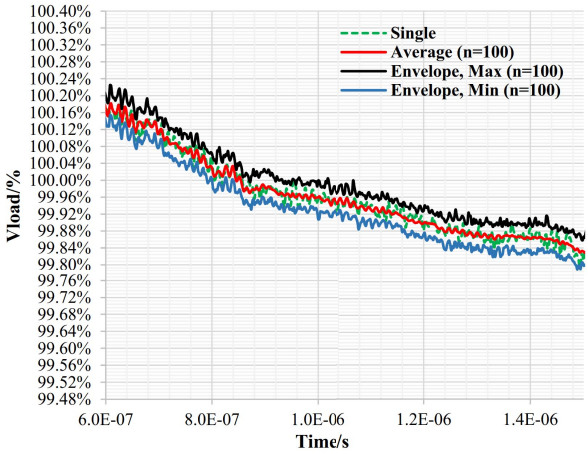

Fig. 12. Measured load voltage with active analog modulation. The red curve (middle) is an average of 100 pulses and the black (top) and blue (bottom) curves are maximum and minimum envelopes of 100 pulses. The vertical sensitivity setting of the oscilloscope was 0.1 kV/div.

in components or in the high-voltage power supply, which charges the pulse capacitors. For the blue curve, the measured flat-top stability is ±0.03% (±1.80 V) over the full 900-ns flat-top duration, at 6.3 kV. However, the flat-top stability is ±0.02% (±1.35 V) over the first 160 ns and the last 160 ns of the flat-top duration, as labeled in Fig. 10. This fulfills the CLIC DR requirements for the flat-top stability of the pulse modulator, for both 1 and 2 GHz specifications of the DRs [1], at approximately a half of the nominal required voltage.

For the orange (top) curve, shown in Fig. 10, the flat-top stability is ±0.02% (±1.55 V) over 900 ns, at 6.3 kV. An average of 1000 pulses, instead of 100 pulses, theoretically increases the resolution of the measurement by ∼1.7 bits [30]. Therefore, the average of 1000 pulses can theoretically be considered to be more accurate than the average of 100 pulses.

B. Measurements on a Repeatability of a Flat-Top Pulse

Fig. 11 shows the average of 100 measured output waveforms (red, middle), a single pulse (green), and minimum and maximum envelopes (blue and black, respectively) for 100 measured waveforms. The prototype inductive adder was equipped with 14 constant voltage layers and one analog modulation layer and the initial capacitor voltage in the constant voltage layers was 494 V. In this measurement the vertical sensitivity setting of the oscilloscope channel was set to 1 V/div and the channel range was 10 V. The dynamic range of the signal from the current transformer (CT) was smaller than the dynamic range of the channel. The conversion coefficient of the CT input signal to the load voltage was 1000 and the measured load voltage was in this case 6.437 kV. In Fig. 11, the curves are shown as relative values with respect to 6.437 kV. The minimum and maximum envelopes are within ±0.4% with respect to the average of the load voltage and this range corresponds to ±0.3% of the range of the oscilloscope channel. The range of the minimum and maximum envelopes is similar to the case where modulation was not applied, which is shown in Fig. 5. Applying active analog modulation either does not degrade the flat-top repeatability, or the degradation of flat-top repeatability is smaller than arbitrary, asynchronous, noise in the measurement setup. The flat-top stability for the average of 100 pulses is ±0.03% over 900 ns in Fig. 11.

Fig. 12 shows the average of 100 measured output waveforms (red, middle), a single pulse (green), and minimum and maximum envelopes (blue and black, respectively) for 100 measured waveforms and for the prototype inductive adder with the exactly same measurement settings as in Fig. 11. The only difference was that in this case the vertical sensitivity of the oscilloscope channel was set to 0.1 V/div and the channel range was 1 V. In this case the dynamic range of the signal from the CT was larger than the dynamic range of the oscilloscope channel, and therefore, an offset of −5.6 V was applied, in order to measure the flat-top of the signal only. This was the smallest sensitivity setting with adequate

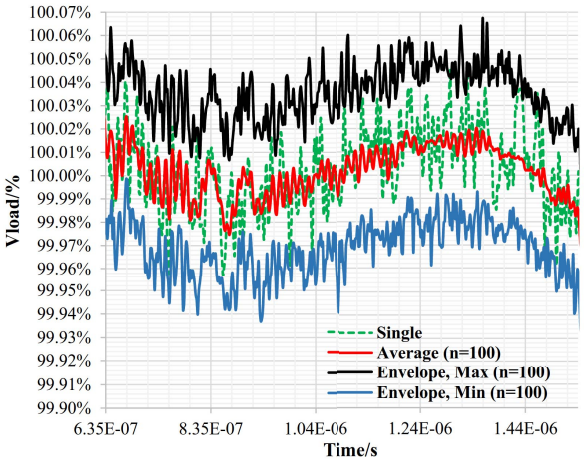

Fig. 13. Measured load voltage with active analog modulation. The red curve (middle) is an average of 100 pulses and the black (top) and blue (bottom) curves are maximum and minimum envelopes of 100 pulses. The vertical sensitivity setting of the oscilloscope was 0.1 kV/div.

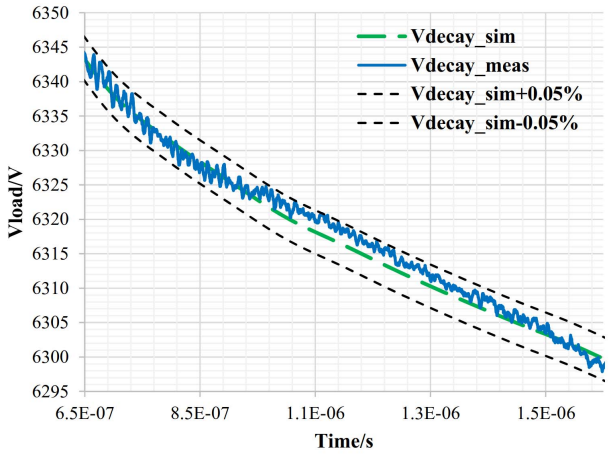

Fig. 14. Simulated optimum waveform for CLIC DR extraction kicker (green, dashed) with ±0.05% stability margins (black, dashed), and an average of 100 measured pulses (blue curve) for the prototype inductive adder, with 17 constant voltage layers and a single active analog modulation layer.

offset range which could be applied with the Rohde & Schwarz RTO1004 oscilloscope used in these measurements. In Fig. 12, the minimum and maximum envelopes are within ±0.06% with respect to the average of the measured waveforms. This range corresponds to ±0.3% of the range of the oscilloscope channel. The flat-top stability of the average for 100 pulses in Fig. 12 is approximately ±0.2% over 900 ns. This measurement was completed with the same settings as the measurements shown in Fig. 11. Clearly, the time domain response of the oscilloscope channel was changed when the sensitivity setting was adjusted and offset applied. The reason for this is not known exactly, but may be related to saturation and recovery of the amplifiers.

Fig. 13 shows measurements in which the stability of the average of the output waveform was adjusted back to the same range as in Fig. 11 by applying analog modulation with a modified control signal. In Fig. 13, the average (red) of 100 measured output waveforms, a single pulse (green), and minimum and maximum envelopes (blue and black, respectively) for 100 measured waveforms are shown. The flat-top stability is within ±0.03% over 900 ns and the minimum and maximum envelopes are within ±0.6% with respect to the average of the 100 pulses. The range of the envelopes is comparable to measurements shown in Fig. 12. Also in this case, the minimum and maximum envelopes correspond to ±0.3% of the range of the oscilloscope channel.

The main conclusion from the measurements shown in Figs. 11–13 is that the sensitivity setting of the oscilloscope significantly effects the measured minimum and maximum envelopes, i.e., it is the main contributor to the repeatability of the measurements. The amplitude of the measured noise depends on the sensitivity setting of a channel. The absolute amplitudes of the minimum and maximum envelopes decreased by a factor of ten when the dynamic range of the channel was decreased by a factor of ten; however, this also caused the shape of the measured waveform to change significantly. Similar measurements were also carried out for intermediate sensitivity settings, between 0.1 and 1.25 V/div and the results were the same: the minimum and maximum envelopes for the recoded pulses were ±0.3% of the range of the oscilloscope channel for all ranges tested.

Regarding the stability of the measured averages of 100 pulses, shown in Figs. 11–13, it is impossible to define exactly which of these is the most realistic, i.e., closest to the average of 100 real waveforms. However, it was shown with these measurements that the flat-top stability, averaged for 100 pulses, could be corrected with analog modulation to be within ±0.03% over 900 ns with both sensitivity settings: this gives confidence that, provided that the flat-top can be accurately measured, e.g., with beam, the analog modulation can appropriately correct the flat-top waveform shape to be within specification. It can also be supposed that the worst pulse out of 100 recorded pulses in Figs. 12 and 13 is within the envelopes, i.e., ±0.6% with respect to the average. Further measurements and applying other measurement techniques are needed to verify the repeatability and the actual stability of a single pulse. These are discussed in Section IX.

C. Measurements With Active Analog Modulation on a Controlled Decay Waveform

In this measurement, the goal was to generate a waveform, which produces the required total electric and magnetic field for the CLIC DR kicker striplines. In optimization studies of the prototype CLIC DR striplines, it was found that the characteristic odd-mode impedance is frequency dependent and in order to generate the required flat-top total field within the stability requirements, the voltage and current need to be modulated during the pulse. The required waveform for the voltage and current is called a controlled decay waveform and it has been derived from detailed simulations [33]. Fig. 14 shows a simulated optimum controlled decay waveform (green, dashed) with ±0.05% error margins for stability (black, dashed) and the measured load voltage (blue) for the prototype inductive adder with active analog modulation.

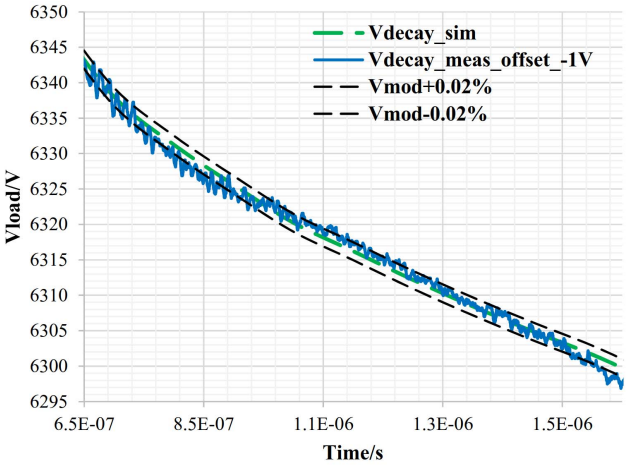

Fig. 15. Simulated optimum waveform for CLIC DR extraction kicker (green, dashed) with ±0.02% stability margins (black, dashed), and an average of 100 measured pulses (blue curve) with −1-V offset for the prototype inductive adder, with 17 constant voltage layers and a single active analog modulation layer.

The measured waveform in Fig. 14 is an average of 100 pulses and the pulse flat-top duration shown is 900 ns. The simulated, optimum, waveform was normalized to 6.3 kV, which is a half of the required nominal output voltage for the CLIC DR kicker striplines. The maximum allowed difference between the optimum, simulated, waveform and the measured voltage is ±0.02% over either 160 or 900 ns, depending on the final specifications. The ensemble average of 100 measured waveforms shown in Fig. 14 is within the ±0.05% error margins; however the stability is not yet adequate, i.e., within ±0.02%, over the full pulse duration of 900 ns. Fig. 15 shows the same measured output waveform but with mathematically applied −1-V dc offset (blue), together with the simulated optimum controlled decay waveform (green) and ±0.02% error margins for stability (black, dashed). The absolute amplitude of the load waveform is not critical, therefore applying an offset for the measured load voltage is acceptable. In Fig. 15, the ensemble average or 100 measured waveforms is within ±0.02% over 200 ns, from 1.3 to 1.5 μs, and therefore, the requirement of the relative ±0.02% stability is fulfilled over this 160 ns.

The main reason for the difference between the simulated and measured waveforms is an error in the shape of the control signal between 950 and 1450 ns and relatively large ripple, approximately ±0.04%, over the first 100 ns of the waveform (Fig. 14), i.e., from 650 to 750 ns elapsed time. This ripple is approximately at 70 MHz, which is theoretically above the cutoff frequency of the inductive adder setup. However, this frequency corresponds to the two-way propagation delay of the high-voltage coaxial cable between the inductive adder and the load, which was approximately 14 ns, and therefore, this ripple was caused by the mismatch of the load impedance, i.e., partial reflection of the pulse from the load. Improvement of the stability of the decay waveform requires further tests and measurements. However, there is not any known hardware limitation as to why the decay waveform could not be improved further with the current prototype inductive adder. Improvement of the pulse shape will be the main subject for further studies in the near future.

D. Flat-Top Stability and Repeatability of the Measurements

1) Flat-Top Stability: In the measurements presented in this paper, the best measured flat-top stability, i.e., the combined ripple and droop, was ±0.02% (±1.55 V) for a 900-ns flat-top duration at 6.3 kV and this was measured for an average of 1000 waveforms. This measurement fulfills the relative and absolute flat-top stability of the 1 and 2 GHz specifications for the CLIC DR extraction kicker systems, although at approximately half of the nominal output voltage. However, the actual voltage and current waveforms for the CLIC DR extraction kicker need to be controlled decay waveforms, as was shown in Section VII-C. This waveform was generated with ±0.02% flat-top stability over 160ns and ±0.05% over 900 ns with respect to the simulated, optimum, waveform (Fig. 14).

In all stability measurements shown in this paper, the stability was measured by using ensemble averaging of 100 or 1000 pulses in order to improve the bit resolution. Ensemble averaging can be applied to reduce the noise of the pulse waveform if the noise is considered to be arbitrary and asynchronous with the pulse. At first, in all measurements shown in this paper, averaging effectively reduced the noise significantly, which means that it was not synchronous with the pulse. Second, the cut-off frequency of the prototype inductive adder with the load is estimated to be 56 MHz, as was explained in Section VI. This is the main reason to expect that the high-frequency components beyond that frequency were not generated by the prototype inductive adder. Also, the time jitters in the turn-ON of the MOSFET switches and gate drivers used in the inductive adder stack are small, the datasheets show nanosecond range, and all the constant voltage layers were equipped with trigger cables of equal length and all trigger cables were supplied from the same trigger source. Therefore, the use of ensemble averaging in the measurements of the waveform stability is considered to be appropriate for improving the bit resolution and to filter arbitrary noise. The stability of a single pulse could not be defined with adequate resolution with the current measurement setup. However, it can be concluded that in the measurements of the minimum and maximum envelopes, shown in Figs. 12 and 13, even the worst pulse was within the ±0.06% range of the measured ensemble average.

In Section VII-B, it was shown that the change of the sensitivity setting of the oscilloscope also changed the time domain response of the channel during the pulse and, as a result, the measured stability was degraded from ±0.03% to ±0.2% over 900-ns pulse flat-top. However, as it was shown, the stability could be adjusted back to ±0.03% over 900 ns by analog modulation. According to these measurements, the resolution and bandwidth of the analog modulation method was found to be adequate for the required waveform stability range of the CLIC DR extraction kicker system.

2) Flat-Top Repeatability: The requirement for the flat-top repeatability for the CLIC DR kicker inductive adders

is ±0.01% at 12.5 kV. In the measurements shown in this paper, it was found that the minimum and maximum envelopes were dominated by the sensitivity settings of the oscilloscope. In measurements shown in this paper, the minimum and maximum envelopes were approximately ±0.2%–0.3% of the maximum range of the channel, at all sensitivity settings tested. A point to note is that the minimum and maximum envelopes had the same relative maximum amplitude of ±0.3% of the channel range with and without the analog modulation. Therefore, applying of analog modulation did not degrade the flat-top repeatability so significantly that it would have been seen by the envelope measurements. Also, as mentioned in Section IV, filtering of the dc current from the HV and LV power supplies were tested in earlier studies and it did not improve the minimum and maximum envelopes, which means that the amplitude of the noise coming from the power supplies was smaller than the arbitrary noise in the measurements setup.

The smallest minimum and maximum envelopes in the measurements shown in this paper, in Figs. 12 and 13, are within ±0.06% of the ensemble average of 100 pulses, are six times worse than the repeatability requirement for the CLIC DR kicker system. Both stability and repeatability measurements require further studies and applying of different measurement techniques, which are discussed in Section IX.

3) Evaluation of the Resolution of the Flat-Top Measurements: The resolution of the measurement can be estimated with the following equation:

$$R = \frac{V_{r,\mathrm{ADC}}}{2^{N_{\mathrm{ADC}}-1}}. \tag{1}$$

In (1), R is resolution, $V_{r,\mathrm{ADC}}$ is the maximum absolute voltage range of the single channel of an oscilloscope and N_{ADC} is the number of bits of the analog-to-digital converter (ADC). If ensemble averaging is applied, the vertical resolution of the ADC is improved by the following equation [30]:

$$R_{\mathrm{Enh}} = \frac{\log_2 n}{2}. \tag{2}$$

In (2), R_{Enh} is the resolution enhancement (in bits) of the ADC, which is gained by taking an average of n pulses. The nominal effective number of bits of the Rohde & Schwarz RTO1004 oscilloscope, with the high-resolution option, was 14 bits with the bandwidth of the oscilloscope limited to 100 MHz. The effective number of bits is typically 1–2 bits less [31], because the resolution is degraded due to quantization noise, nonlinearity of preamplifiers, missed digitizing levels, and a change of signal during the sampling process [32]. If the worst estimate is used and two bits are neglected, 12 can be used as the bit resolution of the measurement. According to (2), averaging for 100 pulses gives 3.3 more bits. The total range of the measurement channel of the oscilloscope was set to 8 kV in the measurements shown in Sections V and VI, and to 1, 8, or 10 kV in measurements shown in Section VII. Table IV summarizes the resolution of the measurements presented in these sections. In Table IV, n is the number of averaged pulses for computing the enhancement of the vertical resolution of the ADC by applying (2), and R_{Enh} is the resolution enhancement in bits, given by averaging of n samples. $N_{\mathrm{ADC,eff}}$ is the effective bit length of the ADC, R_{Rel} is the relative resolution and R_{Abs} is the absolute resolution of a measurement.

TABLE IV
SUMMARY OF RESOLUTION OF THE MEASUREMENTS PRESENTED IN SECTIONS IV-B–IV-E

	Envelope and a single pulse	*Average of 100 pulses*	*Average of 1000 pulses*
n	1	100	1000
R_{Enh} (bits)	0	3.3	5.0
$N_{ADC,eff}$(bits) [neglecting 2 bits]	12	15.3	17
R_{Rel} (%)	0.024	0.0025	0.0008
R_{Abs} (V) [1 kV range]	0.24	0.025	0.008
R_{Abs} (V) [8 kV range]	1.92	0.200	0.064
R_{Abs} (V) [10 kV range]	2.40	0.254	0.080

VIII. CONCLUSION

In this paper measurements on the first 20 layer, full-scale, prototype inductive adder for the CLIC DR extraction kicker system have been presented. For the initial measurements, analog modulation was not applied and there was a clear droop in the output pulse. In the second measurement passive analog modulation was applied in order to improve the flat-top stability of the output waveform. In the third set of measurements, active analog modulation was applied to generate a flat-top pulse with the best achievable flat-top stability. In the measurements presented here, the best measured flat-top stability, i.e., the combined ripple and droop of an ensemble average, was ±0.02% (±1.55 V) for 900-ns pulse flat-top duration for an average of 1000 pulses and ±0.03% (±2.5 V) for an average of 100 pulses, at 6.3 kV.

The flat-top repeatability of the prototype inductive adder was also initially investigated, by recording minimum and maximum envelopes of the pulses without modulation and with active analog modulation. Additional measurements were also carried out with an early stage five-layer assembly of the prototype inductive adder, to investigate the contributions of the high-voltage and low-voltage power supplies to the flat-top repeatability. Different sensitivity settings for the oscilloscope channel were also applied. The smallest measured minimum and maximum envelopes for 100 pulses were ±0.06% of the average of 100 pulses over 900-ns flat-top at 6.5 kV. However, the envelopes were approximately ±0.2%–0.3% of the channel range in all repeatability measurements and therefore are limited by the oscilloscope: the repeatability of the output waveforms of the prototype inductive adder can be expected to be better than these. Measurement of the repeatability requires further studies.

In the last measurement, a controlled decay waveform was generated with respect to an optimum decay waveform required for the prototype striplines. This reference waveform for the voltage and current gives the total electric and magnetic field with the required flat-top stability. The decay waveform was generated at a half of the nominal voltage required for a single stripline electrode, i.e., at 6.3 kV. The measured

ensemble average of 100 waveforms was within ±0.05% over 900 ns and ±0.02% over 160 ns. The relative flat-top stability is already adequate for the 2-GHz design of the CLIC DR extraction kicker systems but it is not adequate for the 1-GHz design, which requires up to 900-ns long pulse duration [1].

The flat-top stability measurements reported in this paper demonstrate that the active analog modulation allows very fine control over the shape of the flat-top. Thus, once the striplines and inductive adders are installed in an accelerator, and the field pulse flat-top measured with beam, the shape can be appropriately modulated.

IX. Future Work

The next step is to carry out measurements at nominal 12.5-kV output voltage and to improve the flat-top stability of the decay waveform to ±0.02% over 900 ns. The goal is to demonstrate that the inductive adders can meet the demanding specifications for the CLIC DR extraction kickers. Measurements will be continued by using different measurement methods: a differential amplifier setup developed at Paul Scherrer Institute in Switzerland [34]. In this case the reference voltage or current is a precisely controlled dc source and the difference of two signals is measured. Another technique is a pulse canceling method presented in [16, pp. 207–211], in which case the difference of two pulses with opposite polarities are measured with a single CT.

In the near future, a second full-size, nominally 12.5 kV, prototype inductive adder will be assembled with additional eight layers. The goal is to have two different operation modes for the same modulator: 12.5-kV pulses for extraction and 17.5-kV pulses for dumping the beam [35]. Finally, the two prototype adders will be tested together with the CLIC DR prototype extraction stripline kicker [2] in an accelerator laboratory. These tests will require an automated control system for the droop and ripple compensation, which is under design. The inductive adder is also seen as a promising alternative technology for use in existing systems at CERN [36] and for future projects, e.g., for the future circular collider [37].

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