EXIT Chart Aided Convergence Analysis of Recursive Soft m-Sequence Initial Acquisition in Nakagami-m Fading Channels

Abbas Ahmed, Panagiotis Botsinis, SeungHwan Won, Lie-Liang Yang, and Lajos Hanzo

***Abstract*—A delay of less than one millisecond is required by low-latency 5G wireless communication systems for supporting the "tactile" Internet. Hence, conventional initial synchronisation cannot be readily employed because of its potentially excessive delay. In this paper, an extrinsic information transfer (EXIT) chart assisted approach is used for the convergence analysis of m-sequences using recursive soft sequence estimation (RSSE) in the context of Nakagami-m fading channels. Explicitly, the novelty of our work is based on employing a new type of EXIT charts operating without using interleavers. This is a challenge, because the original EXIT charts rely on the employment of long, high-delay interleavers for ensuring that the inputs to the decoders become uncorrelated. We then evaluate the performance of various classes of m-sequences with the aid of the proposed EXIT charts and demonstrate that the m-sequences generated by the lower order polynomials maximize the mutual information more promptly with the aid of our RSSE scheme than those that belong to a higher order polynomial.**

***Index Terms*—Exit chart, m-sequence, nakagami fading channel, recursive soft sequence estimation (RSSE).**

I. Introduction

In the current era of mobile communication android phones, tablets, notebooks and laptops are in great demand throughout the world, which has resulted in an exponential increase of data traffic [1], [2]. Hence the information transmission over the channel should be as bandwidth-efficient as possible [1], [2]. Fortunately, the performance of wireless systems can be enhanced using iterative decoding, where extrinsic soft information is exchanged between the constituent receiver components [3]. The increased tele-traffic has led to the development of new enabling techniques operating at increased millimetre wave carrier frequencies, where more bandwidth is available for small cells [1], [2]. These advances will improve the area spectral efficiency in tele-traffic hot spots, such as stadiums, shopping malls etc. However, the Global Positioning System (GPS) cannot be used for indoor environments as a centralised time reference due to its high building-penetration loss.

Pseudo Noise (PN) sequence acquisition was conceived for the initial synchronisation of classic spread-spectrum communication systems [4]. Ward proposed an m-sequence acquisition arrangement as early as 1965 [5], which was later relied upon by the solutions conceived in [6], [7]. The basic principle relies on generating m chips by a local m-sequence generator based on the most likely received m-sequence. Once at least m chips have been received, we can update the estimate of the received sequence upon receiving each new chip. Naturally, the received chip may be contaminated by noise, which may hence lead to loading erroneous values into the local m-sequence generator of the receiver [6], [8]. By invoking the iterative Soft Input Soft Output (SISO) decoding principle, we can improve the initial sequence acquisition performance [4], [9], [10]. Historically speaking in the literature [6], chip-by-chip simulations of the Erroneous Loading Probability (P_e) were used as the tool of evaluating the performance of m-sequences using the Recursive Soft Sequence Estimation (RSSE) scheme of Section II. Our novel contributions are:

- In Section III we conceive a new EXIT chart tool [3], relying on soft decision feedback for improving the performance of the system as compared to the hard decision approach, which is achieved at the cost of a modest increase in complexity [6]. The correlation of chips inherent in the m-sequences is exploited for maximizing the Mutual Information (MI). The MI is a more suitable metric than the error probability for evaluating the m-sequences because it may also be used in a real-time online fashion, since it is based on the calculated Log Likelihood Ratios (LLR).
- Given our new EXIT charts, in Section IV we demonstrate that the m-sequences relying on low-order Generator Polynomials (GP) achieve higher MI than high-order GPs using the same number of RSSE iterations. We also show that the convergence behaviour of low-order GPs is better than that of the high-order GPs. Furthermore, having fewer feedback taps proves to be more beneficial at a given GP order.

II. System Model

The RSSE acquisition scheme [6] is illustrated in Fig. 1, which consists of four fundamental building blocks, namely the m-sequence generators, the soft chip registers, the SISO detector and the phase tracking loop. These blocks are explained in detail in the relevant sub-sections followed by the RSSE acquisition scheme.

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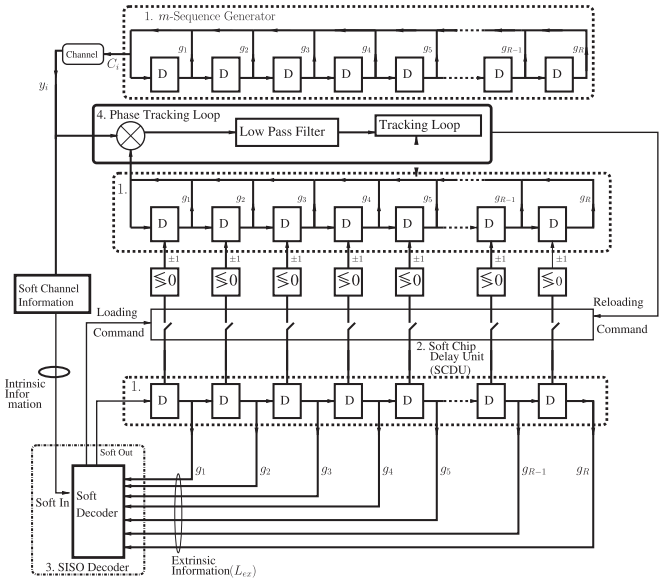

Fig. 1. RSSE iterative acquisition scheme.

A. m-Sequence Generator

The m-sequences employed are referred to as maximum-length sequences [4], which are generated by the feedback shift register of the transmitter seen in Fig. 1, where 'D' represents the unit time delay and the coefficients $g_1, g_2, \ldots, g_R$ represent the presence or absence of the feedback connections. The above configuration leads to the following GP:

$$g(D) = 1 + D^{r_1} + D^{r_2} + \ldots + D^R, \tag{1}$$

where R is the highest order GP coefficient and $g(D)$ has to be a primitive polynomial [7]. According to Fig. 1, the binary output sequence c_i, for $i = 0, 1, \ldots$, can be generated by the recursion of

$$c_i = c_{i-r_1} c_{i-r_2} \ldots c_{i-(R)} = \prod_{j=1}^{N} c_{i-r_j} \, i = 0, 1, \ldots \tag{2}$$

The m-sequences are normally used for spreading information, but in the context of initial synchronization they are not used for spreading information bits, but rather for aiding the initial synchronization between the BS and the UE. They are adopted because of their cyclic nature. Please note in the m-sequence generator of Fig. 1 that the feedback chip is transmitted to the receiver, instead of the output of the last shift register stage. The latter would have resulted in the generation of an m-sequence. However, in this specific code acquisition problem, the state of a register stage is transmitted, instead of the bit of a conventional m-sequence. This is done so that the receiver may lock on to the correct states of each register stage after a minimum of R transmissions, instead of 2^R transmissions, which would have been required if an m-sequence was transmitted. Therefore, in our problem the transmitted bits are the states of the first register stage of the m-sequence and they do not spread information bits. Based on the proposed approach, we are able to acquire the current state of the m-sequence generator at the transmitter and load the phase tracking loop from that point onwards. Note that correctly acquiring the output sequence of the last shift register stage is equivalent to acquiring the feedback chip sequence.

B. Soft Chip Register and SISO Detector

The soft-chip-register at the receiver of Fig. 1 consists of R number of Soft-Chip-Delay-Units (SCDUs). It may be observed from Fig. 1 that the number of delay units in the SCDU is the same as that in the m-sequence generator. The m-sequence generator and the SCDU use the same feedback connections as the m-sequence generator of the transmitter, since both the transmitter and the receiver know the GP. The task of the SCDU is to store and shift the instantaneous LLR values of R consecutive chips. Since in the beginning, the probability of having transmitted either chip value is the same, the LLRs are initialised to zero. These R LLR values will determine the hard values of the consecutive chips that will be loaded into the m-sequence generator after making a hard decision, as shown in Fig. 1. The SISO detector exploits the previously computed LLR values stored in the SCDU as the *a priori* information [6], [7]. The intrinsic information processed by the SISO detector is received from the channel. The soft output of the SISO detector is then shifted to the left-most position of the SCDU registers, while the right-most SCDU's value is discarded [6], [7].

C. Soft Channel Outputs

The received signal corresponding to chip c_i can be expressed as $y_i = \alpha_i c_i + n_i$, $i = 0, 1, \ldots$. When communicating over a fading channel, α_i denotes the fading amplitude, which is assumed to obey the Nakagami-m_l distribution. Furthermore, n_i represents the Additive White Gaussian Noise (AWGN) having a zero mean and noise spectral density of N_0. Given y_i, the LLR of c_i is expressed as

$$\begin{aligned} L_{ex}(c_i) &= L(c_i|y_i) = \log\left[\frac{P(c_i = +1|y_i)}{P(c_i = -1|y_i)}\right], \\ &= L_{ch,\,i} \cdot y_i + L_{apr}(c_i), i = 0, 1, \ldots \end{aligned} \tag{3}$$

where $L_{ch,\,i} = 4\alpha_i \frac{E_c}{N_0}$ represents the reliability value of the channel output and $L_{apr}(c_i)$ is the *a priori* LLR of the ith chip. E_c represents the transmitted chip energy, and $\frac{E_c}{N_0}$ represents the Signal-to-Noise Ratio (SNR). It can be observed from Fig. 1 that the system behaves recursively, where the previous soft outputs of the SISO detector obtained at the time indices of $(i-1), (i-2), \ldots, (i-R)$ are fed back to the SISO detector. Therefore, the extrinsic information provided by them can be readily exploited for enhancing the correct decoding probability of the chip c_i. Let the previous R number of soft outputs of the SISO detector be $L_{ex}(c_i - 1), L_{ex}(c_i - 2), \ldots, L_{ex}(c_i - R)$. In contrast to the *a priori* LLRs of conventional EXIT charts [11], in our system the magnitude of the *a priori* LLR of the ith chip is set to be equal to the LLR of the least confident previous chip that was used to create it. The sign of the ith chip's *a priori* LLR is equal to the product of the signs of the constituent chips' LLRs, since this represents the modulo-2 additions in the transmitter's generator polynomial. Therefore, the process of computing the

a priori LLR of the ith chip $L_{apr}(c_i)$ is expressed as [6]–[8]

$$L_{apr}(c_i) \approx \left[\prod_{r=1}^{R} \text{sign}(L_{ex}(c_{i-r}))\right] \times \min\{|L(c_i-1)|, |L(c_i-2)|, \ldots, |L(c_i-R)|\}. \quad (4)$$

The soft output of the SISO detector $L_{ex}(c_i)$ may be found by combining (3) and (4). If the channel's output SNR is sufficiently high, the LLR values of the last R consecutive chips will increase upon increasing the number of iterations in the receiver. The reliabilities associated with the R consecutive chips improve, while the erroneous loading probability of the generator - which is defined as the probability of the event that the m-sequence generator of Fig. 1 is loaded with at least one erroneous chip - decreases upon increasing the number of iterations. If the amplitudes of the LLR values in the SCDUs become sufficiently high after a number of iterations, then the SISO detector can carry out hard-decisions to obtain the binary $+1$ or -1 chip values, which are then loaded into the delay units of the receiver's m-sequence generator of Fig. 1. During the lth iteration, with $l = 1, \ldots, L$, R number of extrinsic LLRs have to be calculated, so that all the estimated values in the shift register are updated at the receiver. This requires the transmission of R chips during each iteration. Therefore, after L iterations a total of $R \cdot L$ received chips have been transmitted.

D. Phase Tracking Loop

Prior to despreading, the SNR is usually insufficiently high for reliable carrier phase tracking. The despread signal is passed to a low-pass filter and then to the tracking loop of Fig. 1. If the tracking loop is capable of obtaining the correct phase, the code acquisition process is successfully completed. By contrast, if the tracking loop is incapable of tracking the phase, the reloading command of Fig. 1 will be activated and this time the m-sequence will have different values in the delay units of the local m-sequence generator. This process will continue until successful code acquisition is achieved. The main task of the Phase Tracking Loop (PTL) in Fig. 1 is to reliably detect the transmitted signal and to generate a stable output so that the transmitter and the receiver are perfectly synchronised, thus improving the SNR. The Local Oscillator (LO) in the PTL maintains phase-matching and if there is any phase drift, the LO adjusts its frequency to compensate for it.

III. EXIT Chart Analysis for m-Sequence Design

The concept of EXtrinsic Information Transfer (EXIT) charts was introduced by Brink [3], [12] as a powerful tool of analysing the convergence behaviour of iteratively decoded systems. Explicitly, the EXIT chart is capable of predicting the specific SNR value, at which a vanishingly low Bit Error Ratio (BER) can be achieved. This becomes possible without performing time-consuming bit-by-bit decoding based Monte Carlo simulations. In this paper we conceive a new application of EXIT curves for predicting the convergence behaviour of the polynomials used for the sake of investigating the evolution of the input/output MI

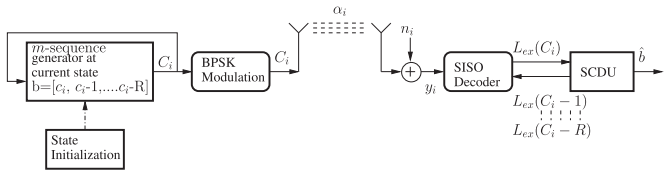

Fig. 2. The system model used for the RSSE scheme of Fig. 1.

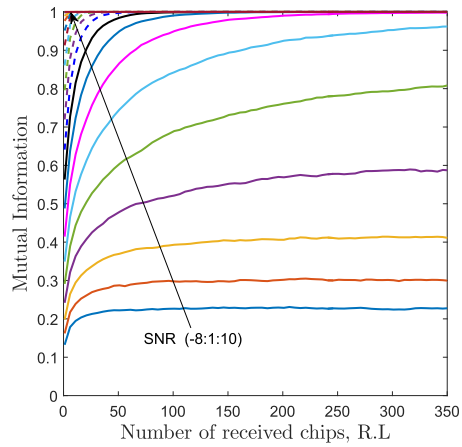

Fig. 3. Mutual Information (MI) versus the number of received chips for the GP $g_1(D) = 1 + D^2 + D^5$, and for various SNR values.

exchange between the receiver's SISO components in consecutive iterations. Note that the EXIT charts are used in an off-line mode for predicting the behaviour of the different m-sequences and the required number of decoding iterations for various SNR values. Once the system components and the system parameters have been decided based on their EXIT chart behaviour, there is no mutual information calculation and no EXIT chart reliance.

In a conventional EXIT chart, the inner EXIT curve, the outer EXIT curve and the decoding trajectory can be simulated in parallel, without depending on each other's, data from the other simulations. The inner and outer EXIT curves predict the values that the stair-case-shaped decoding trajectory would have, independently of each other. This is possible due to the employment of interleavers between the inner and outer decoding components. However, the independent simulation of the inner and outer EXIT curves in facilitated by the idealised simplifying assumption of having infinitely long interleavers, whilst the simulation of the decoding trajectory uses an interleaver with finite length. Therefore, the stair-case-shaped decoding trajectory may not exactly match the performance predicted by the inner and outer EXIT curves. Generally, the longer the interleaver's length, the better the performance becomes. In the self-concatenated approach of our system, the same detector/decoder is activated iteratively, using its own output as part of its inputs, as depicted in Fig. 2. The two inputs of the SISO decoder are the channel's output and the output of the SCDU. Therefore, the inner and outer EXIT curves are identical, but they are reflected with respect to the diagonal $y = x$ of the EXIT chart seen in Fig. 5 and Fig. 6. Hence, we may observe a conceptual similarity between our current initial acquisition problem and the self-concatenated decoding approach of [13]. Having said that, there is a substantial difference between them, because in [13]

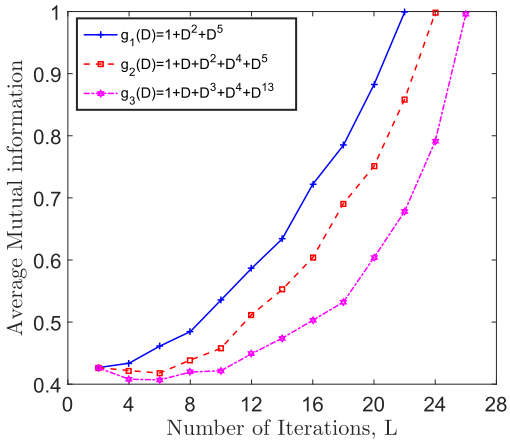

Fig. 4. Mutual information (MI) versus the number of decoding iterations when SNR $=$ 0 dB and the Nakagami Fading channel has $m_l = 3.0$.

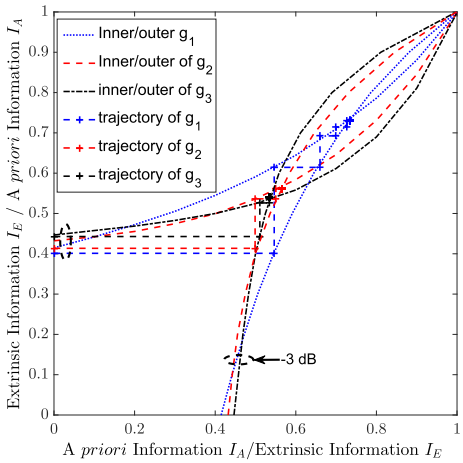

Fig. 5. EXIT chart for the GPs of $g_1(D) = 1 + D^2 + D^5$ (blue), $g_2(D) = 1 + D + D^2 + D^4 + D^5$ (red) and $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$ (black) over Nakagami channels, when $m_l = 3.0$ at SNR $= -3$ dB.

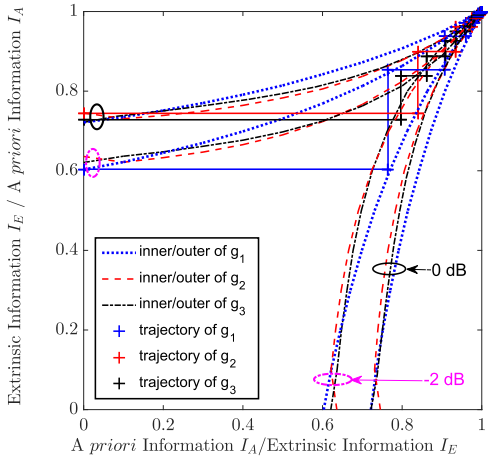

Fig. 6. EXIT chart for the GPs of $g_1(D) = 1 + D^2 + D^5$ (blue), $g_2(D) = 1 + D + D^2 + D^4 + D^5$ (red) and $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$ (black) over Nakagami channels, when $m_l = 3.0$ at SNR $= -2$ dB and SNR $=$ 0 dB.

an interleaver was used for shuffling the output of the decoder before feeding it back to its input. By contrast, in this paper we conceive EXIT charts without the need for interleavers. We arrange for this by dispensing with iterations invoked for decoding the same bit sequence. Instead, we use iterations for the online exploitation of the inherent correlation of the chips of the m-sequence, as imposed by the feedback shift register of Fig. 2. This is the main factor that distinguishes our novel EXIT-chart from the conventional EXIT charts. At the receiver, the SISO detector's output will change depending on the *a priori* LLR values L_{ex}, which in turn, consist of the extrinsic LLR values of previous iterations. In Fig. 2 at the transmitter, the m-sequence generator's state is initialized to a predetermined state, which is known at the receiver. In contrast to conventional m-sequence generators, the output of the m-sequence is the feedback chip, which is also transmitted over the channel. In other words, assuming that BPSK modulation is used, the value of the ith transmitted chip c_i also becomes the value of the first register stage in the transmitter's m-sequence generator. After it is transmitted over the noisy channel, the received signal is fed to the SISO decoder, along with the stored extrinsic LLR values $L_{ex}(c_{i-1}), \ldots, L_{ex}(c_{i-R})$ in the last R decoding iterations, which were calculated for the R previously transmitted chips. Based on these past extrinsic LLRs, the *a priori* LLR of c_i is computed from (4). Afterwards, the extrinsic LLR of c_i is calculated based on (3), and the same procedure is followed for the next chip c_{i+1}. The SCDU stores the most recently R calculated extrinsic LLRs and shifts them accordingly. After a predetermined number of decoding iterations, a hard decision is performed on the stored extrinsic LLR values in the SCDU and the current estimated state of the transmitter's m-sequence generator $\hat{\boldsymbol{b}}$ is obtained.

A. Self-Concatenated Approach

In the self-concatenated approach, there is only a single decoder, which is continuously used with different inputs, as depicted in Fig. 2. The first input of the SISO detector is the channel's output. In contrast to the conventional EXIT charts the channel's output is different during each decoding iteration. The second input of the SISO decoder is the output of the SCDU, which again, acts similarly to the interleaver of a conventional iterative receiver, since it essentially shifts the previously calculated extrinsic LLR values. The most likely $(2^R - 1)$ transmissions of the m-sequence have already been hypothesized by the transmitter and the receiver, therefore the SISO decoder is ready to calculate $L_{apr}(c_i)$ based on (4). Please note that the receiver exploits the knowledge of the specific m-sequence that has been selected only at the stage of calculating the *a priori* LLR values. The contents of these shift registers will keep on changing during each SISO iteration, therefore we have to store the most recently calculated R extrinsic LLR values at all times. Hence, we use iterations for the online exploitation of the inherent correlation of the $(2^R - 1)$ transmissions of the m-sequence, as imposed by the m-sequence generator.

B. Mutual Information

In this contribution, we calculate the MI between the transmitted chips and the associated extrinsic LLRs by using the time-averaging method, hence we may use the LLR-based MI metric online [3].

IV. Simulation Results

In this section, simulation results are presented for characterising the performance of our RSSE in Nakagami-m_l fading channels. We assume that the channel magnitude remains constant over a set of R consecutive chips. The three different GPs that we compare are $g_1(D) = 1 + D^2 + D^5$, $g_2(D) = 1 + D + D^2 + D^4 + D^5$, and $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$. The selection criteria of these GPs are based on the number of taps, as well as on their order. More specifically, both $g_1(D)$ and $g_2(D)$ have an order of 5, while $g_3(D)$ has an order of 13. At the same time, $g_1(D)$ has three non-consecutive taps, while $g_2(D)$ has five taps, two of which are consecutive. Finally, $g_3(D)$ also has five taps, two of which are consecutive. In our analysis $R \cdot L$ represents the total number of chips processed by the SISO detector, where R represents the polynomial's order and L represents number of iterations. Before evaluating the Erroneous Loading Probability P_e, we have investigated their performance based on the MI.

In Fig. 3, the relationship between the MI and the number of received chips is shown, when the polynomial $g_1(D)$ is employed. It can be observed from Fig. 3 that the MI of the polynomial $g_1(D)$ increased for a given number of received chips, when the SNR is increased. At the same time, fewer received chips are required in order to reach the unity MI target, when a higher SNR is encountered. Based on Fig. 3, we may conclude that for SNRs above -3 dB, the MI approaches unity after receiving fewer than 300 chips. The generator polynomial $g_1(D)$ evaluated has $R = 5$ register stages, therefore the maximum number of decoding iterations in the figure is $L = 350/R = 350/5 = 70$.

Fig. 4 depicts the MI versus the number of iterations at an SNR of 0 dB, when different GPs are employed. In our simulations, the Nakagami fading parameter is $m_l = 3.0$. It may be observed that the MI reaches its maximum value after less than 30 iterations, regardless of the GP employed. It may be noted from Fig. 4 the number of chips varies, depending on the generator polynomial used and the number of iterations employed. For example, if $g_1(D)$ is used, since it is associated with order $R = 5$, and it uses $L = 21$ iterations, the number of received chips will be $R \cdot L = 105$ which can be visualised in Fig. 3 for the particular value of $SNR = 0$ dB. Since, $g_3(D)$ is used so it is linked with $R = 13$, and utilizes $L = 26$ iterations hence, the received chips will be $R \cdot L = 338$. Fig. 4 shows that the GPs $g_1(D)$ and $g_2(D)$ outperform $g_3(D)$ because of their lower order, while $g_1(D)$ achieves the best performance, due to its lower number of employed taps. As, the extrinsic information is dominated by the minimum of the LLR values of all the feedback branches. Therefore, the generator polynomial using a low number of feedback branches has a higher probability of providing the true extrinsic information for the SISO acquisition scheme, than that using a high number of feedback branches, because in the latter the average LLR might still be high, despite having a single low LLR like in the case of $g_1(D)$ with respect to $g_2(D)$. In a nutshell, GPs having a lower number of taps are preferred, because the detrimental influence of noise imposed on their chips results in less grave iteration-induced error propagation than for their counterparts with higher number of taps.

Fig. 5 shows an EXIT chart for our self-concatenated iterative RSSE scheme, at an $SNR = -3$ dB. The Nakagami fading value is $m_l = 3.0$. The inner and outer receiver component EXIT curves both represent the same decoder, therefore, they are symmetrical with respect to the diagonal $y = x$ line. The staircase-like curves correspond to the Monte-Carlo simulation-based decoding trajectories of the proposed system. In Fig. 5 it can be observed that the polynomials could not reach the maximum point and the top right corner at [1 1] as our inner and outer curves of EXIT charts intersect before this point and the trajectory stops. This indicates that we need to simulate above -3 dB SNR. The same information was obtained from Fig. 3 where the relationship between the MI and the number of received chips was plotted.

Fig. 6 shows an EXIT chart for our self-concatenated iterative RSSE scheme, at an SNR value of -2 dB and 0 dB for the same Nakagami fading value of $m_l = 3.0$. All decoding trajectories approximately match their associated inner and outer component curves. According to the EXIT chart properties of iterative decoding, an infinitesimally low BER may only be achieved by an iterative receiver, if there is an open EXIT tunnel between the EXIT curves of the decoder. At a higher SNR, the open tunnel between the two EXIT curves is wider, hence the trajectory requires fewer iterations for higher SNR values. Furthermore, based on Fig. 6, we may conclude that a better match between the decoding trajectory as well as the inner and outer EXIT curves occurs at higher SNR values. In Fig. 6 it can be observed that the polynomial $g_1(D)$ requires the fewest decoding iterations to reach the top right corner at [1, 1] for both SNR values. Since $g_2(D)$ requires fewer decoding iterations to reach the [1, 1] corner, we may conclude that it outperforms $g_3(D)$. This shows that the EXIT chart based performance prediction agrees with the MI-trends of Fig. 3, and that lower order polynomials have faster convergence capabilities. Therefore, when comparing GPs of different order, higher order GPs perform worse than lower order GPs as they require more data and have large memory component which exhibits excessive confidence in their own soft estimates and hence they do not benefit enough from an iterative scheme.

After investigating the results in EXIT charts, we verified our simulation results in terms of the Erroneous Loading Probability, P_e versus SNR, which is measured in dB. The Nakagami fading value m_l is fixed to 3.0. It can be observed from Fig. 7 that the performance of the GPs for $L = 10$ iterations is inferior to that when $L = 100$, since by allowing a higher L more chips are transmitted and more decoding iterations are performed. Therefore, by allowing more decoding iterations L, the SISO decoder will eventually reach the (1, 1) point of perfect convergence and P_e will become infinitesimally low. Fig. 8 thus demonstrates that as the value of L increases, the performance

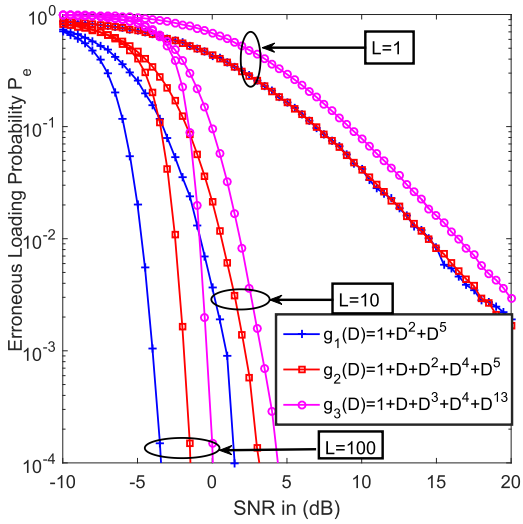

Fig. 7. Erroneous loading probability P_e, versus the SNR, performance for various numbers of chips invoked into the proposed recursive SISO detector, when transmitting the said polynomials over Nakagami Fading channels when $m_l = 3.0$.

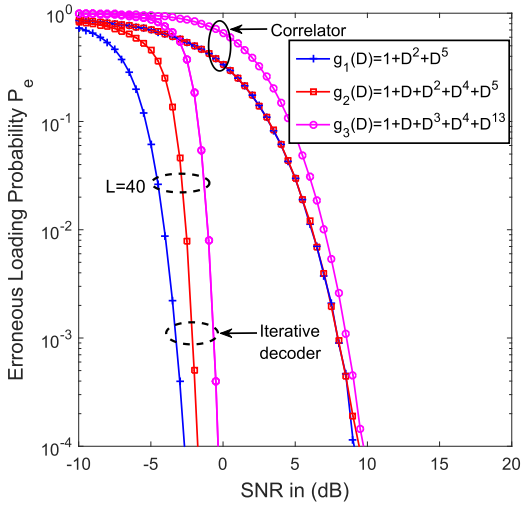

Fig. 8. Erroneous loading probability P_e versus the SNR performance for various numbers of chips invoked into the proposed recursive SISO decoder, when transmitting the generator polynomials of $g_1(D) = 1 + D^2 + D^5$, $g_2(D) = 1 + D + D^2 + D^4 + D^5$ and $g_3(D) = 1 + D + D^3 + D^4 + D^{13}$ over AWGN channel.

of all polynomials tends to improve. We may also observe that $g_1(D)$ outperforms the other two GPs, because it only has three taps and none of them are consecutive taps. On the other hand, even though both $g_2(D)$ and $g_3(D)$ have two consecutive taps, $g_2(D)$ performs better, because it has a lower GP order. Hence, it may be deduced that P_e depends both on the number of taps as well as on the GP order.

In Fig. 8 we have compared the acquisition performances of the RSSE scheme to those of the correlator for m-sequences of various lengths, when transmitting over AWGN channels. More specifically, in Fig. 8 we have chosen three polynomials $g_1(D)$, $g_2(D)$ and $g_3(D)$, where $g_1(D)$ and $g_2(D)$ have a polynomial order of 5 and a length of $N = 31$ chips, while $g_3(D)$ has the polynomial order of 13 and a period of $N = 8191$ chips. Fig. 8 shows that the m-sequence can reliably be acquired at an SNR value of -3, -2 and -0.5 dB by invoking as few as 40 iterations. By contrast, when a correlator is used, the PN code acquisition scheme has to operate at an SNR value of 10 dB in order to achieve the P_e of 10^{-4}. Hence, the attainable SNR gain of using the proposed RSSE acquisition scheme at an P_e of 10^{-4} is about 7, 8 and 9.5 dB, when $g_1(D)$, $g_2(D)$ and $g_3(D)$ are considered, respectively.

V. Conclusion

A novel EXIT chart design is proposed for an m-sequence acquisition system, which operates without using conventional interleavers. The m-sequence generator's state is estimated at the receiver using the self-concatenated approach, where the correlations between consecutive chips are exploited during each iteration. It was shown that a low order GP yields a wider EXIT tunnel, which translates to faster m-sequence acquisition, or, equivalently, error-free acquisition at lower SNR values. The erroneous loading probability results verify the validity of the proposed EXIT chart design. It has also been observed that for GPs with similar order, those with fewer taps outperform GPs with higher number of connected taps.

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