Analysis of Bipolar Integrated Circuit Degradation Mechanisms Against Combined TID–DD Effects

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***Abstract*— Integrated circuits sensitive to both total ionizing dose (TID) and displacement damage (DD) effects can exhibit degradation profiles resulting from a combination of degradation mechanisms induced by both effects. This work presents circuit simulations based on experimental data to explain degradation mechanisms induced by combined TID and DD effects on a bipolar IC current source. First, the effect of the degradation of each internal transistor on the circuit's response is evaluated by applying electrical parametric changes. Then simulations are performed from different degradation scenarios based on observed circuit behaviors to reproduce the different TID, DD, and combined TID–DD responses. These simulations show that a synergistic interaction between a current leakage induced by DD on a transistor located in the bandgap reference part with the gain degradation of a current mirror induced by both TID and DD appears to be responsible for the combined TID–DD response. It is also shown that the circuit degradation rate depends on the DDD/TID rate ratios encountered during the exposition.**

***Index Terms*— Displacement damage (DD), IC radiation response, nonionizing energy loss, particle accelerator, total ionizing dose (TID).**

I. Introduction

THE total degradation response of integrated circuits exposed to radiation results from the degradation of all their internal transistors [1], [2] independently of the technology used (CMOS, BiCMOS, or bipolar). While CMOS technology is only affected by total ionizing dose (TID) and not by displacement damage (DD) dose (DDD) (for standard DDD that COTS are exposed to), the bipolar technology, and thus the BiCMOS one as well, can be affected by both TID and DD, and even enhanced low dose rate (LDR) sensitivity (ELDRS) effect.

This interaction of the radiation effects at the internal circuit level can make challenging the qualification of devices exposed to environments inducing both effects such as the ones present in high-energy accelerators, nuclear reactors, or deep space missions. At CERN, the qualification of ICs against such combined effects is a major concern for radiation hardness assurance (RHA). The large hadron collider (LHC) environments present a wide range of DDD/TID rate ratios that can lead to completely different degradation rates as it has been demonstrated in our previous work [3] with a bipolar IC current source exposed to different ratios.

While no qualification standards exist for ICs exhibiting combined TID–DD internal circuit effects, a similar phenomenon has been intensively studied in the literature, which is the qualification of circuits exhibiting circuit effects induced by ELDRS. For this effect, it has been shown that for most of the devices the total circuit degradation could be related to the degradation of a single transistor in the circuit such as in [4] and [5]. However, this is not systematically true, and as it is the case for TID and DD, it has also been shown that the different internal transistors of an IC can exhibit different sensitivities to the ELDRS effect and therefore a device can present completely different degradation profiles depending on the TID dose rate [6]. Therefore, the proposed methodology to qualify components against this effect is to identify the worst case responses by irradiation at very LDRs [7], [8], assessing the LDR degradation or dependence of the device.

In our previous work [3], the same approach was followed and a similar methodology to qualify components against combined TID–DD based on the assessment of the dependence between degradation and failure rate with the DD over TID rate ratio. An example of the application of this methodology was proposed with a bipolar IC whose observed changes in degradation profiles with different DDD/TID ratios were assumed to be due to degradation interactions at the internal circuit level.

This article aims to propose a deeper analysis of the behavior of this component through simulations based on experimental data to understand in detail how in this component the different degradation mechanisms can combine and lead to the observed responses. First, the device response against TID and DD will be presented. Then, the simulation model is introduced and the impact of the degradation of each internal component on the circuit response is demonstrated. Then, based on experimental assumptions two circuit degradation profiles are defined to simulate the device response against TID and DD individually. Finally, it is demonstrated how the impact of the DD on the circuit can be enhanced by the TID in a nonlinear way.

II. Circuit Model

The device used for this study is the LM334, which is a proportional-to-absolute temperature (PTAT) adjustable current source. No simulation model is provided by the

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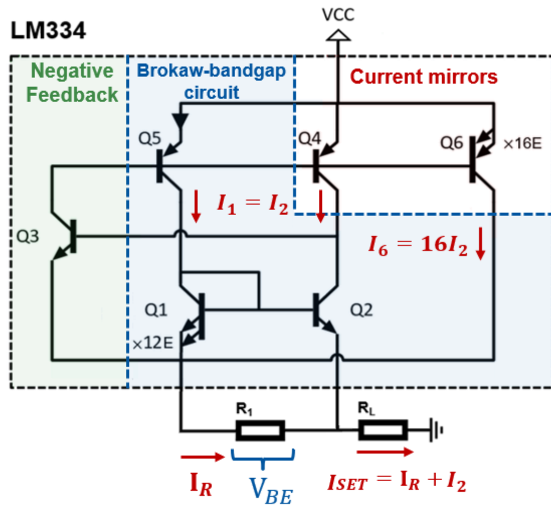

Fig. 1. Simplified internal circuit of LM334 with the different parts underlined.

manufacturer, and therefore the SPICE simulation circuit was developed according to the analysis of the internal circuitry shown in Fig. 1 and the component characteristics described in the datasheet [9].

The circuit is composed of three different parts: a modified Brokaw bandgap circuit, a negative feedback circuit, and a current mirror part. The principle of the circuit is to provide the fixed reference voltage called $\Delta V_{\rm BE}$ on the resistor R1 independently of the resistor value. Therefore, the current flowing through the load resistor is proportional to the R1 resistor. This voltage is provided by the Brokaw bandgap circuit and is equal to the difference in base–emitter voltage of the transistors Q1 and Q2, which is induced by the fact that Q1 is composed of several transistors in parallel. The equation ruling the circuit is the following:

$$\Delta V_{\rm BE} = V_{\rm BE1} - V_{\rm BE2} = \frac{kT}{q}\ln\left(\frac{nI_{c1}}{I_{c2}}\right) = \frac{kT}{q}\ln(n) \quad (1)$$

where k is the Boltzmann's constant, q is the charge of an electron, T is the absolute temperature in K, n is the number of transistors Q1 in parallel, I_{c1} is the collector current of transistor Q1, and I_{c2} is the collector current of transistor Q2. Therefore, since the transistors Q1 and Q2 are identical if I_{C2} is kept equal to I_{C1}, $\Delta V_{\rm BE}$ is linearly dependent on the temperature. For a temperature equal to 25 °C, kT/q is equal to 25.7 mV. In the datasheet, $\Delta V_{\rm BE}$ is equal to 64 mV, and therefore the number of transistors Q1 in parallel is 12.

Then, the role of the negative feedback is to keep the two collector currents equal independently of the voltage supply or the value of the resistor R1 by setting the necessary base current of Q4 and Q5.

Then, the fixed current provided by the circuit in the load resistor is equal to

$$I_{\rm SET} = I_{E1} + I_{C6} + I_{E3} \approx I_{E1} + I_{C6}. \quad (2)$$

The current I_{E3} is equal to the base currents of Q4, Q5, and Q6; it is then negligible compared with the other collector currents for $h_{\rm feQ4-6} \gg 1$. On the other hand, Q6 is a multiplier current mirror design to provide several times the current I_{C1}. In the datasheet, the ratio of $I_{\rm SET}$ to I_{E1} is equal to 17, which implies that I_{C6} is 16 times higher than I_{E1}, and therefore transistor Q6 is composed of 16 transistors in parallel.

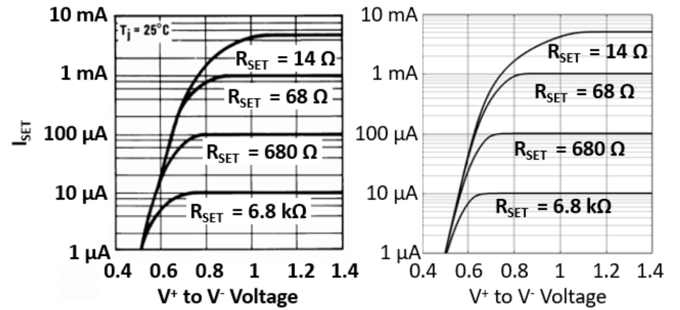

Fig. 2. Output current value of LM334 as a function of V_+ to V_- voltage for different values of set resistances from datasheet (left) and SPICE simulation (right).

TABLE I
TRANSISTOR SPICE PARAMETERS USED FOR THE LM334 SIMULATION MODEL

TYPE	Is (fA)	TF (ns)	H_{fe}	CJC (pF)	CJE (pF)	VAF (V)	Rb (Ω)	Re (Ω)
NPN	0.1	1	50	0.5	1	100	100	5
PNP	0.1	100	50	0.5	1	100	100	5

With the correct estimation of the numbers of transistors in parallel composing Q1 and Q6, it is possible to build a SPICE model with a quite realistic behavior as can be seen from Fig. 2 comparing the simulated output current with the datasheet ones for different values of R1. As previously mentioned, no information about the internal transistors is provided by the manufacturer, and therefore the transistor parameters used in the simulation are arbitrary and have been obtained combining educated guesses and fine-tuning to reproduce the different device electrical characteristics. The parameters used in the model are shown in Table I, where Is is the transport saturation current, $H_{\rm fe}$ the forward active current, CJC the base–collector zero-bias junction capacitance, CJE the base–emitter zero-bias junction capacitance, VAF the forward early voltage, and TF the ideal forward transit time. All the others are the default ones of the SPICE transistor models.

Any degradation of these three main parts will impact the circuit's response.

III. RADIATION RESPONSES

To gather more information on the internal degradation mechanisms, new irradiations against TID have been performed besides the one presented in our previous work [3]. During these irradiations, not only the output current was monitored but also the output current as a function of the voltage supply characteristic at different irradiation steps. The irradiation conditions during these additional tests together with the ones previously performed are summarized in Table II.

For each test, at least five devices were tested. Three types of tests were conducted, TID tests, DD tests, and

TABLE II
IRRADIATION CONDITIONS

Particle (Facility)	Displacement Damage Dose rate [Gy/h]	Ionizing dose rate [Gy/h]	DDD/TID Ratio [Gy/Gy]
Gamma (CC60)	6.8 uGy/h – 2.04 mGy/h	2 – 600	3.57×10^{-6}
Neutron (PROSPERO)	0.62	2	3.1×10^{-1}
Neutron (JSI-TanC)	46.2 mGy/h	15	3.09×10^{-3}
Mixed Field (CHARM)	7.42 mGy/h	0.96	7.73×10^{-3}
	6.31 mGy/h	1.13	5.56×10^{-3}
	4.54 mGy/h	1.82	2.69×10^{-3}
200 MeV Proton (PSI-PIF)	0.23	500	5.56×10^{-4}

combined TID–DD tests. Pure TID responses were obtained with gamma irradiation performed in the CC60 facility of CERN with a cobalt 60 source [10]. It has to be noted that gamma rays also induce DD, but for the TID levels considered for COTS components and the one reached in this study, this contribution is considered negligible. Considering the NIEL values given in [11] and [12] that are around 1.1×10^{-7} MeV.cm^2/g and considering a dose deposited by photons of 3×10^{-2} MeV.cm^2/g for standard average energy of 1.25 MeV, this gives a DDD/TID ratio of 3.57×10^{-6} as shown in Table II. This means that for the maximum ionizing dose reached in this work of 2.5 kGy, the devices are exposed to a DDD of 8.5 mGy, which is considered too low to induce any significant degradation.

The DD response was obtained by exposing devices at the PROSPERO neutron irradiation facility of the Commissariat à l'Energie atomique et aux énergies Alternatives (CEA) [13]. As for the CC60 facility, in the PROSPERO facility the devices are also exposed to a small fraction of TID due to the gamma rays also generated by the nuclear reactor. The DDD/TID ratio measured during the experiment was 3.09×10^{-1}, which means that for the DDD of 4 Gy, the devices were exposed to only 13 Gy, and therefore it is assumed that the level of interactions between TID and DD should be very low.

Then, two possibilities exist to test in different DDD/TID ratio conditions during the combined TID–DD irradiations. The first consists of using monoenergetic charged particle beams. Different ratios can be reached using different particles or different energies of the same particle. For instance, at CERN for radiation qualification purposes, the proton irradiation facility (PIF) of the Paul Scherrer Institute (PSI) is widely used. It provides proton energies ranging from 30 MeV up to 220 MeV, which corresponds to DDD/TID ratios ranging from 3 to 6×10^{-4}, which is rather low compared with levels that have to be reached to be representative of the LHC environments [3], which range from 10^{-4} up to 10^{-2}. Mixing different types of particles and energies would allow achieving values over the whole range, for instance, electrons allow to obtain ratios in the 10^{-5} range while neutron facilities with strong gamma contributions allow reaching the 10^{-3} range. This last possibility was tested with this device, where irradiations have been performed at the Triga Mark II research nuclear reactor of the Jožef Stefan Institute (JSI). In this reactor, the gamma contribution can be quite high depending on the test position selected; during our experiment, the DDD/TID ratio was at 3.09×10^{-3}, which is two orders of magnitude lower than the PROSPERO reactor.

Also, irradiations have been performed at PSI with a 200-MeV proton beam, but as it is often the case for this kind of facility, the ionizing dose rate was quite high, 500 Gy.h^{-1}, as shown in Table II.

In the case of CERN, another solution can be used, which is using different kinds of mixed fields provided by the CERN high-energy accelerator mixed field (CHARM) facility [16]. The CHARM mixed radiation field is composed of the secondary particles resulting from the collision of a 24-GeV proton beam extracted from the proton synchrotron (PS) on cylindrical copper or aluminum targets in the experimental area. Then, using different test locations, targets, and shielding, the facility can achieve a wide range of DDD/TID ratios as shown in a previous work [3]. Three different irradiations at different ratios indicated in Table II were performed to study the impact of combined TID–DD effects on the circuit response at different DDD/TID ratios.

The most important factor to be considered here is the ionizing dose rate. It is assumed that no DDD dependence is expected within the fluxes used during those tests; however, bipolar transistors can show significant sensitivity to dose-rate effects, and therefore dose-rate effects have to be carefully considered to compare the different irradiation tests.

A. Total Ionizing Dose Responses

To investigate possible dose-rate effects and to allow a direct comparison with the combined TID–DD irradiations, a set of devices has been irradiated to different ionizing dose rates, ranging from 2 to 600 Gy(SiO_2).h^{-1}. Based on the circuit radiation responses, the dose rates have been separated into two groups; LDR, which corresponds to the lowest ionizing dose rate used, 2 Gy(SiO_2).h^{-1}, and high dose rates (HDRs), which corresponds to ionizing dose rates from 22 up to 600 Gy(SiO_2).h^{-1}. The device responses corresponding to these two groups are presented in the following sections.

1) Low Dose Rate: The evolution of the output current of five devices with an LDR of 2 Gy(SiO_2).h^{-1} is shown in Fig. 3. As visible, at this rate, the devices seem to suffer from two different degradation mechanisms, the first one inducing a slow decrease of the output current up to 1 kGy(SiO_2) and a second one increasing it back even further the initial value. One can note that during this test the devices have shown a relatively low variability of responses. The evolution of the output current as a function of the voltage supply characteristics for a single device for both before and after 1 kGy(SiO_2) is shown in Fig. 4. As visible, the global shape of the characteristic did not change significantly during the irradiation but only the saturation current level changed, decreasing up to 1 kGy(SiO_2) and then increasing after.

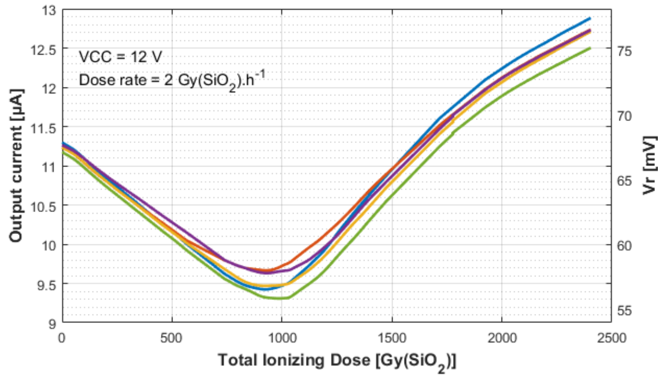

Fig. 3. Output current response of five LM334 components biased to provide about 10 mA and supplied in 12 V up to a TID of 2.5 kGy(SiO_2) at 2 Gy(SiO_2) $\cdot$ h^{-1}.

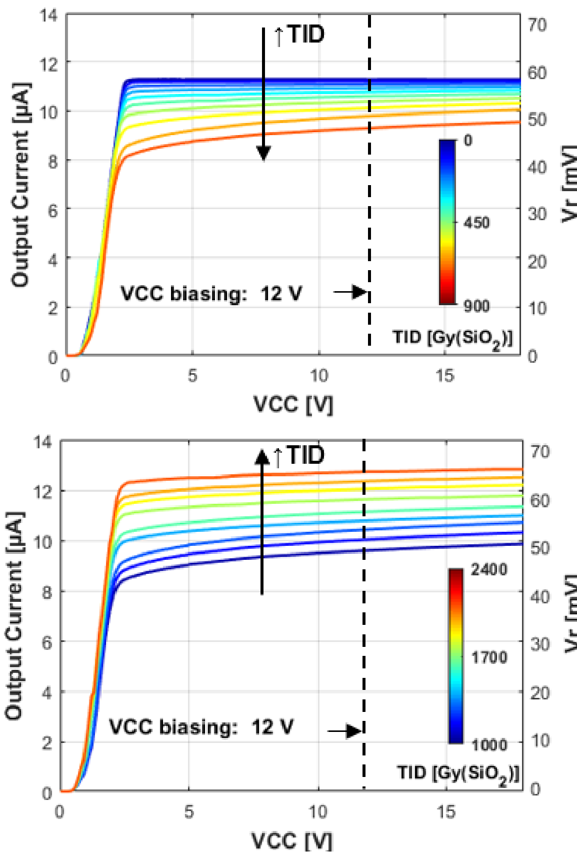

Fig. 4. Evolution of current output as a function of voltage supply against TID up to 1 kGy(SiO_2) (top) and from 1 up to 2.5 kGy(SiO_2) (bottom).

It seems that two degradation mechanisms impact the LDR circuit response with the mechanism responsible for the decrease being dominant below 1 kGy(SiO_2). It can be assumed that the degradation observed is a combination of gain degradations occurring in different parts of the internal circuit as it has been observed for other circuits with similar responses [1], [2]. Assuming that the degradation of the circuit is probably due to the degradation of the current gain of its internal transistors, this could be the result of the degradation of two different transistors or group of transistors with opposed

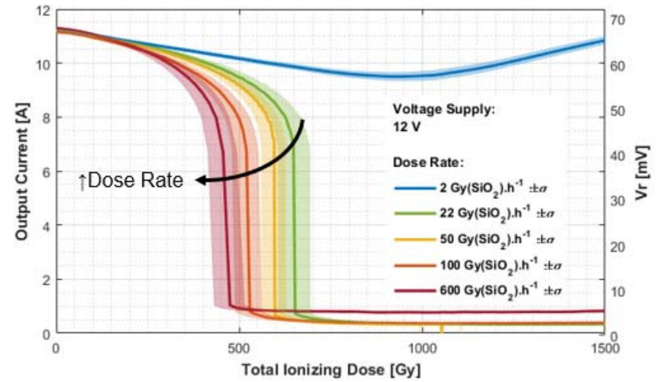

Fig. 5. Output current response of LM334 supplied in 12 V at several HDRs with the LDR response in comparison.

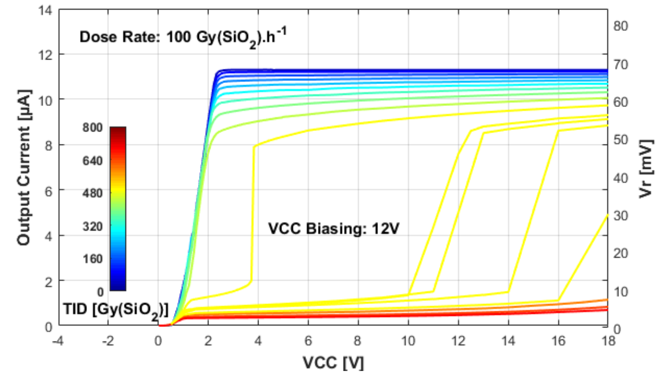

Fig. 6. Evolution of current output as a function of voltage supply against TID up at 100 Gy(SiO_2) $\cdot$ h^{-1}.

effect on the circuit. This kind of phenomenon can happen if the transistor or group of transistors responsible for the first degradation mode reach saturation of their current gain degradation, as it happens at such high cumulated doses, before the second group of transistors responsible for the second degradation mode.

At this stage, already only with TID, at a LDR, different degradation mechanisms with opposite effects seem to occur. The question arises as to how these two mechanisms can evolve when exposed to DD in addition to TID. If the transistors responsible for these degradation mechanisms have different sensitivities to DD, the circuit might exhibit completely different behavior depending on the DDEF/TID ratio.

2) High Dose Rate: Concerning the HDR responses, the degradation profile is different than the LDR response. As visible in Fig. 5 for different dose rates, the current decreases monotonically at a higher rate before suddenly dropping to almost 0. The higher the dose rate, the higher the degradation rate.

Then, the evolution of the $I_{\mathrm{out}} = \mathrm{f(Vcc)}$ characteristic for a dose of 100 Gy(SiO_2).h^{-1} is visible in Fig. 6. From this figure it is possible to see that in addition to the decrease in the saturation current, the minimum startup voltage (referred hereafter as V_{START}) necessary to activate the circuit has rapidly increased with the dose, causing the sudden drop visible in Fig. 5. This kind of behavior is usually due to the degradation of the startup circuit of the device. It has already been observed on similar devices such as voltage

regulators, which use also bandgap-based circuits like in [15], for instance, where the current gain degradation of one of the input PNP transistors was leading to the increase in the startup voltage required to enable the regulation.

It is curious that this effect does not appear at LDRs and seems to be enhanced with higher dose rates. If this effect was due to a current gain degradation, it should either be higher at LDRs if the device is sensitive to ELDRS or at least not be so much lower. This could indicate that this effect is not due to a gain degradation but rather to a current leakage increase. Similar behavior has been observed in the LM117 [2] where an increase in the collector to emitter (I_{C-E}) current leakage of one of the transistors of the bandgap circuit was visible at HDRs and not at LDRs.

B. Combined TID–DD Responses

A first observation that can be made regarding the previously discussed TID data is that the higher degradation observed in the past with protons was certainly due to the difference in the dose rate between the gamma and the proton experiment. Indeed, it can be seen that the degradation response obtained with the gamma source at an ionizing dose rate of 620 Gy(SiO_2).h^{-1} is practically the same as the proton response shown in [3] where the current drops suddenly around a TID of 500 Gy(SiO_2). This indicates that at this high ionizing dose rate, the TID degradation mechanisms seem to dominate over the DD ones at this DDD/TID ratio. However, such a high ionizing dose rate is not representative of the LHC ones, and thus the proton response might overestimate the degradation rate. For this reason, these proton data are not further considered for this study.

Then, the different combined TID–DD irradiation responses showed in comparison to the individual TID and DDD responses scale to the DDD/TID ratios together with their intrinsic device-to-device variabilities were also discussed in [3]. On the other hand, to discuss the data from another perspective, the different combined irradiation responses obtained with different ratios are shown all together in Fig. 7 as a function of DDD. Since in this figure each curve corresponds to a different DDD/TID ratio, no TID axis is shown since the devices are exposed to different amounts of TID for the same DDD. The choice of representing them as a function of the DDD dose instead of the TID is motivated by the outcome of the circuit simulation that will be described in detail in the following section, showing that the primary degradation mechanisms seem to be induced by DDs. Therefore, this figure is further discussed in the combined TID–DD simulation section of this article.

However, two important observations can be made at this stage from these responses. The first one is the fact that the response obtained in the PROSPERO nuclear reactor where the DDD/TID ratio was at 3.1×10^{-1} is very similar to the one observed with HDR where the increase in the startup voltage leading to this sharp decrease in the output current is assumed to be caused by a current leakage. Considering this assumption as correct, since during this test the cumulated TID was only 13 Gy during this irradiation and the fact that the ionizing dose rate was very low, it can be assumed that the current leakage is in this case induced by DDs.

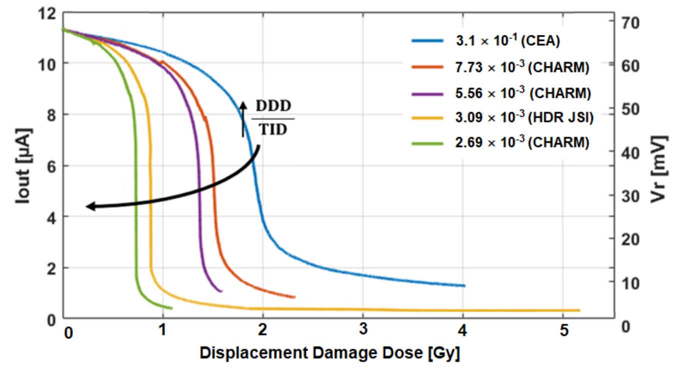

Fig. 7. LM334 DD responses as a function of DDD/TID ratios from experiments performed in the CHARM and JSI Facilities.

Then the second observation is the fact that while increasing the ratio of TID during the different combined TID–DD irradiations, the global degradation shape is similar, but with a higher degradation rate. Therefore, the degradation mechanisms down to the ratio of 2.69×10^{-3} is the same as for the practically pure DD test.

Based on these different assumptions, different types of degradation were applied at the transistor level to see their impact at the circuit level, and from these individual degradations, different circuit degradation scenarios have been simulated to explain the observed degradation curves.

IV. Circuit Simulations

To simulate the radiation effects of BJT on SPICE, it is possible to modify their electric parameters, commonly the current gain (H_{fe}) and the current leakages. However, the response of the circuit also depends on other parameters such as the saturation currents and Early voltages. In our case, none of these parameters is known and arbitrary values giving the same circuit response as in the datasheet have been selected. The variations in these parameters to simulate radiation effects are also arbitrary. However, the main objective of this work is more to understand how the different mechanisms can interact with each other and lead to the observed circuit degradation responses rather than identifying the exact amount of internal degradation.

The simulations were performed in two different steps; in the first one, parametric changes are applied to the transistors individually to understand their impact on the circuit output, and then different scenarios of degradation combinations were tested to reproduce the observed circuit radiation responses.

A. Current Gain Degradations

The first type of degradation applied is the current gain H_{fe} decrease or said differently, the increase in the base current. Two different impacts at the circuit level can be observed. With this type of degradation, two different effects on the circuit response were observed, the increase or the decrease in the bandgap voltage reference depending on the transistor impacted.

1) Bandgap Reference Voltage Decrease: The decrease in the bandgap reference voltage, which in return controls the fixed output current, can be induced by the degradation of any of the transistor Q3, Q4, Q5, or Q6.

Focusing first on the effect of the decrease in the gain of Q4, Q5, and Q6, their degradation will lead to the decrease in their collector current for the same base current. This will decrease the current flowing through R1, and thus ΔV_{BE}. To compensate for this effect, the feedback transistor Q3 will increase proportionally its collector current, and thus the base current of Q4–6, to maintain the same output current satisfying $I_{C1} = I_{C2}$ and $\Delta V_{\mathrm{BE}} = 0.64$ mV. However, at the same time that Q3 increases its collector current, it increases its base current, which drains the collector current of Q4 feeding the current I_{C2} of the Brokaw cell. Therefore, while Q3 compensates the excess current gain of Q4–6, it also decreases the current I_{C2}. Therefore, when the increased base current of Q3 is no more negligible compared with I_{C2}, it is not possible anymore for the circuit to keep the branches of the Brokaw cell balanced. Then, according to (1) if I_{C2} becomes lower than I_{C1}, the ratio of the currents becomes lower than 1 and then ΔV_{BE} decreases. Similarly, the decrease in the current gain of the feedback transistor Q3 itself will lead to the increase in its base current, which will lead to the same decrease in I_{c2}.

The effect of the decrease in the current gain of each of these transistors on the $I_{\mathrm{out}} = \mathrm{f(Vcc)}$ characteristic and the corresponding evolution of ΔV_{BE} as a function of the reciprocal of the gain are shown in Fig. 8. These values have been calculated considering an arbitrary initial current gain of 50 for each of them. It can also be seen that Q6 being composed of 16 transistors in parallel has a much greater impact than Q4 and Q5 for the same degradation. It has to be noted that the impact of the degradation of Q4–6 is greatly dependent on the initial current gain of Q3. For a high initial Q3 gain, a larger degradation of Q4–6 is necessary to have the same effect.

2) Bandgap Reference Voltage Increase: On the other hand, decreasing the current gain of the transistors Q1 and Q2 of the Brokaw cell will lead to the increase in the voltage reference. Starting with Q1, the main effect of its gain degradation is to affect its ability to mirror the current I_2. The current of Q1 can be described with the following equation neglecting the Early effect:

$$I_2 = \frac{1}{1 + \frac{2}{h_{\mathrm{fe}_{C2}}}} \cdot I_1. \quad (3)$$

Before irradiation, the first term is practically equal to 1 due to the high gain value. While the radiations decrease the gain, this term decreases, and the current I_2 becomes lower than I_1. Therefore, in (1) since I_2 decreases, the ratio of I_1 over I_2 becomes higher than 1, which increases the voltage reference ΔV_{BE}.

A similar effect occurs with the degradation of Q2. While its gain decreases, its collector current is also decreases, leading to the same effect as the degradation of Q1. The impact of these two mechanisms on the ΔV_{BE} degradation is also shown in Fig. 9.

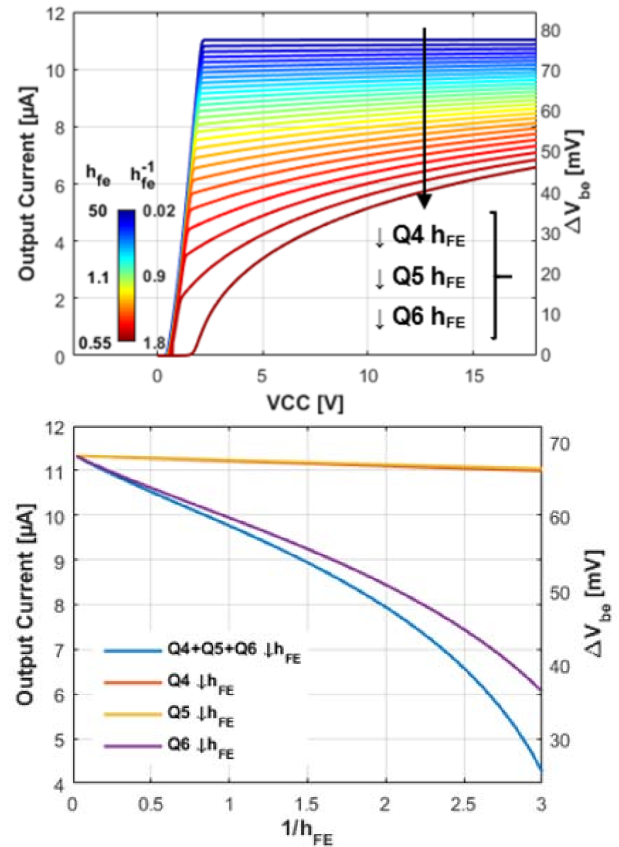

Fig. 8. Degradation impact of transistors Q4, Q5, Q6, and Q4–6 on LM334 $\Delta V_{BE} = \mathrm{f(VCC)}$ characteristics (top) and on ΔV_{BE} change (bottom).

B. Current Leakage Increase

It has been shown in [2] and [14] that the transistors Q1 and Q2 of the Brokaw circuit could suffer from the collector to the emitter (C–E) with TID at HDR. In the LM334, the feedback reaction is connected to Q2 and thus can be affected by a current leakage on Q2.

To simulate the C–E leakage parts, high resistances are placed between the collector and emitter terminals of Q1 and Q2 in the same way as in [15]. By decreasing their values, it is possible to simulate the increase in current leakage due to radiation. The effect of Q2 $I_{\mathrm{C-E}}$ increase is shown in Fig. 10. It can be seen that the current leakage induces an increase in the startup voltage V_{START}. Additionally, the minimum base current required by Q3 depends on the collector current it has to provide to start the Brokaw cell circuitry. This minimum current will be proportional to the current gain of the transistors Q4–6 and more particularly to the one of Q6 since it requires much more current. Consequently, the decrease in the gain of Q6 will enhance the effect of the current leakage of Q2. This enhancement can be seen in Fig. 10 where the change in the startup voltage is shown as a function of the current leakage for several Q6 current gain values.

C. TID Circuit Response

The most likely scenario explaining the observed degradation curves is that in the first place, the combined degradation rate of Q3–6 dominates over the degradation rate of Q1 and Q2, leading to the decrease in the bandgap voltage. Then

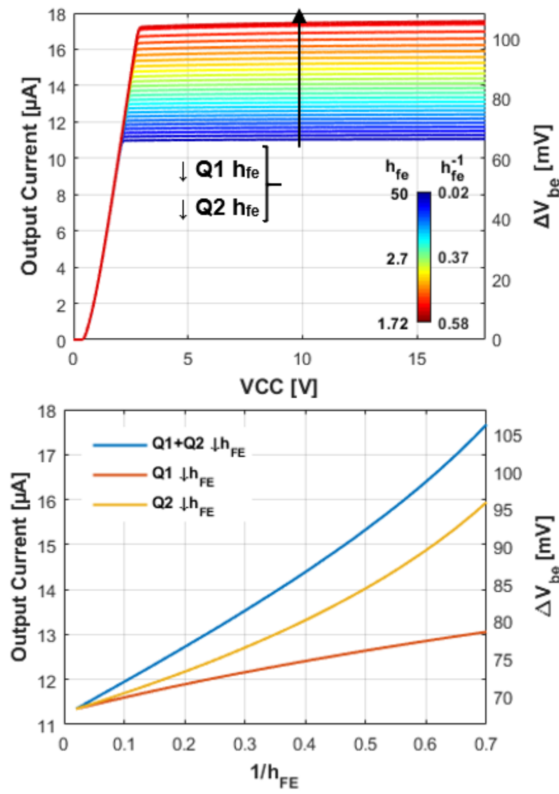

Fig. 9. Impact of the degradation of the transistors Q1 and Q2 on LM334 $\Delta V_{BE} = f(V_{+}-V_{-})$ characteristics (top) and on the change in ΔV_{BE} (bottom).

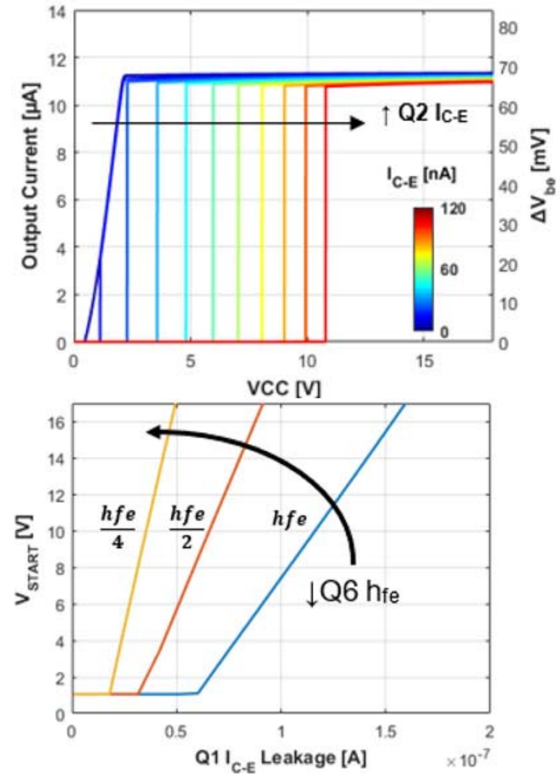

Fig. 10. Impact of Q2 collector to emitter current leakage (I_{C-E}) on LM334 $\Delta V_{BE} = f(V+-V_{-})$ characteristics (top) and on the evolution of the voltage required to start (VSTART) the circuit (bottom).

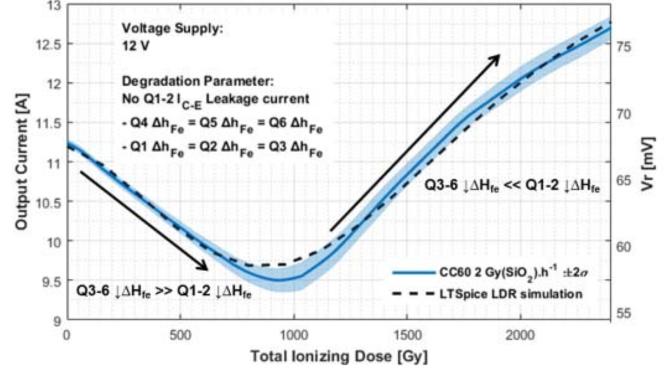

Fig. 11. Output current degradation observed during TID LDR irradiations with a cobalt 60 source and simulated.

in a second time, the gain degradation of Q3–6 reaches a saturation and the effect of the gain degradation of Q1 and 2 dominates, leading to the increase in the bandgap voltage. The two groups of components being different kinds of transistors (PNP versus NPN), it is not surprising their degradation does not saturate at the same levels.

It is difficult to estimate which of Q3 or Q6 contributes most to the decrease in the reference voltage. A scenario was tested in simulation considering a degradation of Q3 of the same order of magnitude as Q1 and Q2 and a degradation of Q6 greater than the first two based on the fact that with the same manufacturing process, PNP transistors might be more sensitive than the NPN ones. In this scenario, the degradation of Q6 is gradually brought to saturation after having reduced the reference voltage to 57 mV while the saturation point of the Q1 and Q2 transistors is set to appear much later. The ratio of the degradation rate of the Q3–6 group to the Q1 and Q2 group has been selected according to the decrease rate observed under irradiation and to their respective simulated change rate in the voltage reference shown previously. The resulting degradation shape obtained by simulating this scenario scaled to the one observed under irradiation is shown in Fig. 11. As it can be seen, this scenario allows achieving a good approximation of the experimental curve even though only an acquisition of the degradation of the internal elements under irradiation could confirm it.

Considering this scenario as realistic, it is clear that total circuit degradation is a combination of multiple degradation mechanisms, some mutually enhancing, others competing. Under these conditions, any difference in the sensitivity of the different transistors when exposed to different DDD/TID ratios could lead to different circuit degradation profiles.

D. Combined TID–DD Circuit Response

The great similarity between the simulation of the evolution of the characteristics as a function of the leakage current of Q2 and the observed characteristics strongly suggests that this mechanism is mainly responsible for circuit degradation. As mentioned above, this increase in the startup voltage has been observed on devices exposed to DD only and combined TID–DD at low ionizing dose rates while it has not been observed on devices exposed to low ionizing dose rate only. This suggests that the current leakage on Q2 is induced by DD effects.

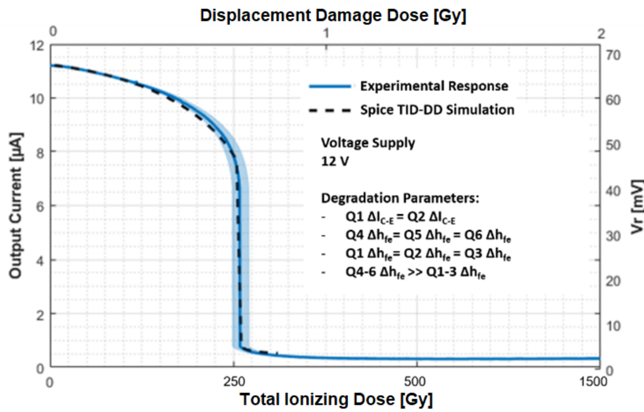

Fig. 12. Output current degradation observed during combined TID–DD irradiations at the CHARM Facility and simulated.

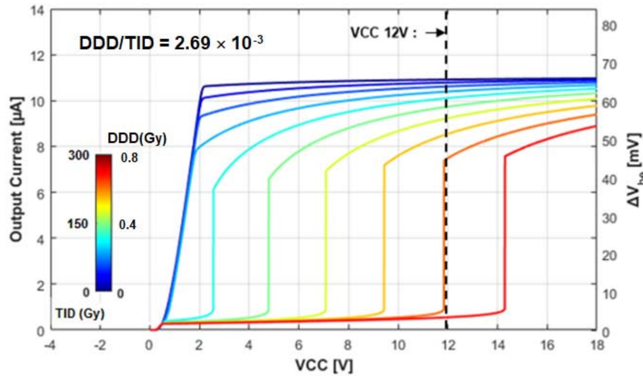

Fig. 13. Simulated characteristic output current evolution observed against TID–DD irradiation.

This scenario was tested in simulation, by applying the same current leakage on Q2 and Q1 transistors in addition to gain degradations. Concerning these, the same parameters as for the low ionizing dose rate simulation were kept meaning the same degradation rate for Q1–3 and Q4–Q6 with the degradation rate of the Q4–Q6 group higher than the Q1–Q3 group. However, in this case, a linear increase in the reciprocal current gain corresponding to the DD effects is applied in addition to the TID-induced degradations. This will have as effect that there will be no saturation of the damages, and therefore the initial degradation mechanisms including the decrease in the output current will never be compensated by the second degradation mechanism inducing its increase.

The resulting simulated output degradation is visible in Fig. 12, while the evolution of the current characteristics is visible in Fig. 13 in comparison to the experimental data. As it is visible, the simulated response achieves a good approximation of the experimental data once normalized to the same dose. Especially the shape of the evolution of the characteristic is particularly close to the experimental one. Therefore, the assumptions used for simulation seem to be reasonably representative of the real degradation mechanisms, even though only the monitoring of the internal transistor degradations could confirm it.

Finally, the most important outcome of this simulation is the fact that the combined TID–DD circuit response is due to: 1) gain degradations induced by TID and DD and 2) current leakage induced by DD only. Then, as shown in Fig. 10, the impact of the current leakage on Q2 leading to the startup voltage increase is enhanced by gain degradation of Q6 induced by both TID and DD. This means that the effect of the DD on the circuit is enhanced by the TID, and in a nonlinear way.

For this reason, the experimental data are shown in Fig. 13 as a function of the DDD. In this way, knowing that for each curve the degradation rate for each ratio is much higher than what could be reasonably expected from the individual responses as shown in [3], it seems that the experimental data support the above-presented explanation on the increase in the degradation rate with the increase in the ratio. Even though keeping in mind that only internal measurements after irradiation could give a definitive confirmation of these assumptions.

V. CERN RHA IMPLICATIONS

Considering the analysis presented in this work, it is clear that when exposed to the LHC environment, the wide range of DDD/TID ratios of the LHC can potentially lead to a wide range of degradation rates for this component and potentially many others.

Therefore, particular attention has to be paid when qualifying devices potentially sensitive to such effects. Since in the framework of regular and quantitative component RHAs such a methodology cannot be systematically followed, due to the relatively high amount of work to achieve such a simulation and the fact that for commercial components the internal design is not always known, another methodology should be followed for qualification. A methodology based on DDD/TID ratio tests was proposed in [3], consisting of first identifying the ratio to which the system will be exposed to in operation, by measurements or simulations, and second by irradiation the devices to a certain number ratios representative of the target operational environments. Then since the final step is to calculate the failure levels of the device according to the system requirements against the different ratios and to verify that it is compliant with the radiation levels associated with the different ratios in operation.

For instance, for the studied device, the different failure levels calculated for a maximum variation in 30% of the initial output current for the different tested ratios are shown in Fig. 14. In this figure, the failure levels obtained with combined TID–DD response with HDR TID are marked in blue since they are not representative of the real behavior. The two failure fits are figures of merit calculated from the simulation models together with the additional assumptions that below ratios of 10^{-3}, the DD becomes negligible and above ratios of 0.1 the TID becomes negligible, and thus the failure levels are constant since there is no interaction between the different effects. For the fits, the second failure contribution called "bandgap failure" concerns the case where the degradation limit is overpassed due to the drift of the bandgap voltage due to the TID contribution only.

It can be seen from the figure that in the case of this component, for about 80% of the ratios the device will be exposed to in operation, the device will show a very low level of combined TID–DD circuit effects, while for the 20%

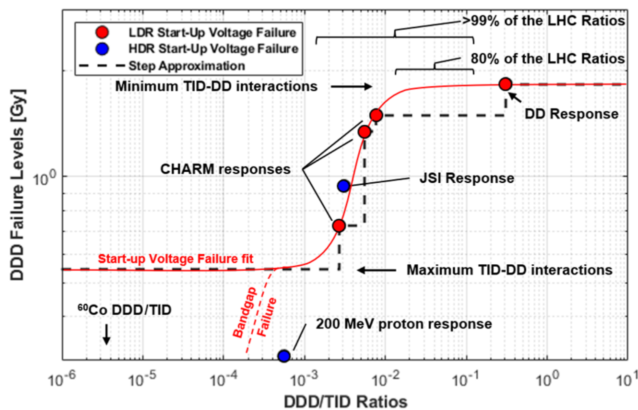

Fig. 14. LM334 failure levels expressed in DDD for different DDD/TID ratios obtained in different test facilities. Failures levels correspond to a change in the current output above a ±30% tolerance. The two failure fits are figured of merit calculated from the simulation model.

remaining the combined effects are a real driving factor to be considered for qualification. Such a qualification methodology can then be applied without the need of performing simulations or knowledge of the internal structure.

VI. Conclusion

In this work, it has been introduced that integrated circuits sensitive to both TID and DD effects could exhibit combined TID–DD circuit effects when exposed to both effects simultaneously. Such interactions between the internal degradation mechanisms could lead a component to exhibit a various range of degradation profiles when exposed to a wide range of DDD/TID ratios such as the ones that can be found in high-energy accelerator environments.

To give an example of how TID- and DD-induced degradation mechanisms can interact at the circuit level depending on the DDD/TID ratio, degradation simulations have been performed on the internal circuit of a case study component, the LM334, which has been shown to be sensitive to this effect in previous work.

Thanks to the additional TID irradiations that have been performed at different dose rates, three different degradation mechanisms have been identified; one inducing the decrease in the output current, one inducing the increase in the output current, and the last one inducing the increase in the startup voltage. Then, to understand the cause of these different mechanisms, a SPICE model reproducing the characteristic of the component based on the internal circuit given in the datasheet has been built.

Afterward, a first set of simulations have been performed where the impacts of a current gain decrease and the emitter current leakage of each transistor on the circuit's response were analyzed. From this analysis, it has been shown that the three different observed degradation mechanisms could be reported to the degradation of three different groups of transistors.

Finally, from this analysis, two circuit degradation scenarios were proposed, combining specific degradation conditions for those three groups, to reproduce the degradation profiles observed against TID only and combined TID–DD. Besides being in good agreement with the experimental data, these circuits simulations have shown that the impact of the DD that seems to be induced in one of the transistors on the circuit response can be enhanced by the degradation of the current gain of another transistor in the circuits induced by TID and DD. Therefore, it has been shown that the level of interaction between these two mechanisms seems to depend on the DDD/TID ratio, which is in agreement with the observed increased degradation rate as a function of the ratios.

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