Energy-Resolved Soft-Error Rate Measurements for 1–800 MeV Neutrons by the Time-of-Flight Technique at LANSCE

Hidenori Iwashita, Gentaro Funatsu, Hirotaka Sato, Takashi Kamiyama, Michihiro Furusaka, Stephen A. Wender, Eric Pitcher, and Yoshiaki Kiyanagi

***Abstract*— Problems caused by neutron-induced soft errors in electrical devices are becoming increasingly common in various applications. The neutron-energy-dependent soft-error rate is indispensable for evaluating the frequency of such errors in different neutron fields. We have observed the energy-dependent neutron-induced error rates continuously over the energy range of 1–800 MeV at Los Alamos Neutron Science Center (LANSCE). This was made possible by using extremely fast circuits built into field-programmable gate arrays (FPGAs) for time-of-flight measurement. Current experimental results revealed the overall trend of the error rate, which gradually increases up to 20 MeV. Interestingly, the rate depended on the type of device, and the errors occurred even below the threshold energy of the nuclear cross section of silicon, 2.75 MeV.**

***Index Terms*— Field-programmable gate arrays (FPGAs), neutron radiation effects, particle accelerator, single-event upset (SEU) cross section, time-of-flight (TOF) technique.**

I. Introduction

MODERN society's infrastructures are becoming increasingly dependent on digital technologies and are undergoing a digital transformation [1], [2]. However, although people enjoy greater convenience in everyday life, various issues such as software bugs in electronic device logic and compromised security have become major social problems [3]. In addition, there are random phenomena called bit errors in semiconductor devices such as in large-scale integrated circuits (LSIs) including memory chips. Soft errors caused by cosmic rays are one category [4], but there are many cases where the causes are unknown [5], making them very difficult problems to solve. At present, neutrons generated by cosmic rays are the main cause of soft errors in semiconductor devices of electronic equipment used on the ground [6], [7]. When cosmic rays arrive from outer space, they collide with oxygen or nitrogen nuclei in the atmosphere, and various secondary particles are generated by a spallation reaction. Among these particles, neutrons have particularly strong penetrating power because they are uncharged and can pass through the concrete structures of buildings. When neutrons pass through a semiconductor device on an electronic circuit board, it can interact with the silicon nucleus and generate secondary ionizing particles, although it is a very rare event. The ionizing particles can reverse internal logic states in the chip, referred to as a single-event upset (SEU) [8]. The rate of SEUs per device (unit area) becomes nonnegligible as the degree of LSI integration becomes greater. This is because the design rule, which is related to the minimum processing linewidth, becomes narrower each year, and the critical charge of an SEU becomes less along with the linewidth. Recent progress in larger integration and increasingly finer microfabrication technologies has resulted in dramatic increases in the occurrence of soft errors in contrast to hard errors that permanently disable semiconductor devices [9], [10]. Fig. 1 shows the relationship between the design rule and failure in time (FIT), which is the number of failures per billion hours per device, in the case of static random access memory (SRAM)-based field-programmable gate arrays (FPGAs). Furthermore, the rate of multiple bit upsets is increasing with narrowing of the design rules. For example, in a real-world information network consisting of 10 000 communication units, each with 5 of the 10 000 FIT LSIs in stacks, about 12 soft errors will occur on a daily basis. At this rate, network operators would not be able to handle all the errors. Also, soft errors may cause network equipment to be hung up and lead to a breakdown in some network services [5]. Occasionally, in a worst case scenario, the breakdown can grow to become widespread one. Such kinds of effects due to SEUs are not limited to those occurring in information network devices but may also occur in various other electronic devices used in modern society. Consequently, SEUs may have serious impacts when such devices are incorporated into medical instruments, automobiles, airplanes, trains, and personal computers, to name but a few.

Therefore, it is crucial to design and fabricate semiconductor devices and systems to minimize the SEU error rate measured

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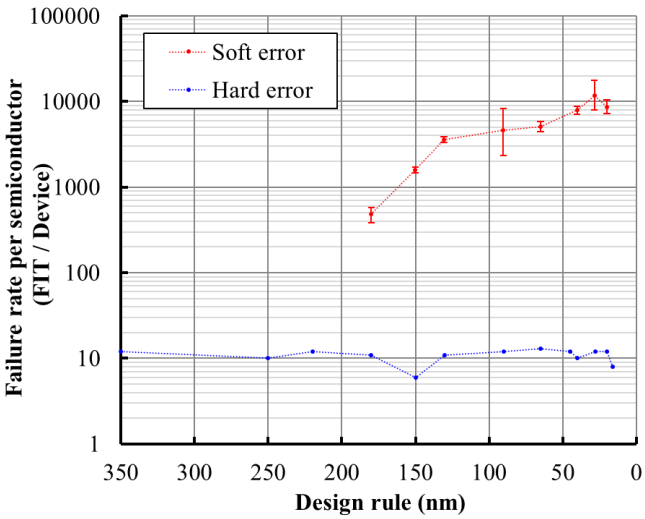

Fig. 1. Relationship between the design rule and FIT, which is the number of failures per billion hours per device, in the case of an SRAM-based FPGA. Recent progress in integration and microfabrication technologies has resulted in a dramatic increase in the occurrence of soft errors in contrast to hard errors, which permanently disable semiconductor devices [9], [10].

in FIT units to ensure the reliability and safety of these devices and systems. In order to calculate the expected number of failures due to soft errors in various neutron environments (natural, space, building, accelerator, nuclear plant, underground, etc.), the number of neutrons per unit time at each neutron energy, and the SEU cross section at this energy, are required for a wide energy range of impinging neutrons [11]. The SEU cross section $\sigma_{\mathrm{SEU}}(E_{\mathrm{n}})$ is defined as

$$\sigma_{\mathrm{SEU}}(E_{\mathrm{n}}) = \frac{N_{\mathrm{SEU}}(E_{\mathrm{n}})}{\Phi(E_{\mathrm{n}})} \tag{1}$$

which identifies a neutron fluence $\Phi(E_{\mathrm{n}})$ as the total number of neutrons per unit area impinging on the semiconductor device, and the total number of SEUs, $N_{\mathrm{SEU}}(E_{\mathrm{n}})$, generated by these neutrons. Specifically, it indicates the probability that one neutron per unit area causes a soft error. Note that the SEU cross section for each neutron energy will differ for each semiconductor device. In addition, neutrons in the natural environment and neutrons generated by accelerators have distinct energy distributions. Therefore, the soft error rate (SER) in a specific neutron irradiation environment can be defined as

$$\mathrm{SER} = \int_0^\infty \sigma_{\mathrm{SEU}}(E_{\mathrm{n}})\phi(E_{\mathrm{n}})dE_{\mathrm{n}} \tag{2}$$

using the neutron flux $\phi(E_{\mathrm{n}})$ (number of neutrons with energy E_{n} crossing a unit area in a unit time) at each neutron energy E_{n} and SEU cross section $\sigma_{\mathrm{SEU}}(E_{\mathrm{n}})$. Thus, the SEU cross section is the most important basic datum necessary for calculating the failure rate of semiconductor devices due to soft errors. However, even this SEU cross section has been measured at only a few points in the neutron energy range of 1–176 MeV [12], [13]. One method to measure it is to use a (quasi-)monoenergetic neutron beam. In Tohoku University, the Nuclear Engineering Department has the Dynamitron accelerator-based facility (FNL) capable of generating monoenergetic neutrons at energies of 1, 2, 5, and 15 MeV [12], [13], and the Radioisotope Center (CYRIC) has an azimuthally varying field (AVF) cyclotron, generating quasi-monoenergetic neutrons at 35, 45, and 65 MeV [4]. The Svedberg Laboratory (TSL) has a cyclotron-generating quasi-monoenergetic neutrons at 21, 47, 96, and 176 MeV [14]. In these facilities, there is no one that can measure the SEU cross section at energies higher than 176 MeV. As a consequence, there are no data on SEU cross sections continuously covering a wide range of neutron energies using this method, so the whole photograph of the cross section is yet to be clarified.

Therefore, we tried to measure the energy-resolved SEU cross section by the time-of-flight (TOF) technique [15] for a wide energy range. Accordingly, we devised a method to detect errors in the desired time resolution using an FPGA [16], [17] and measured the SEU cross section using the TOF technique at the Los Alamos Neutron Science Center (LANSCE).

II. Measurement Methods

A. TOF Technique

The TOF technique makes it possible to determine the neutron velocity v (i.e., neutron energy) by measuring the flight time of a neutron along a known path. In the sub-GeV region, neutrons have velocities close to the speed of light, thus we need to consider the relativistic effects. The neutron energy E_{n} is determined from

$$E_{\mathrm{n}} = \frac{m_0c^2}{\sqrt{1-\left(\frac{v}{c}\right)^2}} - m_0c^2 = \frac{m_0c^2}{\sqrt{1-\left(\frac{L}{ct}\right)^2}} - m_0c^2 \tag{3}$$

where m_0 is the neutron rest mass, v is its velocity, c is the velocity of light, L is the flight path length, and t is the neutron flight time. Using the TOF technique, it is possible to determine the energy of the neutron that caused a soft error by measuring the time at which the soft error occurred. The TOF of the sub-GeV neutrons that cause an SEU is very short, for example, 1.4 μs at 1 MeV and 79.3 ns at 800 MeV with the LANSCE path length of $L = 20$ m. For this reason, we chose a time duration of 8 ns for the detection of SEU to get time resolution of $\Delta t/t = 10\%$ at 800 MeV (see Fig. 2). However, it is impossible to measure TOF in the desired time resolution using conventional SRAM. Furthermore, because an ordinary SRAM reads data sequentially, it takes several milliseconds to scan sufficient data for soft-error detection. This makes it impossible to achieve nanosecond-order TOF measurements by using an SRAM. Even if many sets of SRAM and memory-readout circuits are made using on-chip SRAM in an FPGA, it is impossible to scan several M-bits in an order of nanoseconds. Therefore, we designed circuits that can detect a soft error due to a malfunction in logic circuits composed of configuration random access memory (CRAM) that determines the logic of the FPGA. In this case, determination of a CRAM bit error is possible at the operating frequency of the FPGA. In addition, it is possible to monitor a capacity equivalent to several 10 Mb FPGAs. We devised a circuit that can detect an SEU in nanoseconds, and we have conducted SEU cross

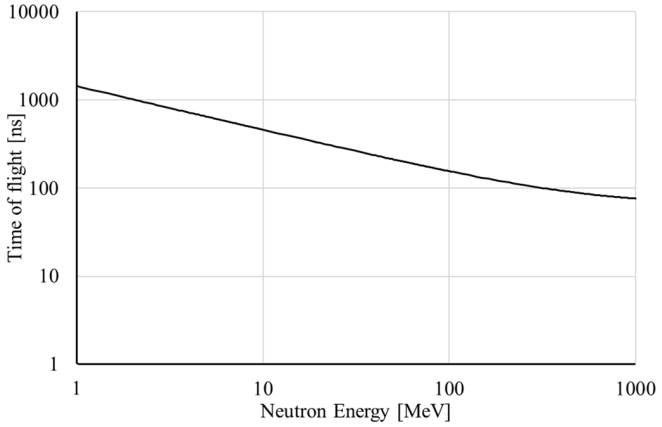

Fig. 2. Neutron energy versus the TOF at $L = 20$ m. The neutron energy E_n is determined from (2), where m_0 is the neutron rest mass, v is its velocity, c is the velocity of light, L is the flight path length, and t the neutron TOF.

section measurements of FPGAs depending on the neutron energy, using the TOF technique.

B. Soft Error Detection in the Nanosecond Order Using FPGA

We first considered using the cyclic redundancy check (CRC) [18] circuit, which can detect the CRAM errors, built into modern FPGAs to get TOF information. The FPGA stores circuit design data in an SRAM-based CRAM and can program logic circuits and wiring using bits of the CRAM. Then, when a CRAM bit is inverted by an SEU, it is immediately transmitted to a logic circuit or a wiring and then it rewrites them, which is not the effect intended by the programmer of FPGA [19]. Recent FPGAs have the ability to detect bit errors by CRC [18] in order to detect soft errors of the CRAM. However, the neutron energy cannot be specified with the TOF technique by the CRC of a CRAM because a detection time of several tens of milliseconds is required in order to check all the CRAM bits. Therefore, we focused on any logic malfunction in the circuit caused by CRAM errors. When a bit error occurs in a CRAM bit related to circuit operation, the circuit operation changes immediately, and a logic malfunction occurs. Since FPGA circuits can operate at several hundred MHz, a logic malfunction can be detected in nanoseconds by programming user circuits to detect the malfunction. For this purpose, we programed a user circuit that has a large number of registers and monitors.

The basic principle of this measurement is shown in Fig. 3. This FPGA, which is also a device under test (DUT), operates at 250 MHz and outputs an error signal that triggers the TOF signal when a logic error occurs due to a soft error. As shown in Fig. 3(a), register comparator units [see Fig. 3(b)] consist of two multiplexer units (MUXs), two 32-bit registers, and a comparator detecting a logic malfunction. The logic malfunction is detected by comparing the two output signals of the MUXs. Fig. 3(c) shows the details of the MUX that constitutes one bit of the 32-bit register. A flicker signal whose value is inverted at every positive edge of the clock is fed to one of the four lines of the lookup table (LUT) input. One of the two CRAM values is selected by the flicker signal. When the value

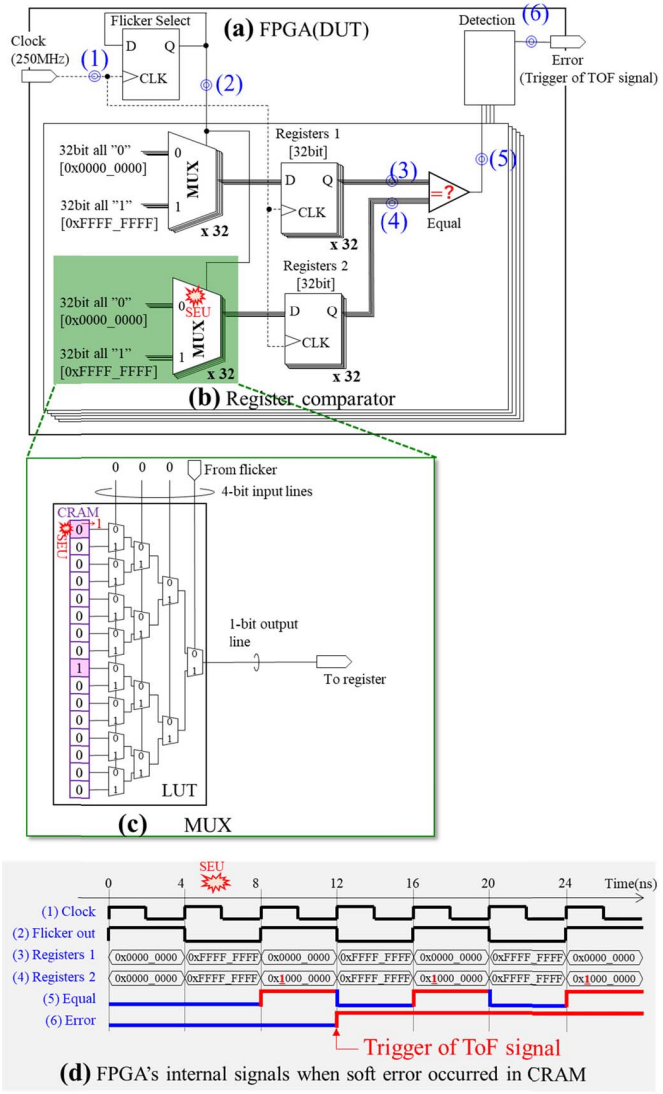

Fig. 3. High-speed logic malfunction detection circuit. (a) This FPGA, also it is a DUT, operates at 250 MHz and outputs an error signal that triggers the TOF signal when a logic error occurs due to a soft error. (b) Register comparator units consist of two MUXs, two 32-bit registers, and a comparator detect a logic malfunction. The logic malfunction is detected by comparing the two output signals of the MUXs. (c) Details of the MUX that constitutes one bit of the 32-bit register. A flicker signal whose value is inverted at every positive edge of the clock is fed to one of the four lines of the LUT input. One of the two CRAM values is selected by the flicker signal. When the value of the one of two CRAMs changes due to a soft error, the value read also changes. (d) Timing diagram of the FPGA's internal logic at signal monitoring points at (1)–(6) when a soft error occurred in the CRAM. When the flicker is "1," 0xFFFF_FFFF is output from the registers 1 and 2 at the next clock, and when flicker is "0," $0 \times 0000\_0000$ is output. When a soft error occurs, the output value of the register changes, so a logic malfunction is detected.

of the one of two CRAM changes due to a soft error, the value read also changes. Fig. 3(d) shows the timing diagram of the FPGA's internal logic at signal monitoring points (1)–(6) in Fig. 3 when a soft error occurred in the CRAM. The output of the registers repeats all "0" ($0 \times 0000\_0000$) or all "1" (0xFFFF_FFFF) alternately, according to the "Flicker Select" signal. If any of the comparison results do not match, the detection module asserts an error and outputs it as a TOF trigger signal. The operation of each MUX is controlled by

LUT in the FPGA. The registers are all 32-bit ones, but we first focus on only one bit of them. The flicker signal is fed into one of the 4-bit input lines in the LUT and all the other three lines are set to "0." As a result, one of the two SRAM bits is selected, one is initially set to 1 and the other 0, result in the time series of alternative "1" and "0." A corresponding bit pattern of the desired logic is stored in a 16-bit (=24-bit) CRAM. When a condition is put into the 4-bit input lines, the result is output to the 1-bitline. The result is then hold by a flip-flop circuit. Therefore, when a CRAM bit is inverted, an incorrect value is written to the register at the next clock timing. There are two identical 32-bit registers, but only one register output is affected by the soft error, and therefore, by comparing the two registers, the error is detected by this circuit. When this circuit is operated with a 250-MHz clock, the logic malfunction can be detected within 8 ns. The neutron energy can then be specified by obtaining the difference between the time at which neutrons were generated and the timing [Fig. 3, (6)] at which a logic malfunction is detected in a few nanoseconds resolution.

However, because only two bits are possibly affected by soft errors out of 8 bits in one of the MUX circuits, not all CRAM errors can be observed as logic malfunctions. In addition, the logic malfunction is detected when the CRAM bit for wiring is inverted because the wiring route in the FPGA is also controlled by the CRAM bits. However, it is difficult for the programmer of FPGA to know the number of bits used for wiring. That is, the design user has no way of knowing how many CRAM bits cause logic malfunctions. On the other hand, the functioning of a CRAM CRC check can detect all CRAM bit errors. Therefore, although the CRAM bit error rate and logic malfunction rate are different, the energy dependent t probability distribution of the logic malfunction and CRAM error is identical since the CRAM error causes the logic malfunction. These relationships can be defined in

$$P_{\mathrm{CRAM}}(E) = P_{\mathrm{LM}}(E) = \frac{N_{\mathrm{CRAM}}(E)}{N_{\mathrm{CRAM}}} \tag{4}$$

where $P_{\mathrm{CRAM}}(E)$ is the probability distribution of the number of CRAM errors as a function of neutron energy, $P_{\mathrm{LM}}(E)$ is the probability distribution of the number of logic malfunctions as a function of neutron energy, $N_{\mathrm{LM}}(E)$ is the logic malfunction counts as a function of E, and N_{LM} is the logic malfunction counts for whole energy range ($N_{\mathrm{LM}} = \int N_{\mathrm{LM}}(E)dE$).

Therefore, the CRAM error cross section that depends on the neutron energy $\sigma_{\mathrm{c}}(E)$ is given as

$$\sigma_{\mathrm{c}}(E) = \frac{N_{\mathrm{CRAM}}(E)}{\phi(E)} = \frac{N_{\mathrm{CRAM}} \times P_{\mathrm{LM}}(E)}{\phi(E)} \tag{5}$$

where $N_{\mathrm{CRAM}}(E)$ is the CRAM error counts as a function of E, N_{CRAM} is the CRAM error counts for the whole energy range, $P_{\mathrm{LM}}(E)$ is the probability distribution of the logic malfunction as a function of E, and $\phi(E)$ is the spectral neutron fluence to which the device was exposed in units of n/MeV/cm^2. For this reason, we measured the logic malfunction relative to the TOF and the CRAM error rate.

C. Facilities

There are four requirements for the accelerator facility to perform this measurement.

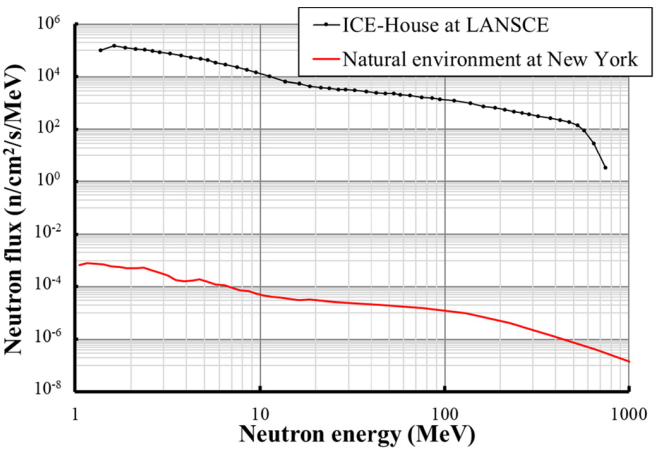

Fig. 4. Neutron energy spectrum at ICE-House in LANSCE and the natural environment spectrum of neutrons induced by cosmic rays under reference conditions (sea level, New York City, midlevel solar activity, outdoors) [11].

1) *A pulsed neutron source with a short pulsewidth*. In order to measure high-energy neutron using the TOF technique, the duration of the pulse of the accelerated particles entering the target is preferably 1 ns or less with the flight path of about 20 m. Note that this requires a beamline directly viewing at the target without a moderator.

2) *A high-energy white neutron source.* To measure a wide neutron energy range up to hundreds of MeV region, neutron source driven by a high-energy proton accelerator is indispensable.

3) The incident neutron energy spectrum should be available or measurable within a specified precision. It is crucial to calculate SEU cross section.

4) Neutron intensity should be high enough.

In this experiment, it takes time to obtain data with satisfactory statistical accuracy because the logic malfunction rate of the proposed method is lower than of CRAM as a whole. In addition to this, in order to obtain a precise energy-dependent cross section by the TOF method, a very high-intensity neutron source is required to obtain high statistical accuracy in short time bins for high energy resolution and the logic malfunction rate is much lower than the CRAM error rate. The best accelerator facility that satisfies the above requirements is the ICE-House or ICE-II at LANSCE [20], [21]. LANSCE is based on an 800-MeV proton linac with relatively long pulsewidth, but it has a storage ring to compress the beam. The facilities mentioned above utilize a short proton beam pulse of 125 ps [22]. Fig. 4 shows the neutron energy spectrum measured by a fission chamber installed 19.7 m from the target at LANSCE, together with neutron spectrum in a natural environment [11]. Thus, LANSCE has a neutron energy spectrum close to that in the natural environment, with about four order of magnitude higher neutron flux.

III. Experiment

We performed the experiment at the ICE-House in LANSCE and irradiated DUTs which are three types of commercially available FPGAs with design rules of 28, 40, and 55 nm. We measured logic malfunctions as a function of neutron

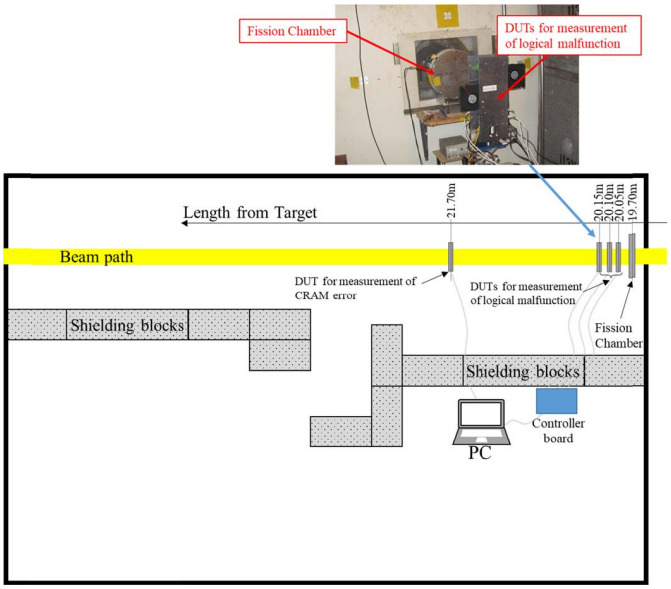

Fig. 5. Our experimental setup at the ICE-House. The experimental area is separated into two sections by a thick concrete and polyethylene wall. One of the sections contains the neutron beam (beam area), in which the DUTs are placed. The yellow line shows the neutron beam entering from the right and exiting to the left. The other section is equipped with all the monitoring equipment (controller board and PC). The fission chamber was installed at a length of 19.70 m from a neutron production target. The DUTs for measurement of the logical malfunction were installed at a length of 20.05, 20.10, and 20.15 m. The DUT for measurement of CRAM error was installed at a length of 21.70 m.

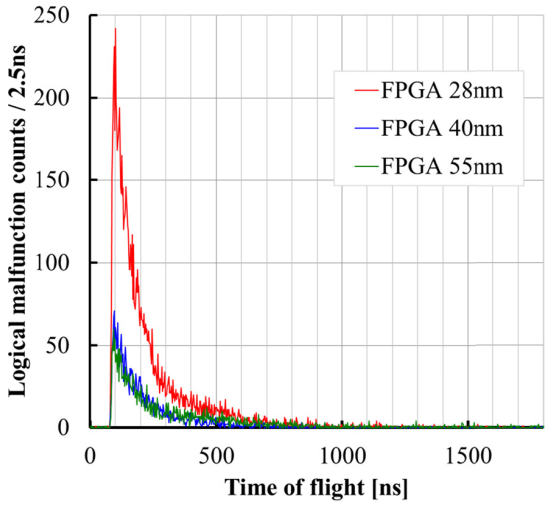

Fig. 6. Results of TOF spectra of logical malfunction counts. The TOF spectra of three FPGAs, which are DUTs, were measured. Since the wiring length of the proton pulse signal was unknown, the energy bin of 700–800 MeV was set as the time position at which peak begin rising. The total counts of logical malfunction in each FPGA are as follows: FPGA 28 nm, 12 713 counts; FPGA 40 nm, 2894 counts; and FPGA 55 nm, 3719 counts.

TABLE I

RESULTS OF MEASUREMENT OF N_{CRAM}

Design rule [nm]	Neutron Fluence above 1.25 MeV [n/cm^2]	CRAM Error Counts per Mbit (N_{CRAM})
28	7.08 x 10^9	5.5
40	5.12 x 10^9	6.2
55	1.37 x 10^{10}	13.5

Results of measurement of NCRAM (CRAM Error count). The CRAM error counts for each DUT and the irradiated neutron fluence above 1.25 MeV are shown.

energy and CRAM error counts for whole energy range separately. The experimental setup at the ICE-House is shown in Fig. 5. The experimental area is separated into two sections by a thick concrete and polyethylene walls. One of the sections contains the neutron beam (beam area), in which the DUTs are placed. The yellow line shows the neutron beam entering from the right and exiting to the left. The other section is equipped with all the monitoring equipment (controller board and PC). The fission chamber was installed at a distance of 19.70 m from a tungsten neutron production target. The DUTs for measurement of the logical malfunction were installed at distance of 20.05, 20.10, and 20.15 m. The DUT for measurement of CRAM error was installed at a length of 21.70 m.

For the measurement of logic malfunction, DUTs and the controller board are connected by four signals (error, status, reconfiguration, and power). The error signal is a timing signal at which a logic error is detected. The status signal indicates the status of the DUT during startup, monitoring, and error occurrence. The reconfiguration signal is for reconfiguring the FPGA in the DUT from the controller board. The power signal controls the power supply of the FPGA in the DUT from the controller board. The DUTs are recovered after an error by reconfiguring or restarting the FPGA power supply. The controller board calculates the time difference between the proton pulse and the error signal and performs recovery control of the DUTs. And the controller board outputs the time difference value to the PC.

For the measurement of CRAM error counts for whole energy range, the CRC function of the FPGA was used to detect CRAM errors. The CRC value is calculated when generating the configuration bitstream [9], [23], [24]. After the configuration bitstream is loaded into the FPGA, the CRC circuit of the FPGA calculated the CRC value of the CRAM and compares it with the precalculated CRC value. When a soft error occurs in the CRAM, the CRC values become inconsistent, and the error can be detected.

IV. RESULT AND DISCUSSION

The results of TOF spectra of logical malfunction counts of three FPGAs are shown in Fig. 6. The total counts of logical malfunctions in each FPGA are as follows: FPGA 28 nm, 12 713 counts; FPGA 40 nm, 2894 counts; and FPGA 55 nm, 3719 counts. Since the wiring length of the proton pulse signal was unknown, the energy bin of 700–800 MeV was set as the time position at which peak begin rising. Fig. 7 shows $P_{\mathrm{LM}}(E)$ converted into neutron energy by the TOF technique with same energy bin of the fission chamber and divided by the width of the energy bin. These error bars are calculated with the standard error (1σ: 68% confidence interval).

Table I shows the CRAM error counts. Fig. 8 shows the spectrum of neutron fluence irradiated in the CRAM error measurement.

Fig. 9 shows the CRAM SEU cross section calculated from the measured logical malfunction time distribution, CRAM error count, and neutron fluence. These error bars are calculated with the standard error (1σ: 68% confidence interval). The SEU cross sections tend to increase rapidly from 3 to

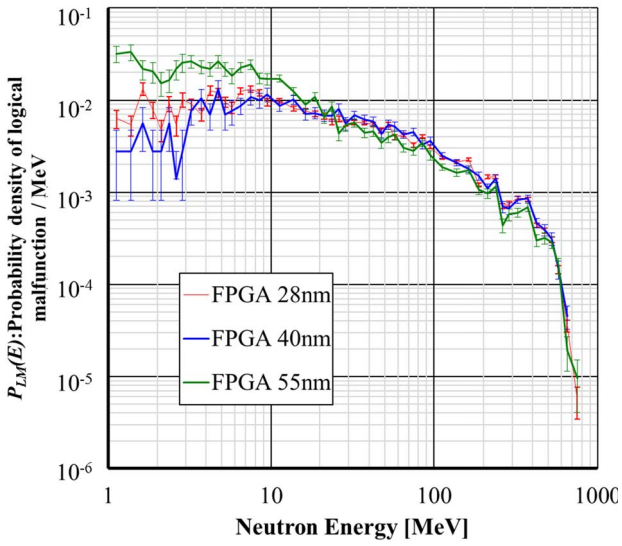

Fig. 7. Results of the neutron energy spectra of probability density of logical malfunction. The energy dependence of probability density was calculated from total counts and Fig. 6 converted into the neutron energy.

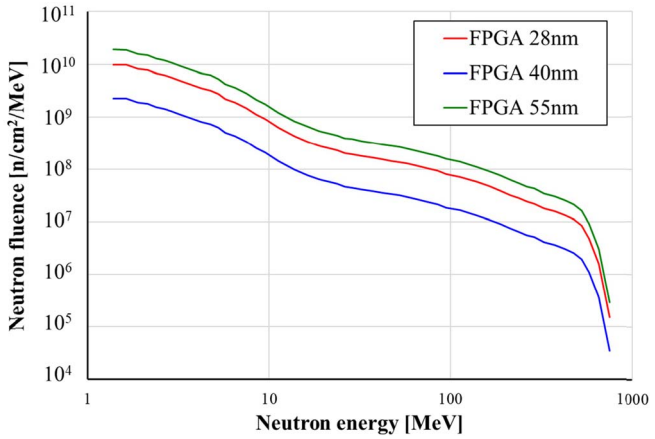

Fig. 8. Result of measured spectra of neutron fluence $\phi(E)$. The spectra of the neutron fluence were measured using the fission chamber during the CRAM error measurement. These fluences were obtained after correction to the fluences at the DUT position, considering the difference in length between the fission chamber and the DUTs.

20 MeV and remain almost constant thereafter. There is a difference in the absolute value of the cross sections among the three devices, although they are similar to each other. In the energy range from 1 to 3 MeV, the difference is several times. The device type for an Abe and Watanabe [25] simulation is not the same as the devices in this experiment, but the trend of SEU cross sections is similar to the one in their simulation. According to their simulation, SEUs below 5 MeV are caused by elastic recoils of O and Si ions. They also found that the sharp increase in the SEU cross section appeared near the threshold energies of the (n, p) and (n, α) reactions and is caused by secondary He and H ions. Their simulation showed that the sharp increase in gradient is enhanced by making the critical charge smaller. Generally, the smaller the design rule is, the smaller the critical charge tends to be [25]–[27], but FPGA 40 nm was the largest sharp increase. We infer that the reason for this is that FPGA 28 nm adopts high-k metal

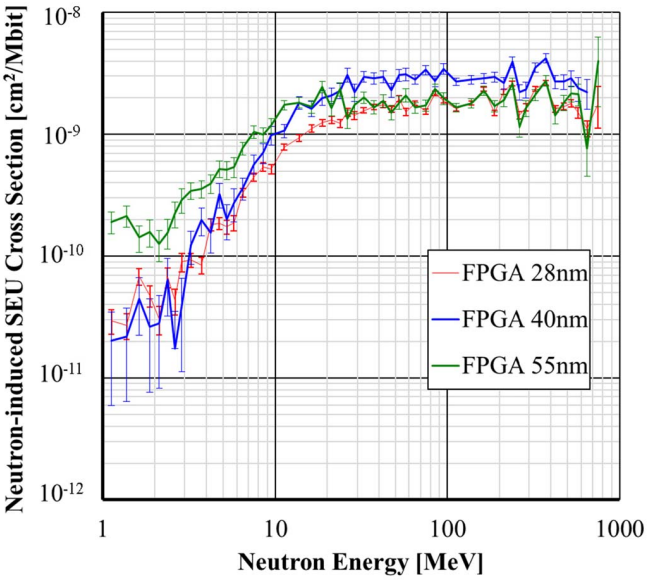

Fig. 9. SEU cross sections of the CRAM. The SEU cross sections tend to increase rapidly from 3 to 20 MeV and remain almost constant thereafter. There is a difference in the absolute value of the cross sections among the three devices, although they are similar to each other. In the energy range from 1 to 3 MeV, the difference is several times. The difference between the low-energy and high-energy SEU cross sections was larger for FPGA 40 nm and smaller for FPGA 55 nm.

gate (HKMG) technology. HKMG achieves a high dielectric constant by using metal for the gate [28]. As a result, both the gate capacitance and the critical charge increased, so it is estimated that the FPGA 28 nm had a milder increase than FPGA 40 nm. To confirm this, it is necessary to perform measurements with the HKMG and SiO_2 gate devices under the same design rules.

V. Conclusion

In summary, we devised a new method to measure the neutron-induced SEU cross section for the FPGA using the TOF technique up to 800 MeV. With this method, we could measure the SEU cross section with high energy resolution from 1 to 800 MeV at the ICE-house of LANSCE. The results showed the complete photograph of the SEU cross section. The most important contribution of these cross sections is that they enable us to calculate the SERs in any kind of neutron environment.

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