Heavy-Ion Microbeam Studies of Single-Event Leakage Current Mechanism in SiC VD-MOSFETs

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***Abstract*— Heavy-ion microbeams are employed for probing the radiation-sensitive regions in commercial silicon carbide (SiC) vertical double-diffused power (VD)-MOSFETs with micrometer accuracy. By scanning the beam spot over the die, a spatial periodicity was observed in the leakage current degradation, reflecting the striped structure of the power MOSFET investigated. Two different mechanisms were observed for degradation. At low drain bias (gate and source grounded), only the gate-oxide (at the JFET or neck region) is contributing in the ion-induced leakage current. For exposures at drain–source bias voltages higher than a specific threshold, additional higher drain leakage current is observed in the p-n junction region. This provides useful insights into the understanding of basic phenomena of single-event effects in SiC power devices.**

***Index Terms*— Heavy ion, leakage current degradation, microbeam, silicon carbide (SiC) vertical double-diffused power (VD)-MOSFET, single-event effect (SEE), single-event leakage current (SELC).**

I. Introduction

SILICON carbide (SiC) is a wide bandgap material of great interest for high-power and high-temperature electronic applications, including space [1], [2] and accelerators [3]. Higher breakdown field and thermal conductivity makes SiC a very attractive material for power electronics compared to silicon [4], [5]. However, like their silicon counterparts, SiC power devices (MOSFETs and diodes) are sensitive to single-event effects (SEEs). In particular, a unique SEE signature is observed in SiC power devices under heavy-ion irradiation [6]–[9]. For power MOSFETs, single ions can cause permanent degradation that leads to a gradual increased leakage in both drain and gate currents with increasing heavy-ion fluence. This damage is not catastrophic, but the device operation may be altered, which complicates the assessment of radiation tolerance in these parts. This effect is here referred to as single-event leakage current (SELC).

The heavy-ion-induced degradation in SiC MOSFETs was previously studied in [9]. It was observed that the gate area is the most vulnerable part within the MOSFET structure. The results show that the ion-induced leakage path forms from drain to gate when the irradiation bias is below a certain threshold voltage (about 30% of the maximum voltage or $V_{\mathrm{DS\ irr}} = 350$ V for the 80-mΩ die from the second-generation Cree/Wolfspeed studied in the article). Above this bias voltage, a permanent and more severe damage is caused in the MOSFETs and the leakage current is divided between the drain–gate and drain–source paths. Also, the leakage current path and the gate and drain degradation rates were observed to be independent of the prior degradation. Based on the experimental results, an electrical equivalent circuit model was proposed in [9] to explain the current transport in the degraded SiC vertical double-diffused power (VD)-MOSFETs.

SiC power MOSFETs are also sensitive to single-event burnout. Numerous experiments and simulations have been performed to study the SEB in SiC power devices for space and terrestrial environments [10]–[19]. Due to the similarities in results on SiC MOSFETs and diodes, it has been hypothesized that the conventional SEB mechanisms developed in Si MOSFETs, such as parasitic bipolar transistor and tunneling-assisted avalanche multiplication mechanism [20], may be suppressed in SiC devices. Indeed, there is no parasitic n-p-n bipolar junction transistor (BJT) in the diode structure.

In order to extend the exploration of the physical mechanisms of ion-induced failure in SiC VD-MOSFETs, experiments were performed at the Universal linear accelerator (UNILAC) microprobe line at the Helmholtzzentrum für Schwerionenforschung (GSI), Darmstadt, Germany. Au and

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Ca ion beams were used for the experiment. The focused beam (or microbeam) irradiation allows micrometer-accurate localization of the radiation-sensitive regions providing unique information for a deeper physical understanding of the SEE mechanisms in SiC technology. Different regions of the die were exposed to the heavy-ion microbeam, and the ion-induced steps in the gate and drain leakage currents were analyzed as a function of the $x-y$ coordinate within the scanned frame. The striped structure of the die was clearly recognizable and different sensitive regions were identified for different drain–source bias during the exposure, providing insights into the SELC mechanism. Two different responses to the ion strikes were observed in the monitored leakage currents. First, below a certain threshold voltage (about 30% of the maximum rated voltage or $V_{\mathrm{DS\ irr}} > 350$ V for the second-generation Cree/Wolfspeed), only the gate region (above JFET region) was observed to be sensitive to SELC. Second, by increasing the bias during the exposure ($V_{\mathrm{DS\ irr}} > 350$ V), higher sensitivity was measured in the p-n junction region of the vertical MOSFET.

Finally, it is hypothesized that the latter response in the observed SELC is caused by the appearance of extended defects (EDs), generated by an ion-initiated thermal stress, that consequently degrade the p-n junction area.

II. Heavy-Ion Microprobe Experiment

A. Heavy-Ion Microprobe Facility

The GSI's heavy-ion microprobe facility is situated at the end of the linear accelerator UNILAC. The ions enter the microbeam line through object slits, assuring a beam free of scattered particles [21]. The beam is focused to a focal spot of about 500 nm in diameter by means of magnetic quadrupole lenses and it is moved in the focal plane using deflecting magnets, situated downstream of the focusing lenses. The single hits are discriminated by a channel electron multiplier (CEM) which detects the secondary electrons emitted by the materials due to the ion hit. To ensure the irradiation with a preset number of particles and to avoid double hits at the same position, a fast electrostatic beam switch, situated in front of the object slits, is controlled by the hit detection system. When a hit is detected, the microbeam is switched off and the probe moves to the new coordinates.

The irradiation is performed under vacuum, and an optical microscope situated in the chamber allows a precise definition of the area to be scanned with the ion beam.

B. Experimental Setup

Second- and third-generation VD-MOSFETs, available in bare die, from the manufacturer Cree/Wolfspeed were used as devices under test (DUTs). Bare die were chosen in order to avoid the laborious decapsulation process and directly expose the chip surface to the beam to allow sufficient penetration of the heavy ions through the sensitive active layers of the device, without being stopped in the package materials [22]. The references and the technical information of the tested devices are listed in Table I.

TABLE I
List of DUTs

Reference	Gen.	$R_{DS(on)}$ [mΩ]	V_{DS} [V]	$I_{D\ @\ 25}$ [A]	#DUTs
CPM2-1200-0025B	II	25	1200	98	3
CPM2-1200-0080B	II	80	1200	36	7
CPM3-0900-0065B	III	65	900	36	6

TABLE II
Characteristics of the Ion Species

Ion	LET [MeVcm^2/mg]	Range [μm]	Window size [X x Y μm^2]	ΔX [μm]	ΔY [μm]
Au	94	35.4	55x50	1.1	1.56
Ca	17	29.7	30x25	0.93	1.56

Three die individually biased via BNC connectors for gate and drain were mounted on a custom FR-4 carrier board with gold [electroless nickel immersion gold (ENIG)] surface using standard SAC 305 solder paste. The gate and source were connected by aluminum wire bonds with 300-μm diameter and only a single wire was used to reduce the shadowing effect [22]. The drain connection was made onto the carrier board by the large soldered bottom pad. No capacitors or resistors were installed between the contacts. Keithley source measure units (SMUs), models 2636 (two channels, up to 200 V) and 2410 (one channel, up to 1100 V), were used during the irradiation to bias gate and drain, respectively, and to monitor the leakage currents. The cumulative count of heavy ions hitting the device was recorded during the irradiation using a simple digital counter based on an Arduino Leonardo microcontroller board.

C. Heavy-Ion Microbeam Irradiation

Au and Ca ions with an energy of 4.8 MeV/amu and linear energy transfer (LET) values of, respectively, 94 and 17 MeV cm^2/mg were used in the experiments. Each DUT was irradiated several times scanning the beam spot in different pristine regions of the die until the drain leakage current reached a level of several hundred microamperes. Multiple DUTs were tested during the test campaigns. In the case of Au, a scanning area with a size of $55 \times 50\ \mu\mathrm{m}^2$ was selected for each irradiation and a total of 1600 ions in each scan was used. For the Ca beam, 520 ions were used with a scanning area of $30 \times 25\ \mu\mathrm{m}^2$. The average distance between the steps in each, X and Y, direction, for both configurations, was on the order of $\sim 1\ \mu$m (see Table II for details). During the irradiation, the gate voltage V_{GS} was set to 0 V to hold the device in OFF-state, while the drain voltage V_{DS} was set to a constant positive value. Different values for the drain bias were used.

III. Experimental Results

A. Exposure of Different Areas of the 80-mΩ DUT

In this work, the presented results are for the 80-mΩ die from the second-generation Cree/Wolfspeed, but similar

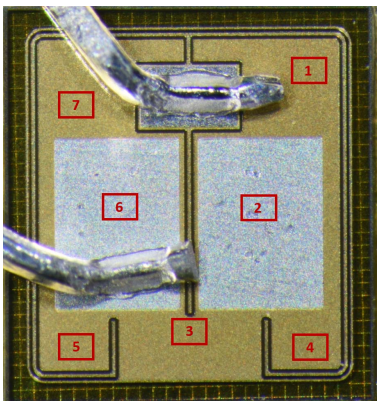

Fig. 1. Regions of the 80-mΩ die irradiated with Au beam (not to scale).

TABLE III
CURRENT DEGRADATION IN DIFFERENT REGIONS

Region *	ΔI_D / ΔI_G (nA) 1st method	ΔI_D / ΔI_G (nA) 2st method
1	237 / 226	192 / 191
2	221 / 215	396 / 396
3	140 / 122	419 / 418
4	178 / 168	344 / 341
5	157 / 166	311 / 313
6	262 / 239	361 / 362
7	366 / 356	555 / 555

* 80 mΩ die exposed to Au-beam at $V_{DS\,irr} = 210\,V$

considerations are valid also for the 25- and 65-mΩ DUTs. For an exemplary 80-mΩ DUT, the irradiated regions are indicated in Fig. 1 (not to scale). During Au irradiation, gradual permanent degradation (SELC) in the device was observed at $V_{\mathrm{DS\ irr}} > 150$ V (∼12.5% of the rated voltage). At drain biases below 350 V (∼30% of the rated voltage), the magnitude and degradation rate of the leakage currents, for both drain and gate, were equal. Similarly, it was observed for the 25-mΩ devices, while for the 65-mΩ devices from the third generation, equal gate and drain current were observed at $V_{\mathrm{DS\ irr}} < 320$ V (∼35% rated voltage).

Two examples for an 80-mΩ die exposed to Au beam in regions 1 and 4 at $V_{\mathrm{DS\ irr}} = 210$ V are shown in Fig. 2. The corresponding positions of the scanning areas are visible on the micrographs in Fig. 2(a) and (d). The leakage current evolution during the irradiations is shown in Fig. 2(b) and (e). The heavy-ion-induced steps were analyzed from the leakage current evolution by using a threshold step height of 2.5 nA to filter the background noise and are reported in Fig. 2(c) and (f).

The total degradation induced by the ion exposures in regions 1–7 at $V_{\mathrm{DS\ irr}} = 210$ V was calculated using two different methods and is listed in Table III. In the first method, the total radiation-induced degradation was calculated by summing all the leakage current steps higher than 2.5 nA. In the second method, instead, the induced degradation was calculated from the $I_D - V_D$ and $I_G - V_D$ measurements performed before and after each run (at $V_{\mathrm{GS}} = 0$ V), considering the leakage current increase at $V_{\mathrm{DS\ irr}} = 210$ V. The sequence of exposures is the same as reported in the table. Generally, the second method gives higher results since additional leakage current increase was caused by the stress induced during the post-irradiation IV measurements. The activation of latent damage in the gate-oxide due to the post-irradiation electrical stress was previously discussed in [23]. Overall, the response is in the order of a few hundreds of nanoamperes and it is consistent between the different areas of the die (as expected). However, some differences are still visible. It has to be considered that not all the ions hitting the device during the scanning within the same window frame cause a permanent increase in leakage current. Also, a pristine area was selected for each irradiation, and the position of the window to be irradiated was not exactly the same with respect to the device structure between different runs (i.e., number of stripes covered by the window). The combination of these effects could be a reason for the different responses observed. Also, the SMU range was automatically selected during the measurements, leading to different measurement sensitivity during the runs due to the elevated baseline for the leakage current caused by the degradation induced by the radiation.

B. Sensitive Areas for Gate and Drain SELC

In order to define the sensitive regions for gate and drain SELC and its dependence on the drain–source bias during the exposure, some runs were analyzed in more detail. The results are reported for an 80-mΩ DUT exposed to Au particles in region 2 at four different $V_{\mathrm{DS\ irr}}$ conditions. The runs were performed consecutively with the same DUT and the results are shown in Fig. 3 for $V_{\mathrm{DS\ irr}} = 210$ V and $V_{\mathrm{DS\ irr}} = 300$ V and in Fig. 4 for $V_{\mathrm{DS\ irr}} = 350$ V and $V_{\mathrm{DS\ irr}} = 400$ V. An optical microscope was used to select the scanning area to be irradiated and the exact positions are shown in the first panel from the top. A pristine area was selected for each new run. During the exposure, I_D and I_G were monitored and the leakage current step evolutions calculated using a threshold of 2.5 nA. The data are presented in the second row of graphs. For the runs at 350 and 400 V, separate axes are used for I_D and I_G, due to the higher degradation rate for the drain current. Also, in the irradiation at 350 V, only a total of 1200 ions were used in the scan, due to a problem with the beam scanner during the exposure. Unfortunately, this was noticed only afterward and the run was not repeated. For the irradiations performed at $V_{\mathrm{DS\ irr}} < 350$ V, as discussed in [9] and as mentioned earlier, the leakage current path is from the drain to the gate, that is, $\Delta I_D \approx \Delta I_G$. For $V_{\mathrm{DS\ irr}} > 350$ V, instead, the leakage paths are divided between the drain–gate and drain–source path. For both the gate and the drain, the current steps induced by the heavy ions were analyzed as a function of the scanner position within the scanning area used in the run. The amplitude of each radiation-induced step was calculated using a threshold value of 2.5 nA for I_D and I_G. If the step was lower than the threshold, it was set to 0 A to filter the noise. Moreover, the SMUs were usually logging data at a slower rate than the ion strikes arrived (especially for low leakage values);

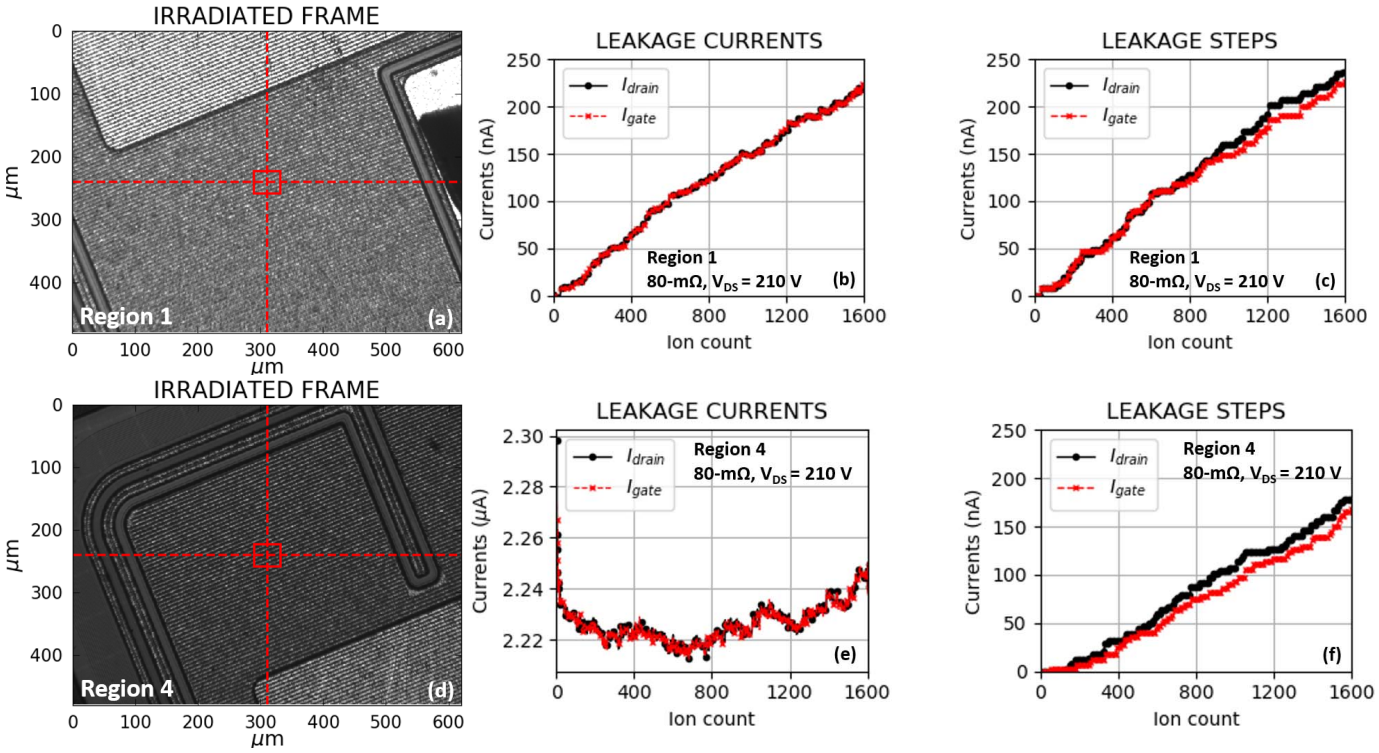

Fig. 2. Au irradiation in regions 1 and 4 of an 80-mΩ at $V_{\mathrm{DS\ irr}} = 210$ V. The exact location of the irradiation is identified by the window frame on the microscope images, respectively, in (a) and (d). The drain and gate leakage current increases are shown in (b) and (e) (for a pristine device, the leakage currents are on the order of 10 pA), while in (c) and (f) is the cumulative sum of the radiation-induced leakage steps.

therefore, for some ion counts, no current data is available. In the analysis, the delta currents are set to 0 A for these ion strike locations. Successively, the data for the scanner position logged as computer-aided measurement and control (CAMAC) standard were converted into the ASCII format and, then, into x–y coordinates (using micrometer units) inside the irradiated frame. Finally, each leakage step was associated with the corresponding scanner position and the heat maps were generated for the gate and drain degradation for each run, as presented in the third and fourth row graphs of Figs. 3 and 4. Additionally, the gate stripes within a distance of 9.1 μm are indicated with dotted lines to guide the eye, based on the technological information available for the device. For each run, the stripes were aligned with the degradation observed in the gate heat map, assuming the sensitive region for the gate leakage current being in the oxide of the gate-stack. The striped structure of the die is clearly visible in the heat map and comparable with the one in the microscope image. Indeed, the periodicity in the lateral response observed in the leakage current degradation analysis reflects the periodicity of the striped structure. This result confirms that the entire MOSFET cell is not uniformly sensitive to SELC, but the response strongly depends on the ion strike location. In general, the sensitive region enlarges with increasing $V_{\mathrm{DS\ irr}}$. In particular, for the irradiations at $V_{\mathrm{DS\ irr}} < 350$ V (Fig. 3), the sensitive regions are aligned with the gate stripes in the neck area (JFET region) for both gate and drain heat maps. However, at $V_{\mathrm{DS\ irr}} > 350$ V (Fig. 4), the sensitive areas for gate degradation are still aligned with the same regions, but those for the drain leakage degradation are now between the gate stripes, i.e., in the p-implanted body-diode region of the VD-MOSFET. This result supports the hypothesis that at increasing drain–source bias during the exposure and approaching the SEB threshold (∼500 V), the body-diode area is contributing to the current amplification process.

C. Cumulative Distribution Function for Gate and Drain SELC

The cross sections for SELC probabilities in different biasing conditions can be represented using complementary cumulative distribution functions (CCDFs) for the measured gate and drain steps. The CCDFs for the four $V_{\mathrm{DS\ irr}}$ conditions discussed earlier are shown in Fig. 5. Each bin represents the probability of the heavy-ion-induced step with a height above a given x-axis value. The distribution was normalized with the total number of ions in the run and the bin width. The probability to measure higher degradation steps increases with increasing drain–source bias during the exposure, as expected. Indeed, at $V_{\mathrm{DS\ irr}} = 400$ V, the maximum step height for drain and gate currents was $\Delta I_D = 1.5 \times 10^{-6}$ A and $\Delta I_G = 2.9 \times 10^{-8}$ A, respectively. The size of the exposure window and the estimated transistor's neck region (within this window) are illustrated in the graphs. For the gate leakage, the probability saturates to values close to the neck area (or JFET region). Probably, the most sensitive areas for gate degradation are those close to the channel, but the resolution is not high enough to explicitly see that ($\Delta X = 1.1$ μm).

D. Test Methodology

During the experiments, an initial overshoot and subsequent leveling in the leakage current were observed once the DUT

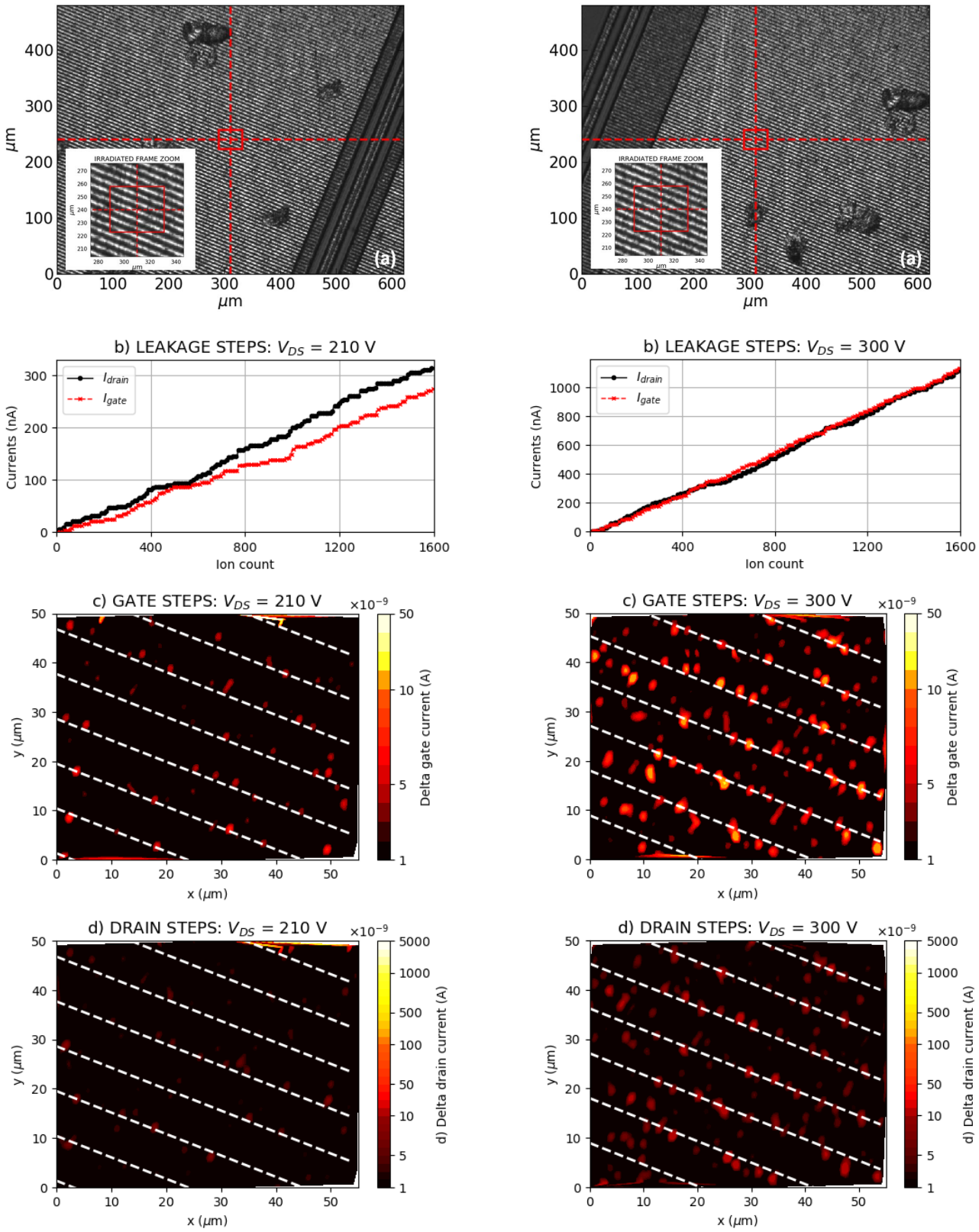

Fig. 3. All the runs refer to region 2 of an 80-mΩ DUT. (Left) $V_{\mathrm{DS\ irr}}$ = 210 V. (Right) $V_{\mathrm{DS\ irr}}$ = 300 V. From the top—(a) Frame selected for the irradiation in region 2 is visible on top of the microscope image; (b) drain and gate leakage current evolution during the irradiation; (c) and (d) the gate and the drain current steps are, respectively, represented as a function of the scanner position. The gate stripes were plotted within a distance of 9.1 μm, based on the technological information in (c) and (d) and they are comparable with the stripes in the zoom visible in (a).

had been degraded to a certain level. In the run shown in Fig. 2(b), the device exposed to the beam was pristine, while in the run shown in Fig. 2(e), the part was already damaged. In the latter case, the leakage current was on the order

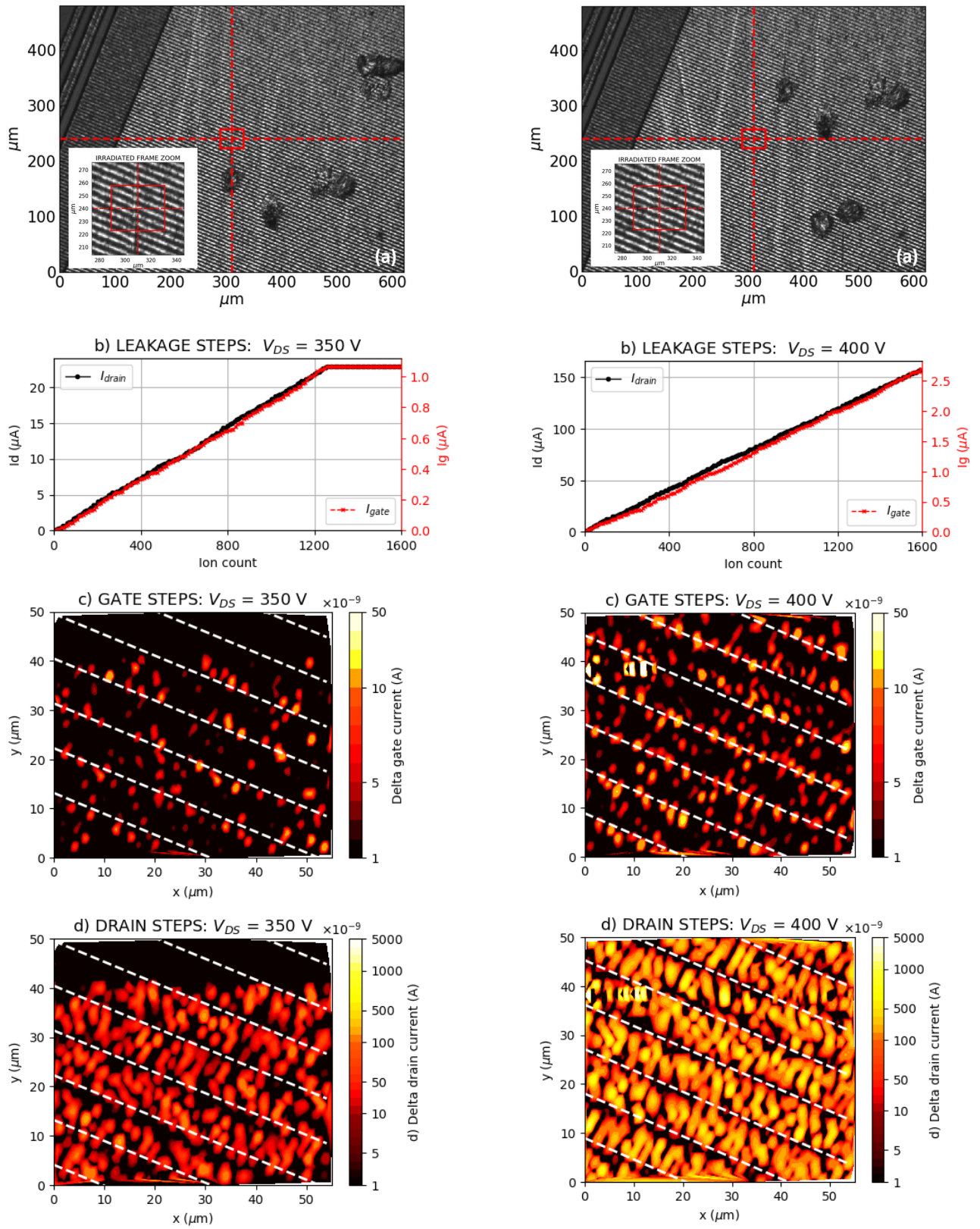

Fig. 4. All the runs refer to region 2 of an 80-mΩ DUT. (Left) $V_{\mathrm{DS\ irr}}$ = 350 V. (Right) $V_{\mathrm{DS\ irr}}$ = 400 V. From the top—(a) Frame selected for the irradiation in region 2 is visible on top of the microscope image; (b) drain and gate leakage current evolutions during the irradiation; (c) and (d) the gate and the drain current steps are, respectively, represented as a function of the scanner position. The gate stripes were plotted within a distance of 9.1 μm, based on the technological information in (c) and (d) and they are comparable with the stripes in the zoom visible in (a).

of microamperes. Comparing the current evolutions, for the degraded part [Fig. 2(e)], higher current values are measured promptly after the V_{DS} bias was applied, followed by an immediate decrease in the current over the increase of the ion

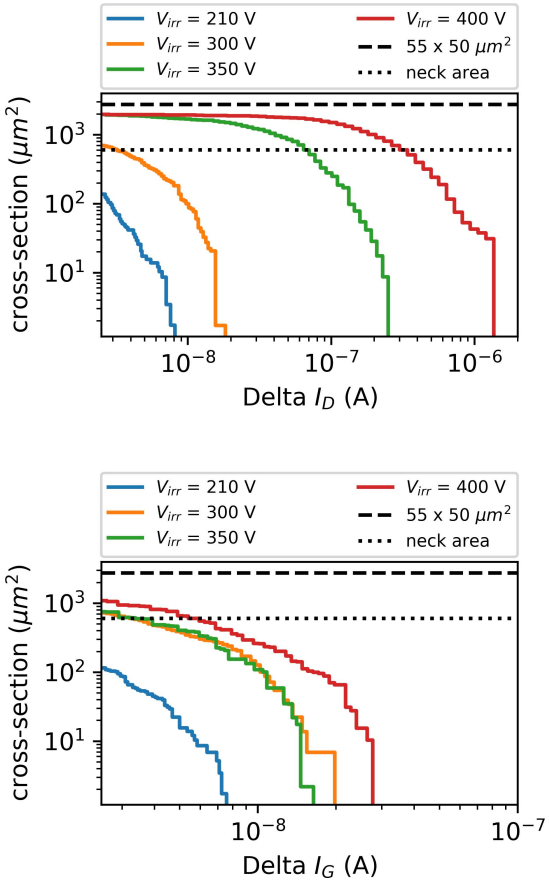

Fig. 5. CCDF for the measured cross section of the gate and drain SELC at different drain–source bias during the irradiation. For reference, the size of the exposure window and the estimated transistor's neck area (or the JFET region) are illustrated in the graphs.

count. During the experiments, the irradiation started before the system reached the steady-state condition, so the increase in the ion-induced leakage current was partially masked by this effect of overshoot and its leveling. In order to get rid of this effect in the analysis, the total degradation was then calculated summing all the leakage current steps over 2.5 nA, instead of considering the delta between the final and the initial value of the current. However, this effect has been identified as part of a testing methodology for future work. Unfortunately, due to the limited number of tested devices still operable, it was not possible to obtain detailed conclusions, and further investigation is needed to better understand the origin of this behavior. However, we suggest a possible explanation due to a thermal effect in the ion-induced damage area within the device. In a degraded DUT, the current can be considered to flow through very small damage sites (i.e., 10–100 nm size) causing very high current densities at localized leaky points. Once the bias is set, the temperature in these local spots increases very rapidly due to the high current density. If the conductivity of the leaky region is inversely proportional to temperature similarly to metals, then it could explain the observed behavior in the leakage current promptly after applying the bias voltage. Additional studies are needed to validate this hypothesis.

Finally, since the work was performed in the context of the basic mechanism research, it was decided to avoid installing

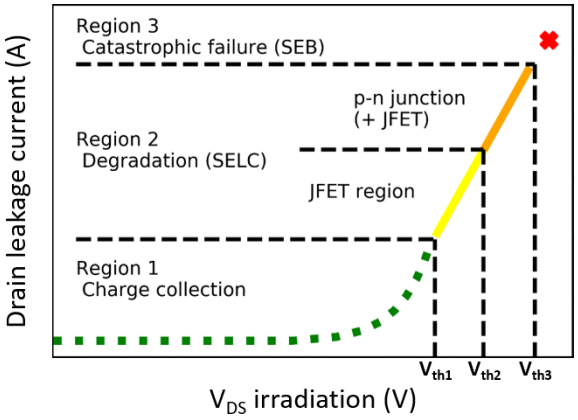

Fig. 6. Three characteristic regions of damage for SiC power MOSFETs as a function of the drain–source bias during the heavy-ion irradiation. Two subregions are identified for degradation (region 2). First, between V_{th1} and V_{th2}, the area underneath the gate (JFET or neck region) is the most sensitive for SELC. The second mechanism is newly added at biases higher than V_{th2}, when higher SELC is measured in the p-n junction area, but a smaller leakage remains also through the gate-oxide.

any additional capacitances to limit the external influences on the observed results. Therefore, the setup used was different from the one recommended by the military standard (MIL-STD-750 M1080).

IV. Discussion on SELC Mechanism

The microbeam results confirm that two different mechanisms are governing the SELC, involving different areas of the MOSFET structure. One mechanism is attributed to oxide damage (above the JFET or neck region) that results in the leakage path between the drain and the gate. The other degradation mechanism is triggered when the bias applied during the exposure is sufficiently high to reach certain electrical conditions within the p-n junction. These different areas for ion-induced drain leakage response are illustrated in Fig. 6, where the three regions discussed in [9] are updated with the new considerations. At low bias voltages, the ion-induced charge is collected with a similar multiplication mechanism as in Si MOSFETs and no permanent damage is observed in the device. At higher bias, two subregions are identified for degradation. First, between V_{th1} and V_{th2}, the area underneath the gate (the JFET area) is the most sensitive for SELC. More precisely, the channel area should also be included in this consideration. The second mechanism is observed at biases higher than V_{th2}, when higher SELC is measured in the p-n junction region, but a smaller leakage remains also through the gate-oxide. In the third region, at sufficiently high bias above V_{th3}, a catastrophic single-event burnout failure occurs.

Concerning the first mechanism of degradation, similarities are found with Si power MOSFETs soft oxide breakdown which was previously discussed in [23] and [24]. The increase in the leakage current was explained through the Quantum Point Contact (QPC) model. According to this theory, conductive paths are generated in the oxide which behave as point contacts between the gate and the substrate [25]. Similarities are found also with the precursor ion damage mechanism in Si MOS structures with thin oxides as described in [26]. This

mechanism was described as an unrelated effect with respect to single-event gate rupture (SEGR).

For the second SELC mechanism via p-n junction, a common explanation for SiC power MOSFETs and junction barrier Schottky (JBS) diodes is proposed. Experimental data previously presented in [10] suggested that a common mechanism is responsible for leakage current degradation in SiC power MOSFETs and JBS diodes when exposed to heavy ions. Technology computer-aided design (TCAD) simulations of the two structures were also discussed in [10]. Ion-induced highly localized energy pulses were demonstrated and are proposed as a common mechanism for SELC degradation in SiC power MOSFETs and JBS diodes. However, no TCAD simulations were reported yet concerning the difference observed experimentally for heavy-ion irradiations at $V_{\mathrm{DS\ irr}} < 350$ V and $V_{\mathrm{DS\ irr}} > 350$ V. Moreover, in [27], molecular dynamics (MD) simulations of heavy-ion-induced defects for SiC Schottky diodes have been performed. The structure of the ion track was obtained after the first 100 ps when the energy has already dissipated into the bulk and the atoms in the core of the track have cooled down. The results suggest that the combination of the ionization of the impinging ion and the applied bias can result in prompt Joule heating that leads into amorphous regions within the material. Indeed, the energy deposited via Joule heating is sufficient to cause a phase transition in the material, which is unlikely to recrystallize back completely, leaving permanent structural modification in SiC lattice, as suggested in [28].

It is hypothesized that the common mechanism described in [10] for SELC in JBS diodes and SiC power MOSFETs only involves the SELC through the p-n junction, and therefore observed for voltage bias higher than V_{th2} ($V_{\mathrm{DS\ irr}} > 350$ V for the studied DUTs). The SELC via p-n junction originates from the thermal stress induced by the highly located power dissipation. The thermal transient and excessive lattice temperature probably cause the formation of permanent EDs, which remain after the switch off of the irradiated device, for example, MD simulations showed that the amorphous region along the ion track appears starting from certain values of applied V_{DS}[27]. However, MD simulations now give rather qualitative results and there were no experimental studies yet to investigate the sites of heavy-ion impact. For this reason, the material modifications induced by the heavy-ion strike in biased SiC power devices are still a matter of discussion. Those EDs can be amorphous pockets, different dislocations, stacking faults, different SiC solid-phase (polytype) inclusions, clusters, and so on. More could be stated about the ED nature investigating the irradiated structure by electron microscopy and optical methods [29]–[31]. However, it should be clearly stated that the experiments were performed using a specific device type from one manufacturer; as both design as well as the resulting efficient carrier concentration in the specific areas will vary between device types and manufacturers, the results cannot be transferred to all SiC power devices without further analysis.

Finally, the role of the p-n junction degradation under SEB conditions needs to be further investigated taking into account also other types of devices from different manufacturers.

V. Conclusion

A unique SEE signature named SELC is observed in SiC power devices under heavy-ion irradiation. Microprobe experiments were performed at GSI, Darmstadt, Germany, with Au and Ca ion beams in order to study the SELC mechanism. Second- and third-generation commercial SiC VD-MOSFETs from the manufacturer Cree/Wolfspeed were used as DUTs.

Different regions of the die were exposed to heavy ions, and detailed analyses were done for the second-generation 80-mΩ devices. The response to heavy ions was observed to be homogenous over the scanned areas around the die (as shown in Fig. 1).

The ion-induced steps in the gate and drain leakage current were plotted as a function of the x–y coordinate within the frame scanned by the microprobe. A comparison was made for irradiations with Au at different drain–source bias during the exposure. The striped structure of the die is clearly visible in the gate and drain SELC heat maps. Two mechanisms involving different areas of the MOSFET structure were observed for the heavy-ion-induced degradation. First, at lower bias, the area underneath the gate (the JFET or neck region) is the most sensitive for SELC. The second mechanism gets activated at higher biases, and stronger SELC response is observed in the p-n junction region (smaller leakage contribution remains through the gate-oxide).

For the first mechanism, similarities are found with the Si power MOSFETs soft oxide breakdown, previously explained with the QPC model. Concerning the second mechanism of degradation, it is discussed that at sufficiently high bias, the highly localized power dissipation caused by the heavy-ion strike generates a thermal transient and excessive lattice temperature. The thermal stress causes the formation of permanent EDs which degrade the p-n junction. For example, MD simulations showed that the amorphous region along the ion track appears above certain values of applied V_{DS}. However, the material modifications induced by the heavy-ion strike in biased SiC power devices are still a matter of discussion and the nature of the EDs should be further investigated.

Finally, it is hypothesized that SELC is the manifestation of the same mechanism in JBS diodes and SiC power MOSFETs only when it involves the SELC through the p-n junction of the MOSFET, and therefore, for voltage bias higher than a certain threshold ($V_{\mathrm{DS\ irr}} > 350$ V for the studied DUTs).

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