Experimental Investigation of the Joint Influence of Reduced Supply Voltage and Charge Sharing on Single-Event Transient Waveforms in 65-nm Triple-Well CMOS

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***Abstract*— Full waveforms of single-event transients (SETs) in inverter chains were measured under focused heavy-ion microbeam irradiation. Inverter chains of varying spacings were irradiated with ^{48}Ca and ^{197}Au ions. The influence of changing the supply voltage from subthreshold to nominal level on SET forming and propagation was investigated, and the role of charge sharing is discussed. Key factors that influence SET widths and cross sections are identified across the applied range of supply voltages. A simple method is presented for estimating average SET widths at decreased supply voltages, and is based on the SET width measurements at nominal supply voltage, transistor-level simulations, and extracted circuit parameters. The proposed method matches well with the measured data.**

***Index Terms*— Analog on-chip measurement, charge sharing, CMOS, heavy ions, single-event effects (SEEs), single-event transients (SETs), supply voltage.**

I. Introduction

As TECHNOLOGY progress pushes the scaling of integrated circuits further, the increased transistor density along with smaller operating voltages has led to increased susceptibility to single-event effects (SEEs). An energetic particle passing through silicon close to a circuit node can induce a single-event transient (SET), which can propagate to a memory element, and create a single-event upset (SEU).

Since high transistor density and low supply voltage are very desirable for cost and energy efficient designs, it is important to understand how these properties affect the SEE sensitivity of circuits. Bringing sensitive nodes closer together has been shown to increase SEU rate in conventional radiation-hardened circuits, such as dual-interlocked cell (DICE) flip-flop, due to a charge sharing effect [1], [2]. Decreasing the supply voltage has also been reported to negatively affect the radiation hardness of a circuit [3]–[5]. Even small fluctuations below the nominal supply voltage were shown to cause considerable increase in the SET pulse widths, and consequently in the SEU rate [6].

However, intentionally enhancing the charge sharing effect can also be utilized to reduce the SET sensitivity. If multiple collecting nodes are made to react in the opposing manner, the individual node contributions can cancel each other out, as proposed and demonstrated in [7]–[10]. It has been shown in simulations that charge sharing can also be observed under low-voltage operation [11]. Even though struck nodes show increase in produced SET pulse widths when the supply voltage is decreased, Qin *et al.* [12] suggest that pulse widths of propagated SETs may actually decrease, thanks to the charge sharing effect.

II. Related Work

SEEs have been studied in deep sub-micrometer nodes, either in simulations or by subjecting fabricated circuits to ionizing particles in experiments. Most of these experiments utilized pulsewidth measurement techniques [13], [14] to obtain the SET cross sections and pulsewidth distributions of digital SETs in chains of inverters [3], [6], [7], [15]. These approaches are proven well and provide valuable insights into the characteristics of resulting SETs. However, the investigation of SETs directly at the origin of the pulse, as well as the details of analog SET shapes, is important for distinguishing different underlying collection and propagation phenomena. In this paper, such investigations have been predominantly carried out using simulations [6], [7], [10]–[12], [16], [17].

In [18] and [19], we have presented a different approach to SET measurements, where full analog waveforms of pulses are being captured. For each ion hit, we can capture an SET waveform directly at the struck node, after propagation through subsequent inverters, and the resulting SET at the output of the targeted inverter chain.

In this paper, we utilize our SET measurement solution to directly observe influences of varying supply voltage (VDD) and circuit spacing to SET properties. As the supply voltage is decreased, observed SET widths span several orders

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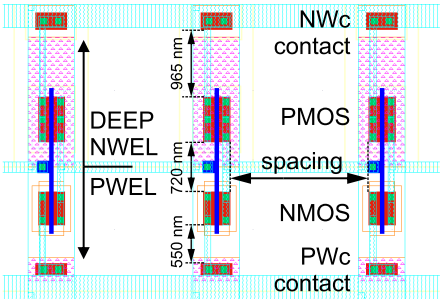

Fig. 1. Layout of inverter cell used in targets.

TABLE I
INVERTER DIMENSIONS AND SPACING IN TARGET CIRCUITS

	nMOS	pMOS	PWc	NWc
***W* [nm]**	480	650	170	240
***L* [nm]**	60	60	450	450
DUT	**DUT1**	**DUT2**	**DUT3**	**DUT4**
Spacing [μm]	0.12	0.25	2	4
Monitored outputs	OUT1 - OUT3	OUT1 - OUT4	OUT1 - OUT4	OUT1 - OUT4

of magnitude, making it difficult to perform measurements across the whole range of supply voltages with a single circuit [5], [13], [14]. As our approach allows measuring SET widths ranging many orders of magnitude, we are able to investigate SETs from subthreshold to nominal supply voltage.

III. TEST CHIP AND EXPERIMENTAL SETUP

The target inverter chains have been designed and placed on the test chip, and fabricated in UMC 65-nm CMOS low-leakage low-k technology. The test nodes are connected to the on-chip analog multiplexers used for SET sensing [20]. The layout of one section in the test inverter chain circuit is given in Fig. 1, and the relevant device dimensions are given in Table I. All target circuits have been placed in a common deep n-well/triple-well area. The analog multiplexer circuits present a small capacitive load of $C_{\text{in}} = 4$ fF to the test nodes, with an additional parasitic capacitance from the interconnect lines $C_{\text{interc}} = 4 - 13$ fF, as calculated by the extraction tool. The multiplexer signal path features a large dc-to-8.5-GHz bandwidth, and total harmonic distortion below 2% for a 1-$V_{p\text{-}p}$ input signal, thus preserving the analog shape of observed SETs. The output of each multiplexer is on-chip 50 Ω terminated, in order to suppress signal reflections in the cables providing connection to the input of a high-speed oscilloscope.

Data presented here were collected during two experiment sessions at the microbeam facility in GSI, Darmstadt, Germany. Two chip samples were irradiated with a focused heavy-ion beam with an energy of 4.8 MeV per atomic mass unit—one sample was scanned with ^{48}Ca ions [linear energy transfer (LET) = 17 MeV·cm^2/mg], and the other with ^{197}Au ions (LET = 95 MeV · cm^2/mg). The beam control and data collection system is described in [18] and [19]. The exposed chip was bonded onto the RF circuit board, placed inside the vacuum chamber, and connected to the outside instruments via the feedthroughs. The acquisition of waveforms was done by two high-speed real-time oscilloscopes. The test chip position could be tuned using an *xyzφ* stage, while the beam spot position could be finely controlled using magnetic deflectors. The beam was focused into a ∼500-nm diameter spot in the target plane using microslits and a magnetic lens. The ion beam was steered across the target areas, with steps in the range of 200–450 nm for the Ca experiment and 450–970 nm for the Au experiment. Inverter chain targets were scanned at various supply voltages, which are given in Table II.

TABLE II
USED SUPPLY VOLTAGES IN EXPERIMENTS

Experiment	Supply voltage [V]				
^{48}Ca	-	0.4	0.6	0.8	1
^{197}Au	0.3	0.4	0.6	-	1

IV. RESULTS

Our measurement setup enables us to simultaneously capture the response of multiple nodes for every ion hit, as well as to track the ion-hit location. This allows us to replicate a scenario similar to that used in previously reported 3-D simulations [7], [11], [12], [16], where both responses of a node that is hit (active node) and the subsequent node in the inverter chain (passive node) are being observed. We will refer to SETs from these nodes as "direct-hit" and "indirect" SETs, respectively. It should be noted that contrary to these previous works, inverters in our test circuits are more sensitive to ion hits when their output is in logic state "1," i.e., when the corresponding nMOS device is turned OFF. This is the consequence of all nMOS transistors in our test circuits being placed in a p-well of the triple-well [21], while all pMOS transistors reside in a deep n-well area.

In each of our targets circuits, with the exception of DUT1, we have the access to two active–passive node pairs—we can either take OUT2 node as active and OUT3 as passive or OUT3 as active and OUT4 as passive. Note that OUT1–OUT2 nodes also represent an active–passive node pair, but since the first inverter in the target chain is driven externally, it is expected to exhibit somewhat different behaviors. On the other hand, OUT2–OUT3 and OUT3–OUT4 pairs are being driven by a preceding inverter, and are expected to behave consistently. Unless noted otherwise, collected SET data from these two pairs are combined and presented as such.

For each SET detected at a particular observed node, we can determine if it is a direct-hit or indirect type, by looking if an SET larger than VDD/2 is also present on the preceding node for the same ion-hit event. If such SET did not occur on the preceding node, then the observed SET occurred first along the inverter chain and is thus a direct-hit type. Otherwise, we can assume that an SET from the preceding node is able to propagate to the observed node. In the case of circuits

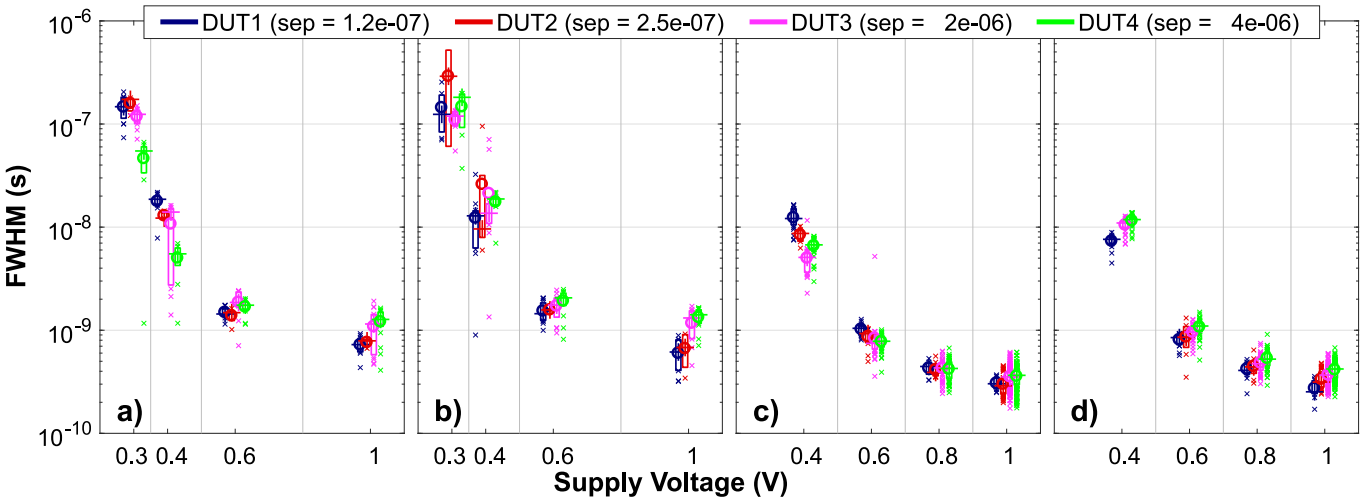

Fig. 2. Measured FWHM distributions of direct-hit SETs. Monitored node is in logic state "1." (a) Au experiment, OUT2. (b) Au experiment, OUT3. (c) Ca experiment, OUT2. (d) Ca experiment, OUT3. "o" symbol represents the average, "+" symbol is the median, the box gives the interquartile range, and the points outside the box, marked with "x" symbol, represent width values of individual SETs that fall outside the interquartile range.

DUT3 and DUT4, this distinguishing method can also be verified by looking at the location of the ion-hit event. In the cases of DUT1 and DUT2, the sensitive regions of neighboring inverters overlap significantly, and the ion-hit location usually cannot be used for this purpose reliably.

In Fig. 2, we present box plots of measured full-width at half-maximum (FWHM) distributions for direct-hit SETs at nodes OUT2 and OUT3, for logic state "1" at these nodes. Only SETs higher than VDD/2 are taken into account. The smallest pulse widths, around 175 ps, are recorded in the Ca experiment at VDD = 1 V, whereas the largest widths reach 520 ns in the Au experiment at VDD = 0.3 V, which represents a span of nearly 3.5 orders of magnitude. At supply voltages above 0.6 V, a steady increase of pulse widths with decreasing VDD is observed, and pulsewidth distributions of OUT2 and OUT3 nodes do not differ substantially. At lower VDD values, where transistors are operating in the near-threshold or subthreshold regions, a more drastic increase of pulse widths can be seen.

As it can be concluded from typical SET waveforms across different VDD values shown in Fig. 3, the pulsewidth of a typical SET is determined by three components: 1) a fast leading edge, which is independent of the circuit speed; 2) a plateau, which depends on the strike location, ion energy, and LET; and 3) a trailing edge, which gets slower with decreasing VDD [4], [6]. The relative contributions of each of the three mentioned components change with the supply voltage. A plateau is dominant at the highest supply voltage of 1 V where the discharging transistors can quickly remove the collected charge, and the SET essentially lasts until the well potential is restored. As VDD decreases, the trailing edge becomes slower, since the discharge current of the device is decreased in relation to VDD. This relation is linear for the simple *RC* transistor model [6] which works well for the triode regime. However, as the supply is further reduced, the discharge transistor operates more and more in the saturation region compared to triode, and the I_d–VDD relation becomes

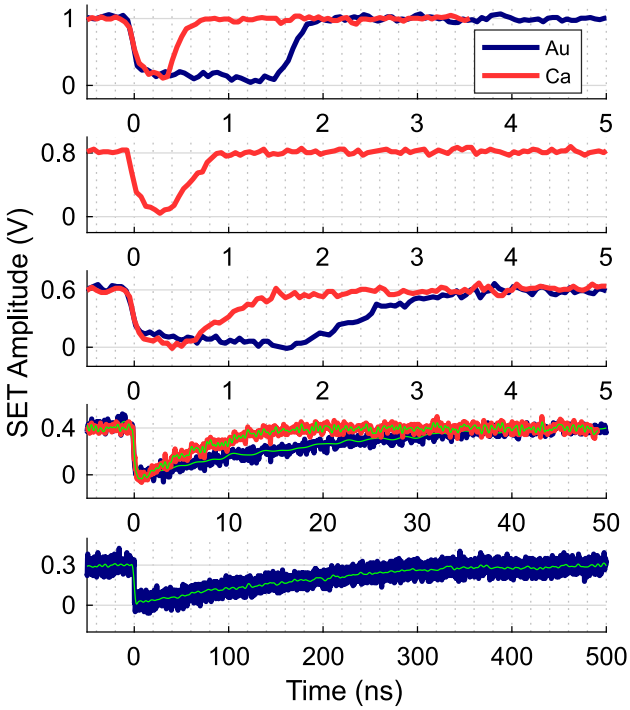

Fig. 3. Captured waveforms of typical SETs for both Au and Ca experiments, and at all used supply voltages. The thin line in the bottom two plots represents the signal after the noise filtering.

quadratic, thus increasing the rate at which the trailing SET edge slows down with decreasing VDD. The plateau, on the other hand, is either not affected by the VDD decrease or is even reduced as the bipolar amplification effect weakens [12]. As noted in [4], once the supply voltage approaches the transistor's threshold value, the discharging current is defined by subthreshold conduction, having exponential dependence on V_{GS} = VDD, thus the duration of the trailing SET edge drastically increases. At this point, the relative contribution of

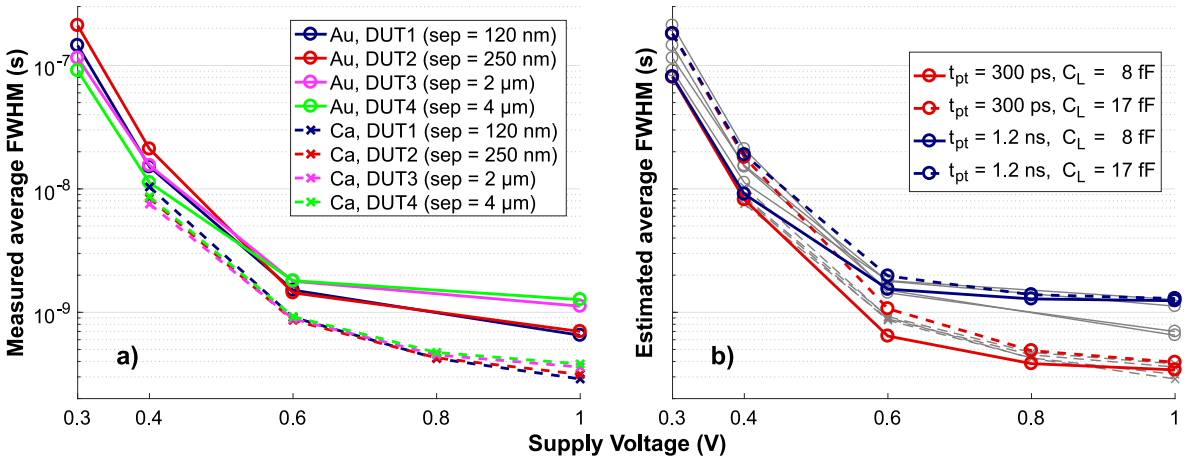

Fig. 4. Average SET pulse widths for active node in logic state "1." (a) Measured values. (b) Values calculated from (1).

plateau component to the overall SET width is very small, and the SET width is almost completely defined by the duration of the trailing edge.

In Fig. 4(a), the average pulse widths for each target are displayed as a function of the supply voltage for direct-hit SETs, when the active node is in the more sensitive state "1." As the supply voltage decreases, the average pulsewidth increases in both Au and Ca experiments, in agreement with results reported in [3]–[6], [11], [12], and [17]. At 1-V supply voltage, the distinction between SETs from Ca and Au experiments is clearly seen. The ^{197}Au ions deposit more charge in the well, which enhances the bipolar amplification, and it takes more time to restore the well potential. This results in a longer plateau and larger pulse widths than those for ^{48}Ca ions. As VDD is decreased, the pulsewidth is more and more determined by the trailing SET edge, while the difference due to plateau decreases. As a result, the difference due to different LETs between Au and Ca experiments in Fig. 4(a) is getting less pronounced at lower voltages, which was also seen in simulations reported in [17], as well as in measurements in [5].

The difference in SET widths between the target circuits is also apparent at VDD = 1 V. Targets with dense inverter spacing (DUT1 and DUT2) show ∼40% smaller average pulsewidth in the Au experiment than targets with large spacing (DUT3 and DUT4). We observed the same behavior in [19], in which we presented data from separate experiment sessions performed on dedicated chip samples. The effect is less pronounced in the Ca experiment, with 24% smaller average pulsewidth for DUT1 compared to DUT4. The differences between target circuits also diminish with reducing VDD, suggesting that denser inverter spacing helps to reduce the plateau duration in direct-hit SETs by stabilizing the well potential.

In the subthreshold regime, the direct-hit SET width is determined completely by the trailing edge decay rate, while the plateau duration is the major contributor at 1-V VDD. In between, the discharge current of the ON-state transistor changes with the supply voltage according to the equations for triode, saturation, and subthreshold modes of operation. Although analytical expressions for drain current in these modes provide good insight into trends that can be expected, more precise predictions can be made using transistor models available in the design kit. We can simulate transistor currents I_{D1} and I_{D2} for V_{DS1} = VDD and V_{DS2} = VDD/2, while keeping V_{GS} = VDD. If we then approximate that the average discharge current of the ON transistor $I_{D,avg}$, as the drain node capacitance C_L is discharged from VDD to VDD/2, is equal to the average of I_{D1} and I_{D2} currents, we can estimate the pulsewidth as

$$t_{pw} = t_{pt} + \frac{C_L}{I_{D,avg}} \frac{VDD}{2} = t_{pt} + C_L \frac{VDD}{I_{D2} + I_{D1}} \quad (1)$$

where t_{pt} is the duration of the SET plateau. Fig. 4(b) shows the values obtained by this approximation for two values of C_L (taken from [20]) and t_{pt}, with I_{D1} and I_{D2} values obtained from simulations with the transistor model from the design kit. The resulting values match well to the measured data. At the nominal supply voltage of VDD = 1 V, the variation of the plateau duration t_{pt} has a strong impact on the SET width t_{pw}, while changing the node capacitance C_L does not produce a notable effect. Hence, the differences in LET and intensity of charge sharing will be well reflected at the upper part of the VDD range. On the other hand, at the lower end of the VDD range, the situation is reversed—varying t_{pt} shows no effect, while the impact of C_L variations is very strong. Since the drain current of a transistor in the subthreshold regime is sensitive to process parameters, the time that it takes for the ON-state transistor to discharge the drain node capacitance C_L, and consequently the SET duration, will be sensitive to process- and mismatch-related variations, as well as to differences in parasitic capacitances coupled to the drain node.

Fig. 5 shows the cross section for both direct-hit and indirect SETs, with state "1" at the active node. The direct-hit cross sections in both Au and Ca experiments are slightly decreasing with VDD for DUT3 and DUT4, whereas it stays rather constant for DUT1 and DUT2. At first, this looks contrary to [3] and [6], which reported cross section to be increasing as VDD decreases. However, in both papers, SET cross section was measured indirectly, by measuring the SEU

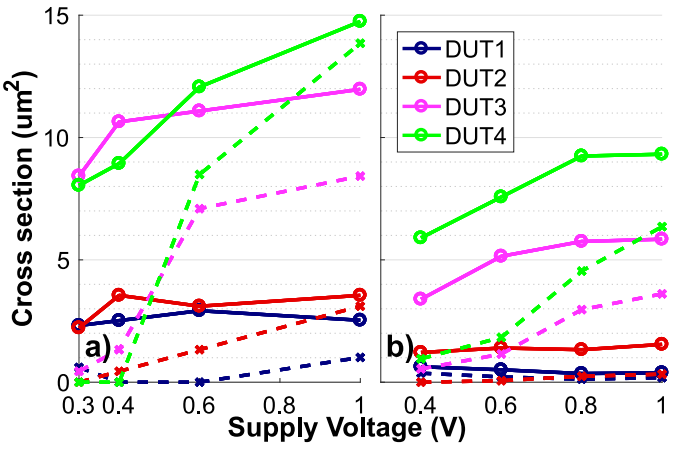

Fig. 5. Direct-hit (full lines) and indirect (dashed lines) SET cross sections, active node is in state "1." (a) Au experiment. (b) Ca experiment.

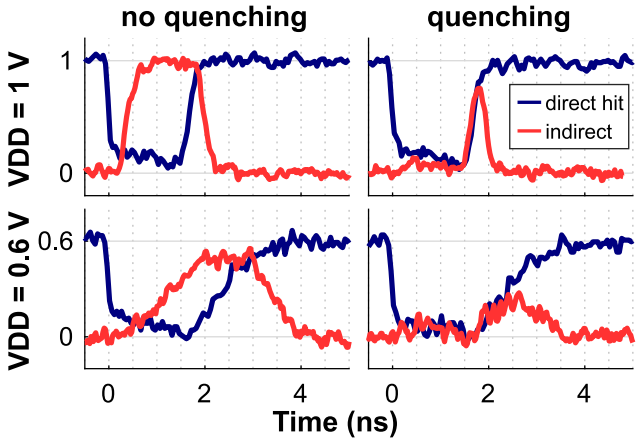

Fig. 6. Pulse quenching occurring in the Au experiment at supply voltages of 1 and 0.6 V.

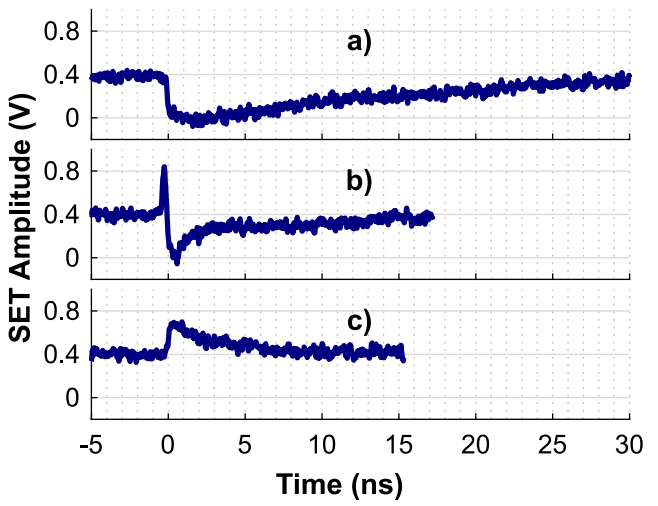

Fig. 7. Simultaneous nMOS and pMOS hits in the Au experiment, for a supply voltage of 0.4 V. Three neighboring hits are shown. (a) Only nMOS hit. (b) Both nMOS and pMOS hits. (c) Only pMOS hit.

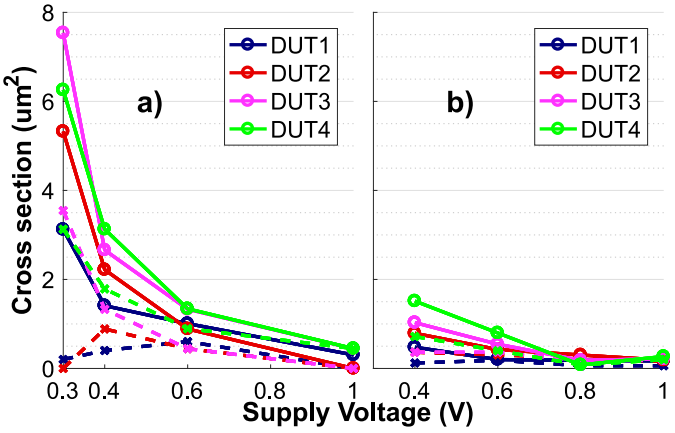

Fig. 8. Direct-hit (full lines) and indirect (dashed lines) SET cross sections, active node is in state "0." (a) Au experiment. (b) Ca experiment.

rate in DICE flip-flops, caused by the incoming SETs, sampled at a fixed clock frequency, which might not have represented real SET count on all voltages equally. At higher VDDs, SETs are several orders of magnitude shorter than at subthreshold, and a large number of them can miss the DICE window of vulnerability.

The decrease of indirect SET cross sections is more pronounced, and especially strong at subthreshold voltages. While it has been confirmed that pulse quenching [7] occurs at higher VDD values and decreases the cross sections of indirect SETs compared to direct-hit ones [19], no significant evidence was found that pulse quenching also causes the cross section reduction at lower voltages [11], [12]. By looking at the typical quenched SETs observed during the Au experiment in Fig. 6, it could be noted that the quenching duration of the indirect SET coincides well with the plateau duration of the corresponding direct-hit SET. Consequently, even if quenching would occur at lower supply voltages, its impact on total SET duration would not be very significant. The observed cross section reduction can rather be explained by the decreased ability of inverters to propagate signals before the thermal equilibrium is reinstated at the originating node.

Although stage-to-stage pulse quenching might not play a significant role at the subthreshold supply voltages, during our measurement cases were observed where "internal" pulse quenching would occur when ions hit the inverter in the region between nMOS and pMOS transistors. In Fig. 7(b), one such occurrence is shown. The first part of the pulse overshoots in the positive direction, which shows that the ON-state pMOS transistor has been hit. The following part goes toward the signal ground, showing that nMOS is also collecting charge from the hit. The resulting SET shape is something in between the shapes displayed in Fig. 7(a) and (b). The trailing edge exhibits two time constants—a fast one, while pMOS is still contributing to the SET, and a slow one similar to the nMOS-only hit, where SET is being dissipated through the ON-state pMOS device. Thus, the pulsewidth of the resulting SET is greatly reduced, as it was suggested in [22].

Interestingly, the direct-hit cross sections for state "0" at the active node, i.e., when pMOS is OFF, show an increase with decreasing VDD (Fig. 8). This could be due to a combination of larger collecting area of the pMOS drain–well junction and

decreased driving strength of subthreshold nMOS transistor, making it unable to remove the excessive charge fast enough.

V. Conclusion

In this paper, we employed our new measurement approach to simultaneously capture analog SET waveforms directly at the struck node and at the subsequent nodes. This enabled us to investigate influences of supply voltage and charge sharing on SET pulse widths and cross section, distinguishing between SET generation mechanisms and effects of their propagation through the circuit. To the best of our knowledge, until now such investigations were performed only by simulations [6], [11], [12], [16], [17]. A simple method was introduced for estimating the range of SET pulses at reduced VDDs, and it matches well with measurement results. At higher VDDs, we observed the influence of different LETs and inverter spacings, whereas in subthreshold region, pulse widths are strongly influenced by process and load capacitance variations. The observed pulse quenching effect and how its impact changes with supply voltage have been discussed. The presented information can be used to supplement the currently available simulation and experimental data.

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