Qualification of the ALICE SAMPA ASIC With a High-Speed Continuous DAQ System

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***Abstract*— During the Long Shutdown 2 of CERN's Large Hadron Collider, foreseen to start in 2019, the ALICE experiment will upgrade its time projection chamber (TPC) detector to cope with a Pb–Pb collision rate of 50 kHz in the next running phase. In the upgraded TPC, the gas electron multiplier (GEM) technology and continuous readout will replace the existing multiwire proportional chambers and triggered readout system. The GEM signals will be processed using a new custom designed mixed-signal front-end chip named SAMPA. The first version of SAMPA was delivered in 2014, and the production of the final version is in progress. This paper gives an overview of the design of the data acquisition system used in testing of the analog behavior of the first SAMPA version and the performance results of a SAMPA coupled to a pulse generator and a GEM detector prototype.**

***Index Terms*— Data acquisition (DAQ), DAQ systems, detector instrumentation, field programmable gate arrays (FPGAs), front-end electronics, front-end systems, gas electron multiplier (GEM) detectors, particle detectors, readout electronics, real-time systems.**

I. Introduction

FOR Run 3 and onward of the ALICE experiment, the Pb–Pb collision rate of CERN's Large Hadron Collider (LHC) will be 50 kHz compared with 8 kHz during Runs 1 and 2. The present time projection chamber (TPC) can sustain a readout rate of 1.5 kHz only, whereas after the upgrade, all interactions with a Pb–Pb rate of 50 kHz will be read out [1]. To make full use of the increased luminosity, the current multiwire proportional chambers of the ALICE TPC will be replaced by readout chambers, featuring the gas electron multiplier (GEM) technology [2]. Since the interaction intervals after the upgrade will be shorter than the particle drift time in the detector, a triggerless, continuous readout will replace the existing triggered readout.

The signals arriving from the GEMs will be processed by front-end cards, each consisting of five custom-made SAMPA ASICs and two gigabit transceivers (GBTx) [3]. Each SAMPA ASIC has 32 individual signal processing channels. The data from these channels will further be multiplexed and transmitted using GBTx via optical links to a common readout unit (CRU). The CRU is an interface to the online computer farm, trigger, and detector control system [4].

Manuscript received June 24, 2016; revised January 29, 2017 and April 5, 2017; accepted May 15, 2017. Date of publication May 25, 2017; date of current version June 26, 2017.

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Digital Object Identifier 10.1109/TNS.2017.2707339

The SAMPA ASIC combines the functionality of the previous PASA [5] and ALTRO [6] chips into one ASIC with doubling the number of channels from 16 to 32, supporting bipolar input signals and adding the possibility to run in a continuous readout mode. The first prototype of the SAMPA ASIC with three channels was produced in 2014. To test its performance, a continuous data acquisition (DAQ) system has been developed using an Altera System-on-Chip field programmable gate array (FPGA) development board [7].

The main goal in developing the DAQ system was to provide a standalone platform that was both compact, as well as easily customizable and deployable to multiple testing groups for both analog behavior qualification, digital verification, radiation testing, and mass production testing. Commonly DAQ systems or test benches are designed for single purpose use or tests, while with this system, we try to provide a common platform and framework to interface with the SAMPA ASIC for different types of tests.

The FPGA-based solution was chosen primarily due to Altera's support for scalable low-voltage signaling (SLVS) differential links [8], [16], required by the SAMPA, and the development kit's support for a high-speed extension cable to the carrier board, required for radiation testing. A custom developed FPGA board was ruled out due to the complexity and time involved in doing the design.

The system supports both the conventional DAQ method where a limited amount of samples are collected in a triggered fashion before being readout, as well as continuous acquisition using direct memory access and a Gigabit Ethernet enabled embedded Linux system [9], [10].

To transmit the data from the DAQ method to the controlling computer, Ethernet is used as it is available on most computers and makes the system more standalone, compared with solutions using PCIe or optical fibers [11], which might have provided higher readout speeds, but would require installing the card in the computer or having an interface board. Crate-based DAQ solutions using VME/ATCA/μTCA/PXI are also commonly used for their high-speed capability [12], but they are more expensive and considered less versatile.

The embedded Linux system has full access to the stream of incoming data as well as the possibility to take over the control of all pins on the SAMPA, providing a lower threshold for non-FPGA developers to develop test and verification applications directly on the embedded system.

A custom mezzanine board was designed for the SAMPA to mount directly on the development board. The data samples are analyzed in real time using the CERN ROOT [13] data

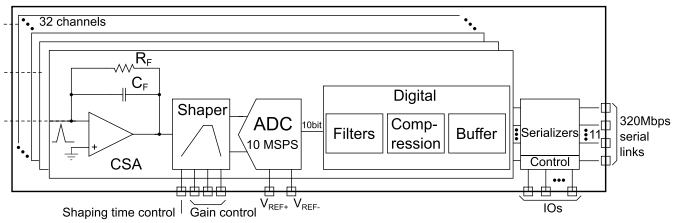

Fig. 1. Block diagram of the SAMPA ASIC consisting of CSA, shaper, analog-to-digital converter, and DSP block made up of different data filters.

analysis framework to monitor the data quality. To control, configure, and monitor the SAMPA and the FPGA board, a software-package with a graphical user interface (GUI) has been developed. The DAQ system was successfully used for testing the three channel readout and is also easily scalable for use with the full 32-channel chip using the built-in data compression capabilities of the SAMPA chip. In Sections III and IV, the readout-system design and its analog behavior performance tests of the SAMPA are discussed.

II. SAMPA ASIC

The SAMPA ASIC is designed for the upgraded front-end electronics of the ALICE TPC as well as the ALICE muon chambers [4]. It is a 32-readout-channel device containing charge-sensitive preamplifiers (CSAs), pulse shapers, analog-to-digital converters (ADCs), and one DSP, as shown in Fig. 1.

The CSA integrates the input charge using a feedback capacitor (C_f). A parallel large-ohmic transistor (R_f) is used to discharge the capacitor, leading the signal to the baseline level with an exponential tail. The following pulse shaping element creates a fourth-order semi-Gaussian shape, which is digitized using a successive approximation type ADC with 10-b resolution and up to 20-MHz sampling rate. The digital signal processing (DSP) section provides different filters, such as baseline-line correction, tail cancelation, zero suppression, and data compression. More details on the ALICE TPC requirements for the SAMPA can be found in [14] and [15].

The first prototype of the SAMPA was fabricated in a 130-nm CMOS technology. The front end was designed with selectable peaking times of 80, 160, and 300 ns, and selectable gains of 4, 20, and 30 mV/fC. The outputs have an equivalent noise charge of 670 e at 18.5-pF capacitance for 160-ns peaking time, 10-b resolution, and up to 20-MHz sampling frequency. Data are transmitted out of the device over three serial data links at 160 Mb/s.

III. High-Speed Data Acquisition System

The FPGA-based DAQ system is specially designed for the qualification of the SAMPA. The DAQ system is designed around an Altera SocKit evaluation board containing an Altera Cyclone V System-on-Chip FPGA [16], which has a built-in dual-core ARM Cortex-A9 microprocessor unit. The SAMPA is mounted on a mezzanine board connected to the development board through a high-speed connector. Control of the SAMPA and the FPGA board is handled through a universal asynchronous receiver/transmitter (UART) connection from the controlling computer. Data packets from the SAMPA are acquired by the FPGA and transmitted verbatim to the readout computer via Gigabit Ethernet.

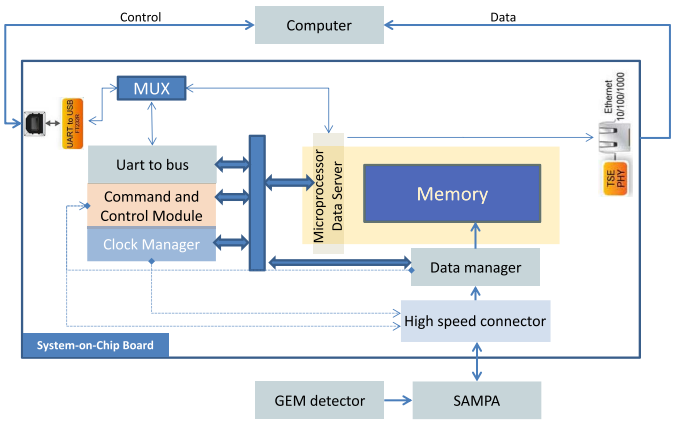

Fig. 2. Schematic overview of the firmware design showing various system blocks.

The intention of the DAQ system is to provide an easily customizable, standalone platform that is also compact and easily deployable to multiple testing groups for the following:

- qualification of the properties of the analog front end and ADC;
- digital verification;
- testing of the radiation tolerance of the SAMPA in regards to single event upsets, single event latchup, and stability;
- mass production testing to filter out bad devices before mounting them on front-end cards.

A custom DAQ solution was chosen due to a number of reasons. The SAMPA uses SLVS differential links [8] for its serial communication links as this is the type of link used by the GBTx ASIC. Altera FPGAs were, at the time, the only devices that could be used for acquisition of data, which also supported SLVS receivers natively. The GBTx ASICs were not available yet. Furthermore, there is support and commercial availability of extension cables for connection between the development board and the mezzanine board, and the CRU is based on an Altera device as well, so development can be shared; additionally, the development board is available at a low cost.

As it is possible to take over the control of the pins to the SAMPA from the control program on the computer or through the embedded Linux systems, custom tests for the SAMPA can be developed by non-FPGA designers through bit-banging the pins. This design methodology provides low development overhead, but it comes with a reduction in performance. For tests of the second prototype, a JTAG boundary scan tester for checking connections between the FPGA and the SAMPA, as well as an automatic test pattern generator for testing of manufacturing defects using the SAMPA design's scan chains was developed in this way.

Section III-A describes the features of the DAQ system used for the analog behavior qualification. A block diagram of the firmware design is shown in Fig. 2.

A. Firmware Design

The firmware design is split into three main parts, a Command and Control unit, a Data Manager unit, and a Data Server, as described as follows. It also contains a

reconfigurable phase-locked loop (the Clock Manager), which enables on the fly reconfiguration of the sampling clock as well as the main clock for the SAMPA digital part. The main modules are all connected to a common Avalon bus together with the microprocessor, which can be accessed by the control program on the computer through a custom UART to Avalon bus bridge. A switch controlled multiplexer facilitates switching between having a serial connection to the bus system or to a Linux serial terminal for debug purposes.

1) Command and Control: The command and control unit acts as a bridge between the computer and the SAMPA for slow control handling and pin control. Additionally, it acts as the main control unit for the surrounding modules, which include a module for handling the slow control communication with the SAMPA for reading and writing the SAMPA's registers, in addition to a module for reset generation and event trigger handling. For the second prototype of the chip, this also includes modules and control for running specialized tests on the SAMPA such as a test of the memory IP-cores through a built-in memory tester in the SAMPA and SLVS link verification through a pseudorandom binary generator and verifier.

2) Data Manager: The first prototype of the SAMPA chip has three serial links running at 160 Mb/s while the final version will have 11 differential serial data links running at 320 Mb/s adding up to 3.52 Gb/s. Data from the SAMPA are packet-based with a fixed length header and a variable length payload. The header contains information on, among other things, the type of packet and the length of the following payload. Filler packets are sent in between the data to let the receiver synchronize to the stream. The Data Manager synchronizes and deserializes the data from each link into 10-b words, verifies the parity of the header, and determines the length of the payload that will follow and if the packet contains data or are filler packets that should be dropped. The valid deserialized packets are further segmented into 64-b words to make processing on a 32/64-b system more efficient. The packets are then further aggregated from the 11 deserializer into four memory writer modules via individual first in/first outs (FIFOs). The memory writers are connected to separate high-speed 64-b, 100-MHz buses to a 400-MHz double data rate (DDR) memory shared with the microprocessor. The system can thus support writing of the full 3.52 Gb/s to memory and the readout speed is only limited by the readout through the microprocessor system. For the second prototype of the SAMPA, the mezzanine cards have been fit with two small form-factor pluggable connectors for offloading of some of the data to another device through the high-speed transceivers of the FPGA, in case readout of the full bandwidth is needed.

The system can be set up to acquire data continuously or to acquire a configurable number of consecutive packets per serial data link. In case an overflow is detected in the FIFOs or the memory, the system drops the payload of the packet and sets an overflow bit in the header, indicating to the data analysis program that the amount of data should be reduced.

As the incoming serial data arrives at a high speed, there is a possibility that the data will be sampled at the changeover point, generating invalid data. To combat this the system uses the DDR registers available in the input pads of the FPGA to provide the value at both the rising and falling edges of the system clock. An autoadjustment function in the control program on the computer selects which input to use for the deserializer based on the deserializer's ability to synchronize to the incoming data stream.

3) Data Server: The data server is a program running on the Linux system of the microprocessor. It handles data transmission and TCP/IP connection control with the remote controlling computer. In addition, it retrieves data uploaded to memory by the Data Manager and transmits it over Ethernet to the controlling computer. As the data from the SAMPA are already packet-based, with a header and payload, it can be transmitted verbatim to the controlling computer with the TCP protocol, minimizing overhead. By using the TCP protocol instead of the UDP protocol, such as in [9], the need for supporting packet retransmission in case of packet loss can be avoided. The data throughput is limited by the Linux system and the microprocessor's Gigabit Ethernet throughput, which has been measured for TCP transmission to be 670 Mb/s with use of the iPerf3 tool [17]. UDP transfers were tested to reach the same speeds if packet loss was taken into account.

As the three ADCs running at 10 MHz only produce 300 Mb/s of data, the bandwidth is not a limitation for the first prototype. On the second prototype with 32 channels, this problem is overcome by limiting the continuous acquisition to about 100 000 packets of 1000 samples each and buffering the acquired data in the memory until it can be read out.

B. SAMPA Communicator

The SAMPA communicator is a graphical user environment, made in C#, to handle control and configuration of the DAQ and the SAMPA. A picture of the interface is shown in Fig. 3. It is designed for easy use by nontechnical users to aid in setting up and running tests on the SAMPA without the need to know details of the operation of the DAQ system. Furthermore, it simplifies register access and provides, among other things, data flow handling, online status information, and access to changing the frequency of the clocks supplied to the SAMPA as well as custom test and control features for radiation testing, digital verification, and mass testing.

C. SAMPA Analyzer

Data handling on the computer side is taken care of by a ROOT program. It sets up the Ethernet connection with the FPGA board, receives data packets, verifies the packet integrity, and decodes the zero suppression compression, if used. It then plots and displays the sampled signals per channel and writes the raw data packets out to a ROOT file for later analysis. When running in continuous acquisition mode, the plots can be set to update only when the data pass a threshold value, similar to the triggering function on an oscilloscope.

The described system was successfully used for testing the first SAMPA prototype and will also be used in testing of the second prototype. The test performance of the DAQ system is discussed in Section IV.

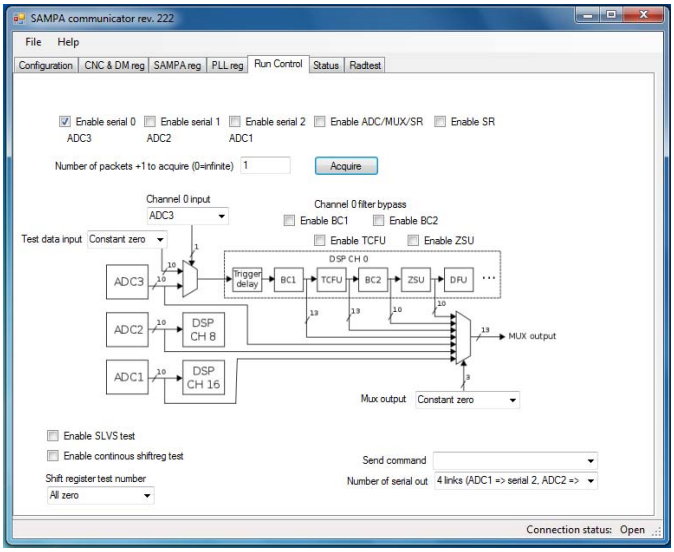

Fig. 3. Picture of the run control part of the SAMPA communicator GUI used for testing of the first prototype.

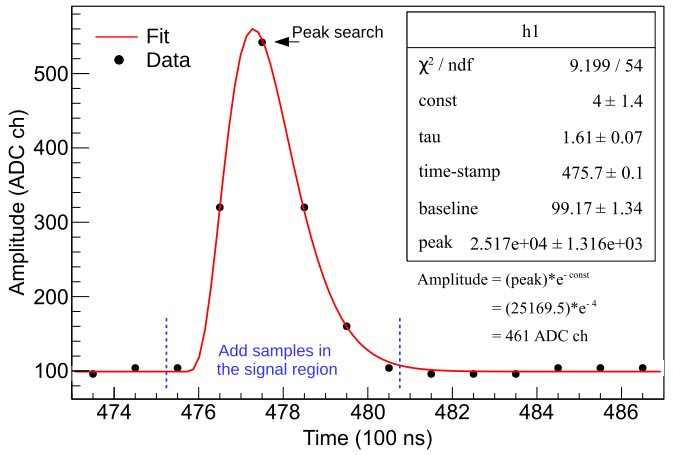

Fig. 4. Example waveform showing the different methods used for waveform feature extraction: peak search (arrow), waveform fitting shown in solid line (red curve), and area of waveform, which is calculated by adding the samples in the signal region (blue vertical dashed line).

IV. Test Setup, Results, and Discussion

The SAMPA and the high-speed DAQ system performance tests were carried out using a pulse generator as well as a GEM detector prototype as signal sources, shown in Fig. 7.

To perform feature extractions (e.g., amplitude, time, and so on) from the recorded signals, different methods, such as peak search, area of waveform, and waveform fitting, are used as shown in Fig. 4. The following equation has been used to fit the experimental data as shown in Fig. 4:

$$f(x) = A\left(\frac{x-t}{\tau}\right)^{N} e^{-N\left(\frac{x-t}{\tau}\right)} + Bl. \quad (1)$$

Here, the waveform amplitude is obtained from Ae^{-N}, where A is the peak and $N = 4$ is the shaping order of the amplifier. Bl is the baseline, τ is the decay time, and t is the start time of the signal.

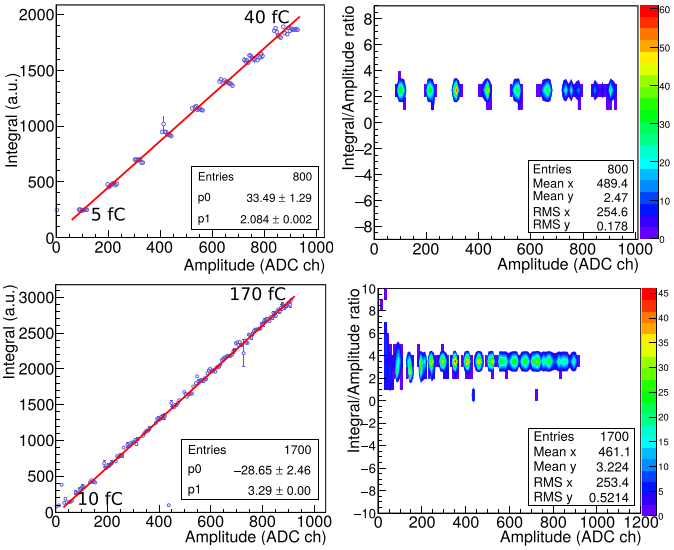

Fig. 5. Left: waveform integral versus the waveform amplitude. The data points for the lowest and the highest injected charge are denoted in fC values. Right: ratio of integral over amplitude versus amplitude. Top: 20-mV/fC gain setting. Bottom: 4-mV/fC gain setting. The waveform amplitude and integral of samples vary linearly with input charge and the constant nature of the integral over amplitude ratio confirms the waveform shape stability.

A. Signal Injection Using Pulse Generator

The test charge was injected into the SAMPA chip by sending a 10-kHz step signal through 1-pF series capacitor. The step signal was generated by using a ramp signal, which slowly charges the series capacitor before returning to zero. During the experiment, the device under test was kept inside a Faraday cage to shield it from external noise sources.

Different signal extraction methods have been tried out, in order to verify their performances with respect to complexity and accuracy. For this, a fixed amplitude test waveform was injected into the SAMPA chip and the pulse height distributions were obtained using three different methods, such as peak search, area of waveform, and waveform fitting. It was concluded that the waveform fitting was the best suited method, and it was therefore used for the following tests.

The SAMPA chip can be operated with different gains as well as at different peaking times, requiring many tests to cover all combinations. Here, we present the results for 4 mV/fC at 300 ns and 20 mV/fC at 160 ns. The gain linearity has been verified by plotting the relation between the waveform amplitude and integral (sum of samples in the signal region) of the waveform as shown in Fig. 5 (left). The input charge was varied from 5 to 40 fC at 5 fC per interval for 20-mV/fC gain (top) and from 10 to 170 fC at 10 fC per interval for 4-mV/fC gain (bottom), acquiring 1000 waveforms for each setting.

It is assumed that if the waveform shape is stable for different input charges, then the ratio of the waveform integral (I) over the amplitude (A) must be constant. Therefore, to verify the waveform stability, the ratio of I over A is plotted against A as shown in Fig. 5 (right). The constant trend of I over A ratio confirms that the waveform shapes are stable for various input charges.

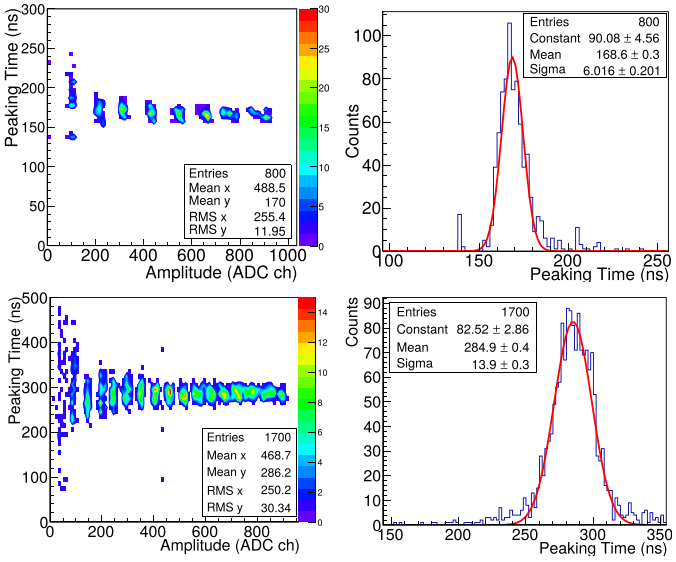

Fig. 6. Left: peaking time versus amplitude of the waveform. Right: y-projection (left). Top: 20-mV/fC gain setting. Bottom: 4-mV/fC gain setting. The peaking time is almost constant for various waveform amplitudes or input charges.

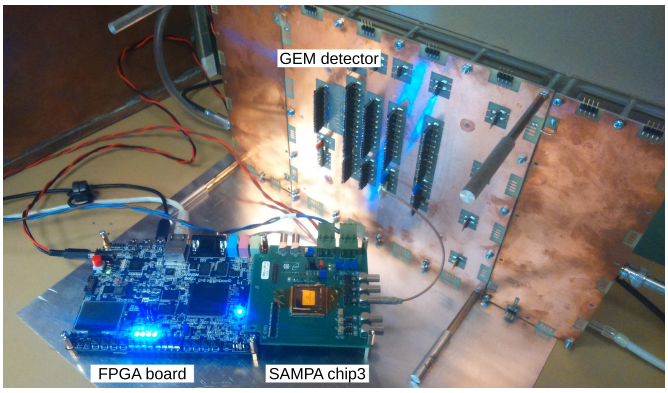

Fig. 7. Photograph of the experimental setup where the SAMPA and the DAQ system were tested using the GEM detector prototype.

The peaking time is obtained using the fit parameter τ, as shown in Fig. 4. The peaking time stability over various waveform amplitudes or input charges was verified by plotting the waveform amplitude as function of peaking time, shown in Fig. 6 (left) and its y-projection is shown in Fig. 6 (right). The top plots are for the 20-mV/fC gain and bottom ones are for the 4-mV/fC gain. According to the left plots, peaking time of the waveform appears to be constant for various waveform amplitudes or input charges. Gaussian fits to the top right and left plots give peaking times of 168.6 ± 6.0 ns and 284.9 ± 13.9 ns. The obtained values are close to the expected values of 160 and 300 ns, respectively.

B. Using GEM Detector Prototype

The upgraded ALICE TPC will make use of GEM foil readout chambers. Hence, to have a realistic test environment, the DAQ system has been tested with a prototype GEM detector. The detector consists of a stack of three standard sized GEM foils. The FPGA board coupled to SAMPA ASIC and GEM chamber is shown in Fig. 7.

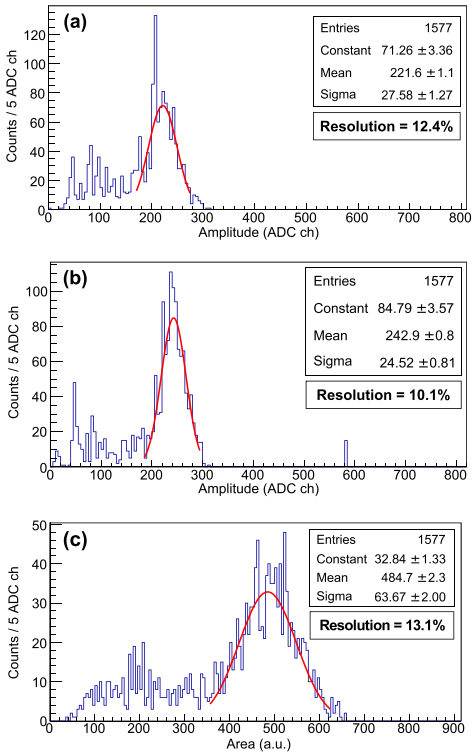

Fig. 8. Fe-55 soft-photon energy spectrum obtained using (a) peak search, (b) fit to the waveform, and (c) integrating samples in the signal region.

To initiate the processes of excitation and ionization inside the GEM detector, a Fe-55 radioactive source was used. The photons emitted by the Fe-55 (5.9 keV) interact with the detector gas as maximum ionizing particles through the photoelectric effect.

The Fe-55 soft-photon energy spectrum is shown in Fig. 8, taken for a detector readout pad size of 6 mm $\times$ 15 mm with $NeCO_2N_2$ gas mixture. For this spectrum, the gain of the GEM detector was 2000 and the gain of the SAMPA chip was 20 mV/fC with a shaping time of 160 ns.

Due to a combination of having a low ADC sampling rate of 10 MHz and a short shaping time of 160 ns, which only gives an average waveform length of three samples, the best result is achieved by fitting to the waveform. The measured energy resolution for fitting is 10.1%, compared with 12.4% and 13.1% for peak search and signal integral, respectively. A resolution of 10.1% satisfies the requirements for the ALICE TPC.

V. Outlook and Conclusion

To test the SAMPA ASIC developed as a part of ALICE TPC upgrade, a high-speed DAQ has been designed and successfully tested using a pulse generator as well as a GEM detector. General tests, such as gain linearity, pulse shape, and peaking time stability, were carried out for various values of the SAMPA input charge. A good gain linearity and pulse shape stability have been observed. The measured peaking time meets the design requirements. Also, the DAQ system has performed very well while it was coupled to the GEM detector. Energy resolution of 10.1% is obtained for Fe-55 soft photons of 5.9-keV energy in $NeCO_2N_2$ gas mixture at a GEM detector gain of 2000. The second prototype of the SAMPA ASIC

with 32 readout channels is expected to be ready for testing in July 2016. The DAQ system reported in this paper, with some updates, will also be used for testing the performance of the second prototype.

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