Compact Modeling of Total Ionizing Dose and Aging Effects in MOS Technologies

I. Sanchez Esqueda, H. J. Barnaby, and M. P. King

***Abstract*—This paper presents a physics-based compact modeling approach that incorporates the impact of total ionizing dose (TID) and stress-induced defects into simulations of metal-oxide-semiconductor (MOS) devices and integrated circuits (ICs). This approach utilizes calculations of surface potential (ψ_s) to capture the charge contribution from oxide trapped charge and interface traps and to describe their impact on MOS electrostatics and device operating characteristics as a function of ionizing radiation exposure and aging effects. The modeling approach is demonstrated for bulk and silicon-on-insulator (SOI) MOS device. The formulation is verified using TCAD simulations and through the comparison of model calculations and experimental $I-V$ characteristics from irradiated devices. The modeling approach is suitable for simulating TID and aging effects in advanced MOS devices and ICs, and is compatible with modern MOSFET compact modeling techniques. A circuit-level demonstration is given for TID and aging effects in SRAM cells.**

***Index Terms*—Aging effects, compact modeling, ionizing radiation, MOSFET, semiconductor devices, SOI.**

I. Introduction

PHYSICS-BASED compact models of advanced electronic devices provide a concise mathematical description of our understanding of the operation of the device, help interpreting experiments and detailed simulations, and enable circuit design [1]. *Understanding and analyzing the impact of ionizing radiation and aging effects in modern MOS technologies requires the incorporation of radiation and stress-induced defects into advanced compact model formulations of device operation*. Additionally, radiation effects mitigation utilizes simulation to support the design of ICs to meet targeted tolerance specifications for a particular radiation environment [2]–[4]. In these environments, energy deposition from ionizing radiation leads to the buildup of oxide-trapped charge and the generation of interface traps degrading the electrical characteristics of MOS devices. Aging mechanisms in advanced MOS technologies are also attributed to charge trapping near and/or trap buildup at semiconductor/oxide interfaces [5], [6].

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Previous studies have resulted in a comprehensive understanding of the basic mechanisms contributing to ionizing radiation effects in MOS systems. These mechanisms include the generation/recombination [7]–[10] and transport [11]–[17] of charged carriers in the oxide film, the trapping of holes that escape initial recombination [18]–[21], and the mechanisms leading to the generation of interface traps [22]–[26]. A review of the basic mechanisms of total ionizing dose (TID) effects can be found in [27]–[30]. Characterization and modeling of ionizing radiation effects in MOS field effect transistors (i.e., MOSFETs) has been traditionally based on dose-dependent shifts in device parameters such as threshold voltage (V_{TH}), subthreshold swing (S), etc. [31]–[34]. The work presented here extends this methodology to a radiation-induced defect based methodology using calculations of surface potential.

In this paper we present the detailed formulation and demonstration of a recently developed physics-based compact modeling approach that captures the charge contribution of oxide trapped charge and interface traps and describes their impact on MOS electrostatics and device operating characteristics. This modeling approach has been applied for modeling TID effects [2]–[4], [35], aging effects attributed to negative-bias temperature instability (NBTI) and hot carrier (HC) damage [36], [37], and recently the impact of stress-induced defects on short-channel effects (SCE) in advanced MOS technologies [38]. The derivation of the model follows the incorporation of oxide trapped charge and interface trap densities (N_{ot} and D_{it}) into expressions of electric field at the semiconductor/oxide interface that are used as boundary conditions in calculating the surface potential (ψ_s) in metal-oxide-semiconductor (MOS) devices. Calculations of ψ_s can be used to describe the impact of radiation and stress-induced defects on the *I-V* characteristics of MOSFETs, $C(V)$ characteristics of MOS capacitors [39], and for accurately extracting parametric shifts as a function of ionizing radiation and/or electrical stressing conditions. Derivation and demonstration of the modeling approach is presented for bulk and SOI devices. Shown in Fig. 1 is the schematic cross-section of an SOI device indicating the buildup of radiation-induced oxide trapped charge and generation of interface traps in oxide regions and at the semiconductor/oxide interfaces.

Section II describes charge contribution from radiation-induced defects and presents the general approach for incorporating the impact of defects into calculations of surface potential for compact modeling of MOS devices. Section III applies the modeling approach by incorporating the charge contribution from oxide trapped charge and interface trap densities (N_{ot} and N_{it}) to solve Poisson's equation and obtain the surface po-

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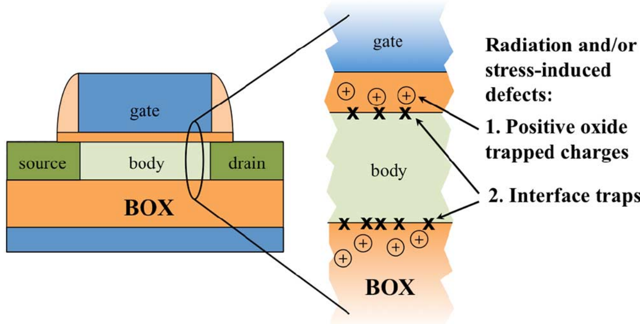

Fig. 1. Schematic cross-section of SOI MOSFET indicating the buildup of radiation-induced oxide trapped charge and the generation of interface traps.

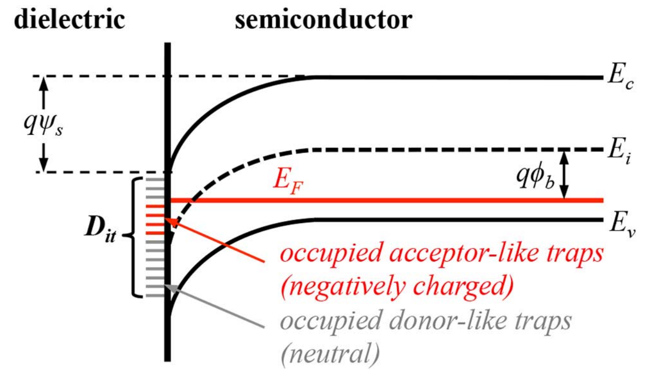

Fig. 2. Energy band diagram summarizing the charge contribution from interface traps in MOS devices. Shown here for a p-type semiconductor in strong inversion and in equilibrium.

tential equation (SPE) used to describe TID and aging effects in bulk and SOI MOS devices. Section IV provides discussion on the applicability of the model and presents further verification using experimental data from irradiated bulk and SOI MOSFETs. Section IV also includes a demonstration of SPICE simulations that incorporate TID and stress-induced defects and describe their impact the circuit level. This demonstration investigates the impact of ionizing radiation and aging effects on SRAM subtreshold operation. Conclusions are provided in Section V.

II. Modeling Approach

The modeling approach described in this paper incorporates radiation-induced defect densities into expressions of electric field at the semiconductor/oxide interface that are used as boundary conditions in calculating the surface potential (ψ_s) in metal-oxide-semiconductor (MOS) devices. The radiation-induced defect densities used in this approach are quantitative representations of trapped charge integrated across the thickness of the oxide (N_{ot}), and the number of interface traps at the semiconductor/oxide interface (N_{it}). In this approach, qN_{ot} accounts for the charge contribution per unit area from trapping centers that do not respond to changes in position of the Fermi level (E_F) (i.e., they have large emission time constants relative to the timescales of interest and are assumed fixed). On the other hand, qN_{it} depends on the position of E_F as interface traps have short time constants and can be assume to respond instantaneously by changing their state of occupancy and charge contribution. Oxide trapping centers near the interface with energy levels in the vicinity of the intrinsic Fermi level (E_i) (i.e., border traps or switching oxide traps) have time constants that may also allow responding to changes in E_F. In our modeling approach these are lumped together with interface traps into N_{it}. The parameter extraction methodology must consider the timescales of interest for a given application when obtaining the densities of the switching vs. fixed charges. Early work by Fleetwood *et al.* [40] identified the distinct properties of switching oxide traps and described how these differ from interface traps in terms of position and electrical response. Different techniques for estimating the density of switching oxide traps are also described in [40], [41].

The dependence of charge contribution from switching traps (i.e., interface and border traps) on E_F can be related to ψ_s using $(E_F - E_i) = (\psi_s - \phi_b)$, resulting in

$$qN_{it} = -qD_{it}\left(\psi_s - \phi_b\right), \tag{1}$$

where ϕ_b is the bulk potential and D_{it} is the number of interface traps per unit area per unit energy. Here we approximate D_{it} as uniformly distributed in energy. This approximation is introduced for simplicity in the derivation of our modeling approach and allows closed-form expressions useful for compact modeling to be obtained. The simplified result obtained from this approximation allows obtaining a good understanding of TID effects and is sufficient for circuit-level (i.e., SPICE) simulations regarding the impact of N_{ot} and N_{it} on the electrostatics of MOS devices and ICs. In this work, N_{it} is considered the effective (or average) interface trap density and is a model parameter that accounts for charge contribution from interface traps with non-uniform energy distributions. A more general description for modeling non-uniform energy distributions of N_{it} is given in [39]. Additionally, early work on MOS devices that describes the characterization of charge-contribution from radiation-induced interface traps can be found in [42]–[44].

All interface traps with energy levels $E_T > E_i$ are treated as acceptor-like and all interface traps with $E_T < E_i$ are treated as donor-like based on the experimentally verified amphoteric nature of traps in the Si/SiO_2 interface [45. 46]. Acceptor-like traps are neutral when empty and contribute negative charge when occupied by an electron (i.e., are ionized when occupied). Donor-like traps are neutral when occupied by an electron and contribute positive charge when empty (i.e., are ionized when unoccupied). The energy band diagram in Fig. 2 summarizes the charge contribution from interface traps in the MOS system. In this case, the energy band diagram is shown for a strongly inverted p-type semiconductor under equilibrium conditions. At the dielectric-semiconductor interface all donor-like traps are neutral and most acceptor-like traps are occupied and contribute negative charge. The net charge contribution from interface traps given by (1) is negative as $\psi_s \approx 2\phi_b > \phi_b$. Under non-equilibrium conditions, splitting of the Fermi level allows treating current flow through the use of quasi-Fermi level gradients. In MOSFETs, current flow in the channel is unipolar and the split in the quasi-Fermi levels can be expressed as $\phi_n =$

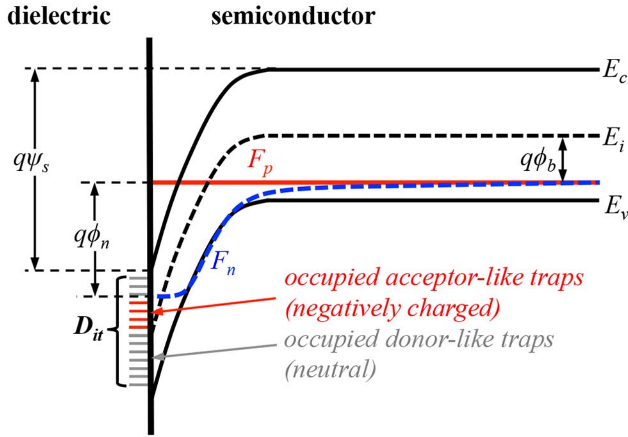

Fig. 3. Energy band diagram indicating charge contribution from interface traps in a p-type semiconductor in strong inversion and non-equilibrium conditions (e.g., in a cross-section of an n-channel MOSFET).

$(F_p - F_n)/q$. ϕ_n varies between the values at the source and drain given respectively by V_{sb} and V_{db} (i.e., the source-to-body and drain-to-body voltages). As indicated in the band diagram shown in Fig. 3, the charge contribution from interface traps under non-equilibrium conditions must account for the split in the quasi-Fermi levels resulting in

$$qN_{it} = -qD_{it}\left(\psi_s - \phi_b - \phi_n\right). \quad (2)$$

It should be noted that for the case of an n-channel MOSFET, as shown in Fig. 3, the minority-carrier quasi-Fermi level (F_n) will vary between source and drain, whereas the majority carrier quasi-Fermi level (F_p) is position-independent. The total charge at semiconductor/oxide interface due to ionizing radiation effects is expressed as

$$Q_T = qN_{ot} + qN_{it} = q\left[N_{ot} - D_{it}\left(\psi_s - \phi_b - \phi_n\right)\right]. \quad (3)$$

TID effects in devices and ICs can be analyzed and modeled by incorporating the charge given by (3) into a description of MOS electrostatics that will be obtained through calculations of ψ_s for our compact modeling purposes. This approach allows a continuous and accurate description of the radiation response from weak to strong inversion for equilibrium and non-equilibrium conditions. This way, it is not required to define artificial modeling parameters such as subthreshold slope, threshold voltage, etc. Instead, the radiation response is captured continuously as a function of N_{ot} and N_{it} as will be demonstrated by comparing model calculations with TCAD simulations. Nonetheless, the extractions of several parameters typically used to analyze device-level characteristics will be presented to demonstrate the radiation response of different MOS devices. It should also be noted that the presented approach is applicable to modeling the effects of aging mechanisms in MOS devices and ICs including negative-bias temperature instability (NBTI) and hot-carrier (HC) degradation. This is possible due to the physics-based nature of the proposed modeling approach for describing the impact of radiation and/or stress-induced defects on the electrical characteristics of MOS devices.

Similar to TID effects, NBTI and HC damage results from charge trapping near and/or trap buildup at the semiconductor/oxide interface [5], [6]. Charge contribution from hole trapping that occurs near the semiconductor/oxide interface (i.e., in border traps) is easily neutralized via emission and is considered the main contributor to the recoverable component of NBTI [47]–[50]. Unlike trapped holes, interface traps created by the depassivation of silicon dangling bonds are often associated with long-term aging effects attributed to the permanent component of NBTI and to HC damage [47], [50]. As with TID-induced interface traps, the occupancy and charge contribution depends on the position of the Fermi-level with respect to the trap energy level and is consequently bias-dependent. However, most existing compact modeling techniques for aging effects are based on fixed V_{th} shifts and fail to capture the distinctive effect each defect type has on the transistor's electrical characteristics [51], [52]. The modeling techniques described in this paper capture the bias-dependent charge contribution from both oxide-trapped charge and interface traps and allow incorporating the buildup and recovery of these defects as a function of stress and/or radiation conditions over time. This method enables the analysis and simulation of the primary long-term reliability degradation mechanisms of ICs in radiation environments by describing the buildup of N_{ot} and N_{it} as a function of stress and radiation exposure. The accumulation of defects is application-specific and defined by the user. In this paper we will focus mostly on TID effects but a more detailed description of modeling aging effects using the proposed defect-based methodology can be found in [36]–[38].

III. Model Formulation and Results

In this section we incorporate the charge contribution from N_{ot} and N_{it} at the semiconductor/oxide interface into calculations of ψ_s in MOS devices. As mentioned in Section II, this is accomplished by incorporating (3) into expressions of electric field at the semiconductor/oxide interface that are used as boundary conditions when solving Poisson's equation. The resulting surface potential equation (SPE) allows calculating ψ_s as a function of process parameters (e.g., oxide thickness, doping concentration, gate-to-semiconductor workfunction, etc.), bias (i.e., the terminal voltages), and the radiation-induced defect densities (N_{ot} and N_{it}). The SPE is the starting point for standard surface-potential-based compact models of MOS devices (e.g., PSP, an advanced surface-potential-based MOSFET compact model [53]–[55]). Here we extend the SPE to incorporate the impact of radiation-induced defects on the electrical characteristics of MOS devices.

Calculations of ψ_s can be used to obtain current and terminal charges in MOSFETs through the Pao-Sah double integral formula [56] or using charge-sheet approximations [57]. Simplified implementations of the charge-sheet model (CSM) that are more suitable for compact modeling applications are used in standard MOSFET compact models (e.g., in PSP) [58], [59]. Calculations of ψ_s can also be used to obtain $C(V)$ characteristics of MOS capacitors and extracting the buildup of radiation-induced defects densities through the comparison with measurements of MOS capacitance [39]. Parametric shifts can be accurately extracted from calculations of ψ_s using the modified SPE at conditions of interest (e.g., at the onset of strong inversion using $\psi_s = 2\phi_b$). In this section of the paper we present the general

approach for deriving and solving the modified SPE that incorporates radiation-induced defect densities in bulk and SOI MOS devices. Additional demonstration of the modeling approach is provided through calculations of current-voltage (*I-V*) characteristics using the CSM, and through extractions of threshold voltage. The model calculations are verified through comparisons with TCAD and experimental data.

A. Bulk MOS devices

For a bulk MOS capacitor with a p-type semiconductor the one-dimensional (1-D) Poisson's equation is given by

$$\frac{d^2\psi}{dx^2} = -\frac{\rho}{\varepsilon_s} = -\frac{q}{\varepsilon_s}\left(p - n - N_a\right), \tag{4}$$

where p, n, and N_a are the hole, electron, and ionized acceptor concentrations respectively. Using Boltzmann statistics for the free carrier concentrations and the property $(d^2\psi/dx^2) = (1/2)(dE_x^2/d\psi)$ allows expressing (4) as

$$\frac{dE_x^2}{d\psi} = -\frac{2\rho(\psi)}{\varepsilon_s} = -\frac{2qN_a}{\varepsilon_s}[e^{-\beta\psi} - 1 - e^{-2\beta\phi_b}(e^{\beta\psi} - 1)], \tag{5}$$

Where $\beta = 1/\phi_t$, and $\phi_t = kT/q$. Separation of variables gives

$$E_x^2(0) - E_x^2(\infty) = -\frac{2qN_a}{\varepsilon_s}\int_{\psi(\infty)}^{\psi(0)}[e^{-\beta\psi} - 1 - e^{-2\beta\phi_b}(e^{\beta\psi} - 1)]d\psi. \tag{6}$$

Integrating (6) we obtain

$$E_s^2 = \left(\frac{2qN_a}{\beta\varepsilon_s}\right)H(\beta\psi_s), \tag{7}$$

where

$$H(\beta\psi_s) = e^{-\beta\psi_s} + \beta\psi_s - 1 + e^{-2\beta\phi_b}(e^{\beta\psi_s} - \beta\psi_s - 1). \tag{8}$$

Here we have used the boundary conditions $\{E_x(\infty) = 0; \psi(\infty) = 0\}$ and $\{E_x(0) = E_s; \psi(0) = \psi_s\}$. Notice that these boundary conditions are only valid for bulk and not for SOI or double-gate MOS devices. To obtain the $V_{gb}(\psi_s)$ relationship we express E_s in terms of V_{gb} (i.e., the gate-to-body voltage). This can be accomplished by using the oxide electric field given by $E_{ox} = (V_{gb} - \Phi_{MS} - \psi_s)/t_{ox}$, where Φ_{MS} is the gate-to-semiconductor workfunction difference and t_{ox} is the gate oxide thickness. The charge contribution from radiation-induced defects is incorporated through the boundary condition on the normal component of the displacement at the semiconductor/oxide interface requiring that

$$\varepsilon_s E_s - \varepsilon_{ox}E_{ox} = Q_T. \tag{9}$$

Combining (3), and (7)–(9) results in [35]–[37]

$$(V_{gb} - \Phi_{MS} + \phi_{nt} - \psi_s)^2 = \gamma^2\phi_t H(\beta\psi_s), \tag{10}$$

where we have defined [2]

$$\phi_{nt} \equiv \frac{q}{C_{ox}}[N_{ot} - D_{it}(\psi_s - \phi_b)], \tag{11}$$

and

$$\gamma = \sqrt{2q\varepsilon_s N_a}/C_{ox} \tag{12}$$

is the body factor. In (11) and (12) $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the oxide capacitance per unit area. Notice that for the MOS capacitor we have $\phi_n = 0$ in (3).

Equation (10) is the modified SPE that incorporates charge contribution from N_{ot} and N_{it} through the *defect potential* ϕ_{nt}. Normalizing (10) by $(\phi_t)^2$ results in

$$(u_g + u_{nt} - u_s)^2 = G\left[e^{-u_s} + u_s - 1 + e^{-2u_b}(e^{u_s} - u_s - 1)\right], \tag{13}$$

where $u_g = \beta(V_{gb} - \Phi_{MS})$, $u_s = \beta\psi_s$, $u_{nt} = \beta\phi_{nt}$, $u_b = \beta\phi_b$, and $G = \beta\gamma^2$. Expanding u_{nt} and gathering the ψ_s terms (i.e., u_s) in the left-hand side of (13) allows renormalizing to obtain [60], [61]

$$(u_g^* - u_s)^2 = G^*[e^{-u_s} + u_s - 1 + e^{-2u_b}(e^{u_s} - u_s - 1)], \tag{14}$$

In (14),

$$u_g^* = \frac{u_g + q(N_{ot} + D_{it}\phi_b)/(\phi_t C_{ox})}{\xi}, \tag{15}$$

$$G^* = G/\xi^2, \tag{16}$$

and

$$\xi = 1 + qD_{it}/C_{ox}. \tag{17}$$

The modified SPE is an implicit function of ψ_s that can be solved to describe the $V_{gb}(\psi_s)$ relationship as a function of N_{ot} and D_{it}. The SPE equation can be solved iteratively using the Raphson-Newton procedure [62], [63] or analytically through non-iterative approximations [64], [65]. Expressing the modified SPE as in (14) allows using an accurate non-iterative algorithm based on a closed-form analytical approximation of ψ_s. This algorithm follows the derivation in [64], [65] while maintaining the contributions of N_{ot} and D_{it} and is further described and demonstrated in [36]. As discussed in [64], the non-iterative approach for calculating ψ_s eliminates convergence issues in circuit simulators that may result from internal iterative loops.

Fig. 4 plots ψ_s as a function of V_{gb} for increasing N_{ot} from solutions to the SPE given by (14). The model calculations are compared to extractions from two-dimensional (2-D) TCAD simulations. Model and TCAD parameters are summarized in Table I. For the results in Fig. 4 we set $D_{it} = 0$ cm^{-2}eV^{-1} to independently verify the accuracy of the model in describing

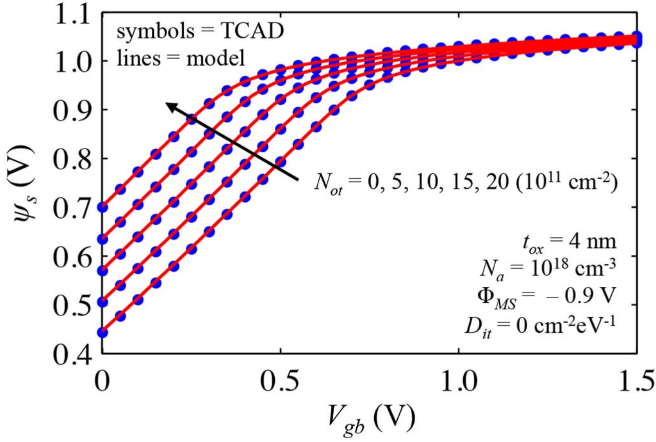

Fig. 4. Model calculations of surface potential (ψ_s) as a function of V_{gb} for increasing oxide trapped charge density (N_{ot}) compared to extractions from 2-D TCAD simulations.

TABLE I
SUMMARY OF MODEL AND TCAD PARAMETERS FOR BULK MOS DEVICES

Paramete	Description	Value	Unit
t_{ox}	*Gate oxide thickness*	4	nm
N_a	*Doping concentration*	10^{18}	cm^{-3}
Φ_M	*Gate workfunction*	4.17	eV
n_i	*Intrinsic carrier concentration*	2.15×10^{10}	cm^{-3}
E_g	*Energy bandgap*	1.08	eV
κ_{ox}	*Oxide relative dielectric constant*	3.9 (SiO_2)	-
T	*Temperature*	300	K
W	*Gate width*	1	µm

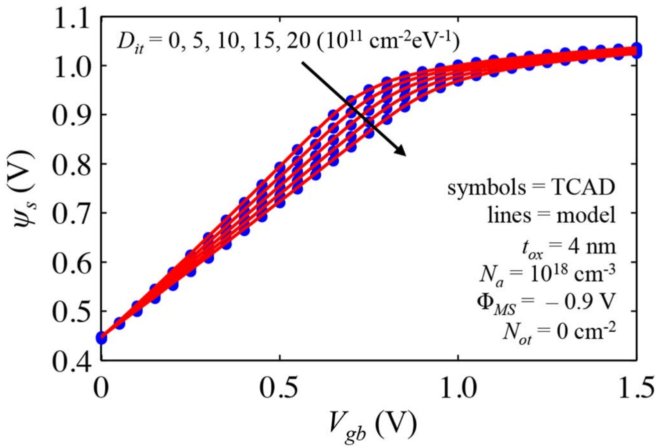

Fig. 5. Model calculations of surface potential (ψ_s) as a function of V_{gb} for increasing interface trap density (D_{it}) compared to extractions from 2-D TCAD simulations.

the impact of radiation-induced oxide trapped charge by comparing with TCAD. Similarly, Fig. 5 plots calculations of ψ_s as a function of V_{gb} and for increasing D_{it} setting $N_{ot} = 0$ cm^{-2}. The comparison in Fig. 5 shows this modeling methodology accurately represents the impact of interface traps on the $V_{gb}(\psi_s)$ characteristics.

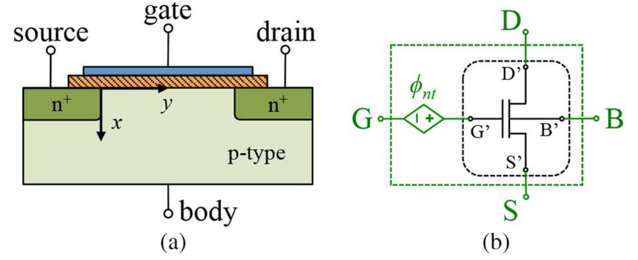

Fig. 6. (a) Cross-sectional diagram of a bulk MOSFET. (b) Sub-circuit schematic of model implementation using a VCVS that connects in series with the gate of the standard FET model (calculations of ψ_s and ϕ_{nt} done in a Verilog-A module).

To obtain the SPE for MOSFETs we first make use of the gradual channel approximation (GCA) that assumes the variation in the lateral field is much smaller than the transverse field (i.e., $|\partial^2\psi/\partial x^2| >> |\partial^2\psi/\partial y^2|$, cf. Fig. 6(a)) allowing using the 1-D Poisson's equation given by (4). However, the non-equilibrium condition due to current conduction requires treating the split due to a gradient in the minority carrier quasi-Fermi level. Making the necessary adjustments to account for ϕ_n in the minority carrier Boltzmann relation when solving the Poisson's equation results in

$$(u_g^* - u_s)^2 = G^* \left[e^{-u_s} + u_s - 1 + e^{-(2u_b+u_n)}(e^{u_s} - u_s - 1)\right], \quad (18)$$

where

$$u_g^* = \frac{u_g + q[\beta N_{ot} + D_{it}(u_b + u_n)]/C_{ox}}{\xi}. \quad (19)$$

The MOSFET SPE given by (18) allows solving for ψ_s along the channel by accounting for the minority carrier quasi-Fermi level gradient using $u_n = \beta\phi_n$. The surface potential at the source and drain ends of the channel (i.e., ψ_{ss} and ψ_{sd}) are computed by respectively setting ϕ_n to V_{sb} and V_{db} and can be used to calculate drain current (I_d) analytically through the CSM. The CSM calculations require some additional considerations to incorporate the charge contribution from N_{ot} and D_{it} as described in [35].

Fig. 7 plots CSM calculations of I_d as a function of V_{gb} for $V_{ds} = 0.1$ V, $V_{sb} = 0$ V and for increasing values of N_{ot} with $D_{it} = 0$ cm^{-2}eV^{-1}. Similarly, Fig. 8 plots calculations of I_d vs. V_{gb} for increasing values of D_{it} with $N_{ot} = 0$ cm^{-2}. I_d is computed using solutions of ψ_{ss} and ψ_{sd} obtained from (18) and compared to 2-D TCAD simulations of a MOSFET with $L = W = 1$ μm. All other parameters are the same as given in Table I. The comparisons in Figs. 7 and 8 serve as further verification that the presented modeling approach accurately describes the impact of radiation-induced defects on the *I-V* characteristics of bulk MOSFETs. Therefore, it can be incorporated into the formulation of surface-potential based compact models of MOSFETs for circuit-level simulations of TID effects. Alternatively, an implementation that is compatible with any compact modeling framework utilizes a voltage-controlled voltage

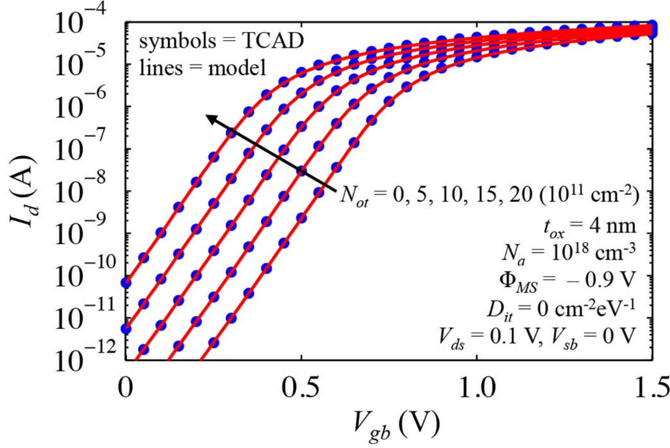

Fig. 7. CSM calculations of drain current (I_d) as a function of V_{gb} for increasing oxide trapped charge density (N_{ot}) compared to extractions from 2-D TCAD simulations.

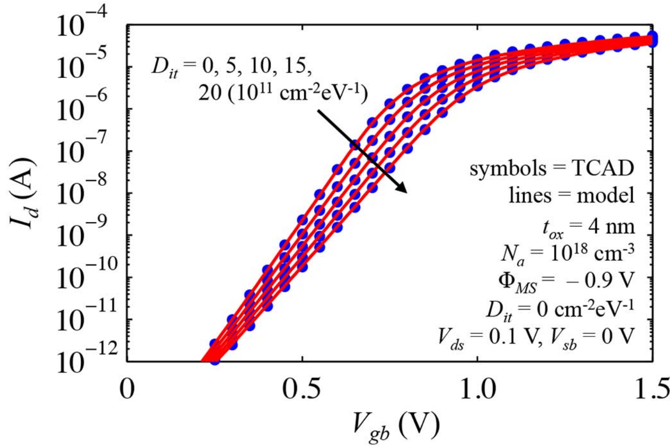

Fig. 8. CSM calculations of I_d as a function of V_{gb} for increasing D_{it} compared to extractions from 2-D TCAD simulations.

source (VCVS) in a sub-circuit "wrapper" that connects in series with the gate of the standard MOSFET. The VCVS accounts for the voltage shift due to TID effects as a function of bias and the defect densities (i.e., N_{ot} and D_{it}). This voltage shift is equivalent to the defect potential ϕ_{nt}. In this approach the calculations of ψ_s and $\phi_{nt}(\psi_s)$ can be performed inside a Verilog-A module that sets the supply voltage of the VCVS. Fig. 6(b) illustrates this methodology, and a SPICE-level demonstration using BSIM compact models can be found in [36], [37].

Aging effects attributed to NBTI and HC damage can result from a significant buildup of N_{ot} and D_{it} at the SiO_2/Si interface in modern CMOS technologies with thin gate oxides. For TID effects the buildup of defects is not significant in thin gate oxides and susceptibility to radiation-induced degradation results from damage (i.e., defect buildup) in thicker isolation oxide regions. The methodology described here can be applied to modeling the impact of stress-induced defects in thin gate oxides [36]–[38] as well as to modeling radiation-induced degradation in isolation oxide regions [35], [61]. For example, the work in [61] presents the implementation of this modeling approach into PSP for modeling radiation-induced degradation in field-oxide FETs (FOXFETs) to describe inter-device leakage in deep sub-micron CMOS technologies.

B. Silicon-on-Insulator (SOI) Devices

In SOI MOSFETs the buried oxide (BOX) region is susceptible to the buildup of radiation-induced defects. This can create a leakage path along the back surface of the Si body and can also affect the characteristics of the front surface through charge coupling under fully-depleted (FD) conditions [3], [4], [66]. SOI devices with thin Si bodies can transition between partially-depleted (PD) and fully-depleted (FD) conditions as a function of the terminal voltages and are said to operate in a dynamic depletion (DD) mode [67], [68]. The DD operation is well known and has been modeled analytically in [67]–[69]. The challenge related to TID effects is developing a new formulation that accounts for the impact of radiation effects defects under DD operation. The buildup of radiation-induced defects in the BOX can cause the transition between PD and FD conditions and consequently any modeling approach for TID effects in SOI devices must be compatible with DD operation. The model must also be suitable for compact modeling purposes without significant loss of accuracy required for SOI circuit simulations. Subsequently, we extend the surface-potential-based compact modeling approach to SOI devices by incorporating the impact of defect buildup in regions near the Si-BOX interface. This new formulation allows describing the impact of TID effects on the DD operation of SOI devices.

For SOI devices we start with the Poisson equation as expressed in (6), but now we integrate across the thickness of the thin Si body (i.e., between 0 and t_{si}, cf. Fig. 9)

$$E_x^2(0) - E_x^2(t_{si}) = -\frac{2qN_a}{\varepsilon_s}\int_{\psi(t_{si})}^{\psi(0)} [e^{-\beta\psi} - 1 - e^{-2\beta\phi_b}(e^{\beta\psi} - 1)]d\psi. \quad (20)$$

Integrating (20) gives

$$E_{sf}^2 - E_{sb}^2 = \left(\frac{2qN_a}{\beta\varepsilon_s}\right)[K(\beta\psi_{sf}) - K(\beta\psi_{sb})] \quad (21)$$

where

$$K(\beta\psi_s) = e^{-\beta\psi_s} + \beta\psi_s + e^{-2\beta\phi_b}(e^{\beta\psi_s} - \beta\psi_s). \quad (22)$$

In the above integration we have used the boundary conditions $\{E_x(0) = E_{sf}; \psi(0) = \psi_{sf}\}$ and $\{E_x(t_{si}) = E_{sb}; \psi(t_{si}) = \psi_{sb}\}$. E_{sf} and E_{sb} are the semiconductor electric field at the front and back surface respectively, ψ_{sf} and ψ_{sb} are the electrostatic potential at the front and back surface respectively. E_{sf} and E_{sb} are related to the front and back gate voltages (i.e., V_{GBf} and V_{GBb}) as given by

$$\varepsilon_s E_{sf} = C_{oxf}(V_{GBf} - \Phi_{MSf} - \psi_{sf}) \quad (23a)$$

$$\varepsilon_s E_{sb} = -C_{oxb}(V_{GBb} - \Phi_{MSb} + \phi_{ntb} - \psi_{sb}) \quad (23b)$$

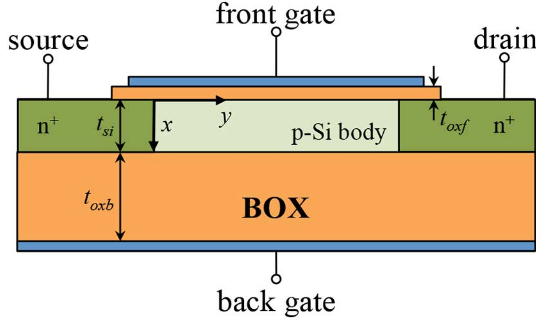

Fig. 9. Cross-sectional diagram of an SOI MOSFET.

where

$$\phi_{ntb} = \frac{q}{C_{oxb}}[N_{ot} - D_{it}(\psi_{sb} - \phi_b)]. \quad (24)$$

Combining (21)–(24) we obtain the SPE for DD SOI devices given by

$$(V_{GBf} - \Phi_{MSf} - \psi_{sf})^2 - \left(\frac{t_{oxf}}{t_{oxb}}\right)^2 (V_{GBb} - \Phi_{MSb} + \phi_{ntb} - \psi_{sb})^2 = \gamma^2\phi_t[K(\beta\psi_{sf}) - K(\beta\psi_{sb})]. \quad (25)$$

For simplicity (25) is normalized as

$$(u_{gf} - u_{sf})^2 - \zeta^2(u_{gb} + u_{ntb} - u_{sb})^2 = G[K(u_{sf}) - K(u_{sb})] \quad (26)$$

where $\zeta = t_{oxf}/t_{oxb}$, $u_{gf} = \beta(V_{GBf} - \Phi_{MSf})$, $u_{gb} = \beta(V_{GBb} - \Phi_{MSb})$, $u_{sf} = \beta\psi_{sf}$, $u_{sb} = \beta\psi_{sb}$, $u_{ntb} = \beta\phi_{ntb}$, and $G = \beta\gamma^2$. Solving for u_{sf} and u_{sb} requires a second equation describing the coupling between the front and back surfaces. This coupling equation is obtained assuming fully depleted conditions (i.e., neglecting the carrier charge) and integrating Poisson's equation resulting in

$$u_{sb} = u_{sf} - u_c - E_{sb}t_{si}/\phi_t. \quad (27)$$

In (27) $u_c = qN_a t_{si}^2/2\varepsilon_s\phi_t$ and from (23b) and (24) we obtain [4], [61]

$$u_{sb} = \frac{u_{sf} - u_c + \eta_c(u_{gb} + u_{nt0})}{1+\eta_c\xi_b}, \quad (28)$$

where $\eta_c = C_{oxb}/C_s$, $C_s = \varepsilon_s/t_{si}$, $u_{nt0} = (q/C_{oxb})(\beta N_{ot} + D_{it}u_b)$, and $\xi_b = 1 + qD_{it}/C_{oxb}$. In a PD condition the front and back surfaces are decoupled and $u_{sb} = u_{sb0}$ can be obtained independently by solving

$$\left(\frac{t_{oxf}}{t_{oxb}}\right)^2 (u_{gb} + u_{nt0} - \xi_b u_{sb0})^2 = \beta\gamma^2 H(u_{sb0}). \quad (29)$$

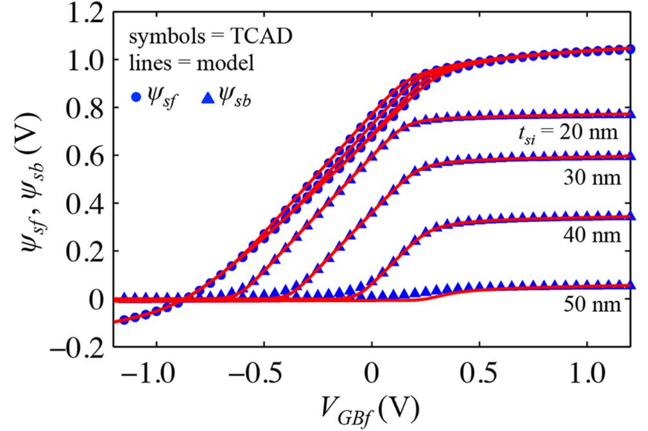

Fig. 10. Model calculations of front and back surface potential (ψ_{sf} and ψ_{sb}) as a function of the front gate voltage (V_{GBf}) compared to extractions from TCAD simulations of SOI devices with various Si body thicknesses (t_{si}). Other parameters are listed in Table II.

The transition between PD and FD conditions is described using a smoothing function to obtain a continuous expression relating the front and back surfaces given by [4], [67], [68]

$$u_{sb} = u_{sb0} + \ln\left\{1 + \exp\left[\frac{u_{sf} - u_c + \eta_c(u_{gb} + u_{nt0})}{1+\eta_c\xi_b} - u_{sb0}\right]\right\}. \quad (30)$$

Equations (26) and (30) are solved for the (normalized) front and back surface potentials u_{sb} and u_{sf} as a function of bias and the radiation-induced defect densities. Fig. 10 plots model calculations of ψ_{sf} and ψ_{sb} as a function of V_{GBf} compared to extractions from TCAD simulations of SOI structure with various Si body thicknesses. Parameters used in the model calculations and TCAD simulations are given in Table II. The transition from a PD to a FD condition occurs where ψ_{sb} changes from a constant $\psi_{sb0} \sim 0V$ (i.e., the decoupled PD value) to a V_{GBf}–dependent value (i.e., as a result of coupling) affecting the $V_{GBf}(\psi_{sf})$ characteristics. As shown in Fig. 10 reducing t_{si} lowers the V_{GBf} value at this transition as it becomes easier to fully deplete the thinner Si body with an applied front gate voltage. However, the value of ψ_{sb0} remains unchanged, as the back surface condition does not vary with t_{si} (for a fixed V_{GBb}) when the body is in PD conditions. However, charge contribution from radiation-induced trapped charge in the BOX and interface traps at the BOX/Si interface will affect the back surface condition when in PD and the transition from PD to FD conditions. Fig. 11 plots model calculations of ψ_{sf} and ψ_{sb} for increasing N_{ot} and D_{it} at the BOX/Si interface compared to TCAD for a fixed $t_{si} = 40$ nm. These results verify our modeling approach for describing the impact of radiation-induced defect buildup at the BOX/Si interface on the electrostatics of SOI structures.

From the model calculations of ψ_{sf} and ψ_{sb} we can obtain I_d using an analytical CSM for thin-film SOI MOSFETs as described in [70]. Fig. 12 plots I_d as a function of V_{GBf} obtained from the CSM using the model calculations plotted in Fig. 11 and from TCAD simulations. For the CSM calculations, the surface potential at the drain end is obtained by accounting for the

TABLE II
SUMMARY OF MODEL AND TCAD PARAMETERS FOR SOI CALCULATIONS/SIMULATIONS

Paramete	Description	Value	Unit
t_{oxf}	*Front gate oxide thickness*	2	nm
t_{oxb}	*Back gate oxide thickness*	200	nm
N_a	*Doping concentration*	5×10^{17}	cm^{-3}
Φ_{Mf}	*Front gate workfunction*	4.17	eV
Φ_{Mb}	*Back gate workfunction*	5.00	eV
n_i	*Intrinsic carrier concentration*	2.15×10^{10}	cm^{-3}
E_g	*Energy bandgap*	1.08	eV
κ_{ox}	*Oxide relative dielectric constant*	3.9 (SiO_2)	-
T	*Temperature*	300	K
W	*Gate width*	1	µm

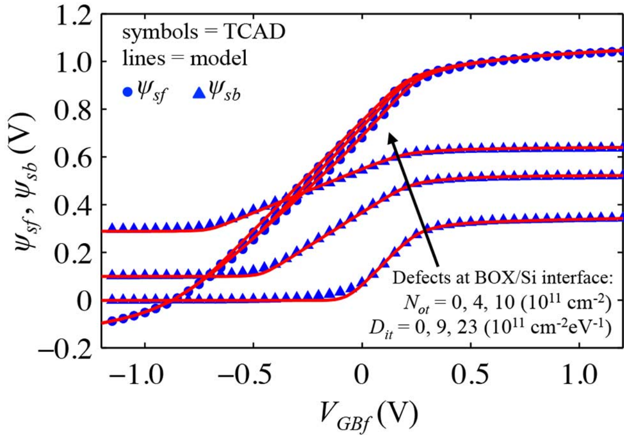

Fig. 11. Model calculations of ψ_{sf} and ψ_{sb} as a function of V_{GBf} for increasing N_{ot} and D_{it} at the BOX/Si interface compared to TCAD for $t_{si} = 40$ nm. Defect densities indicated on plot and other parameters are listed in Table II.

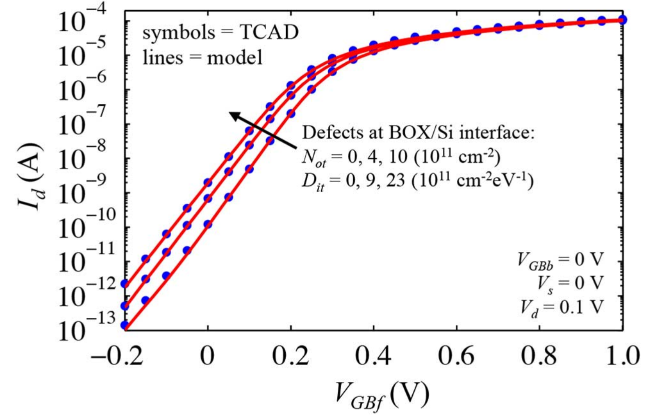

Fig. 12. Charge sheet model (CSM) calculations of I_d vs. V_{GBf} obtained using the modeled ψ_{sf} and ψ_{sb} plotted in Fig. 11 and compared to TCAD simulations for increasing N_{ot} and D_{it} at the BOX/Si interface.

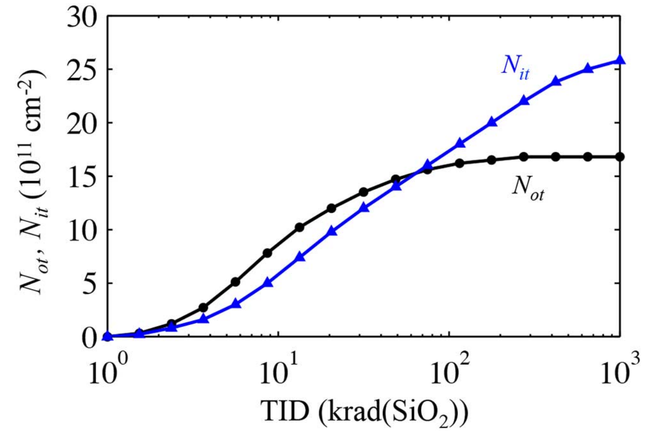

Fig. 13. N_{ot} and N_{it} values specified at the BOX/Si interface as a function of total ionizing dose (TID) used to demonstrate the modeling approach (see text).

split in the quasi-Fermi levels using $u_n = \beta\phi_n$, as was done for the bulk MOSFET. The results in Fig. 12 demonstrate the model effectiveness in describing the impact of radiation-induced defect buildup at the BOX/Si interface on the *I-V* characteristics through the well-known charge coupling effect in SOI devices. Further model verification and demonstration of this radiation-induced degradation mechanisms is obtained by comparing extractions of the front gate threshold voltage (V_{THf}) from TCAD simulations to model calculations as a function of N_{ot} and N_{it} at the BOX/Si interface. V_{THf} is defined as the V_{GBf} value at which $\psi_{sf} = 2\phi_b$ (i.e., at the onset of strong inversion) at the source end of the channel. To better demonstrate the modeling approach we specify the buildup of N_{ot} and D_{it} at the BOX/Si interface as a function of TID as plotted in Fig. 13. Using the defect densities specified in Fig. 13 we extract V_{THf} from TCAD simulations of SOI MOSFETs with various Si body thicknesses and compare them to model calculations. Fig. 14 plots the comparison of V_{THf} and the absolute value of the shift in V_{THf} (i.e., $|\Delta V_{THf}|$) as a function of TID and for $t_{si} = 20$, 30 and 40 nm. Excellent agreement is obtained between the model calculations and extractions from TCAD in capturing the dependence of V_{TH} on radiation-induced defects at the BOX/Si interface as a function of t_{si}. It should be noted that these results are consistent with recent experimental investigations and extractions of V_{THf} from irradiated FDSOI transistors [71] where an observed "turn around" in the threshold voltage shift indicates charge compensation from interface traps. The results in Fig. 14 reveal increased V_{THf} shifts from the coupling of radiation-induced charges at the BOX/Si interface in SOI devices with larger t_{si} when operating in a DD mode. However, this effect is restricted to a limited range of t_{si} (i.e., when in DD operation). Devices with large t_{si} will operate mostly under PD conditions with little impact on the front $V_{GBf}(\psi_{sf})$ characteristics, and devices with small t_{si} will operate under FD saturating the t_{si} dependence.

C. Short-Channel Effects (SCE)

Radiation and reliability studies typically interpret the impact of TID and aging mechanisms on the electrical characteristics of MOSFETs using shifts in threshold voltages without focusing on scaling properties or short-channel effects (SCE). It is important to also model the impact of TID-induced (or stress-induced) trapped charges and interface traps on the lateral position-dependence of the surface potential (ψ_s). This allows describing the impact of N_{ot} and D_{it} on SCE using the defect-based compact modeling techniques described above and provides insight

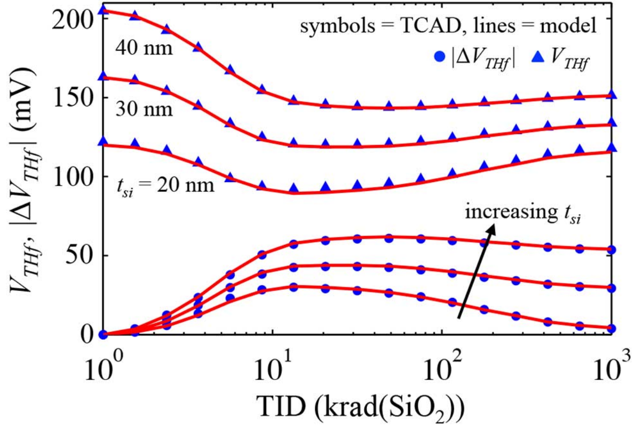

Fig. 14. Comparison of front gate threshold voltage (V_{THf}) and the absolute value of the shift in V_{THf} (i.e., $|\Delta V_{THf}|$) as a function of TID and for t_{si} = 20, 30 and 40 nm. These model calculations and TCAD simulations utilize the specified defect densities plotted in Fig. 13 as demonstration and validation of the modeling approach.

on the influence of radiation-induced defects on 2-D MOSFET electrostatics.

The following formulation incorporates N_{ot} and D_{it} into a SCE model that is based on solving Poisson's equation in the depletion approximation (i.e., in weak inversion) using analytical approximations for the 2-D electrostatic potential $\psi(x,y)$ (cf. Fig. 6(a)). In weak inversion (i.e., neglecting mobile carrier charge) the 2-D Poisson's equation is given by

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{qN_a}{\varepsilon_s}, \tag{31}$$

and the vertical component of the electrostatic potential can be approximated as [72]

$$\psi(x,y)=c_0(y)+c_1(y)x+c_2(y)x^2. \tag{32}$$

The coefficients in (32) are determined from the boundary conditions. For a bulk MOSFET the top and bottom boundary conditions (i.e., at the SiO_2/Si interface and at the edge of the depletion region w_d) give [73]

$$\psi(0,y)=c_0(y)=\psi_s(y), \tag{33a}$$

$$\left.\frac{\partial\psi(x,y)}{\partial x}\right|_{x=0}=c_1(y)=-E_s(y), \tag{33b}$$

$$\left.\frac{\partial\psi(x,y)}{\partial x}\right|_{x=w_d}=c_1(y)+2c_2(y)w_d=0. \tag{33c}$$

From the boundary condition on the normal component of the displacement at the SiO_2/Si interface (i.e., at $x=0$) given by (9) with Q_T given by (3) we obtain

$$E(x=0,y)=E_s(y)=\left(\frac{\varepsilon_{ox}}{\varepsilon_s t_{ox}}\right)[V_{gs}-\Phi_{MS}+\phi_{nt}(y)-\psi_s(y)], \tag{34}$$

Using (34) we obtain the coefficients c_0, c_1 and c_2 as determined by (33) and express $\psi(x,y)$ using (32) as

$$\psi(x,y)=\psi_s(y)+\left(x-\frac{x^2}{2w_d}\right)\left(\frac{\varepsilon_{ox}}{\varepsilon_s t_{ox}}\right)[\psi_s(y)-V_{gs}+\Phi_{MS}-\phi_{nt}(y)]. \tag{35}$$

Substituting (35) into (31), carrying out the differentiation, and setting $x=0$ results in

$$\frac{\partial^2\psi_s(y)}{\partial y^2}-\frac{\psi_s(y)(1+\chi)-\chi(\phi_b+\phi_n)-V_0}{\lambda^2}=0. \tag{36}$$

In (36), $V_0=V_{gs}-V_{fb}-qN_a\lambda^2/\varepsilon_s$, $V_{fb}=\Phi_{MS}-qN_{ot}/C_{ox}$, $\chi=qD_{it}/C_{ox}$, and λ is commonly referred to as the characteristic scaling length and is given by $\lambda=(\varepsilon_s t_{ox}w_d/\varepsilon_{ox})^{1/2}$.

Equation (36) is an analytical simplification of (31) into a one-dimensional (1-D) problem described by a second-order ordinary differential equation that *includes the influence of stress-induced oxide-trapped charge and interface traps*. As described in detail in a previous work [38], further analysis allows obtaining a closed-form solution for $\psi_s(y)$ given by

$$\psi_s(y)=\frac{\varphi_s\sinh[(L-y)/\lambda_T]+\varphi_d\sinh(y/\lambda_T)}{\sinh(L/\lambda_T)}+\eta\chi(\phi_b+Ky^2+V_{sb})+\eta V_0+2\eta\chi K\lambda_T^2. \tag{37}$$

In (37), $\varphi_s=\varphi(0)=\psi_s(0)-\eta[\chi(\phi_b+V_{sb})+V_0]$ and $\varphi_d=\varphi(L)=\psi_s(L)-\eta[\chi(\phi_b+V_{db})+V_0]$, where the boundary conditions on ψ_s at the source and drain are respectively given by $\psi_s(0)=V_{bi}+V_{sb}$ and $\psi_s(L)=V_{bi}+V_{db}$, and V_{bi} is the built-in junction potential. Also, $\eta=1/(1+\chi)$, $\lambda_T=(\lambda)(\eta)^{1/2}$, and $K=V_{ds}/L^2$.

Fig. 15 plots calculations of φ_s along the channel using (37) and compared to TCAD simulations for $D_{it}=0$, 2 and 4×10^{12} cm^{-2} eV^{-1} and for $L=90$ nm. Other parameters are listed in the figure caption. For the calculations in Fig. 15, $V_{ds}=1.0$, $V_{bs}=0$, and $V_{gs}=V_{th0}$ where V_{th0} is the gate voltage for which the minimum ψ_s along the channel (i.e., ψ_{smin}) equals $2\varphi_b$ when $V_{ds}=0V$. Therefore, these calculations demonstrate the impact of interface traps on the potential barrier at the onset of strong inversion. The inset in Fig. 15 shows a closer view of the comparison near $2\phi_b$ demonstrating that the model not only predicts the change in the V_{gs} at which $\psi_{smin}=2\varphi_b$, but also the location of ψ_{smin} along the channel. Oxide-trapped charge by itself only causes an offset in the onset of strong inversion (i.e., a shift in V_{th}) but does not change the lateral potential profile or the location of ψ_{smin}. Therefore, N_{ot} by itself does not impact the SCE (i.e., when N_{ot} is uniform along the channel). As pointed out in [38], this might allow for a characterization technique that separates the radiation-induced buildup of N_{ot} and D_{it}.

The impact of interface traps on the SCE results from the position dependence of their charge contribution. ψ_{smin} determines the onset of strong inversion, and is shifted towards the source side for increasing D_{it} causing a gradient in ψ_s. The increasing gradient of ψ_s indicates a larger contribution from

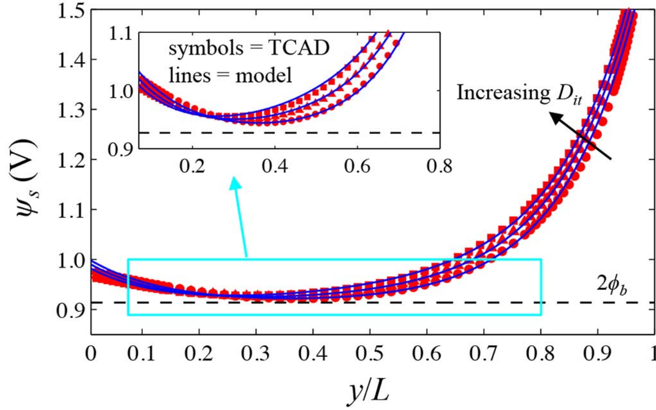

Fig. 15. Calculations of ψ_s from (37) compared to TCAD simulations. $D_{it} = 0, 2, 4 \times 10^{12}$ cm^{-2}eV^{-1}, $V_{bs} = 0$ V, $V_{ds} = 1$ V, $V_{gs} = V_{th0}(D_{it})$, $N_a = 10^{18}$ cm^{-3}, $L = 90$ nm, $W = 1$ μm, $t_{ox} = 2$ nm, $\Phi_{MS} = -0.7$ V, $\varepsilon_s/\varepsilon_0 = 11.7$, $\varepsilon_{ox}/\varepsilon_0 = 3.9$.

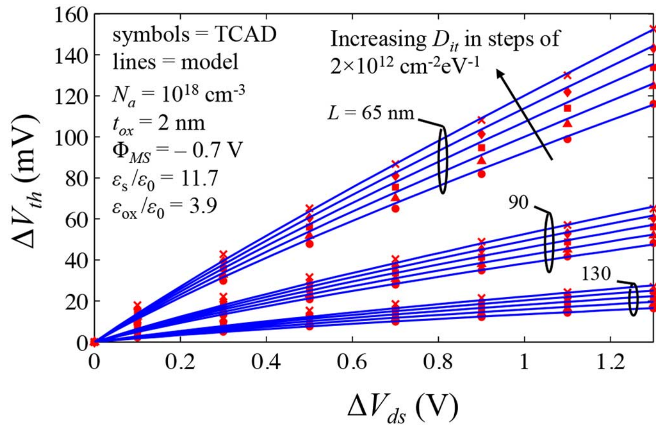

Fig. 16. Calculations of ΔV_{th} vs. ΔV_{ds} (i.e., $V_{ds} - V_{ds0}$, where $V_{ds0} = 0.1$ V) compared to TCAD simulations using increasing values of D_{it} and for $L = 130$ nm, 90 nm and 65 nm.

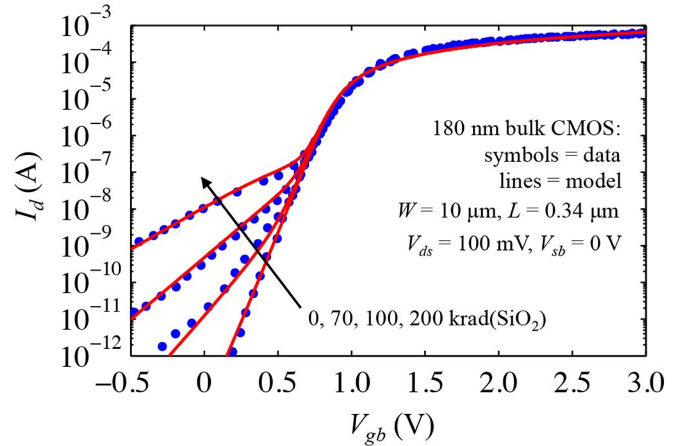

Fig. 17. I_d vs. V_{gb} measurements (symbols) of an n-channel MOSFET from a 180 nm bulk CMOS process for increasing dose of ionizing radiation [74] compared to model calculations (lines).

the lateral field in determining the electrostatics of the channel region resulting in an enhancement of the SCE. Shifts in the gate voltage at the onset of strong inversion (i.e., ΔV_{th}) are calculated from (37) as a function of V_{ds}, L, and D_{it} using $\psi_{smin} = 2\phi_b$. Fig. 16 plots calculations of ΔV_{th} as a function of V_{ds} that result from drain-induced barrier lowering (DIBL) for various L and D_{it}. The calculations are compared to extractions from TCAD simulations (symbols) with good qualitative agreement. These results verify the modeling approach and demonstrate the impact of interface traps on MOS electrostatics and SCE in terms of ΔV_{th}.

IV. Discussion

A. Comparison with Experimental Data

This section presents further verification of the modeling approach through fits to experimental *I-V* characteristics from various CMOS devices exposed to ionizing radiation. For this verification, surface potentials are solved analytically from the formulations presented in Section III and utilized in CSM calculations of I_d. This verification is useful for demonstrating the applicability of the presented modeling approach for incorporating TID effects into compact models that utilize calculations of surface potential for obtaining terminal currents and charges. Calculations of surface potential can also be directly used to analyze and model the impact of TID and/or stress-induced defects on device parameters (e.g., as shown in Figs. 14 and 16). The following verification considers the parasitic "edge" device that results from the buildup of defects in the shallow trench isolation (STI) oxide regions near the channel and operates in parallel to the main device; a field-oxide FET (FOXFET) that results from degradation of the STI oxide and can be used to model inter-device leakage in deep sub-micron bulk CMOS technologies; finally a planar FDSOI MOSFET with radiation-induced defect buildup in the thick BOX.

Fig. 17 plots I_d vs. V_{gb} measurements (symbols) of an n-channel MOSFET from a 180 nm bulk CMOS process for increasing ionizing dose [74] compared to model calculations (lines). The increase in I_d as a function of TID at low gate voltages (i.e., for V_{gb} $<\sim$ 0.5 V) indicates current leakage that results from the activation of a parasitic "edge" device. The thin gate oxide in the active region of the main device does not buildup significant radiation-induced defects. This is determined from the convergence of the I_d measurements at gate voltages where the main device is turned on and its contribution to I_d dominates (e.g., for V_{gb} $>\sim$ 0.5 V). Therefore, our modeling approach can be utilized to describe the radiation response of the parasitic edge transistor and assumes that the main device does not degrade significantly with ionizing radiation. The parasitic device will respond to the buildup of N_{ot} and D_{it} as a function of TID and is modeled as a transistor operating in parallel using an effective oxide thickness, channel width, and doping density. The parallel combination of the parasitic and main devices can be used for modeling TID effects in MOSFETs from bulk CMOS technologies that are susceptible to edge leakage using calculations of surface potentials and terminal currents continuously from weak to strong inversion as a function of TID.

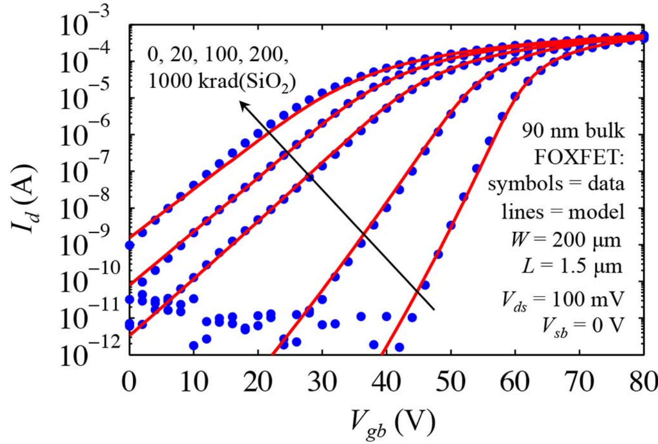

Fig. 18. Measurements of I_d vs. V_{gb} from an n-channel FOXFET fabricated in a 90 nm bulk CMOS process [35] and model fits based on CSM calculations of I_d vs. V_{gb} as a function of N_{ot} and D_{it}.

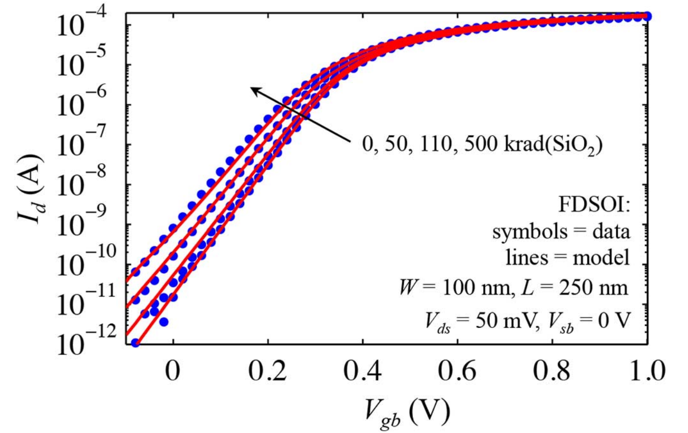

Fig. 19. Measurements (symbols) and model calculations (lines) of I_d vs. V_{gb} for an SOI MOSFET as a function of ionizing radiation [4].

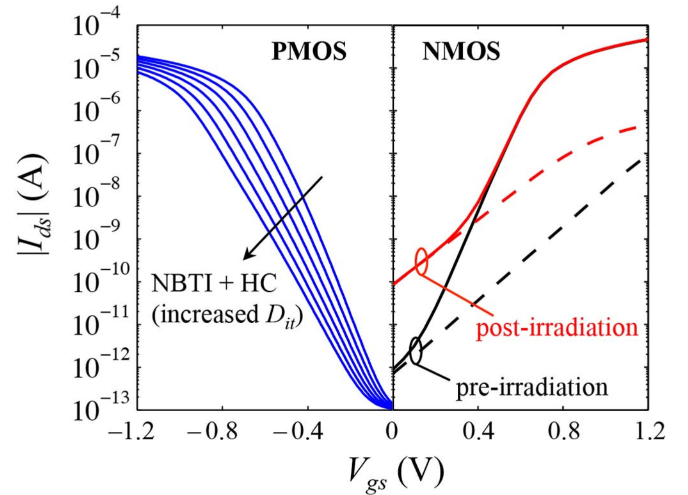

Fig. 20. Spice simulations of PMOS and NMOS I-V characteristics incorporating the impact of NBTI + HC and TID effects respectively. The dashed line corresponds to the simulated NMOS radiation-induced edge parasitic devices.

FOXFETs can be used to characterize defect buildup in STI oxides and analyze the susceptibility of bulk CMOS technologies to radiation-induced inter-device leakage [35], [75]. Inter-device leakage is associated to a conduction path along the base of the STI oxide between n-wells or adjacent p-channel devices. Fig. 18 plots measurements of I_d vs. V_{gb} from an n-channel FOXFET fabricated in a 90 nm bulk CMOS process. Also shown in Fig. 18 are fits based on CSM calculations of I_d vs. V_{gb} as a function of N_{ot} and D_{it}. The model fits indicate the buildup of oxide trapped charge and interface traps in the STI oxide and can be used to extract their densities.

Fig. 19 compares measurements (symbols) and model calculations (lines) of I_d vs. V_{gb} for an SOI device as a function of ionizing radiation [4]. This device has $t_{si} = 40$ nm, $t_{oxf} = 2$ nm, and $t_{oxb} = 150$ nm so defect buildup is expected to be significant in the thick BOX but negligible in the thin gate oxide. Therefore, the measured shifts in the I-V characteristics are a result of charge coupling between the front and back gates as a function of N_{ot} and D_{it} buildup in the BOX/Si interface. This is a well-known TID effect in FDSOI devices that was demonstrated with TCAD and model calculations in Section III. The model fits in Fig. 19 are obtained from calculations of surface potential described in Section III-B and serve as further verification of our modeling approach to describe charge coupling effects as a function of TID in SOI devices.

B. Circuit Simulation and Modeling Demonstration

This section presents a demonstration of SPICE simulations that incorporate TID and stress-induced effects in NMOS and PMOS devices and describe their impact at the circuit level. This demonstration serves as further validation of the proposed modeling approach and presents a methodology for studying the combined impact of TID and aging effects in ICs using commercial simulation tools and standard MOSFET compact models. We study the impact of TID and aging effects on the subthreshold operation of a static random-access memory (SRAM) cell. Ionizing radiation effects are incorporated as increased edge leakage in the NMOS devices resulting from the buildup of N_{ot} and D_{it} along the sidewalls of the isolation oxides near the active region. This is modeled as a parasitic edge device conducting in parallel with the main channel of the transistor. Edge leakage is not included for PMOS devices since the radiation-induced buildup of N_{ot} and D_{it} would increase the threshold for parasitic conduction. Therefore the contribution of parasitic edge leakage would not increase with ionizing radiation for PMOS devices. Instead, we model stress-induced trap buildup at the Si/SiO_2 gate-oxide interface of PMOS devices attributed to the permanent component of NBTI and HC aging effects. Fig. 20 plots Spice simulations of PMOS and NMOS I-V characteristics incorporating the impact of NBTI + HC and TID effects respectively. These simulations were performed with Synopsys H-Spice using a BSIM 4.3 MOSFET compact model template representative of a bulk CMOS process. Radiation-induced shifts in the NMOS parasitic edge devices characteristics, and stress-induced shifts in the PMOS devices are introduced as a function of N_{ot} and D_{it} using a VCVS as described in Section IIIA and illustrated in Fig. 6(b). The following analysis incorporates the simulated impact of aging and TID effects that are shown in Fig. 20 on

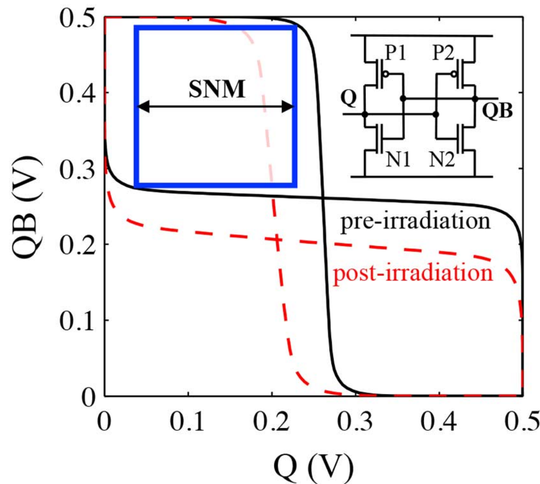

Fig. 21. Simulation of SRAM cell mirrored inverter voltage transfer characteristics (VTC) before and after incorporating the effects of ionizing radiation (i.e., increased NMOS edge-leakage). Inset shows the SRAM cell schematic.

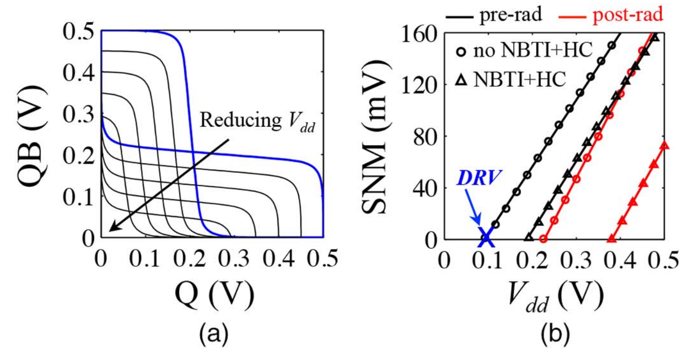

Fig. 22. (a) SRAM mirrored inverter VTC for stepped values of the supply voltage (V_{dd}) ranging from 0.5 V to 0.3 V. (b) Extractions of SNM as a function of V_{dd} before and after incorporating TID and aging effects in the simulations.

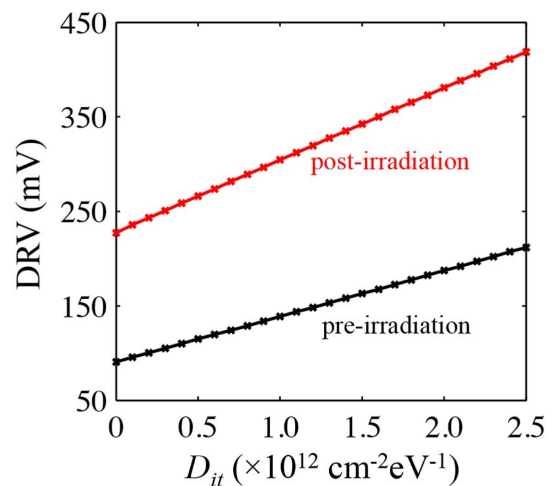

Fig. 23. Extractions of the minimum data rentention voltage (DRV) as a function of PMOS stress-induced trap buildup obtained from simulations before and after incorporating TID effects as edge leakage in NMOS devices.

the static noise margin (SNM) and the minimum data retention voltage of an SRAM cell.

Fig. 21 shows simulations of an SRAM cell plotting the mirrored inverter voltage transfer characteristics (VTC) before and after the incorporation of ionizing radiation effects (i.e., increased edge leakage in NMOS devices as shown in Fig. 20) and for a supply voltage of $V_{dd} = 0.5$ V. The inset in Fig. 21 shows the schematic of the simulated SRAM cell. As illustrated in Fig. 21, the SNM can be extracted as the side length of the largest square that can be nested in the mirrored inverter VTC and is obtained from the simulations using a transformed coordinate system as described in [76]. The SNM can be obtained as a function of V_{dd} by reducing the supply voltage in the simulations. Fig. 22(a) plots the simulated mirrored inverter VTC (post-irradiation) for a stepped reduction of V_{dd} ranging from 0.5 V to 0.3 V. Extractions of the SNM are plotted as a function of V_{dd} in Fig. 22(b) before and after incorporating TID and aging effects in the simulations. The post-rad results in Fig. 22(b) correspond to the post-irradiation *I-V* characteristics of NMOS devices in Fig. 20, while the NBTI + HC results correspond to including a stress-induced trap density of $D_{it} = 2 \times 10^{12}$ cm^{-2}eV^{-1} for PMOS device P1. The results in Fig. 22(b) show that radiation-induced edge leakage in the NMOS devices reduces the SNM for a fixed V_{dd}, and also enhances the impact of stress-induced trap buildup on the stability of the SRAM cell.

The minimum data retention voltage (DRV) of an SRAM cell is defined as the minimum V_{dd} for which data stored in the cell can be preserved. A low DRV is essential for standby mode, dynamic voltage scaling (DVS), low power, and subthreshold SRAM operation [77]–[81]. Additionally, accurately modeling the impact of TID and aging effects on the DRV is essential for high-reliability applications in radiation environments. From the simulations, DRV is extracted at the x-intercept of the SNM vs. V_{dd} characteristics as indicated in Fig. 22(b) (i.e., at SNM = 0). Fig. 23 plots extractions of DRV as a function of PMOS stress-induced interface trap buildup, before and after incorporating TID-induced edge leakage in the simulations. The results in Fig. 23 demonstrate an increased DRV after incorporating NMOS radiation-induced parasitic edge leakage even before adding PMOS stress-induced interface trap buildup (i.e., NBTI + HC). The degradation (i.e., increase) of the DRV due to aging effects, simulated with increased PMOS interface-trap buildup, is enhanced with TID-induced edge leakage as indicated by the increased slope in the DRV vs. D_{it} characteristics plotted in Fig. 23.

The presented analysis of SRAM subthreshold operation describes the combined impact of TID and aging effects on the SNM and minimum data retention voltage. A degradation of the SRAM cell stability is identified through the reduction in SNM following the incorporation of radiation-induced edge leakage in NMOS devices. TID also enhance the impact of NBTI and HC aging effects on the stability and retention voltage of the SRAM cell. This circuit-level demonstration serves as an example and justification of the need for an accurate modeling approach that can simultaneously capture the impact of TID and stress-induced defects on the device characteristics for all regions of operation.

V. Conclusions

We have presented the detailed formulation and demonstration of a physics-based compact modeling approach for total ionizing dose (TID) and aging effects in bulk and SOI MOSFETs. This modeling approach incorporates the charge contribution from interface traps and oxide trapped charge into expressions of electric field at the semiconductor/oxide interface that are used as boundary conditions when solving the Poisson's equation. The resulting surface potential equation (SPE) allows calculating the surface potential (ψ_s) as a function the radiation and/or stress-induced defects, and to smoothly and accurately describe the radiation response of MOS devices from weak to strong inversion for equilibrium and non-equilibrium conditions. The presented modeling approach is compatible with standard surface-potential-based compact models of bulk and SOI MOSFETs. As described in Section III, calculations of ψ_s are used to obtain currents and terminal charges in standard surface-potential-based compact models of MOSFETs (e.g., PSP). The incorporation of radiation and stress-induced defects into the SPE allows investigating and modeling the impact of TID and aging effects in MOS devices and ICs from calculations of surface potential as a function of the defect densities. Calculations of ψ_s can also be used to analyze and predict shifts in device-level parameters used to describe the electrical characteristics of MOS devices (e.g., V_{th}) as a function of ionizing radiation exposure or stress. This helps interpreting experiments, supports the development of radiation-hardening methodologies, and allows modeling the long-term response of devices and ICs in radiation environments.

The modeling approach presented in this paper is verified using two-dimensional TCAD simulations of bulk and SOI devices. The verification is obtained through the comparison of model calculations and TCAD extractions of ψ_s and drain currents as a function of the terminal voltages and the defect densities. For this comparison, drain current is obtained from the charge sheet model (CSM) using the calculations of ψ_s for various densities of trapped charge and interface traps. Further verification and demonstration of the modeling approach is provided by model fits to experimental *I-V* characteristics of irradiated bulk and SOI devices. This verification considers a standard MOSFET a field-oxide FET (i.e., a FOXFET) and a thin Si-film SOI device. For a bulk MOSFET with a thin gate oxide, the radiation response is dominated by parasitic "edge" leakage that results from buildup of defects in the sidewalls of the STI oxide near the main conducting channel. This parasitic leakage path is modeled as a transistor operating in parallel to the main device using an effective (i.e., averaged) channel width, oxide thickness and doping concentration resulting in excellent agreements with experimental data. The comparison of model calculations with degraded *I-V* characteristics from measurements of FOXFETs also results in good fits for all regions of operation further demonstrating the model generality. The modeling approach is also applied to SOI devices and verified through the comparison with the radiation response in thin-film SOI MOSFETs. This comparison verifies the capability of the modeling approach in describing charge coupling mechanisms as a function of TID for SOI devices operating in a dynamic depletion mode (i.e., transitioning between PD and FD operation).

Finally, we present a circuit-level demonstration of the modeling approach using SPICE simulations that incorporate radiation and stress-induced defects in NMOS and PMOS devices. This demonstration investigates the impact of TID and aging effects on the subthreshold operation of static random-access memory (SRAM) cells. Degradation of the SRAM cell stability is determined from a reduction in the SNM due to radiation-induced edge leakage in NMOS devices. Additionally, radiation-induced leakage enhances the impact of aging effects on the stability and minimum data retention voltage (DRV) of SRAM cells. The circuit-level demonstration establishes the advantage of a modeling approach that can simultaneously capture the impact of TID and stress-induced defects on the device characteristics accurately and smoothly for all regions of operation (i.e., from weak to strong inversion).

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