# $1/f$ Noise and Defects in Microelectronic Materials and Devices

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***Abstract*—This paper reviews and compares predictions of the Dutta-Horn model of low-frequency excess ($1/f$) noise with experimental results for thin metal films, MOS transistors, and GaN/AlGaN high-electron mobility transistors (HEMTs). For metal films, mobility fluctuations associated with carrier-defect scattering lead to $1/f$ noise. In contrast, for most semiconductor devices, the noise usually results from fluctuations in the number of carriers due to charge exchange between the channel and defects, usually at or near a critical semiconductor/insulator interface. The Dutta-Horn model describes the noise with high precision in most cases. Insight into the physical mechanisms that lead to noise in microelectronic materials and devices has been obtained via total-ionizing-dose irradiation and/or thermal annealing, as illustrated with several examples. With the assistance of the Dutta-Horn model, measurements of the noise magnitude and temperature and/or voltage dependence of the noise enable estimates of the energy distributions of defects that lead to $1/f$ noise. The microstructure of several defects and/or impurities that cause noise in MOS devices (primarily O vacancies) and GaN/AlGaN HEMTs (e.g., hydrogenated impurity centers, N vacancies, and/or Fe centers) have been identified via experiments and density functional theory calculations.**

***Index Terms*—Border traps, gallium nitride, HEMTs, interface traps, low-frequency noise, MOS devices, noise, oxide traps, radiation response, silicon carbide.**

## I. Introduction

GREAT progress has been made in the last $\sim$ 35 years in understanding the links between low-frequency ($1/f$) noise and defects in microelectronic materials and devices [1]–[10]. Since 1937, it has been known that a thermally-activated random process with a uniform distribution of energies can lead to $1/f$ noise [11]. In 1957, A. L. McWhorter modeled the $1/f$ noise of semiconductors as carrier number fluctuations caused by the tunneling of electrons in and out of surface states [12]. A breakthrough in 1979 was achieved by Dutta, Dimon, and Horn, who developed a method to infer defect energy distributions from low-frequency noise measurements as a function of temperature [1], [13]. This technique was applied first to assist the understanding of the noise of thin metal films [1]–[3], [13]–[23], and then to analyze the noise of Si- and compound-semiconductor-based microelectronic devices and materials [2], [10], [24]–[34].

In this paper the principles that underlie the Dutta-Horn model of $1/f$ noise are briefly reviewed, and examples are shown that verify its applicability to metal films. The model describes changes in the magnitude, temperature dependence, and frequency dependence of the noise of devices with high defect densities annealed at elevated temperature, as well as the noise of metal films subjected to ionizing radiation. These results provide strong evidence that the noise of most metal films is caused by thermally-activated carrier-defect interactions that lead to fluctuations in the mobility of the carriers. Exceptions to this general agreement between experimental data and the Dutta-Horn model are noted primarily for films (e.g., Ni, Cr) in which magnetic interactions dominate over defect scattering [18], [19], [23].

An extensive series of comparisons of the predictions of the Dutta-Horn model are also presented for Si and SiC based MOS transistors and GaN/AlGaN HEMTs. Again, the Dutta-Horn model describes the temperature and frequency dependence of the noise remarkably well [24]–[34]. Overwhelming evidence confirms that the dominant source of noise in semiconductor devices is the thermally activated interaction of carriers with defects. To first order, the noise is caused by carrier number fluctuations, and not lattice scattering (mobility fluctuations). The Dutta-Horn model can be used to infer energy distributions for defects responsible for the noise. To within parametric and experimental uncertainties, these estimates are consistent with estimates of defect densities obtained via other measurement techniques. In several cases, density functional theory calculations provide insight into the microstructures of the defects responsible for the noise in semiconductor devices. A brief discussion of the noise of bipolar junction transistors is also presented.

## II. Background

Any resistive system exhibits noise. Two well understood examples are thermal noise (also known as Johnson noise or Nyquist noise) and shot noise. Thermal noise results from the Brownian motion of charge at any finite temperature. The voltage noise power spectral density of thermal noise $S_{Vt}$ (in units of $V^2/Hz$) depends only on the absolute temperature $T$, resistance $R$, and frequency $f$, as reported and explained theoretically in back-to-back papers published in the *Physical*

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*Review* by Johnson [35] and Nyquist [36] in 1928. For a resistor of any size, shape, or composition,

$$S_{Vt} = 4hfR[\mathrm{e}^{(hf/kT)} - 1]^{-1}. \quad (1)$$

Here $h$ is the Planck constant and $k$ is the Boltzmann constant. When $hf << kT$, e.g., for frequencies below the microwave region ($f \leq\sim 10^{12}$Hz) and temperatures that are not deeply cryogenic (T $\geq\sim$ 10 K), this expression simplifies to:

$$S_{Vt} = 4kTR. \quad (2)$$

Thus, over a broad range of temperatures and frequencies, thermal noise is independent of $f$; i.e., it is a "white noise."

Thermal noise is present regardless of whether current flows. There is also noise associated with current flow that is present any time charge carriers are emitted from a cathode or cross a potential barrier [37], [38]. This "shot noise" results from the Poisson distribution of waiting times $\tau$ before emission or barrier crossing, as demonstrated by Schottky in 1918 [39]. The current noise power spectral density $S_I$ (in units of $\mathrm{A}^2/\mathrm{Hz}$) of the resulting fluctuations is:

$$S_I = 2qI(1 + \omega^2\tau^2)^{-1}. \quad (3)$$

Here $I$ is the current, $-q$ is the electronic charge, and $\omega = 2\pi f$. At high frequencies ($\omega >> 1/\tau$), $S_V$ is proportional to $1/f^2$ for shot noise, which is a spectrum of Lorentzian form [37], [38]. For $f <\sim$ 1 THz, $S_I = 2qI$, which is again white noise.

When current is passed through a resistor, it is often found that, in addition to the thermal noise and shot noise, there is an "excess noise" with magnitude $S_V$, and frequency dependence $\sim 0.7 < \alpha <\sim 1.3$ [1]–[4], [37], [38], [40], where:

$$\alpha = -\frac{\partial \ln S_V}{\partial \ln f}. \quad (4)$$

Here $S_V$ is the excess noise after the thermal noise $S_{Vt}$ is subtracted. For an ohmic system, as is the case for all examples considered in this paper, $S_V/V^2 = S_I/I^2$; equivalently, $S_V = S_I R^2$.

$1/f$ noise was observed first in vacuum tubes by Johnson in 1925 [41]. Eq. (3) shows that a random process with a single characteristic time $\tau$ does not lead to $1/f$ noise. However, Bernamont showed in 1937 [42] that, if the noise results from processes with a distribution of characteristic times $D(\tau)$, and $D(\tau) \sim 1/\tau$ for times $\tau_1 < \tau < \tau_2$, and the pre-factor $A$ is independent of frequency, then the resulting noise,

$$S_V = A\int [D(\tau)(1 + \omega^2\tau^2)^{-1}]d\tau, \quad (5)$$

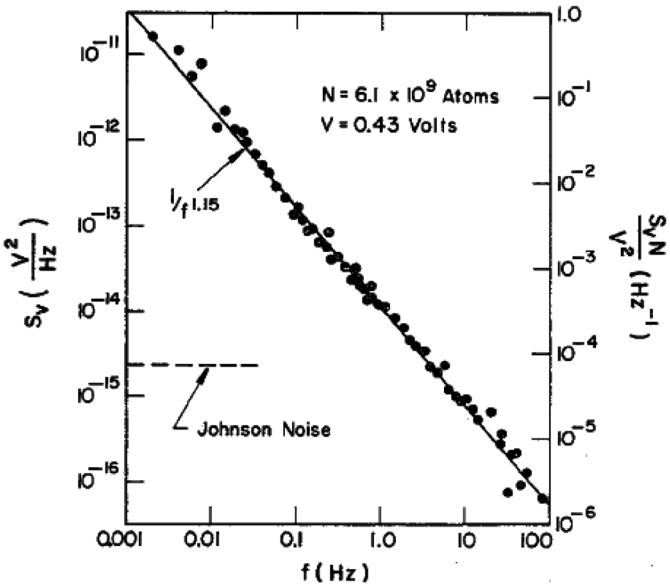


Fig. 1. Excess voltage-noise power spectral density $S_V$ (left hand scale) and normalized noise magnitude $S_V N/V^2$ (right hand scale; N is the number of atoms and $V$ is the voltage) as a function of frequency $f$ for a platinum nanowire. The Johnson (thermal) noise level for this wire is indicated, and subtracted to obtain the excess noise. (After [43], © 1983, American Institute of Physics, AIP).

is proportional to $\sim 1/f$ for $1/\tau_2 < f < 1/\tau_1$ [11], [37], [42]. If the noise results from a random, thermally activated process, for which

$$\tau = \tau_o \exp(E/kT), \quad (6)$$

where $\tau_o$ is a constant and $E$ is the activation energy, then when $D(E)$ is nearly constant, $D(\tau)$ is proportional to $\sim 1/\tau$, and $1/f$ noise is observed [37], [42]. For most electronic systems, it is difficult to determine $D(\tau)$ and/or $D(E)$ via methods other than noise measurements. Moreover, until the work of Dutta and Horn [1], [14], inferring energy distributions from noise measurements was either not possible or required a series of ad hoc assumptions. However, the method of Dutta and Horn enables significant insight to be obtained into the dynamics of the microscopic processes that lead to $1/f$ noise, as we now demonstrate for metals and semiconductor devices.

## III. Thin Metal Films and Wires

The low frequency noise of a platinum nanowire, measured at room temperature, is shown in Fig. 1. Here $S_V \sim 1/f^{1.15}$ for 0.002 Hz $< f <$ 100 Hz [43]. The low frequency limit in Fig. 1 is determined by measuring time, and the high frequency limit is determined by the relative magnitudes of the $1/f$ noise and thermal noise. The noise magnitude increases inversely with decreasing sample volume ($\sim 1/N_A$, where $N_A$ is the number of atoms, which for metals is approximately equal to the number of carriers $N_c$) and with increasing voltage ($\sim V^2$) [38], [43].

The magnitude and frequency dependence of the noise of metal films can vary strongly with temperature [1], [13], [14]. Dutta and Horn demonstrated that, if the noise is caused by a random thermally activated process having a broad distribution

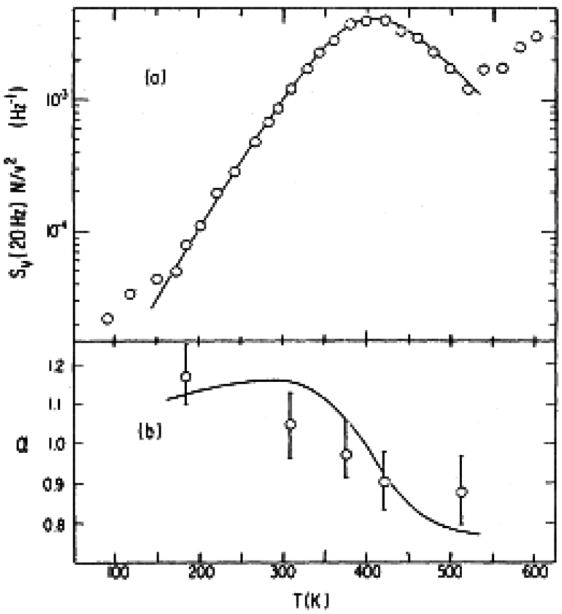


Fig. 2. (a) Normalized noise magnitude at $f = 20$ Hz as a function of measurement temperature for an 80-nm thick Ag film. (b) Measured and predicted values of the frequency dependence of the noise, $\alpha = -\partial \ln S_V / \partial \ln f$ using the experimental results from (a) and Eq. (7) of the text. (After Dutta, Dimon, and Horn [14], © 1979, AIP).

of energies relative to $kT$, not necessarily an approximately constant $D(E)$, the frequency and temperature dependences of the noise are correlated via [1], [14]:

$$\alpha(\omega, T) = 1 - \frac{1}{\ln(\omega\tau_0)} \left( \frac{\partial \ln S_V(T)}{\partial \ln T} - 1 \right). \tag{7}$$

Here $\tau_o$ is the characteristic time of the process leading to the noise. This is typically associated with scattering by defects. For details of the derivation of (7), and/or alternative formalisms that lead to similar correlation, please see [1], [2], and [18]. For noise that is successfully described by Eq. (7), one can infer the shape of the defect-energy distribution $D(E_o)$ from noise measurements versus temperature via:

$$D(E_0) \propto \frac{\omega}{kT} S_V(\omega, T) \tag{8}$$

where the defect energy is related to the temperature and frequency through the simple expression [1], [14]:

$$E_o \approx -kT \ln(\omega\tau_o). \tag{9}$$

If the noise is the result of thermally activated processes involving two energy levels, for example, $E_o$ is the barrier that the system must overcome for the system to move from one configurational state to the other [1], [2].

Dutta and Horn verified that Eq. (7) could describe the noise of different types of as-processed thin metal films. For example, Fig. 2 shows the noise of a long, narrow resistive Ag strip. In Fig. 2(a), the normalized noise magnitude is plotted as a function of temperature. In Fig. 2(b) the measured frequency dependence is compared with the prediction from Eq. (7). To

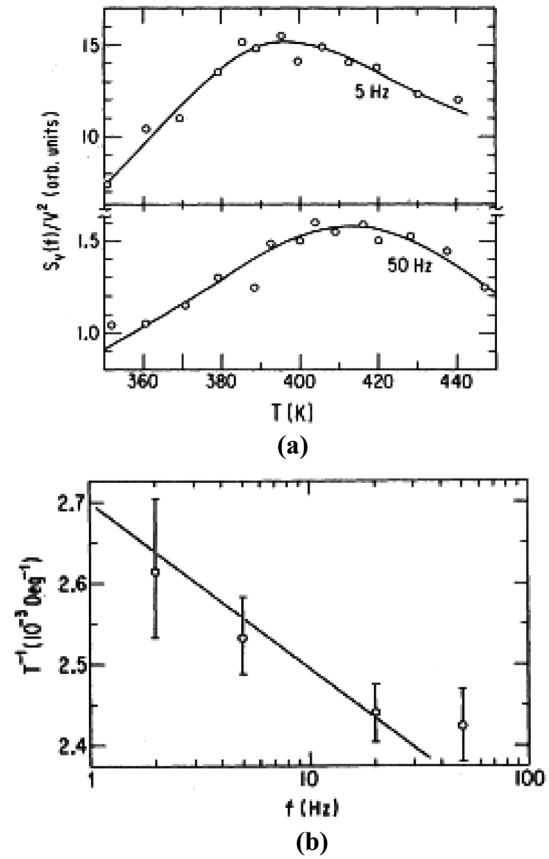


Fig. 3. Inverse temperature of the peak in noise magnitude as a function of the frequency at which the noise is measured. The solid line is the prediction of Eq. (7) of the text. (After Dutta and Horn [1], © 1981, AIP).

within the error bars, reasonable agreement is observed [1], [14]. Note that, for temperatures below the peak in Fig. 2(a), the derivative $\partial ln S_V / \partial ln T$ is positive. In Fig. 2(b) values of $\alpha$ are greater than one for this temperature range. At the peak, $\partial ln S_V / \partial ln T$ is zero and $\alpha \approx 1.0$. For $\sim 400$ K $< T <\sim$ 500 K, $\partial ln S_V / \partial ln T$ is negative and $\alpha < 1.0$. Good agreement is also found for Au and Cu [1], [14], and for Pt [43], [44].

Because $\alpha$ changes with temperature, the location of the peak temperature in the noise vs. temperature curve in Fig. 2(a) changes with measuring frequency. A detailed plot of the temperature dependence of the noise near the peak is shown in Fig. 3(a) for $f = 5$ Hz and $f = 50$ Hz. Fig. 3(b) plots the variation of the temperature of the noise peak as a function of measuring frequency, and shows that the results are consistent with Eq. (8). That is, higher measuring frequency leads to higher temperatures for the peak in noise magnitude. These results demonstrate the internal self-consistency of the Dutta-Horn model, and provide strong circumstantial evidence that the noise of thin metal films is caused by defects [1].

Over the next $\sim 10$ years, a large number of studies were performed to evaluate the extent to which the Dutta-Horn model describes the $1/f$ noise of metals. Fig. 4 shows the temperature dependence of the noise magnitude of a AuPd nanowire with a 53-nm diameter through three heating and cooling cycles. These wires were known from studies of Anderson localization and/or electron-electron interactions at low temperature [45] to

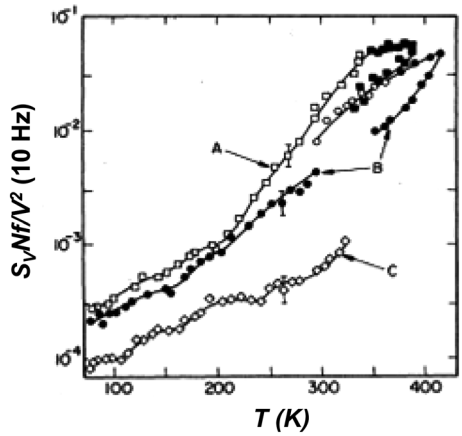


Fig. 4. Normalized noise magnitude at $f = 10$ Hz as a function of measuring temperature during three separate cooling and heating sequences for a 53-nm diameter AuPd nanowire with a resistivity of $180 \pm 20$ $\mu\Omega$cm before sequence A began, $160 \pm 18$ $\mu\Omega$ cm before B, $145 \pm 16$ $\mu\Omega$cm before C, and $125 \pm 14$ $\mu\Omega$cm after the completion of all annealing sequences. Annealing was performed in situ during the noise measurement process for sequences A and B. Before the measurements in C, the wire was heated to $\sim$ 470 K in an Ar environment. The uncertainties in resistivity are a result of uncertainties in the sample dimensions. (After Fleetwood and Giordano [16], © 1985, AIP).

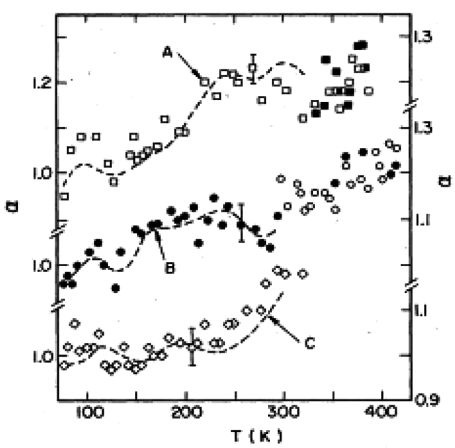


Fig. 5. Measured and predicted values of the frequency dependence of the noise, $\alpha = -\partial \ln S_V / \partial \ln f$, using the experimental results from Fig. 4 and Eq. (7) of the text. (After Fleetwood and Giordano [16], © 1985, AIP).

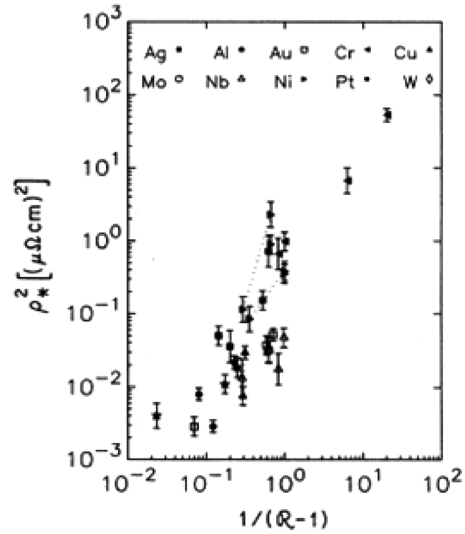


Fig. 6. Normalized noise magnitude ($\rho_*^2$, which is proportional to $S_V Nf/V^2$) at $f = 1$ Hz and $T = 300$ K as a function of $1/(\mathcal{R}-1) = (\rho - \rho_L)/\rho_L$, which is the ratio of defect and/or impurity scattering to phonon scattering. Larger values of $1/(\mathcal{R}-1)$ correspond to more defective films, which show much higher noise than less defective films. (After Scofield et al. [46], © 1985, AIP).

decrease in resistance with heating above 300 K as defects were annealed and/or as impurities (most likely from the sputtering process used in fabrication [16], [45]) were removed. Significant decreases in noise and resistivity were observed through the heating cycles in Fig. 4. Moreover, Fig. 5 demonstrates that the Dutta-Horn model describes accurately the changes in frequency dependence $\alpha$ that occur [16]. This provides strong evidence that the $1/f$ noise of metals results from defects and/or impurities.

Scofield *et al.* performed a comprehensive comparison of noise magnitudes for a variety of metal films with the fraction of the resistivity caused by defect and/or impurity scattering, shown in Fig. 6[46]. The relative resistance ratio is defined as $\mathcal{R} = \rho/(\rho - \rho_L)$, where $\rho$ is the total resistivity and $\rho_L$ is the component due to phonon (lattice) scattering. Hence, $1/(\mathcal{R}-1) = (\rho - \rho_L)/\rho_L$ is the ratio of defect and/or impurity scattering to phonon scattering, and $\rho*^2$ (proportional to $S_V Nf/V^2$) is the normalized noise magnitude. Reduced defect and/or impurity scattering corresponds to reduced noise magnitudes in Fig. 6. This strongly affirms that the $1/f$ noise of the metal films is caused primarily by defects or impurities. The results of Figs. 2–6 and related studies convincingly rule out a significant role for lattice scattering (as proposed by Hooge and Vandamme [47], for example) for the noise of metals [46].

In Figs. 4–6 it is not always clear whether defects or impurities play a more dominant role in the observed $1/f$ noise. Pelz and Clarke irradiated Cu films with 500-keV electrons and demonstrated a significant increase in $1/f$ noise [21], [48], as illustrated in Fig. 7. Here, clearly it is radiation-induced defects that cause the increased noise, and not impurities. The frequency dependence of the noise of both un-irradiated and irradiated devices (Fig. 7(a) follows the Dutta-Horn model, as shown in Fig. 7(b). Building on calculations by Martin [49], Pelz and Clarke used plausible assumptions about carrier-defect scattering to demonstrate that a local-interference model [50] provides order-of-magnitude estimates of carrier mobility fluctuations consistent with the results of Fig. 7, as well as providing a first-order estimate of the magnitude of the room temperature noise of metals with moderate disorder (e.g., consistent with results in Fig. 6[46], [50]). The noise of more significantly disordered films and/or the noise of metals at cryogenic temperatures can be described via this mechanism and/or the universal conductance model of Feng, Lee, and Stone [22], [50]–[54]. Carrier number fluctuations are typically not important to the noise of metals, owing to their high free carrier densities [1], [2].

Zimmerman and Webb demonstrated that impurities and/or their interactions with defects also strongly affect the noise of metal films. Fig. 8 shows the noise of a 100-nm thick Pd film at 80 K (1) without exposure to hydrogen, and (2)–(4) at 80 K, 155 K, and 280 K after sufficient exposure to introduce a 5% concentration of hydrogen into the films [20]. After hydrogen is introduced, the noise at 80 K is still proportional to $\sim 1/f$, and

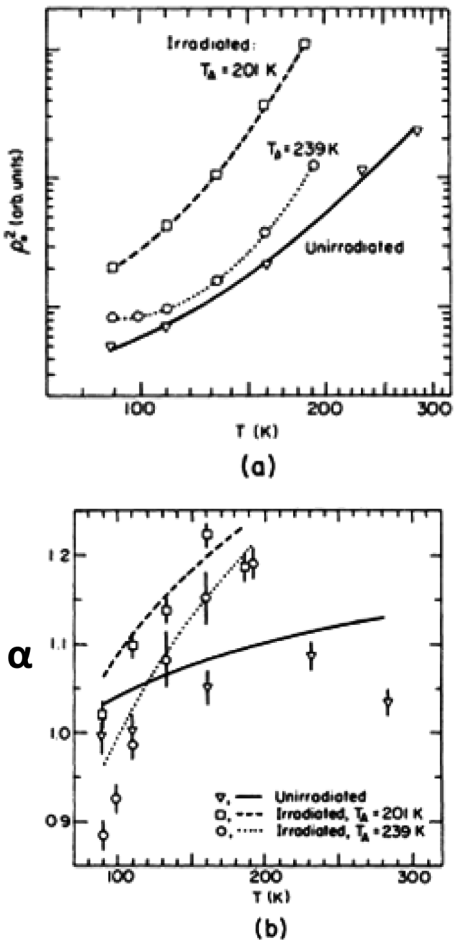


Fig. 7. (a) Normalized noise magnitude $\rho_*^2$ versus temperature $T$ before and after a 100-nm thick Cu film was irradiated at 90 K with 500 keV electrons. Irradiated films were annealed at $T_A = 201$ K and $T_B = 239$ to stabilize the response before the post-irradiation noise was measured. (b) Measured and predicted values of $\alpha = -\partial \ln S_V / \partial \ln f$, the frequency dependence of the noise, are compared using the experimental results from (a) and Eq. (7) of the text. (After Pelz et al. [21], © 1988, AIP).

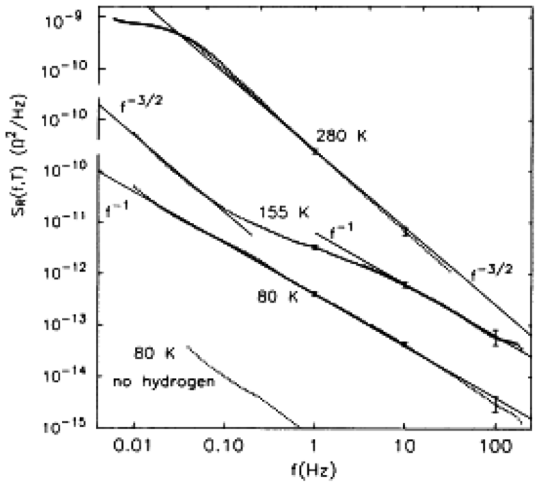


Fig. 8. $1/f$ noise as a function of frequency, temperature, and hydrogen exposure for 100-nm thick Pd films. The upper three curves are for devices with 5% atomic hydrogen. The lower curve was not exposed to hydrogen. (After Zimmerman and Webb [20], © 1988, AIP].

increases by more than two orders of magnitude. At 280 K, the noise is proportional to $1/f^{1.5}$, which is consistent with $H^+$ diffusion [20]. At 155 K, the noise transitions from a $\sim 1/f$ dependence at higher frequencies to $H^+$ diffusion noise at lower frequencies. This demonstrates that diffusing species cannot lead to $1/f$ noise [55] unless sufficient trapping occurs to modify the nature of the transport.

Figs. 2–8 provide strong evidence that the low-frequency noise of thin metal films and wires is due primarily to carrier-mobility fluctuations resulting from the interactions of carriers with defects and/or impurities. In all cases shown here, and most cases in the literature [1]–[3], [13]–[23], the Dutta-Horn model describes the noise well. Exceptions are observed for ferromagnetic (e.g., Ni [23]) and anti-ferromagnetic (e.g., Cr [18], [19]). In Ni, the noise is dominated by fluctuations in the ordering of magnetic domains [23]; the noise of Cr is attributed to rotations of the polarization of spin-density wave domains [19].

At best, only order-of-magnitude estimates can be obtained of the densities and energy distributions of the defects and impurities that lead to noise in metals. This is because it is difficult or impossible to obtain information from other techniques that is sufficiently quantitative to enable more accurate predictions of the noise to be made on the basis of knowledge about the material properties of the metal films. Nevertheless, comparison of experimental results with the Dutta-Horn model invariably leads to significant insight into the potential origins of the noise [1]–[3], [13]–[23].

Finally, from an application perspective, there have been several efforts to correlate the low-frequency noise and metallization reliability of Al and/or Cu lines with dimensions comparable to those used in ICs [6], [56]–[59]. However, metal lines on ICs are much thicker than the thin films and wires in Figs. 1–8. Thus, the excess noise in these structures that is observed at high currents and elevated temperatures typically (but not always [57], [59]) shows a $\sim 1/f^2$ dependence owing to the electromigration-induced resistance drift that occurs during the measurement [56]–[59].

## IV. MOS Transistors

### A. Temperature and Voltage Dependence

Although the model of Dutta and Horn was developed to describe the noise of thin metal films, which is caused primarily by fluctuations in carrier mobility [1]–[3], Eqs. (7)-(9) are quite general in nature [1], [2], [18]. Over the last $\sim$ 30 years, the model has been applied successfully to semiconductor devices as well. Although other interpretations have been offered (e.g., [38], [47], [60]), the evidence (including that reviewed here) is overwhelming that carrier number fluctuations associated with trapping at and emission from defects and/or impurities, and not mobility fluctuations, are by far the most important source of low-frequency noise in semiconductor devices [2], [4], [7], [10], [24], [27], [30], [61]–[65]. The Dutta-Horn model often provides significant insight into the defect-energy distribution for semiconductor devices.

Fig. 9 shows one of the initial tests of the Dutta-Horn model for $Si/SiO_2$ devices, which was performed by Black and co-workers [24]. In Fig. 9(a) the noise magnitude is plotted as

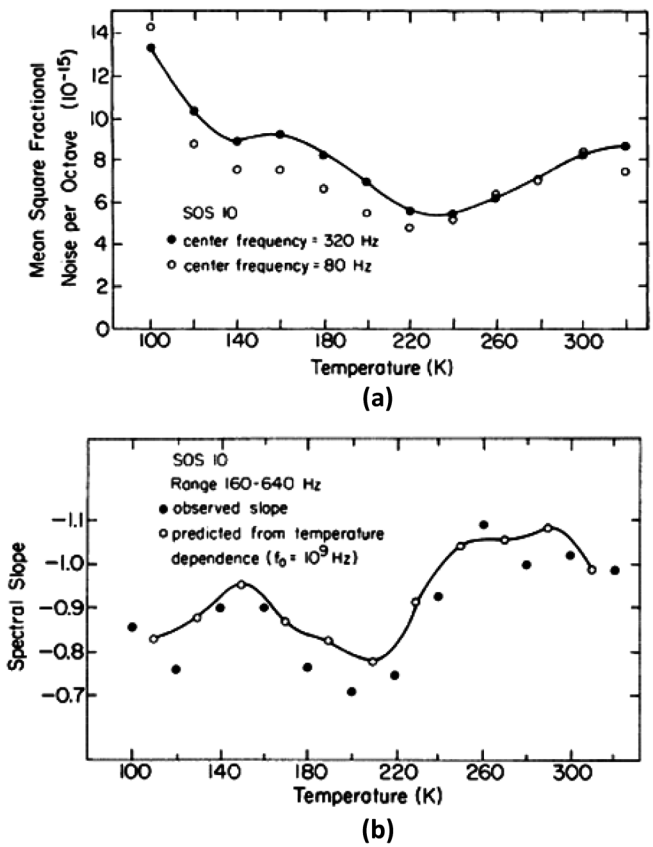


Fig. 9. (a) Temperature dependence of the normalized noise magnitude in two frequency bands for a Si-on-sapphire Hall-bar structure with an 80-nm oxide, grown on lightly doped $p$-type Si. (b) Measured and predicted values of the frequency dependence, $\alpha = -\partial \ln S_V / \partial \ln f$, using experimental results from (a) and Eq. (7). (After Black et al. [24], © 1983, AIP).

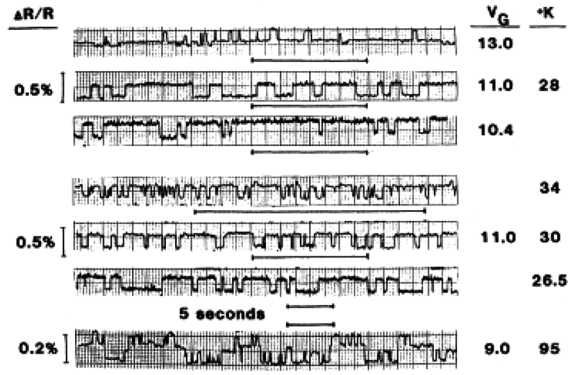


Fig. 10. Discrete resistance switching events (random telegraph noise) as a function of gate voltage and temperature for a $p$MOS transistor with a 65 nm gate oxide and dimensions $L = 1.0$ $\mu$m and $W = 0.15$ $\mu$m. At higher temperatures and lower values of gate voltage, the signal transitions from a region in which only discrete resistance fluctuations are observed to a region in which $1/f$ noise is observed. For transistors with larger gate area on the same chip, only $1/f$ noise is observed. (After Ralls et al. [65], © 1984, AIP).

a function of temperature for silicon-on-sapphire Hall-bar test structures. The frequency dependence of the noise is plotted in Fig. 9(b) and compared with the prediction of the Dutta-Horn model. Excellent agreement is observed. Black *et al.* demonstrated that the noise of these structures is not quantitatively described by the number fluctuation model in its original form, in which charge carriers tunnel into and out of traps in the oxide [12], [24], [61]–[63]. This is because tunneling depends on temperature only weakly, so thermally activated defect reconfiguration must play a role [2], [24]. Good agreement was also observed between experiments and predictions of the Dutta-Horn model in early tests of noise in MOSFETs by Surya and Hsiang [64].

Additional evidence that thermally active processes are important to MOS $1/f$ noise was provided by Ralls *et al.*, who investigated the low-frequency noise in MOSFETs with $\sim 1$ $\mu$m channel length, and observed a transition from random telegraph noise to $1/f$ noise for increasing temperatures and/or larger devices [65]. Fig. 10 shows resistance fluctuations as a function of gate voltage and temperature from $\sim$ 28 K to 95 K. At the lowest temperatures, only a single prominent trap is active, which leads to large changes in device resistance. The noise power spectral density for these devices and conditions is Lorentzian in form [1], [2], [4], [11]. As the temperature is increased, resistance switching rates become faster, and more traps become active. For higher temperatures and/or larger devices, discrete resistance fluctuations are not observed. Instead, $1/f$ noise is found [65]. These results led Ralls *et al.* to speculate (correctly) that the superposition of the effects of a large number of defects similar to those leading to random telegraph noise leads to $1/f$ noise in semiconductor devices. Over the next $\sim 5$ years, an extraordinary amount of work was done to characterize the electronic properties (capture and emission times, energy, cross section, etc.) of a large number of individual defects in MOS devices, tunnel junctions, and other nano-structures [15], [66]–[73]. This work is reviewed at length by Kirton and Uren [4], for example.

A number of investigators have used noise measurements at room temperature to estimate defect densities in MOS devices. Unless information about the temperature dependence of the noise is available, Eq. (9) cannot be applied to estimate the defect-energy distribution. However, the McWhorter model as adapted to MOS transistors enables one to obtain first-order estimates of effective trap densities for defects with energy levels that are reasonably close to the Si conduction band (for $n$MOS transistors) or valence band (for $p$MOS transistors) [12], [25], [61]–[64], [74]–[79]. The simplest form of the McWhorter model attributes the noise to tunnel-assisted charge exchange between the Si channel and defects in the near-interfacial $SiO_2$ [12], [61]–[63], [80]. For traps that are distributed approximately uniformly in space throughout the oxide and in energy in the silicon band gap, the changes in trap occupancy with time lead to $1/f$ noise. For constant drain current and gate bias, in the linear region of MOS operation, the transistor is essentially a gated resistor, and the $1/f$ noise is described in this model case by:

$$S_{V_d} = \frac{q^2}{C_{ox}^2} \frac{V_d^2}{(V_g - V_t)^2} \frac{k_B T D_t(E_f)}{LW \ln(\tau_1/\tau_0)} \frac{1}{f}. \qquad (10)$$

Here $S_{Vd}$ is the excess drain voltage noise power spectral density, $V_t$, $V_g$, and $V_d$ are the threshold, gate, and drain voltages, $C_{ox}$ is the gate oxide capacitance per unit area, $L$ and $W$ are

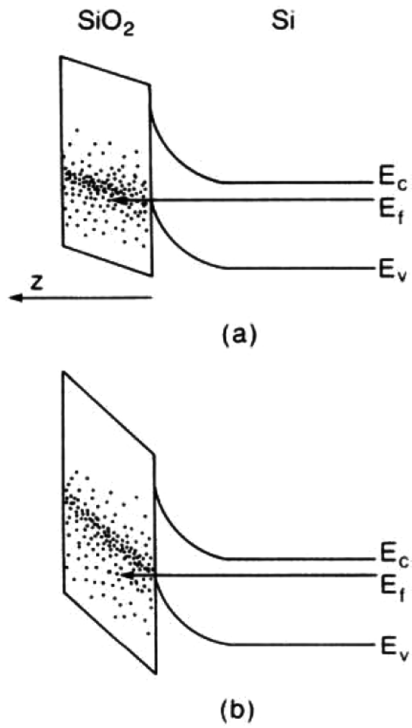


Fig. 11. Energy bands for a $p$MOS $Si/SiO_2$ transistor for (a) lower and (b) higher applied electric field. The dots are a notional representation of trapping sites in the $SiO_2$. The $1/f$ noise of a MOS transistor is sensitive to defects within a few $kT$ of the Fermi level, which means that changing the bias enables one to probe a different range of defect energy levels in the near-interfacial $SiO_2$. (After Surya and Hsiang [25], © 1986, AIP).

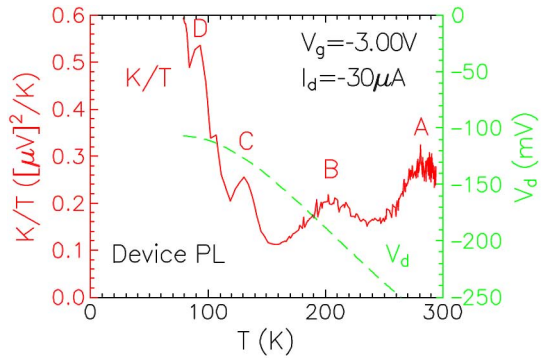


Fig. 12. $K/T$ as a function of temperature $T$ for a surface channel $p$MOS transistor with a 60 nm thick oxide, with dimensions $L = (3.45 \pm 0.10)\mu$m and $W = (16.0 \pm 0.5)\mu$m. Here $K(V_g, T) = [S_V(f, V_d, V_g, T) - S_V(f, 0, V_g, T)](V_g - V_{th})^2 (V_d)^{-2}$ is the normalized excess noise spectral density in a frequency band from 5 Hz to 50 Hz. (After Scofield et al. [27], © IEEE, 1994).

the transistor channel length and width, $D_t(E_f)$ is the number of traps per unit energy per unit area at the Fermi level $E_f$, and $\tau_0$ and $\tau_1$ are minimum and maximum tunneling times, respectively [12], [63], [81], [82]. This model has been extended to include the effects of non-uniform spatial and energy distributions [1], [2], [4], [10], [25], [26], [79] and/or correlated mobility fluctuations that are associated with changes in the charge states of the defects [78], [80], [83]. In addition, the "unified model" developed by Hung *et al.* has been adapted for common use in TCAD device simulation tools [80]. Noise models that attempt to incorporate number fluctuations and lattice scattering (e.g., [47], [60], [81], [83]) provide additional degrees of parametric freedom, but are not physically justified, since there is no evidence that lattice scattering is a significant source of low-frequency noise in either metals or semiconductor devices [2], [18], [24], [27].

As illustrated by the noise vs. temperature curves in Fig. 9, for example, defects responsible for low-frequency noise in MOS devices are not usually distributed evenly in space or energy. $D_t(E_f)$ often varies with voltage, temperature, and frequency. Hence, the voltage, temperature, and frequency dependences of the noise usually deviate from the first-order, simplified model values in Eq. (10). Varying the gate bias enables one to probe different regions of the semiconductor and/or insulator band gaps, even at room temperature [25]–[27], [30]–[32], [64], [74]–[76], [78]–[81], [83]–[86]. For example, Fig. 11 shows that, when the gate bias is changed, the Si surface potential changes slightly, but the band bending is more significant in the $SiO_2$ insulator [25]. In the simplest form of the McWhorter model, which assumes tunneling is the rate-limiting step that leads to the $1/f$ noise, the portion of the $SiO_2$ defect energy distribution that is most easily accessible to noise measurements is the region within a few $kT$ of the Fermi level [11], [12], [63], [82]. Within the context of this model, there is a straightforward relationship between the applied gate bias during noise measurements at a given temperature and the spatial distribution of the traps in the near-interfacial $SiO_2$ [25], [63], [75], [78], [79], [87]–[89]. For thermally activated noise, it is not as easy to infer the spatial distribution of the defects, but varying the gate bias still provides useful and complementary information to varying the temperature [25], [27], [84].

Scofield *et al.* performed a detailed study of the interplay between bias and temperature in probing the energy distribution of the noise of MOS devices, as shown in Figs. 12 and 13. Fig. 12 shows the normalized noise magnitude as a function of temperature for a $p$MOS transistor. Thermally activated features are observed, including four distinct, broad peaks A-D. These features are consistent with thermally activated kinetics for the noise process, as described via the Dutta-Horn model. These and other studies of the temperature dependence of the noise, as well as detailed evaluations of the corresponding charge trapping and emission kinetics, essentially rule out simple tunneling models, except perhaps at very low temperatures [2], [10], [22], [24], [27], [84], [90], [91].

The voltage dependence of the noise in the vicinity of the peaks is shown in detail in Fig. 13. If a peak exists in the defect energy distribution, then changing the voltage also affects the peak location. At fixed temperature, the variation in $D_t(E_f)$ that leads to a peak in noise vs. temperature also leads to a corresponding peak in noise vs. gate voltage, as illustrated in Fig. 13. Peak A is apparent in $S_{Vd}(T)$ in Fig. 12 and $S_{Vd}(V_g)$ in Fig. 13(a); peaks B and C are present in Figs. 12 and 13(b); and peaks C and D are present in Figs. 12 and 13(c).

Note that $K/T$ in Fig. 13(a) increases approximately linearly (neglecting the small bump) with increasing magnitude of $V_g$ for the voltage range $2.5\text{ V} \leq -V_g \leq 5\text{ V}$. Over the range of voltages in Fig. 13(a) for which $K/T$ is proportional to $V_g$, $S_V$ is proportional to $V_d^2/(V_g - V_{th})$. Similar voltage dependences

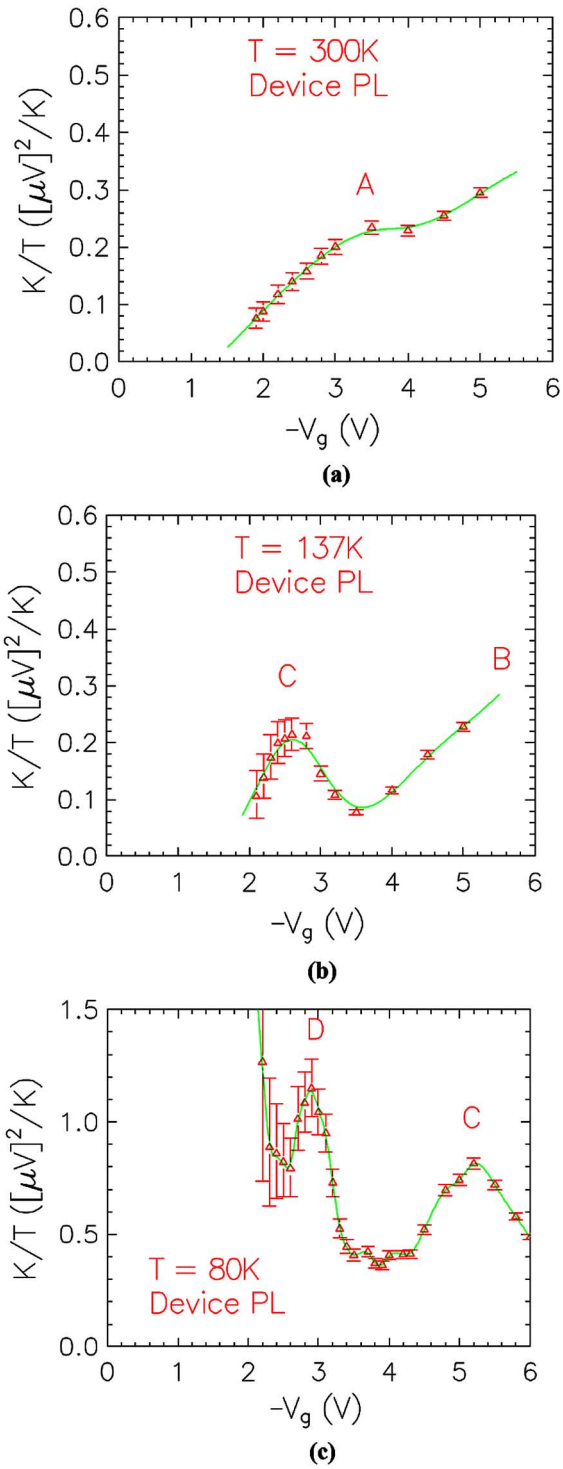


Fig. 13. $K/T$ as a function of gate voltage for the devices of Fig. 12 at temperatures of (a) 300 K, (b) 137 K, and (c) 80 K. Noise peaks A-D correspond to the similar features observed in Fig. 12. (After Scofield et al. [27], © IEEE, 1994).

at room temperature for $p$MOS transistors are often interpreted as evidence that the noise is due to mobility fluctuations caused by lattice scattering, as proposed by Hooge, Vandamme, *et al.* [27], [38], [47], [60], [81], [83]. Evaluating both the voltage and temperature dependence of the noise in Figs. 12 and 13 shows this is not the case for these devices. We now explore this point in more detail.

Often it is convenient to explicitly parameterize the gate voltage and frequency dependence of the noise due to carrier number fluctuations via an expression of the form:

$$S_{V_d}(f, V_d, V_g) = \frac{K}{f^{\alpha}} \frac{V_d^2}{(V_g - V_t)^{\beta}} \tag{11}$$

Note that Eq. (11) with $\alpha = 1$ and $\beta = 2$ contrasts clearly in voltage dependence with Hooge's empirical formula, which when applied to MOS transistors in the linear mode of operation, can be written [7], [38], [47]:

$$\begin{aligned} S_V/V_d^2 &= S_I/I^2 = \alpha_H/N_c f \\ &\approx \alpha_H(q/LWC_{ox}) f (V_g - V_{th})^{-1} \end{aligned} \tag{12}$$

Here $\alpha_H$ is a dimensionless parameter, and $\beta = 1$. Thus, the Hooge model specifies a fixed value of $\beta = 1$; the number fluctuation model with uniform $D_t(E_f)$ leads to $\beta = 2$; and the number fluctuation model with non-uniform $D_t(E_f)$ does not specify a particular value of $\beta$. Instead, deviations from $\alpha = 1$ and $\beta = 2$ are evidence of non-uniform $D_t(E_f)$.

A number of $\beta$ values have been observed in the literature [60]. This occurs simply because a non-uniform $D_t(E)$ is the most common case observed for metals and semiconductor devices [1], [2], [5], [7], [10], [24]–[34], [78]–[80], [84], [92]–[94]. Variations in $D_t(E)$ occur naturally from process variations during device fabrication. In addition, high-field stress, aging, exposure to moisture and/or ionizing radiation, etc. can also change $D_t(E_f)$ for a single device, often quite significantly [5], [10], [30]. For example, Fig. 14 shows the noise magnitudes of $n$MOS and $p$MOS transistors that were (1) not exposed to moisture (control) or irradiated, (2) exposed to moisture but not irradiated, (3) irradiated, but not exposed to moisture, or (4) both exposed to moisture and irradiated. For the control $n$MOS device in Fig. 14(a), before irradiation $\beta = 1.7$ and after irradiation $\beta = 1.9$; for the moisture-exposed $n$MOS device in Fig. 14(a), before irradiation $\beta = 1.5$ and after irradiation $\beta = 1.8$. For the control $p$MOS device in Fig. 14(b), before irradiation, $\beta = 0.4$; after irradiation the average value of $\beta$ is $\sim 1.2$, but the slope is multi-valued. For the moisture-exposed $p$MOS device in Fig. 14(b), prior to irradiation, $\beta = 0.9$ and after irradiation $\beta = 2.0$ [30]. Clearly, these kinds of variations in $\beta$ are not consistent with Eq. (12).

In the absence of ad hoc assumptions, it is not easy to quantitatively map the voltage dependence of the noise into a defect-energy distribution [87]–[89], e.g., via an expression similar to Eq. (9). However, using the approach of Hung *et al.* [80], it is possible to map the applied gate voltage to the Fermi level, referenced to the Si band gap [30], [80]. This enables one to see the trends in the defect-energy distribution with respect to the Si band edges. The resulting energy distributions are shown in Fig. 15 for moisture-exposed $n$MOS and $p$MOS devices, before and after irradiation [30].

Before irradiation, the inferred defect-energy distribution increases toward the conduction and valence band edges for the $n$MOS and $p$MOS devices, respectively. After irradiation, the

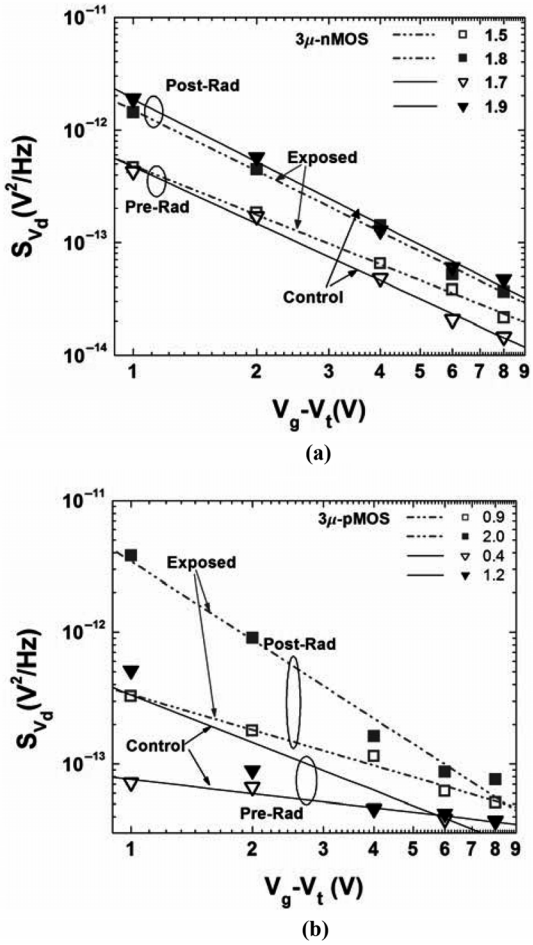


Fig. 14. $S_{Vd}$ at $\sim$ 10 Hz vs. $V_g - V_t$ for (a) $n$MOS and (b) $p$MOS transistors with 37 nm oxides, and dimensions $L = (3.45 \pm 0.10)\mu$m and $W = (16.0 \pm 0.5)\mu$m. Results are shown for devices with or without exposure to moisture (85% relative humidity at 130°C for one week). Both control and moisture-exposed devices were measured before and after irradiation with 10-keV X-rays to 500 krad($SiO_2$) at a dose rate of 31.5 krad($SiO_2$)/min at 6 V gate bias. During the noise measurements, the drain voltage $V_d$ was held at a constant $\pm$100 mV. (After Francis et al. [30], © IEEE, 2010).

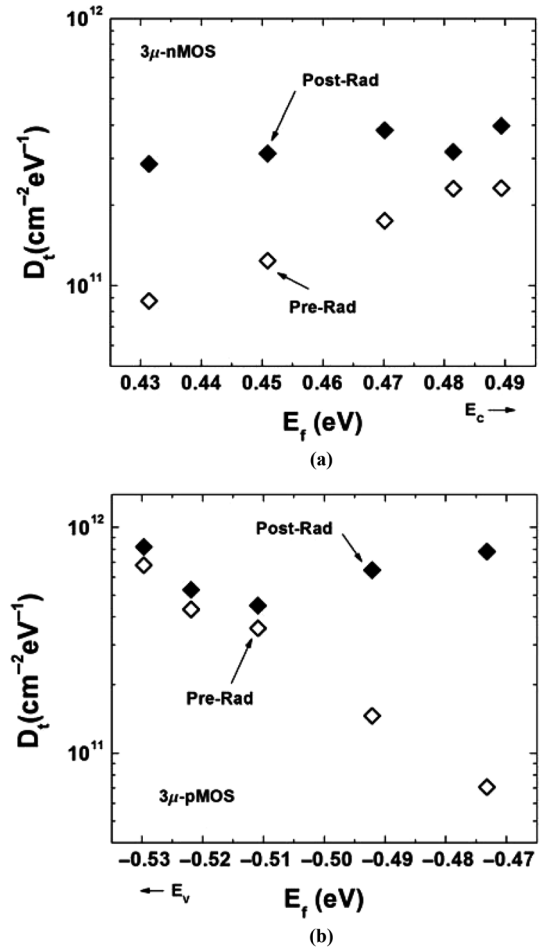


Fig. 15. Trap distribution as a function of Fermi level for the moisture exposed (a) $n$MOS and (b) $p$MOS transistors of Fig. 14, before and after 500 krad($SiO_2$) total dose irradiation. (After Francis et al. [30], © IEEE, 2010).

defect-energy distribution for both of these devices is more uniform than before irradiation. For the $p$MOS devices, the defect-energy distribution after irradiation remains nearly constant at energies closer to the Si valence band, but increases strongly at energies closer to midgap. Similarly increasing defect energy distributions toward midgap have also been observed after irradiation or high-field stress using measurement techniques other than low frequency noise [5], [93]–[97], so the trends in the noise data are consistent with the expected, underlying changes in defect density.

We now illustrate the use of measurements of the temperature dependence of the noise and the Dutta-Horn model to gain insight into defect-energy distributions in MOS devices. Fig. 16 shows the $1/f$ noise of $n$MOS transistors with 32 nm oxides (a) before irradiation, (b) after 500 krad($SiO_2$) X-ray irradiation, and (c) after 200 °C post-irradiation anneal at 0 V. The noise increases after the device is irradiated [7], [10], [28], [92], [98]–[104], and decreases after annealing [7], [10], [28], [98], [99]. Fig. 17 shows that the measured and predicted frequency dependences of the noise satisfy the Dutta-Horn relation, Eq. (7), before and after irradiation and annealing [10], [28]. This makes it possible to use Eq. (9) to extract defect energy distributions, as shown in Fig. 18. The energy scale inferred from this analysis assumes $f \approx$ 1Hz, for convenience, and $\tau_o \approx 1.8 \times 10^{-15}$ s, as estimated via detailed thermally stimulated current measurements and analysis [10], [105], [106]. After annealing, the energy distribution of the defects changes from pre-irradiation values. Evidently, this particular irradiation and annealing sequence has modified the defect energy distribution in such a way that the average defect density in Fig. 18(c) is similar to that in Fig. 18(a), but the peaks in noise vs. temperature now occur in different locations. Such variations in defect energies can be caused by changes in atomic spacing and shifts in position of nearest-neighbor atoms to accommodate near-interfacial strain, for example [10], [107].

Taken together, the results of Figs. 12–18 show that relying primarily on the voltage dependence of transistor noise measured only at room temperature can lead to incorrect conclusions about the origins of the noise [2], [24], [27], [30]. This illustrates the inherent risks of using an experimental test of a single parameter as primary evidence of model validation. Thus, while Hooge and co-workers deserve significant credit for introducing a practical and easily implemented method to param-

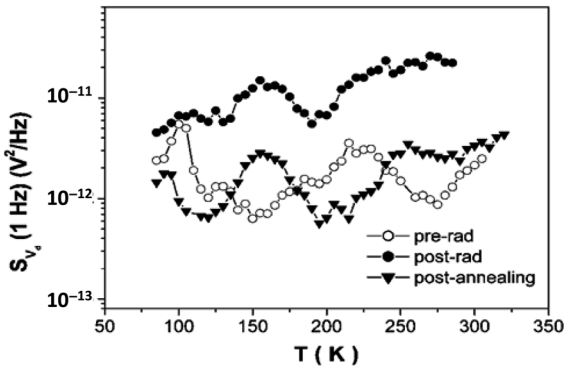


Fig. 16. Normalized noise magnitude at $f = 1$ Hz vs. temperature before and after 500 krad($SiO_2$) X-ray irradiation, and after the device was annealed for 24 h at $\sim 200°$C. These $n$MOS transistors have 32 nm oxides, and dimensions $L = (3.45 \pm 0.10)$ $\mu$m and $W = (16.0 \pm 0.5)$ $\mu$m. Devices were irradiated with 10-keV X-rays at 278 rad($SiO_2$)/s at 6 V gate bias, with all other pins grounded. For the noise measurements, the drain was biased at 100 mV, and $V_{GS} - V_{th} = 2$ V. (After Xiong et al. [28], © IEEE, 2002).

eterize low-frequency noise [7], [38], [47], [60], a wealth of data demonstrate that the $1/f$ noise of semiconductor devices is due to carrier number fluctuations and not mobility fluctuations. Thus, Eq. (12) is generally not applicable to the noise of semiconductor devices. The above results show that, in contrast, the Dutta-Horn model provides extremely useful information into the origins of the noise. That such measurements are not performed more commonly is due primarily to the length of time (often several days) required to complete a series of tests similar to those illustrated in Figs. 16–18. Hence, in practice, extensive noise measurements vs. temperature are typically only performed when one either needs to characterize device response as a function of operating temperature, or when detailed basic mechanisms studies are performed.

### *B. Defect Microstructures and Energies*

Unlike the case of metals, where the specific defects responsible for the noise are not usually easy to identify, a significant body of experimental and theoretical work shows that O vacancies in $SiO_2$ play a dominant role in determining the $1/f$ noise of MOS transistors [5], [7], [10], [28], [30]–[33], [82], [92], [98]–[111]. For example, a strong correlation has been observed between the $1/f$ noise $K = S_{Vd} f (V_g - V_t)^2 / V_d^2$ of $n$MOS transistors before irradiation and threshold-voltage shifts due to net positive radiation-induced oxide-trap charge $\Delta V_{OT}$ after irradiation, as shown in Fig. 19[7], [82], [108]–[113]. The noise measurements shown in Fig. 19 were performed at room temperature; threshold voltage shifts due to oxide and interface trap charge were estimated via the midgap method of Winokur *et al.* [114]. Using the first-order, number fluctuation model of Eq. (10) and plausible assumptions about the defects responsible for the noise and hole trapping, the correlation in Fig. 19 can be accounted for numerically via: [7], [82], [109], [110]:

$$K = \frac{q^2 k T f_{OT} t_{ox}^2}{L W \sigma_t \varepsilon_{ox}^2 E_g \ln(\tau_1/\tau_o)}. \tag{13}$$

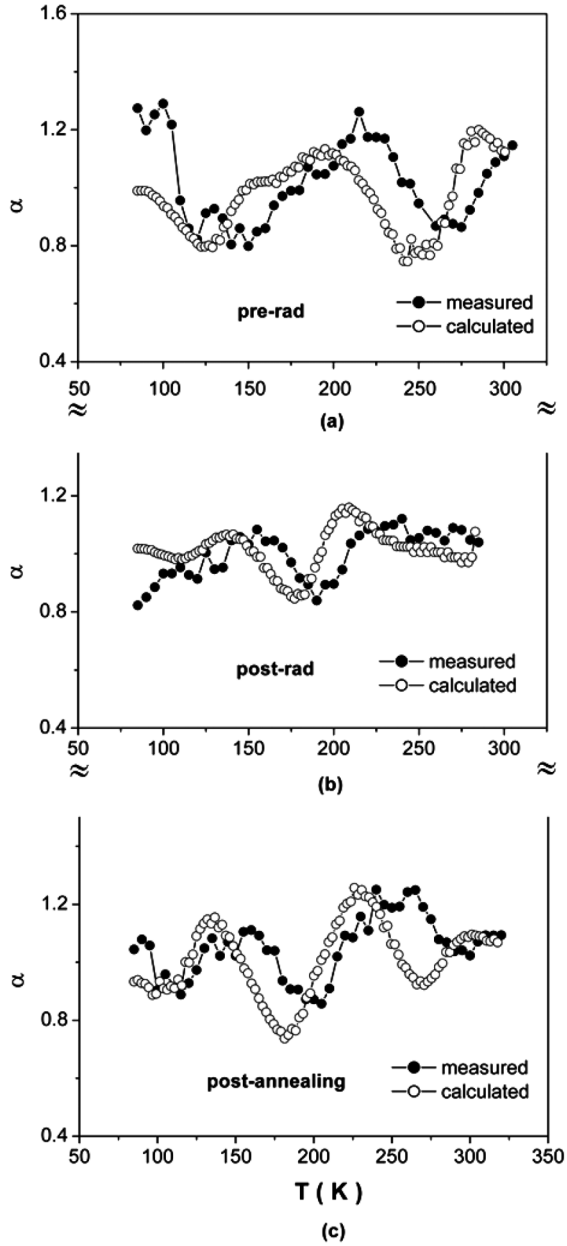


Fig. 17. Measured and predicted values of the frequency dependence of the noise, $\alpha = -\partial \ln S_V / \partial \ln f$, using the experimental results from Fig. 16 and Eq. (7) of the text. (After Xiong et al. [28], © IEEE, 2002).

Here $f_{OT}$ is the $SiO_2$ hole-trapping efficiency (i.e., the probability that a given hole created by ionizing radiation exposure is trapped); $t_{ox}$ is the oxide thickness; and $E_g$ is the $SiO_2$ band gap. For simplicity, Eq. (13) assumes that: (a) defects with similar average, effective capture cross sections $\sigma_t$ are responsible for both $1/f$ noise and radiation-induced-hole trapping, (b) the pre-irradiation noise is proportional to the density of oxide traps, which is proportional to $f_{OT}/\sigma_t$, (c) oxide traps near the $Si/SiO_2$ interface are distributed approximately uniformly in space and energy, (d) carrier number fluctuations are the dominant cause of the noise, and (e) the defects responsible for the $1/f$ noise have capture and emission cross sections similar to bulk oxide traps located deeper within the $SiO_2$, responsible for most radiation-induced oxide-trap charge [7], [10],

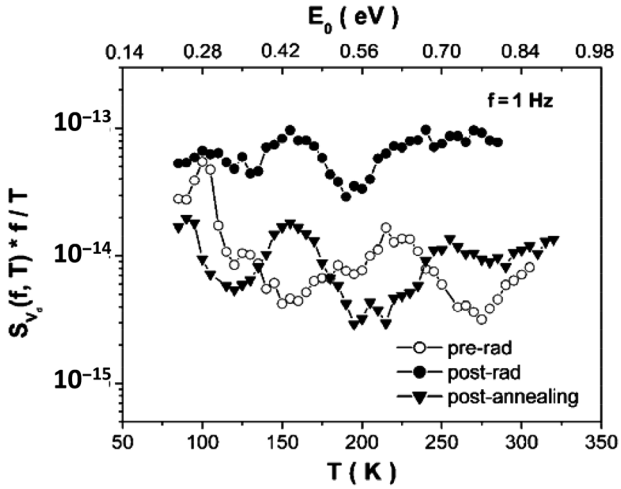


Fig. 18. $S_V f/T$, which is proportional to $D(E_o)$ by Eq. (9), as a function of temperature for the devices of Figs. 16 and 17. The energy scale inferred from Eq. (7) is given on the upper x-axis for f $=$ 1 Hz and $\tau_o \approx 1.8 \times 10^{-15} s$. (After Xiong et al. [28], © IEEE, 2002).

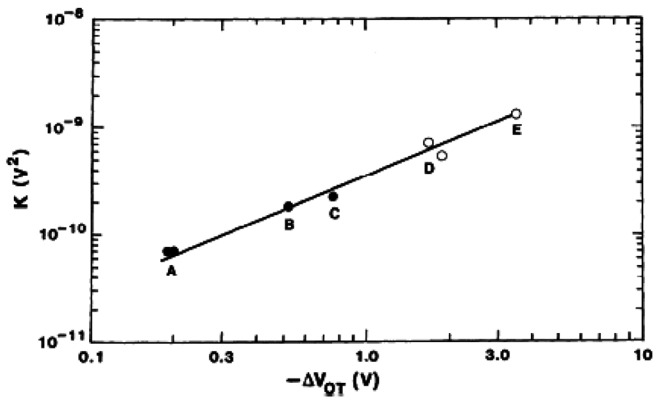


Fig. 19. Normalized noise magnitude $K$ as a function of threshold-voltage shifts due to radiation-induced oxide-trap charge $\Delta V_{OT}$ for 3.5 $\mu$m $\times$ 16 $\mu$m, nMOS transistors with gate oxides of different thickness (A, D: 32 nm; B, E: 48 nm; C: 60 nm) and radiation hardness (A-C hard; D, E soft) processed in the same lot. Noise measurements were performed in the linear region of device operation; values of $\Delta V_{OT}$ were obtained from room temperature irradiation to 100 krad($SiO_2$) in a Co-60 source at a rate of $\sim$ 278 rad($SiO_2$)/s at an oxide electric field of $\sim$ 3 MV/cm. (After Fleetwood and Scofield [109], © 1990, AIP).

[82], [109], [110]. Assumptions (a), (d), and (e) are validated in [10], and (b) and (c) are similar to the assumptions made in Eq. (10), so the applicability and limitations of Eq. (13) are similar to that of Eq. (10).

One plausible candidate for an O vacancy center that can cause $1/f$ noise is the dimer O vacancy defect illustrated in Fig. 20(a)[10], [115]–[120]. Another is the $E_\gamma{}'$ defect, which is depicted in Figs. 18(b) and 18(c)[118]–[126]. The local atomic spacing and bond angles determine whether O4 has a nearest neighbor Si close enough to bond with the puckered Si1. The 4-fold coordinated, puckered Si vacancy center shown in Fig. 18(b) forms a stable dipole upon electron capture, while the 5-fold coordinated, puckered configuration shown in Fig. 18(c) does not [10], [118].

We now consider how O vacancy-related defects such as those depicted in Fig. 20 can lead to $1/f$ noise. In a $p$MOS

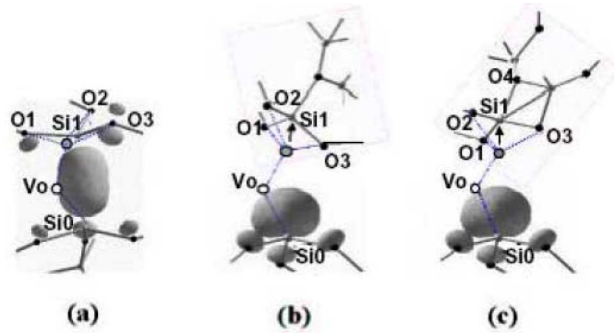


Fig. 20. Schematic illustrations of unpaired electron densities (gray regions) and atomic configurations of (a) a dimer O vacancy center, (b) a relaxed O vacancy center associated with the $E'_\gamma$ defect (the $E'_{\gamma 4}$), and (c) a second type of O vacancy center also associated with the $E'_\gamma$ (the $E'_{\gamma 5}$). The differences between defects (b) and (c) are the coordination of the atom denoted by the arrows and marked "Si1," with 4-fold coordination in (b) and 5-fold coordination in (c). (After Lu et al. [118], © 2002, AIP).

transistor, the capture and re-emission of a hole from a dimer O vacancy near the $Si/SiO_2$ interface can straightforwardly result in $1/f$ noise. This defect has a high effective capture cross section, a modest barrier for re-emission, and thus can potentially contribute to $p$MOS noise before or after irradiation [10], [99], [107], [127]. Charge transfer may occur via simple tunneling, trap-assisted tunneling, and/or thermal activation. Similar processes are inferred to occur in fast measurements of the recoverable component of negative-bias temperature instability (NBTI) in $p$MOS transistors [128]–[132] on time scales similar to typical low-frequency noise measurements, as illustrated schematically in Fig. 21. For very high field stress, both net hole trapping and increased noise are observed; in the absence of high field stress, net hole trapping is minimal, so primarily noise is observed. Fig. 21 is an extension of the model of reversible hole trapping in $SiO_2$ developed by Lelis, Oldham, *et al.* [125], [133]. The time dependence and energetics of the processes illustrated in Fig. 21 and later versions incorporating hydrogen [134], [135] are explored in detail in the contexts of NBTI and random telegraph noise by Grasser *et al.* in [129]–[132], [134], [135]. This remains a significant topic of intense study.

The $1/f$ noise of an $n$MOS transistor before or after irradiation may also result from the thermally assisted capture and emission of an electron by a dimer O vacancy. Defect functional theory (DFT) calculations show the probability of capturing an electron from the Si increases with increasing separation of the Si1-Si0 bond at the center of the complex shown in Fig. 20(a), as shown schematically in Fig. 22. At an equilibrium spacing of $\sim 0.25 - 0.30$ nm in the bulk $SiO_2$, the electron trapping level of the neutral dimer in Fig. 20(a) is near the $SiO_2$ conduction band, and therefore not able to capture an electron at or below room temperature. However, if the Si-Si bond is stretched to $\sim 0.35 - 0.4$ nm, near-midgap states can open up that may at least metastably capture an electron, with the energetics of capture becoming more favorable with increasing Si-Si spacing [10], [119]. These kinds of stretched Si-Si bonds are likely to exist preferentially near the $Si/SiO_2$ interface [10], [125], in which a significant amount of strain must be accommodated [125], [133], [136]–[141]. When an electron is captured,

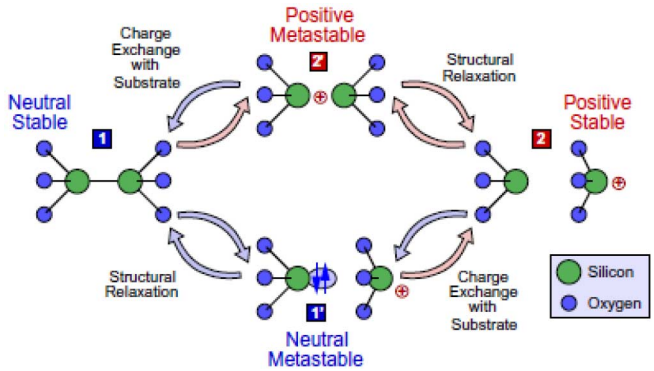


Fig. 21. Schematic illustration of (1) a dimer O vacancy that can capture a hole (2') and then release it (1) or relax into a puckered configuration (2). The further capture of an electron by a trapped hole (2) neutralizes the trapped positive charge, forming a dipole (1'). This defect can reversibly exchange an electron with the Si, or relax to reform the initial dimer (1), under suitable bias conditions. All changes in charge states that occur on $\sim$ ms to $\sim$ s time scales can contribute to the noise for typical measurements performed on $\sim$ Hz to $\sim$ kHz time scales. Defect (1) is the same as shown in Fig. 20(a), and defect 2 is similar to those in Figs. 20(b) and 20(c). (After Grasser et al. [131], © 2012, Elsevier.) More recent versions of this figure in [134], [135] are more complex and also include hydrogen.

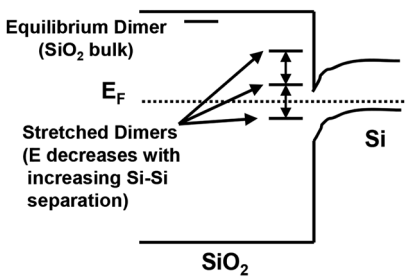


Fig. 22. Energy levels of dimer O vacancies in bulk $SiO_2$ with equilibrium Si-Si atomic spacing of $\sim 0.25-0.30$ nm and near-interface O dimer vacancies with stretched Si-Si spacing of $\sim 0.35-0.40$ nm and a distribution of energy levels near midgap. (After Fleetwood et al. [10], © 2002, IEEE).

the Si-Si spacing decreases due to the increased electron density between the two atoms. This leads to a rise in trap energy level and electron re-emission. The time scale for the atomic relaxation process is the rate-limiting step [10]. Especially for an $n$MOS transistor that is irradiated or subjected to high field stress, electron exchange with 4-fold-coordinated, puckered O vacancy defects is also a possible source of noise [10], [118], [121], [125]–[127].

In addition to the O vacancy-related defects considered in Figs. 18–20, several hydrogen-related defects may also contribute to MOS $1/f$ noise. For example, Blöchl and Stathis [142] used DFT calculations to show that the hydrogen bridge (essentially the dimer defect in Fig. 20(a) with a H atom bridging the Si-Si bond [142]), is a prime candidate for the defect responsible for stress-induced leakage current in ultrathin oxides. The energy levels for the H bridge defect range from $\sim$ 4 to $\sim$ 6.5 eV above the $SiO_2$ valence band, with positive, neutral, and negatively charged states all residing within this band. When charged, the H bridge undergoes a significant relaxation that strongly changes its energy level (by $\sim$ 2.5 eV) [142]. These kinds of defect reconfiguration are similar to the behavior of the E′ defects in Figs. 20 and 21, and therefore also likely to contribute to MOS $1/f$ noise [10], [134], [135].

Note that, in all cases considered, the low-frequency noise process involves defect relaxation and reconfiguration. Hence, it is not only the energy of a defect relative to the Si and/or $SiO_2$ band gaps that influences whether a defect can contribute to $1/f$ noise. The (typically thermally activated) barrier to defect reconfiguration also plays a critical role [2], [10], [130]–[132], [134], [135]. Therefore, the values of $D(E_o)$ that one infers from Eqs. (8) and (9) of the Dutta-Horn model are sometimes not easily referenced to either the Si or $SiO_2$ band gap. As shown schematically in Fig. 22, a pre-requisite for a defect to contribute to the measured noise is that one charge state of the defect lie above the Fermi level, and another lie below it. With the assistance of thermally assisted defect reconfiguration, a change in charge state can occur even if each energy level is more than a few $kT$ above or below the Fermi level [10], [143], in contrast with the (simplifying) assumptions of the number fluctuation model in original form.

That the defect energy distribution before irradiation or high field stress often increases toward the conduction band edge more strongly for $p$MOS devices than for $n$MOS devices [27], [60] may result from a relatively larger role of interface traps in $p$MOS noise than $n$MOS noise (see discussion below). Interface traps may function more commonly as a trap-assisted tunneling intermediary for hole injection into $SiO_2$, since the barrier for hole injection ($\sim$ 4.8 eV) is much greater than the barrier for electron injection ($\sim$ 3.1 eV), and the tunneling probability is strongly influenced by the energy barrier at the interface [132]. These differences in distributions may also result from the different roles and configuration dynamics of O vacancies near the $SiO_2$ interface. As one simple example, electron tunneling from the Si is inhibited under negative gate bias ($p$MOS) but favored under positive bias ($n$MOS), which affects the density and relative stability of defects in the 1' and 2 configurations in Fig. 21[118], [125]. These are fruitful topics for additional experimental and theoretical study.

### C. Oxide, Interface, and Border Traps

All of the defects discussed so far are near-interfacial oxide traps that exchange charge with the underlying Si. Thus, by definition, these are border traps [10], [110], [127], [144], as illustrated schematically in Fig. 23. Because the defects that cause the noise are a subset of the total oxide-trap charge, it is often not straightforward to compare estimates of defect densities obtained via low-frequency noise measurements, e.g., using Eq. (10), with estimates obtained via other methods. However, reasonable agreement among comparable methods has been reported in many studies.

The effective radiation-induced border-trap density $\Delta D_{bt}$ estimated via low-frequency noise measurements of $n$MOS transistors exposed to 1Mrad($SiO_2$) with 10-keV X-rays was $\sim 6.5 \times 10^{11}$ cm$^{-2}$ in [5], while estimates of the lower bound of $\Delta D_{bt}$ based on hysteresis measurements performed on capacitors processed and irradiated similarly to the $n$MOS transistors was $\sim$ $3.0 \times 10^{11}$ cm$^{-2}$ [5], [127]. Given the uncertainties inherent to each approach, this level of agreement

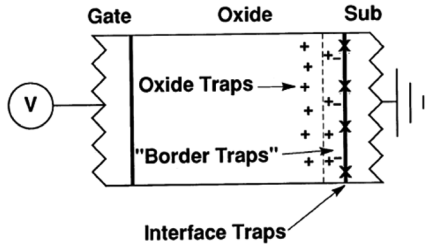


Fig. 23. Schematic illustration of defects in MOS devices. Border traps are near-interfacial oxide traps that exchange charge with the underlying Si on the time scale of the measurements being performed. (After Fleetwood et al. [110], © Elsevier, 1995).

is reasonable. But of course it is preferable to compare estimates of trap densities on the same devices. A dual-transistor border-trap (DTBT) technique was developed to address this need [102]. This method requires that $n$MOS and $p$MOS transistors with identically processed oxides, e.g., on the same chip, be irradiated under identical conditions, with the same applied electric fields. Bulk-oxide-trap charge densities are approximately equal for $n$ and $p$MOS transistors on the same chip under these conditions [127], [145], [146]. It is assumed that interface and/or border traps predominantly shift $n$MOS transistor threshold voltages $\Delta V_{thn}$ positively, and shift $p$MOS transistor threshold voltages $\Delta V_{thp}$ negatively [114], [123], [145]–[147]. DTBT analysis depends on the assumption that interface traps respond (on average) much faster to changes in MOS surface potential than border traps. This difference in response time is due to the usual delay in communicating with traps in the oxide, as opposed to those directly at the interface [5], [101], [127], [148]. Using these plausible assumptions, expressions can be derived to estimate radiation-induced charges in radiation-induced interface-trap ($\Delta N_{it}$), border-trap ($\Delta N_{bt}$), and net bulk-oxide-trap ($\Delta N_{ot}$) charge densities per unit area [102], [127], [147]:

$$\Delta N_{it} \approx \Delta D_{itn}\phi_n + \Delta D_{itp}\phi_p, \tag{14}$$

$$\Delta N_{bt} \approx (C_{ox}/q)(\Delta V_{thn} - \Delta V_{thp}) - \Delta N_{it}, \tag{15}$$

$$\Delta N_{ot} \approx -(C_{ox}/2q)(\Delta V_{thn} + \Delta V_{thp}) + (\Delta D_{itn}\phi_n - \Delta D_{itp}\phi_p)/2. \tag{16}$$

Here $\Delta D_{itn}$ and $\Delta D_{itp}$ are the $n$MOS and $p$MOS transistor interface-trap densities (per unit area per unit energy) estimated from 1-MHz charge-pumping measurements using (for example) the technique developed by Groeseneken *et al.* [102], [149], and $\phi_n$ and $\phi_p$ are $n$MOS and $p$MOS transistor bulk potentials. In the DTBT method, contributions of border traps and interface traps to individual $n$ or $p$MOS transistors are not distinguished. Instead, Eq. (14) is a high-frequency weighted average of the radiation-induced interface-trap densities for $n$MOS and $p$MOS transistors, and average, effective border-trap densities through the accessible portion of the Si band gap (the center 0.7–0.8 eV) are obtained via Eq. (15) [102], [127].

Fig. 24 shows the oxide, interface, and border trap charge densities inferred from Eqs. (14)–(16) for MOS transistors with radiation-hardened 25 nm oxides irradiated with 10-keV X-rays

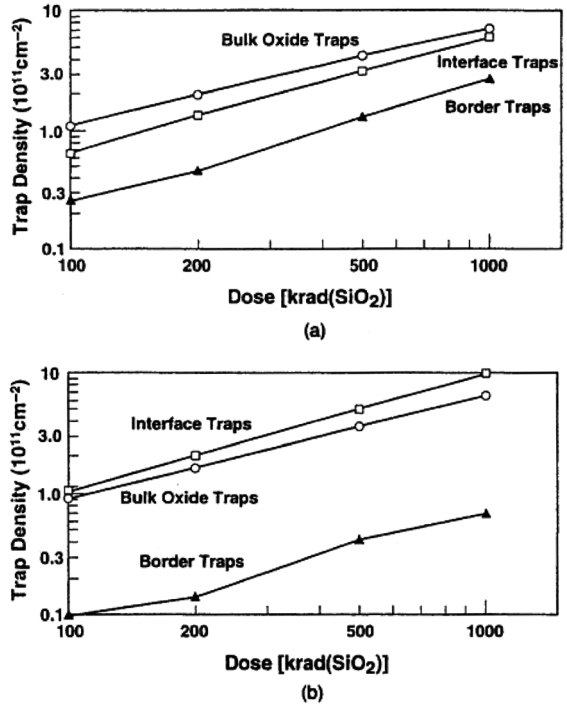


Fig. 24. Bulk oxide, interface, and border-trap charge densities inferred from Eqs. (14)–(16) for MOS transistors with 25 nm oxides irradiated with 10-keV X-rays at a dose rate of 158 rad(SiO$_2$)/s at an applied gate bias of 5 V for (a) transistors with $L = 1.2$ $\mu$m and $W = 50$ $\mu$m, and (b)$L = 50$ $\mu$m and $W = 50$ $\mu$m. (After Fleetwood et al. [102], © 1994, AIP).

to 1Mrad(SiO$_2$). The inferred border-trap densities are less than the inferred oxide- and interface-trap charge densities for these devices and irradiation conditions. In addition, Eq. (10) is used to estimate $\Delta D_{bt} \approx \Delta D_t(E_f)$ from noise measurements performed at room temperature before and after irradiation, and adjusted to cover the same portion of the Si band gap spanned by the DTBT method via [102]:

$$\Delta N_{bt}(\text{noise}) \approx (\phi_n + \phi_p)\Delta D_t(E_f) \tag{17}$$

Estimates of $\Delta N_{bt}$ (noise) at 1.0 Mrad(SiO$_2$) for the devices of Fig. 24 are (a) $3.6 \times 10^{11}$ cm$^{-2}$ and (b) $1.4 \times 10^{11}$ cm$^{-2}$. These values are (a) $\sim$ 1.3-times and (b) $\sim$ 2-times higher than DTBT estimates obtained via Eq. (16)[102]. This level of agreement is quite reasonable given the approximate natures of Eqs. (10) and Eqs. (14)–(17).

In the MOS noise literature, authors often attribute the observed noise to interface traps (e.g., [4], [65], [75]), instead of oxide or border traps, which is usually the result of obsolete and/or imprecise nomenclature [5], [7], [144]. However, there are some cases in which interface traps truly do appear to affect the observed low-frequency noise of Si/SiO$_2$ transistors. One example is relatively high-frequency noise. Tsai and Ma showed that, while the noise of $n$MOS transistors measured below $\sim$ 10 kHz scales with oxide-trap charge density, the noise at higher frequencies is affected more strongly by interface traps [101]. This occurs because charge exchange typically occurs more rapidly with defects at the Si/SiO$_2$ interface than with oxide or border traps [7], [101], [102]. The noise of $p$MOS

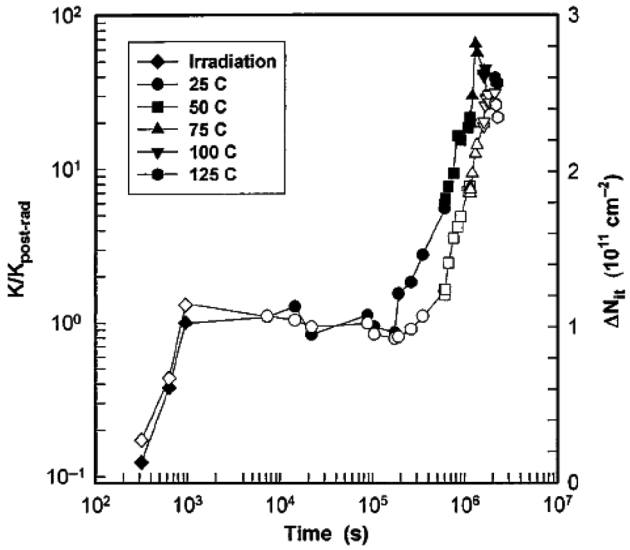


Fig. 25. Normalized noise magnitude $K$, relative to its level immediately after 75 krad$(SiO_2)$ irradiation (left hand scale, solid symbols), and effective interface-trap densities (right hand scale, open symbols) for $p$MOS transistors with 50 nm oxides fabricated by Oki Semiconductor that were irradiated at 25°C to 75 krad$(SiO_2)$ at $V_{GS} = 6$ V, and then annealed at 6 V bias for various times and temperatures. (After Johnson and Fleetwood [151], © 1997, AIP).

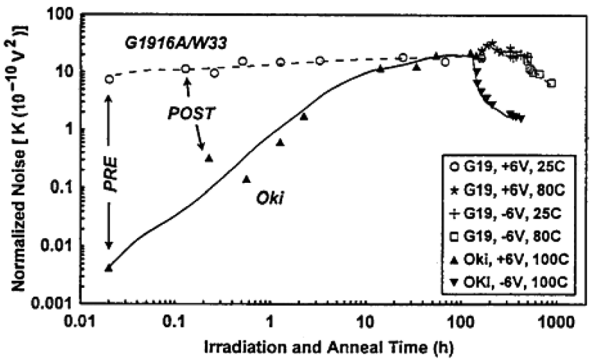


Fig. 26. Normalized noise magnitudes $K$ for Oki Semiconductor and Sandia (lot G1916A/W33) $p$MOS transistors as functions of irradiation and annealing time. The Oki devices were Co-60 irradiated at +6 V to 75 krad$(SiO_2)$ at 25 °C at a dose rate of 92 rad$(SiO_2)$/s; the Sandia devices were irradiated with 10-keV X-rays to 200 krad$(SiO_2)$ at 25 °C and a rate of 1667 rad$(SiO_2)$/s. (After Fleetwood et al. [112], © 1997, IEEE).

devices after irradiation or high-field stress has been observed sometimes (but not always) to correlate more closely with the buildup and annealing of interface-trap charge than oxide-trap charge [99], [150]. Fast trapping and recovery events that occur during NBTI measurements on $\mu$s-to-ms time scales also can result from interactions of charge carriers with either interface traps or fast border traps [88], [89], [127]–[132], [134], [135], [148].

A striking correlation between $1/f$ noise in $p$MOS devices and interface-trap buildup is shown in Fig. 25[112], [151]. In these devices, the interface-trap charge density is relatively stable for days, or even months at room temperature, but then increases dramatically [112], [151]–[154]. This "latent" interface trap buildup can be accelerated significantly by increasing the temperature at which a device is baked under bias after irradiation [152], [153]. Latent interface-trap buildup is associated with interactions of hydrogen with O vacancies in $SiO_2$, and is typically only seen in devices with large O vacancy densities [112], [154]. Why the post-irradiation noise of these devices correlates with interface-trap buildup is not completely understood [112]. But note that the noise increases nearly two orders of magnitude in Fig. 25, while the interface-trap density increases by less than a factor of three, so it is not *just* the increase in interface-trap density that leads to the increase in the noise.

The noise of the Oki transistors is compared with that of transistors with similar dimensions fabricated at Sandia National Laboratories [112] in Fig. 26. Each device traps positive charge in $SiO_2$ with high efficiency [82], [108], [109], [112], [153]. However, the pre-irradiation noise of the Sandia devices, which are known to be surface-channel devices, is much larger than that of the Oki devices. After the Sandia devices are irradiated to 200 krad$(SiO_2)$ with 10-keV X-rays, their noise increases by less than a factor of 2. In contrast, after the Oki devices are irradiated to 75 krad$(SiO_2)$, their noise increases by nearly a factor of 100. During the positive-bias annealing sequence in Fig. 26, the noise of the Oki devices increases until it is comparable to that of the Sandia devices. Hence, the data of Fig. 26 suggest the as-processed Oki devices may exhibit buried channel conduction [155]. This is commonly accomplished via shallow boron implantation, which enables surface scattering to be reduced, and the hole mobility to be increased. Separating the conduction channel from the surface reduces the $1/f$ noise [60] because the bulk Si has fewer defects than the interfacial region [60], [112]. This limits both the opportunity for charge exchange between channel carriers and interface or border traps, as well as the concomitant scattering.

After irradiation and/or positive-bias annealing, the conduction of the Oki devices evidently transitions from predominantly occurring in the buried channel to also occurring in the surface channel. This can happen when the implanted boron is passivated by hydrogen that transports through the $SiO_2$ and reacts with boron dopants [112], [156]–[158]. The strong correlation between the increases in noise and $\Delta N_{it}$ strongly suggests that the same sequence of events (i.e., hydrogen diffusion and reactions [153], [154]) leads to (1) a dramatic, delayed increase in $1/f$ noise, (2) a transition from surface to buried channel conduction, and (3) latent, thermally-activated interface-trap buildup [112]. While these results are intriguing, it should be noted that they are also quite unusual, since neither latent interface-trap buildup nor the strong correlation between low-frequency noise and interface-trap buildup illustrated in Fig. 25 is commonly observed in Si MOS transistors [7], [110], [112], [151]–[154].

### *D. Silicon-on-Insulator and Multi-Gate Devices*

The noise of MOS transistors built on silicon-on-insulator (SOI) wafers can be larger than that of otherwise equivalent transistors on bulk wafers, because higher defect densities are often associated with buried channel or sidewall oxides than with gate oxides [159]–[161]. Fig. 27 shows a schematic diagram developed by Simoen *et al.* [156] which shows that relatively lower noise levels typically are exhibited by partially depleted (PD) SOI transistors, bulk transistors, and fully depleted

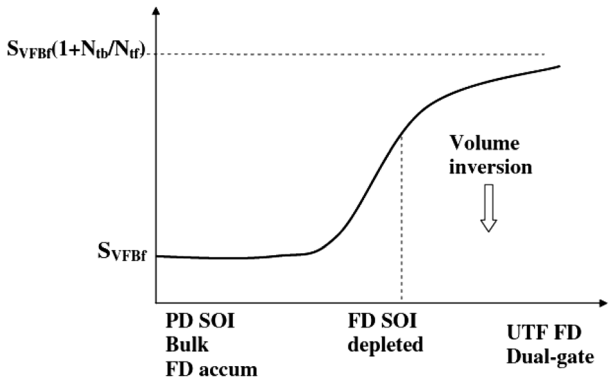


Fig. 27. Schematic illustration of the relative noise magnitudes of partially and fully depleted SOI MOSFETs built in single or multiple-gate technologies. It is assumed for this comparison that the interface of highest quality (lowest defect density) is the Si/gate oxide interface. Volume inversion increases the mobility and reduces the noise. (After Simoen et al. [161], © 2007, Elsevier).

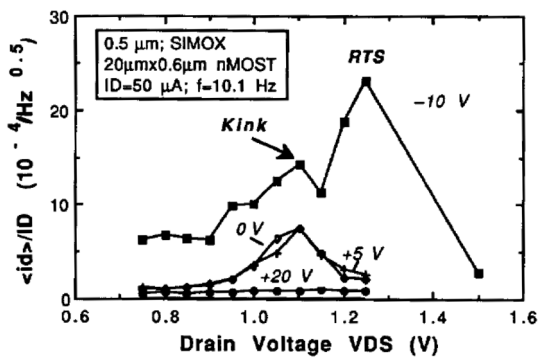


Fig. 28. Normalized room-mean square current noise of a partially depleted SOI transistor. The gate oxide thickness is 20 nm. (After Simoen et al. [160], © 1994, IEEE).

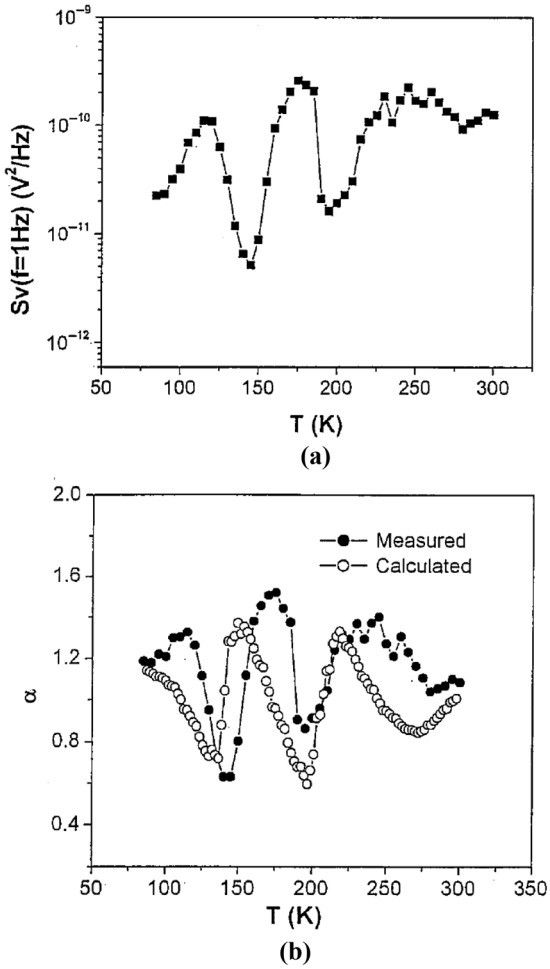


Fig. 29. Excess drain-voltage noise power spectral density $S_V$ and (b) frequency dependence $\alpha$ for PD SOI MOSFETs with 170 nm SIMOX buried oxides, with $L = 0.6\,\mu$m, $W = 2.3\,\mu$m, and gate oxide thickness of 12 nm. Noise measurements were performed at a back-gate bias that was 4 V above threshold, at $V_D = 100\,$mV. Eq. (7) was used to calculate values of $\alpha$. (After Xiong et al. [168], © 2003, SPIE).

(FD) SOI transistors with the back-gate in accumulation. These are cases in which charge exchange with defects in the buried oxide is limited. Relatively higher noise levels can be observed for FD SOI transistors with the back-gate in depletion, and/or for ultrathin film (UTF) FD or multiple gate transistors, which are cases for which charge exchange with the buried oxide occurs more easily [161]. However, dual-gate devices can exhibit "volume inversion," in which lateral and/or back gates can cause the current to flow preferentially in the bulk of the MOSFET body, away from interfaces, thereby reducing surface scattering and carrier-defect interactions [162]–[165]. This increases the mobility of the device and reduces the noise, compared to levels that would otherwise be observed [161]–[165].

Floating body effects can increase the noise of partially depleted devices [159]–[161]. For example, Fig. 27 shows the root-mean-square current noise normalized by the bias current, a ratio that is proportional to $(S_I/I^2)^{1/2}$, as a function of drain bias for partially depleted SOI transistors built on SIMOX wafers [160]. The back-gate bias strongly affects the noise of these devices. When the drain is biased with $V_{DS}$ in the range of $\sim 1.0$ V to $\sim 1.5$ V, the noise can be enhanced greatly. For the case of $-10$ V back gate bias and $V_{DS} = 1.25$ V, random telegraph noise is observed because the channel resistance is unstable at these voltages [159]–[161]. This is the "kink region," caused by impact ionization that leads to charge buildup in the body. The fluctuations in charge density that occur in the body with time over this range of biases lead to corresponding changes in the surface potential and therefore in the channel resistance [166], [167]. This kink-related enhancement of the noise does not occur in fully depleted devices, for which the body potential is under complete gate control [160], [161].

The noise of SOI devices can be measured for the top and back gate devices separately. For example, Xiong *et al.* measured the temperature dependence of the low-frequency noise associated with the buried-oxide-to-Si interface of SOI MOSFETs [168]. Fig. 29 shows (a) the noise magnitude and (b) the frequency dependence of the noise of PD SOI transistors with 170 nm SIMOX buried oxides. Several broad peaks are observed in Fig. 29(a), associated with defects in the buried oxide. While the microstructure of these defects is not known, O vacancies and other oxygen deficient centers are commonly observed in SIMOX and other SOI buried oxides [169]–[172], and the peak locations for the buried oxides in Fig. 29 are similar to

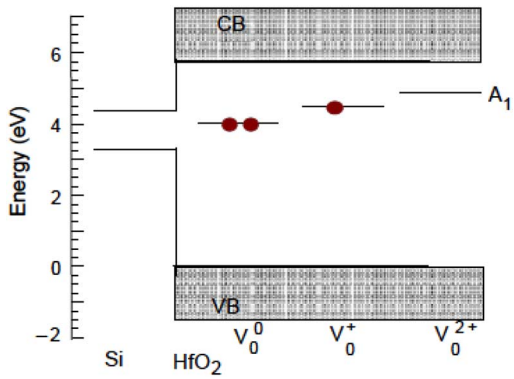


Fig. 30. Energy levels of O vacancies in $HfO_2$, calculated using density functional theory. (After Robertson et al. [179], © 2006, Elsevier).

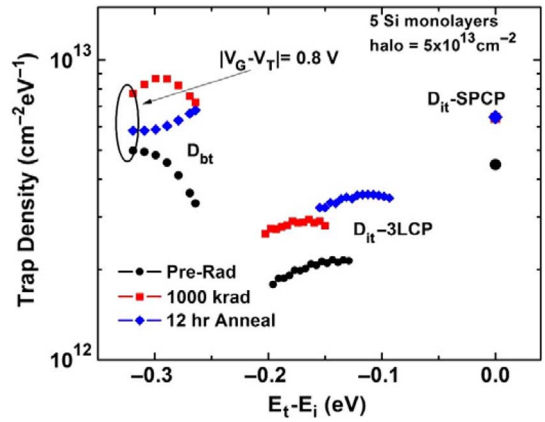


Fig. 31. Effective density of border traps $D_{bt}$ obtained from measurements of $1/f$ noise, and estimated densities of interface traps $D_{\rm it}$ from three-level (3LCP) and square-pulse (SPCP) charge pumping measurements, as a function of trap energy $E_t - E_i$ referred to the Ge band gap, for Ge $p$MOSFETs with a 4 nm $HfO_2$ gate dielectric, and $W/L = 9.8\ \mu{\rm m}/5\ \mu{\rm m}$. Irradiations were performed with a 10-keV X-ray source at a dose rate of $31.5\ {\rm krad(SiO_2)/min}$. All irradiations and measurements were performed at room temperature, with the drain and source biased at $-1$ V and all other terminals grounded. (After Francis et al. [31], © 2012, IEEE).

those of the MOS gate oxides in Fig. 16. This suggests that O vacancies are responsible for the noise in both cases. The buried oxides in Fig. 29 were not irradiated prior to noise measurement. For differently processed SIMOX buried oxides that were exposed to ionizing radiation before noise measurement, diffusion noise was observed in addition to $1/f$ noise [168], most likely as a result of proton motion in the buried oxide [20], [168], [173].

### *E. High-K Dielectrics and Alternate Channel Devices*

The above examples all refer to transistors with $SiO_2$ gate dielectrics. High-K gate dielectrics are increasingly used in CMOS IC fabrication. Typically, transistors with high-K dielectrics have higher defect densities and correspondingly higher noise magnitudes than devices with $SiO_2$ gate dielectrics. Of most practical current interest is the noise of transistors with gate stacks that incorporate $HfO_2$ dielectric layers [174]–[176], which inevitably include a thin interfacial layer (typically a few monolayers) of $SiO_2$. While the microstructures of the specific defects that lead to the noise in transistors with high-K gate stacks are not known in detail, a wide variety of defects have been identified in $HfO_2$, with O vacancies once again being among the most significant [177]–[181]. For example, Fig. 30 shows calculations of O vacancy levels in $HfO_2$ performed by Robertson *et al.* These show that the neutral O vacancy has a gap state at a suitable level for metastable charge exchange with Si [179], making it a strong candidate for the dominant defect causing low frequency noise in MOS devices with $HfO_2/SiO_2$ gate dielectrics.

Advancements in developing high-K dielectrics and epitaxial growth methods have enabled the development of Ge channel devices that are candidates for incorporation into highly-scaled CMOS technologies in the near future [182], [183]. The defects that lead to low-frequency noise in these devices are similar to those that cause $1/f$ noise in Si channel devices. Fig. 31 shows a comparative study of the interface-trap and border-trap densities for Ge channel devices that have a five-monolayer Si cap and $HfO_2/SiO_2$ gate dielectric layers, before and after the devices were irradiated to $1{\rm Mrad(SiO_2)}$ with 10-keV X-rays, and after the devices were annealed for 12 h at room temperature. The noise measurements were performed as a function of gate voltage, and energy levels are referenced to the Ge band gap [31]. This benchmark is useful for comparing effective interface-trap and border-trap densities as a function of gate bias, but does not provide information regarding the energy levels of defects in the $HfO_2/SiO_2$ dielectric layers, as noted in Sections III-A and III-B. Before and after irradiation, trap densities in Fig. 31 are 1-2 orders of magnitude higher than the interface and border trap densities of $Si/SiO_2$ devices in Fig. 24 above, as a result of the higher defect densities associated with the high-K dielectrics and/or $Ge/Si/SiO_2$ interfacial layers [31]. Similarly elevated defect densities and noise levels are observed for III-V devices with high-K gate dielectrics [29], [184]. A significant reduction in defect density is required before these devices can enter mainstream CMOS manufacturing.

### *F. SiC MOS Devices*

Wide-band-gap semiconductors like SiC exhibit low-frequency noise that is associated with both interface traps and border traps [32], [33], [185], [186]. The role of interface traps is relatively more important in wide-gap semiconductors than narrow-gap materials because much slower time constants are associated with deep interface traps in wide gap materials than for typical interface traps in Si or Ge [187], [188]. Fig. 32 shows the excess input-referred gate-voltage noise power spectral density $S_{vg} = S_{Vd}(V_{GS} - V_{th})^2/V_d^2$ and effective trap density $D_t(E_f)$ at ~10 Hz as a function of temperature for SiC MOS devices with a 55 nm NO-nitrided oxide. The magnitude of the $1/f$ noise decreases by $\sim$ 77% as the temperature increases from 85 K to 510 K. Using Eq. (10), the effective density of traps $D_t(E_f)$ is estimated to be $\sim\ 2.3 \times 10^{13}\ {\rm eV^{-1}cm^{-2}}$ at $T = 85$ K, $\sim\ 2.6 \times 10^{12}\ {\rm eV^{-1}\ cm^{-2}}$ at $\sim$ 300 K, and $\sim\ 1 \times 10^{12}\ {\rm eV^{-1}\ cm^{-2}}$ at $\sim$ 510 K. The decrease in noise with increasing temperature is consistent with the decrease in the effective density of charged interface traps.

Fig. 33 shows the frequency dependence of the noise ($\alpha$) as a function of T for the data of Fig. 32. The overall shape of the measured $\alpha(T)$ curve is consistent with the Dutta-Horn model

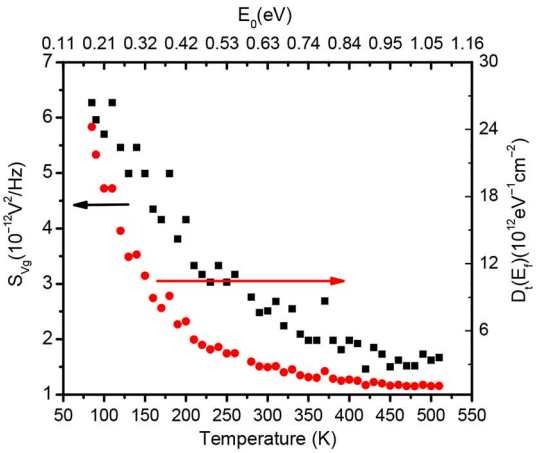


Fig. 32. Excess input-referred gate-voltage noise power spectral density $S_{vg}$(left axis) $= S_{Vd}(V_{GS} - V_{th})^2/V_d^2$ and calculated effective density of traps $D_t(E_f)$ at $\sim$ 10 Hz (right axis) vs. temperature from 85 K to 510 K, for SiC MOS devices with a 55 nm gate oxide that received a post-oxidation NO anneal at 1175 °C for 2 hours. (After C. X. Zhang et al. [33], © IEEE, 2013).

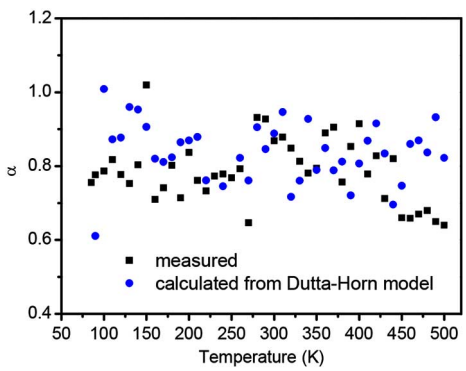


Fig. 33. Measured and predicted values of the frequency dependence of the noise, $\alpha = -\partial \ln S_V / \partial \ln f$, using the experimental results from Fig. 32 and Eq. (7) of the text. (After C. X. Zhang et al. [33], © 2013, IEEE).

prediction. This enables the use of Eq. (8) to estimate the energy distribution of defects, as shown on the upper x-axis of Fig. 32. First principles calculations using DFT show that carbon vacancy clusters on the SiC side of the $SiC/SiO_2$ interface (see Fig. 34) have activation energy levels of $\sim$ 0.1 to 0.2 eV [33]. These defects appear to account for at least some of the increased noise at low temperature [32], [33]. Fluctuations in occupancy of N dopants [189]–[191] may also contribute to the increase in noise magnitude with decreasing temperature that is observed in Fig. 32. Hence, the defects that cause low-frequency noise in SiC MOS devices, especially at low temperatures, can be quite different both in location and in microstructure from those responsible for the noise in Si MOS devices.

## V. GaN/AlGaN HEMTs

The application of Dutta-Horn analysis (Eqs. (7) and (8)) and DFT calculations have also provided significant insight into the low-frequency noise of GaN/AlGaN high-electron mobility transistors (HEMTs). Fig. 35 shows the low frequency noise measured over a temperature range of 85 K to 450 K for GaN/AlGaN HEMTs grown under Ga rich conditions by molecular beam epitaxy (MBE) on 4H-SiC substrates [34].

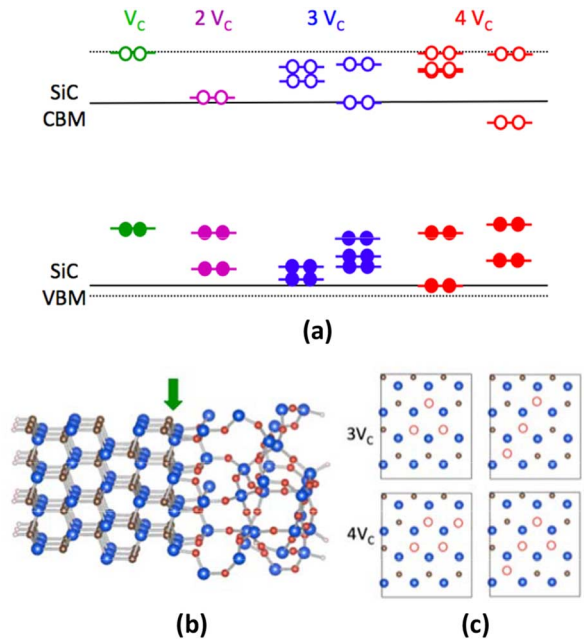


Fig. 34. (a) Defect levels of C vacancy clusters on the SiC side of the $SiC/SiO_2$ interface. The dotted black lines represent the SiC conduction and valence bands, obtained from the interface model shown in (b). The solid black lines represent the band positions after correcting for the quantum confinement effect due to the finite slab thickness. (c) Locations of removed C atoms are shown for the first SiC layer (green arrow in (b)) for the clusters of 3 and 4 C vacancies in (a). (After C. X. Zhang et al. [32], © 2013, IEEE).

The devices were irradiated with 1.8 MeV protons to a fluence of $10^{14}$ protons/cm$^2$ using the Vanderbilt Pelletron facility, with all pins grounded. That the low-frequency noise is well described by the model of Dutta and Horn is verified in Fig. 36, which enables us to relate the temperature dependence of the noise to the defect-energy distribution via Eq. (8) in Fig. 35. Peaks are observed in the noise magnitude at $\sim$ 90 K and $\sim$ 400 K, which correspond to energies of $\sim$ 0.2 eV and $\sim$ 0.9 eV, respectively. The magnitude of the low-temperature peak increases with irradiation, and the high temperature peak decreases by a similar amount. In addition, a noise peak at $\sim$ 0.5 eV is observed after proton irradiation. After a fluence of $10^{14}$ protons/cm$^2$, this new peak decreases, and the 0.2 eV peak increases significantly. The 0.9 eV peak does not change significantly with fluence. Interestingly, the $1/f$ noise magnitude at room temperature actually *decreases* with irradiation for these devices [34].

DFT calculations suggest that the peak at $\sim$ 0.2 eV observed in the GaN/AlGaN noise is most likely due to an oxygen DX center in AlGaN; i.e., $O_N$ [192]. The 0.9 eV and 0.55 eV peaks observed in Fig. 35 are most likely associated with hydrogenated substitutional oxygen impurities, i.e., $O_N - H$ defects, which are depicted schematically in Fig. 37. The DFT calculations show that the energy barriers for reconfiguration of the $O_N - H$ defect complexes are 1.0 and 0.5 eV for structures I and II in Fig. 37(a), respectively. These barriers reflect the energy that is required for a hydrogen atom to move near a substitutional oxygen atom. Thus, if H is initially in configuration I, then an energy of $\sim$ 1 eV is required to move it into configuration II, after which electron capture is favored, leading to a

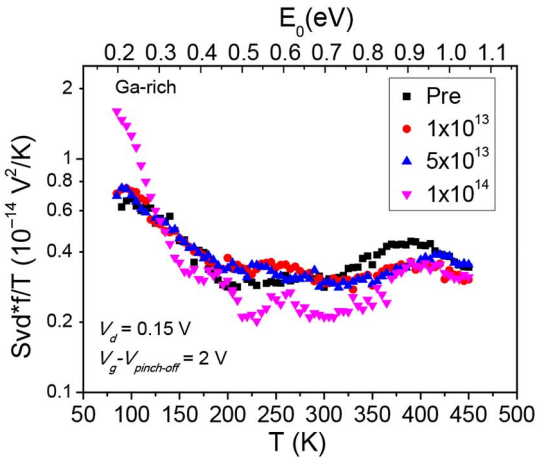


Fig. 35. Normalized noise at $f = 10$ Hz, before and after proton irradiation, for Ga-rich HEMTs. Here $V_g - V_{pinch-off} = 2$ V, and $V_d = 0.15$ V. The devices are 150 $\mu$m wide. The gate length ($L_G$) is 0.7 $\mu$m, the gate-to-drain separation ($L_{GD}$) is 1 $\mu$m, and the gate-to-source separation ($L_{GS}$) is 0.5 $\mu$m. The energy scale on the upper x-axis is derived from Eq. (7). Fluences are quoted in protons/cm$^2$. (After Chen et al. [34], © 2013, IEEE).

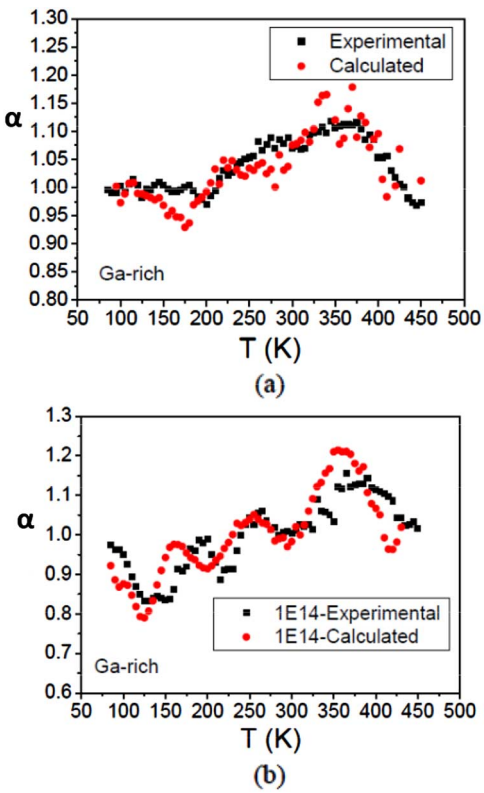


Fig. 36. Measured and predicted values of the frequency dependence of the noise, $\alpha = -\partial \ln S_V / \partial \ln f$, using the experimental results from Fig. 35 and Eq. (7) of the text. (After Chen et al. [34], © 2013, IEEE).

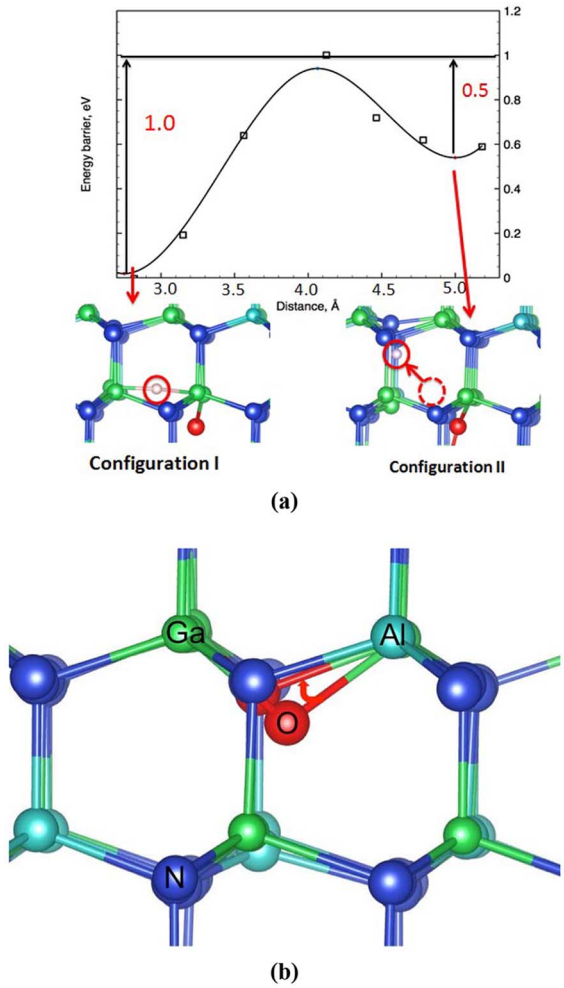


Fig. 37. (a) Energy barriers as a function of O-N distance and defect configurations (I) and (II) of $O_N - H$ (smaller light atom) and (b) $O_N$DX configurations, which are consistent with the defect energy levels shown for the devices of Fig. 35. (After Chen et al. [34], © 2013, IEEE).

0/-1 charge state transition. However, if a negatively charged $O_N - H$ defect is in configuration II, then after releasing an electron, only 0.5 eV is necessary to switch to configuration I.

During proton irradiation, a H atom can be removed from an $O_N - H$. This can occur via interaction of transporting holes with the $O_N - H$, a process that is similar to what occurs in irradiated $Si/SiO_2$ structures when a transporting H is near an O-H complex [157], [193], [194]. This reaction occurs with a low energy barrier, as shown in Fig. 37(a). The decreases in the 0.9 eV defect peak and increases in the 0.2 eV defect peak each can be related to hydrogen removal from the $O_N - H$ complex [34]. The resulting reactions reduce the $O_N - H$ density and increase the $O_N$ defect density, as shown in Fig. 37(b). The small peak near 0.55 eV in Fig. 35 is likely caused by a reverse transition from configuration II in Fig. 37(a) to configuration I. At larger fluences, the reductions in the 0.9 eV and 0.55 eV peaks are much smaller than the increase in the 0.2 eV peak, strongly suggesting that new low-energy defects also are generated at the highest fluences by proton irradiation. These newly created defects most likely are N vacancies [192], [195].

At least some defects with different microstructures are observed if devices are exposed to high-field stress, instead of proton irradiation. Fig. 38 shows the noise of a GaN/AlGaN HEMT that is similar to the devices of Figs. 35 and 36 which was exposed to a series of stresses with increasing drain bias [196], leading to significant transconductance degradation [196], [197]. For each bias condition, devices are stressed for $\sim$ 11 h. Prominent defect peaks are observed at temperatures of $\sim$ 80 K, $\sim$ 220 K, and $\sim$ 350 K, with the greatest increase in

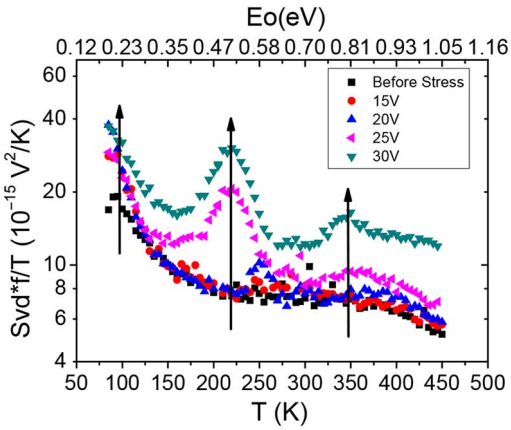


Fig. 38. Normalized noise magnitude at $f = 10$ Hz as a function of temperature and high-field stress. The noise is measured in the linear region of device response, with $V_{ds} = 0.1$ V and $V_{gs} - V_{th} = 2$ V. The normalization is equivalent to the inferred defect-energy distribution $D(E_0)$ from Eq. (8). (After Chen et al. [191]).

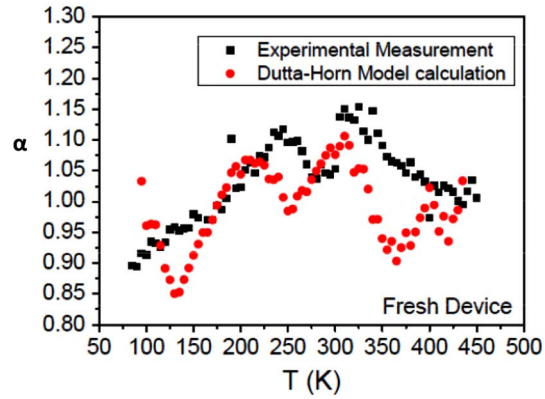


Fig. 39. Measured and predicted values of the frequency dependence of the noise, $\alpha = -\partial \ln S_V / \partial \ln f$, using the experimental results from Fig. 38 and Eq. (7). These results are for an unstressed device. Similarly good agreement is found for devices that have been stressed. (After Chen et al. [191]).

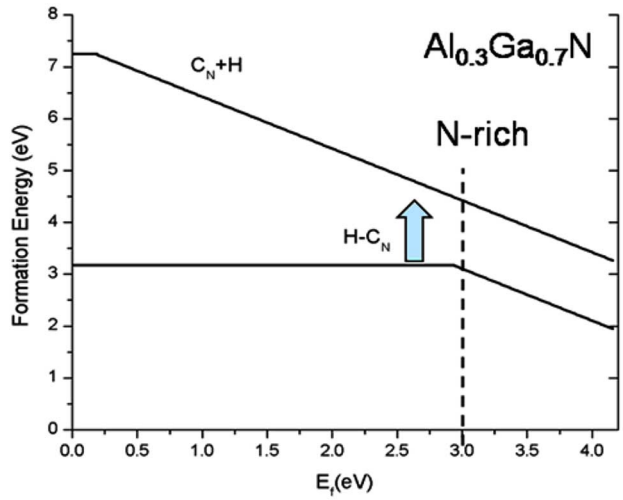


Fig. 40. Formation energy of substitutional carbon at an N-site versus Fermi energy in AlGaN. The singly hydrogenated defect can fluctuate between the negatively charged state (sloped line) and neutral state (flat line) for typical operating conditions, for which $E_F \approx 3.0$ eV, contributing to the observed noise. The completely dehydrogenated state is negatively charged for all typical operating biases. (After Roy et al. [204], © 2011, IEEE).

post-stress noise occurring for the 220 K peak. The temperature dependence of the noise is described well by the Dutta-Horn model (Fig. 39), allowing us to estimate defect energy distributions via Eq. (8), as shown on the upper x-axis in Fig. 38. After 20 V stress, a large increase in the 0.2 eV peak is observed, along with a small peak near 0.6 eV. A large peak at $\sim 0.57$ eV grows at higher stress levels. Another small peak appears at 0.8 eV [196].

DFT calculations were performed to identify the defects responsible for peaks in the energy distributions in Fig. 38, with an emphasis on Fe centers, since these are known from previous work to often lead to defect peaks at or near $\sim 0.57$ eV [198]–[200]. These defects can be passivated by hydrogen during growth, and depassivated during high-field stress. Upon dehydrogenation by hot electrons, $\mathrm{V_N - Fe_{Ga}}$ and $\mathrm{V_{Ga} - V_N}$ complexes are found to be responsible for the central noise peak in Fig. 38[196]. Another defect that contributes to the post-stress noise in this energy range is $\mathrm{V_{Ga} - O_N - H}$ which, upon dehydrogenation, has an energy level in the same range [196]. Hydrogenated Ga vacancies and divacancies ($\mathrm{V_{Ga} - V_N}$) also contribute to the central peak [201]. In contrast, the growth of the 0.2 eV defect is due to stress-induced dehydrogenation of an $\mathrm{O_N - H}$ complex [34], similar to what is found after proton irradiation in Fig. 35. DFT calculations also suggest that the increase in the 0.8 eV peak during stress mayb be caused by migration of $\mathrm{V_{Ga}}$ to form a $\mathrm{V_{Ga} - O_N - H}$ defect complex. The migration barrier of $\mathrm{V_{Ga}}$ is $\sim 1$ eV in the absence of an electric field, and is lowered in the presence of electric field due to the high charge state of the defects [202].

In the above discussions, we have focused primarily on defects that are responsible for increases in noise magnitude. For example, dehydrogenation of the $\mathrm{O_N}$ defect in AlGaN can lead to a significant increase in noise at low temperature. During both irradiation (e.g., Fig. 35[34]) and hot-carrier-stress [203], [204], the noise at a given temperature can also decrease. Fig. 40 shows a formation energy diagram for a different impurity: substitutional C in AlGaN. The slope of the line denotes the charge state of the defect [200]. In Fig. 40, the flat portion of the curve denotes a neutral charge state; the sloped regions denote charge of $-1$. A defect that contributes to noise must be able to fluctuate in charge state during measurement, which the $\mathrm{H - C_N}$ can do, but the bare carbon impurity cannot. Removing the H from the $\mathrm{C_N}$ therefore leads to a shift in threshold voltage, but a decrease in noise. Thus, it is not possible to predict without computational study whether removing hydrogen via irradiation or hot-carrier stress will increase or decrease the contribution of a defect or impurity center to the noise [200], [203], [204].

## VI. A Brief Note on Bipolar Transistors

The low-frequency noise of bipolar junction transistors (BJTs) has also been studied extensively for more than 40 years [6], [37], [38], [205]–[208]. Depending on the transistor geometry and bias conditions, shot noise, thermal noise, Lorentzian noise due to a single prominent trap that functions as a generation-recombination center, and/or $1/f$ noise due to a distribution of traps are all commonly observed [205]–[208]. There is evidence that "MOS-like" noise can be observed from defects in the oxide that overlies the base-emitter junction

of BJTs with poly-crystalline Si emitters [206], [209]–[211]. However, although the temperature dependence of the noise of BJTs has been measured by a number of authors [207], [212]–[214], current knowledge about the microstructure of the defects responsible for the noise is not nearly as advanced for BJTs as for MOS devices, or even for GaN HEMTs. The interested reader is directed to [214], e.g., for a review of these studies. Similar phenomena are observed in SiGe and GaAs heterojunction bipolar transistors [207], [215]–[218]. Clearly, this is an area where future work focused on underlying defect properties would benefit the field greatly.

## VII. Summary and Conclusions

The model of $1/f$ noise developed by Dutta and Horn [1] has now been evaluated and found to describe well the responses of a wide variety of materials and several different types of semiconductor devices. These include thin metal films, Si and SiC MOSFETs, and GaN/AlGaN HEMTs. It is the overwhelming conclusion of these studies that the dominant source of low-frequency noise in microelectronic materials is carrier-defect interactions that lead to fluctuations in the number of charge carriers in the device. Changes in the charge state of a defect also affect the scattering rate. A first-order estimate of the effective defect density can be obtained using a simple number fluctuation model of the noise that was originally developed by A. L. McWhorter [12], which is straightforward to apply to MOS transistors that are operating in the linear mode [62], [63], [82]. Employing the Dutta-Horn and/or number-fluctuation models of $1/f$ noise enables one to obtain estimates of the relevant, effective defect-energy distributions for MOS transistors that agree with estimates obtained via other techniques to within a factor of $\sim 2$. Density functional theory calculations facilitate the identification of the microstructures of the defects that are responsible for the low-frequency noise of MOS transistors and GaN/AlGaN HEMTs. In the future, the application of similar techniques to present and emerging microelectronic devices and materials is likely to provide similarly significant insights into their low-frequency noise and the defects that limit their performance, reliability, and radiation response.

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