Influence of Transfer Gate Design and Bias on the Radiation Hardness of Pinned Photodiode CMOS Image Sensors

Vincent Goiffon, *Member, IEEE*, Magali Estribeau, *Member, IEEE*, Paola Cervantes, Romain Molina, Marc Gaillardin, *Member, IEEE*, and Pierre Magnan, *Member, IEEE*

***Abstract*—The effects of Cobalt 60 gamma-ray irradiation on pinned photodiode (PPD) CMOS image sensors (CIS) are investigated by comparing the total ionizing dose (TID) response of several transfer gate (TG) and PPD designs manufactured using a 180 nm CIS process. The TID induced variations of charge transfer efficiency (CTE), pinning voltage, equilibrium full well capacity (EFWC), full well capacity (FWC) and dark current measured on the different pixel designs lead to the conclusion that only three degradation sources are responsible for all the observed radiation effects: the pre-metal dielectric (PMD) positive trapped charge, the TG sidewall spacer positive trapped charge and, with less influence, the TG channel shallow trench isolation (STI) trapped charge. The different FWC evolutions with TID presented here are in very good agreement with a recently proposed analytical model. This work also demonstrates that the peripheral STI is not responsible for the observed degradations and thus that the enclosed layout TG design does not improve the radiation hardness of PPD CIS. The results of this study also lead to the conclusion that the TG OFF voltage bias during irradiation has no influence on the radiation effects. Alternative design and process solutions to improve the radiation hardness of PPD CIS are discussed.**

***Index Terms*—Active pixel sensor (APS), charge transfer efficiency (CTE), CMOS image sensor (CIS), CTI, dark current, deep submicron process, DSM, equilibrium full well capacity (EFWC), full well capacity (FWC), gamma-ray, image sensor, integrated circuit, interface states, ionizing radiation, monolithic active pixel sensor (MAPS), pinned photodiode (PPD), pinning voltage, pre-metal dielectric (PMD), radiation damage, radiation effect, radiation hardening, RHBD, shallow trench isolation (STI), spacer, total ionizing dose (TID), transfer gate (TG), trapped charge.**

I. Introduction

NOWADAYS, pinned photodiode CMOS image sensors (PPD CIS) [1] are the most popular solid-state image sensors for visible applications. In particular, this technology of imager is used in a growing number of applications where a good ionizing radiation hardness is required (e.g. space remote sensing applications, medical imaging, scientific instruments, nuclear power plant safety, particle physics instruments, military applications…). In order to anticipate these device behaviors in radiation environment and to possibly improve their hardness, the first step is to understand and localize the degradations. However, the total ionizing dose (TID) induced degradations in PPD CIS are not well identified and their origins are still unclear.

TID induced dark current increase in PPD CIS has been reported by several workers and several degradation sources have been proposed (illustrated in Fig. 1): the peripheral trench isolation (source 1 Fig. 1) around the PPD in [2], [3], [4], the transfer gate (TG) channel oxides (sources 3 (shallow trench isolation (STI) sidewall) and 4 (gate oxide)) [4], [5], [6], the PMD (pre-metal dielectric) on top of the PPD and/or the TG sidewall spacer (sources 2 and 5) [5], [6].

Moreover, additional radiation induced effects have recently been reported, such as charge transfer efficiency (CTE) and full well capacity (FWC) variations with TID [6], [7]. As for dark current, the mechanisms behind these degradations have still to be understood. Nevertheless, it seems clear that the TG and its vicinity play a key role in these parasitic effects.

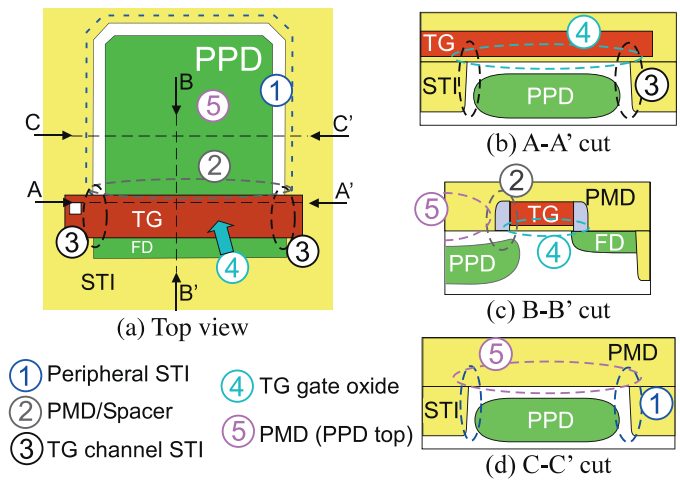

Fig. 1. Possible degradation sources in TID irradiated PPD CIS. PPD = pinned photodiode, TG = transfer gate, FD = floating diffusion, STI = shallow trench isolation and PMD = pre-metal dielectric.

Manuscript received July 11, 2014; revised September 19, 2014; accepted September 20, 2014. Date of publication October 29, 2014; date of current version December 11, 2014.

V. Goiffon, M. Estribeau, P. Cervantes, R. Molina, P. Magnan are with ISAE, Université de Toulouse, Image Sensor Research Team, F-31055, Toulouse, France (e-mail: vincent.goiffon@isae.fr).

M. Gaillardin is with CEA, DAM, DIF, F-91297 Arpajon, France.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNS.2014.2360773

Another important topic, especially for qualification tests, is the effect of bias conditions during irradiation. It has been recently observed that, up to 10 kGy, sensors grounded during irradiation behave similarly to sensors operated with nominal bias and command signals during irradiation [6]. This experiment was performed with a negative TG OFF voltage (V_{LOTG}) during exposure. If the radiation damage is related to the TG, a positive V_{LOTG} voltage during exposure could possibly enhance the degradation. Since both positive and negative V_{LOTG} are used in commercial products and scientific instruments, it appears here again that a clarification is necessary.

The main purpose of this work is to advance the understanding of the reported TID induced effects in PPD CIS by comparing selected pixel designs in which the TG and its vicinity have been modified to differentiate the degradation mechanisms. A similar approach was developed in [5] but it was then focused on dark current and mainly on PPD dimension variations which were not sufficient to study properly the TG related effects. A secondary objective is to determine if the sole radiation-tolerant design that has been proposed in literature [8], [9] really improves the radiation hardness of the pixel. Finally this study also addresses the influence of V_{LOTG} during irradiation.

After the presentation of the experiment and the studied devices, the experimental results are presented and briefly analyzed in the third part. Finally, in the last part before the conclusion the degradation mechanisms and their localization are further discussed.

II. Experimental Details

A CMOS imager, constituted of $256 \times 256 - 7$ μm-pitch-4T-PPD pixels has been designed and manufactured using a 180 nm pinned photodiode CIS process of a world leading Asian foundry (same foundry as technology B in [6]). Three identical integrated circuits have been tested and irradiated for this study. The sensor is divided in ten sub-arrays each constituted of about 6550 identical pixels. Seven of these sub-arrays were used to study PPD and TG design variation effects. These seven layouts are illustrated in Fig. 2 and their key features are listed in Table I.

Most of the pixel types (except the enclosed layout ones) have a square PPD of about 2.5×2.5 μm^2 and they mainly differ from each other by the layout of the TG or its immediate vicinity. The TG design of the Ref pixel is a direct implementation of the minimum design rules of this process. It is interesting to notice that this layout generates a little bottleneck before the TG. Since when the PPD width is reduced, the pinning voltage is also reduced [10], [11], this bottleneck is likely to induce a potential barrier. Pixel LongTG is the same except that the TG length is doubled, it should reveal any effect linked to TG length or area. Pixel LongBN is the same as Ref except the bottle neck part is longer (it should induce a higher barrier and inform on the role of the barrier on the degradation). In WideTG, the bottleneck is suppressed and the TG runs along the PPD border. STI0.7 is similar to LongBN except that the STI is recessed 0.7 μm away from the PPD. Finally, two enclosed layout TG (ELTG) designs have been used. Such design is supposed to improve the radiation hardness of the PPD [8], [9], especially to reduce

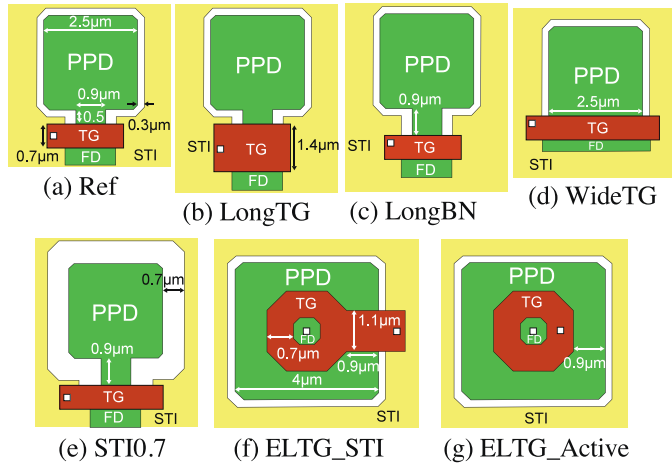

Fig. 2. Photodiode, TG and FD layouts of the studied pixels (a) Ref, (b) LongTG, (c) LongBN, (d) WideTG, (e) STI0.7, (f) ELTG_STI, (g) ELTG_Active.

TABLE I
Key Features of the Studied Pixels

	Ref	LongTG	LongBN	WideTG	STI0.7	$\mathrm{ELTG_{STI}}$	$\mathrm{ELTG_{Act.}}$
V_{pin} (V)	0.58	0.57	0.47	0.63	0.47	0.59	0.59
C_{ppd} (fF)	7.5	7.7	8.2	7.6	7.3	9.8	10.2
EFWC (ke^-)	23	23	22	23	18	32	34
FWC_{Φ}^{dep} (ke^-)	38	38	39	37	33	45	46
FWC_{Φ}^{acc} (ke^-)	41	41	41	40	36	46	46
A_{ppd} (μm^2)	6.7	6.7	7	5.8	7	12	11
P_{ppd} (μm)	11	11	12	10	12	16	15
A_{TG} (μm^2)	1	2.1	1	2.1	1.6	4.4	3.4
L_{TG} (μm)	0.7	1.4	0.7	0.7	0.7	0.7	0.7
W_{TG} (μm)	1.5	1.5	1.5	3.1	2.3	8	7.3
CVF ($\mu V/e^-$)	25	25	25	18	25	25	25

the dark current increase with irradiation. There are two ways to realize this design based on the cross sectional view presented in [8]. The first one is to extend the polysilicon gate to the STI to allow the contact formation (as in the $\mathrm{ELTG_{STI}}$ pixel). Another solution is to directly contact the gate on the active region ($\mathrm{ELTG_{Active}}$). This second solution should lead to better results since the TG channel never reach the STI, however, such "gate contact on active" is forbidden by the design rules of most CMOS foundries.

If not stated otherwise, the measurements have been performed at 22°C with high and low TG bias levels set to $V_{\mathrm{HITG}} = 3.3$ V and $V_{\mathrm{LOTG}} = -0.6$ V respectively and with the pixel and reset supply voltages fixed to 3.3 V[1]. All the full well capacities obtained under illumination ($\mathrm{FWC_{\Phi}}$) were measured with a photon flux approximately equal to 2×10^{12} photon.s^{-1}.cm^{-2}. The maximum FWC values reached in this study (i.e. at the maximum photon flux) was still in the linear range of the readout chain and in the input range of the off-chip analog to digital converter (ADC) for all the studied pixels. Therefore, the saturation levels reported here correspond well to the photodiode FWC and not to the readout chain or ADC saturation voltage.

All the ^{60}Co irradiations were performed "biased" (i.e. operated with nominal bias voltages and standard dynamic command signals), at 6 $\mathrm{Gy(SiO_2)/h}$ (and room temperature), at TRAD facility, Toulouse, up to a maximum dose of

[1]The reset (RST) MOSFET has a negative threshold voltage and the device is then operated in hard reset mode [12].

10 kGy(SiO_2). During a CIS operation, the TG is turned ON less than 1 μs and the rest of the time (i.e. the frame duration, which was about 40 ms during the radiation exposure), the TG is OFF and thus biased to V_{LOTG}. Therefore, the most important voltage to study the degradation of the TG and its surrounding is the V_{LOTG} voltage. Two TG OFF voltage biases were used. One is supposed to be the worst case condition by pushing the defect toward the Si/SiO_2 interface, a positive value: $V_{\mathrm{LOTG}} = +0.4$ V that is typical of "anti-blooming operation". This worst case condition was used on two studied imagers. A third imager was irradiated with a negative V_{LOTG} ($V_{\mathrm{LOTG}} = -0.6$ V). If the TG bias has an influence on the TID effects, there should be a significant difference between the two irradiation conditions.

III. Radiation Induced Degradations

A. Overview and Effect of Bias During Irradiation

The three irradiated CIS were fully functional after the maximum TID with no variation of the readout chain performance, no change in conversion factor (CVF), no visible change of power consumption and no dramatic sensitivity drop at the optical wavelength used for the opto-electrical characterization ($\lambda = 650$ nm). This result was expected on this generation of CIS processes (180 nm) in this TID range [6], [13] despite the fact that radiation-hardened-by-design transistors are not used.

The results obtained on the three CIS have been carefully compared after each irradiation step and no significant difference was observed between the three devices (i.e. well in the range of typical device mismatches) despite the differences in bias conditions of the TG during exposure. This is in good agreement with [6] which reports no difference between PPD CIS irradiated ON and those grounded during exposure. However, this is in clear contradiction with [14][2] that demonstrates an effect of duty cycle on the dark current increase. There is no obvious explanation for these discrepancies and more data on more technologies and bias conditions would be needed to clarify this point.

B. Charge Transfer Efficiency

CTE measurements have been performed in accumulation regime ($V_{\mathrm{LOTG}} = -0.6$ V) using a pulsed LED (as in [6]). The pulse is synchronized in such a way that it is entirely temporally localized in a single frame. Moreover, its intensity is tuned so that the output signal of the lighted frame corresponds to half the equilibrium full well capacity (EFWC) (i.e. the FWC that is reached in equilibrium condition [15], with no illumination) whatever the TID for each pixel sub-array. Comparing the number of electrons on the lighted frame and on the following ones allows us to estimate the CTE (the lower is the number of residual electrons, the better is the CTE) [16].

[2]In [14] the tested device is a 5T-PPD CIS contrary to the sensor studied here which is a 4T-PPD CIS. However there is no obvious reason why the additional TG used in a 5T-PPD pixel would lead to different conclusions regarding the effect of TG biasing during irradiation.

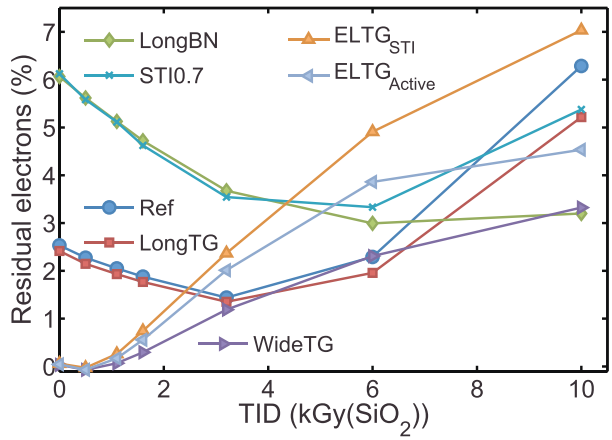

Fig. 3. Number of residual electrons (in the dark frame that follows the pulse frame) with regards to the TID. Number of electrons in the frame integrating the pulse is around EFWC/2 for each pixel type and each TID step.

As can be seen in Fig. 3, before irradiation the different types of pixels exhibit very different CTE due to their different designs. All the pixels with a bottleneck (Ref, LongTG, LongBN and STI0.7) exhibit poor CTE which agrees well with the existence of a potential barrier under the TG that limits the transfer [11]. This is confirmed by the fact that the two pixels with the longest bottleneck (LongBN and STI0.7) exhibit the worst performances, suggesting the existence of a larger potential barrier. Reducing the length of the bottleneck decreases the height of the barrier and so the number of residual electrons.

After irradiation and until 3 kGy, the pixels with a bottleneck improve (which can be explained by a lowering of the potential barrier) whereas the ones that are not initially limited by a potential barrier are degraded with TID. In this case, this can be due to the creation of a potential pocket and/or the trapping of signal electrons at an oxide interface. Ref and LongTG pixels differ from their TG area and perimeter, as well as WideTG with ELTGs pixels. However, Ref and LongTG pixels have the same CTE and the same comment can be made by comparing the WideTG pixel to the ELTG ones. This demonstrates that charge trapping at the STI interface (source 3 in Fig. 1) or at the gate oxide interface (source 4) does not limit the transfer efficiency before and after irradiation. So the most likely cause of CTE degradation is the creation of a potential pocket. For high TID, every pixel exhibits a degradation of its CTE due to this potential pocket.

It is worth noting that on the same technology, one can observe two opposite evolutions of the CTE with TID, depending on the limiting parameter before exposure (and thus on pixel design).

C. Pinning Voltage Characteristic

The pinning voltage (V_{pin}) of a pinned photodiode can be defined as its maximum channel potential [17] (i.e. the bottom of the PPD potential well). When this pinning voltage is reached[3] (usually at the end of a transfer phase), the N-doped region of the PPD is fully depleted and there is no remaining electron in the

[3]This is done by turning the TG ON and applying a high voltage (e.g. 3.3 V) on the floating diffusion.

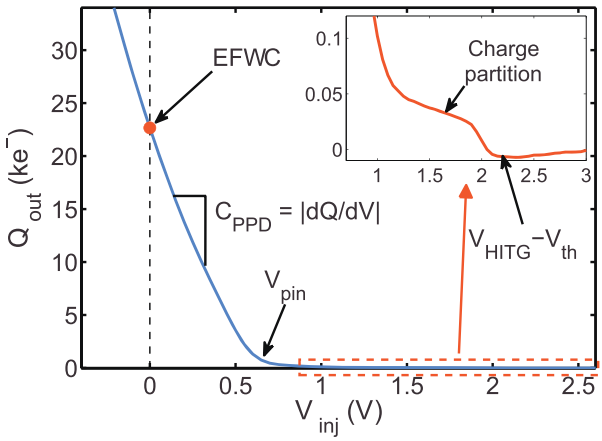

Fig. 4. Pinning voltage characteristic measured on the WideTG pixel sub-array. The physical parameters that can be extracted from this characteristic (i.e. pinning voltage $V_{\rm pin}$, the EFWC, and TG threshold voltage $V_{\rm th}$) are indicated.

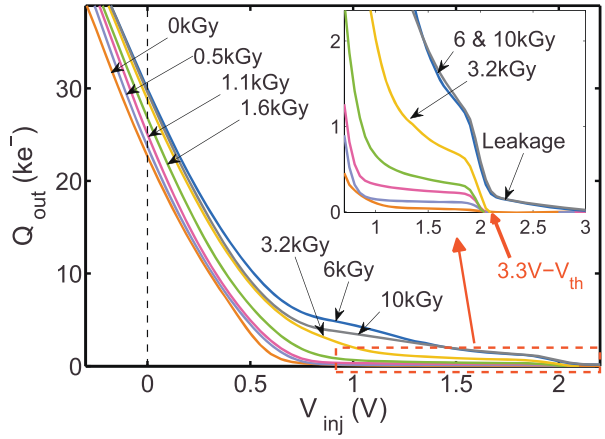

Fig. 5. WideTG pixel pinning voltage characteristic evolution with TID. The inset presents a magnification of the curves around the threshold voltage extraction point.

potential well. A measurement technique[4] has been previously proposed [4] to estimate the pinning voltage of a CIS directly at the output of the integrated circuit. It has been recently demonstrated that this characteristics can be used to extract the physical parameters of the PPD-TG structure [6], [17]. The pinning voltage characteristic measured on the WideTG pixel sub-array with the experimental conditions described in [17] is presented in Fig. 4. As shown in the figure, the EFWC can be directly measured on this curve by measuring the charge injected in the PPD with a zero injection voltage. The pinning voltage corresponds to the knee voltage at which the injected charge starts to increase with decreasing $V_{\rm inj}$. However, as discussed in [17], this knee voltage determination can be very subjective and its value can change with the magnification of the curve (as can be observed in the following figures by comparing the inset to the main graph). In order to obtain objective pinning voltage values that can be used to determine the evolution of this parameter with TID, the integral extrapolation technique proposed in [17] was used in this work. The slope of the characteristic directly provides the PPD capacitance.

The charge partition mechanism occurs in a pinned photodiode when an inversion channel is formed below the transfer gate and when this gate is suddenly turned OFF [18], [19], [20]. As explained in [17], this phenomenon can be observed in Fig. 4 for $V_{\rm inj}$ between 1 and 2.1V. The injection voltage at which the charge partition step occurs ($V_{\rm inj} = 2.1$ V in Fig. 4) corresponds to $V_{\rm inj} = V_{\rm HITG} - V_{\rm th}$, with $V_{\rm th}$ the TG threshold voltage (so $V_{\rm th} = 3.3 - 2.1 = 1.2$ V here with body effect). It means that the position of this step in the curve directly inform on the TG threshold voltage value. Therefore, it appears that this characteristic is a very convenient tool to get a quick overview of the health of the PPD-TG structure.

Fig. 5 presents the evolution of this characteristic with TID (on pixel WideTG). The curve is clearly shifted to the right by ionizing radiation with no change of slope. It leads to a steady increase of pinning voltage and of EFWC but not to any capacitance variation, contrary to what was suggested in [6]. At 10 kGy the characteristic seems to shift back to the left but this effect is most likely an artifact induced by the large CTE degradation undergone by this pixel. Indeed, poor CTE (below 99%) is known to induce a visible left shift of the characteristic [17]. Before irradiation, the percentage of residual electrons was too low (below 1%) to have an influence on the WideTG pixel characteristic, but at the highest TID, the left shift induced by the CTE degradation compensates the right shift observed at the previous TID steps.

It is interesting to notice that the injected signal in the charge partition regime (for $0.8\ {\rm V} < V_{\rm inj} < 2.1\ {\rm V}$) rises with TID. This effect is in good agreement with the TID induced potential pocket hypothesis proposed in the previous section. Indeed a deeper potential pocket below the TG leads to a larger amount of charge stored below the inverted gate and thus, to a larger amount of injected electrons through the charge partition process.

The magnification of the charge partition regime presented in the inset of Fig. 5 shows that the charge partition threshold stays equal to 2.1 V even after 10 kGy. Hence, it can be concluded that the TG threshold voltage is not modified by ionizing radiation in this TID range and that the TG gate oxide is not significantly degraded. This conclusion is in very good agreement with the fact that no obvious deterioration was observed on the CIS digital and analog CMOS circuits and with the absence of gate oxide degradation reported on similar MOSFETs manufactured on a comparable CMOS process in the same TID range [21]. A last effect is visible in the inset: the appearance of a leakage for injection voltages above the charge partition threshold (i.e. when the TG gate to source voltage is below $V_{\rm th}$). Since the TG threshold voltage is unchanged, and since the TG is supposed to be in the depletion regime for $V_{\rm inj} > 2.1$ V, it means that a large subthreshold leakage appears after 6 kGy (it may have appeared at a lower TID but with no visible effect on this characteristic). This well-known TID induced subthreshold leakage is attributed to positive charge trapping in the STI sidewalls on the TG channel edges [22], [23].

[4]The basic principle of this technique is to inject signal electrons in the PPD through the TG by applying an injection voltage ($V_{\rm inj}$) to the floating diffusion (FD) during the integration phase. When the injection voltage is below the pinning voltage, the injected charge rises with decreasing $V_{\rm inj}$ whereas almost no signal charge is injected when $V_{\rm inj}$ is higher than $V_{\rm pin}$.

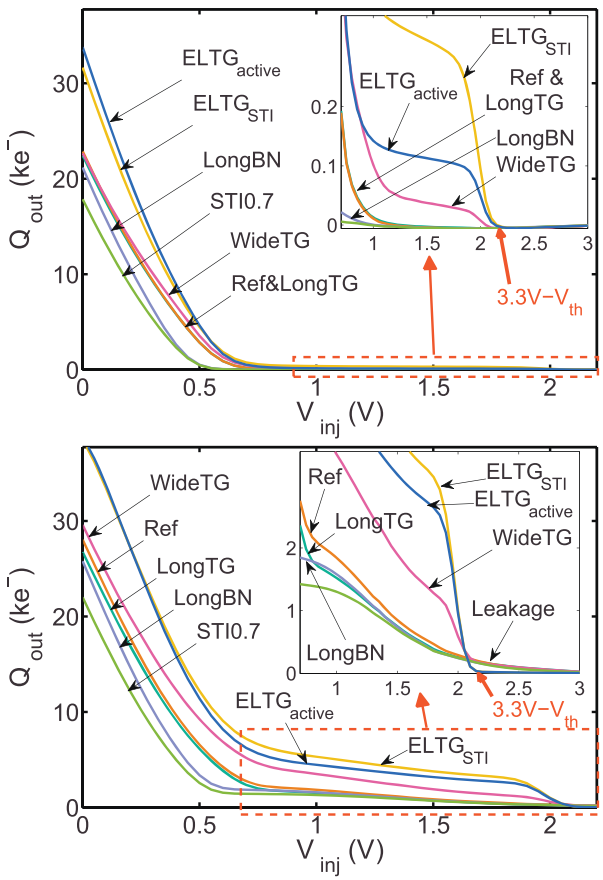

Fig. 6. Pinning voltage characteristics of the seven studied pixels before (top) and after (bottom) irradiation (10 kGy(SiO_2)). The insets present a magnification of the curves around the threshold voltage extraction point.

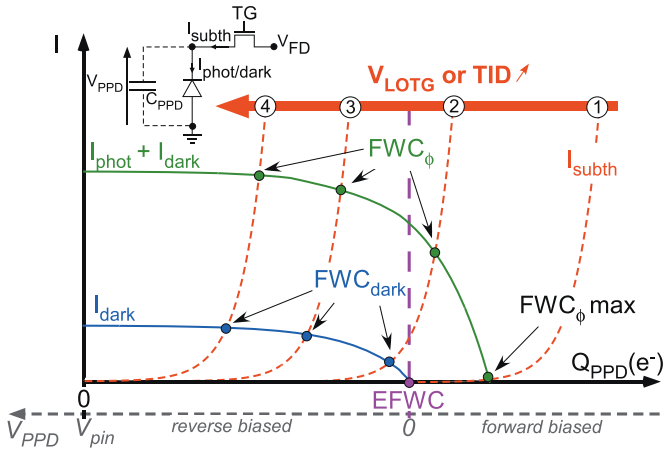

Fig. 7. Illustration of the different full well capacity definitions based on the analytical model developed in [15], [24]. The EFWC is defined as the x-intercept of I_{dark} (and also as the FWC value corresponding to $V_{PPD} = 0$). The FWC_{dark} is defined as the FWC value at the intersection between I_{dark} and I_{subth}. The FWC_{Φ} is defined as the FWC value at the intersection between $I_{phot} + I_{dark}$ and I_{subth}. Q_{PPD} is the PPD stored charge (in e^-).

The pinning voltage characteristics of all the studied pixels are presented in Fig. 6 before and after 10 kGy. Before irradiation (top figure), most of the pixel designs have a pinning voltage around 0.6 V, which is expected since V_{pin} is defined by the doping concentration of the PPD and should not be influenced by the TG design. Nevertheless, pixels LongBN and STI0.7 exhibit a lower pinning voltage (0.47 V instead of 0.6 V) and a lower EFWC than the other designs. In reality, the pinning voltage in the middle of these PPD is the same as the one in the other pixels but the poor CTE of the LongBN and STI0.7 pixels (due to their long bottleneck) give rise to this apparent shift and thus, to an underestimation of V_{pin} and EFWC [17].

In the inset of Fig. 6 top subfigure the charge partition regime is clearly visible for the pixels without a potential barrier (WideTG and ELTG designs) whereas the potential barrier in the other designs prevents the charge from being injected through the charge partition mechanism, and thus, these pixels do not exhibit the charge partition step.

After 10 kGy all the V_{pin} curves exhibit the same degradations (bottom subfigure of Fig. 6), whatever their TG design: a right shift (of the same magnitude) with TID and no capacitance variation. This shows that the phenomenon at the origin of this V_{pin} increase is independent of the TG design. It is also not related to the peripheral STI because the STI0.7 pixel undergoes the same effect as the other layouts. It strongly suggests that the cause of this degradation is located uniformly, on the top of the PPD.

Some differences between pixels can be noticed in the inset of the bottom subfigure of Fig. 6: there is no subthreshold leakage after 10 kGy on the ELTG pixels whereas all the other ones suffer from this leakage. This is clearly due to the absence of STI in the channel of the ELTG pixels (as in a classical enclosed layout transistor (ELT) layout).

D. Full Well Capacity

FWC variation has been recently reported [6] but this study was limited to the FWC evolution in the accumulation regime. More recent publications on PPD FWC modeling [15], [24] have demonstrated that depending on the measurement conditions (V_{LOTG} and photon flux), the FWC can be limited by different mechanisms with different location inside the pixel possibly leading to different evolutions with TID. Fig. 7 is an illustration of the model developed in [15], [24]. No more charge can be collected by the photodiode capacitance C_{PPD} when the photodiode total current is null, i.e. when the subthreshold current I_{subth} is equal to the dark current I_{dark} plus the photo-current I_{phot}. As discussed in Section III-C, the EFWC corresponds to the total charge accumulated when V_{PPD} is null (i.e. when I_{dark} is also null). Hence, as can be seen in Fig. 7, EFWC is directly related to the pinning voltage V_{pin}. With a substantial contribution of the subthreshold current (case 2 in Fig. 7), the dark signal reaches a saturation level (defined here as FWC_{dark}) at the intersection of I_{dark} and I_{subth}, which is lower than the EFWC. Finally, under illumination, if I_{subth} is negligible (for example if TG is accumulated and in absence of subthreshold leakage, case 1 in Fig. 7), the saturation level reached (defined here as FWC_{Φ}) is much larger than EFWC. An increase of I_{subth}, due for example to an increase of V_{LOTG} (or to a subthreshold leakage), leads to a decrease of the measured FWC_{Φ}.

In order to collect as much information as possible to determine the degradation sources of the FWC with TID, we follow here the evolution of EFWC, FWC_{dark}, FWC_{Φ}^{acc} and

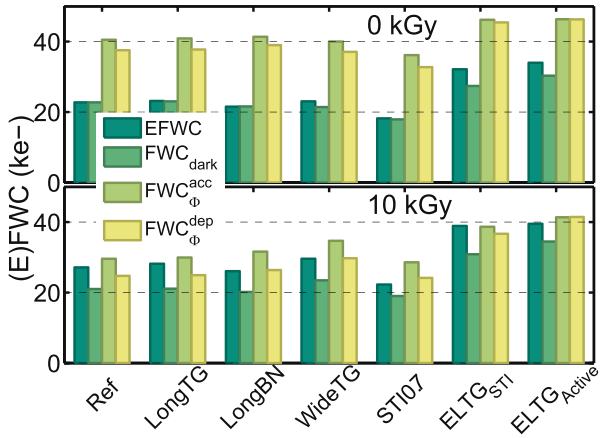

Fig. 8. Studied pixels FWC comparison before (top) and after (bottom) irradiation (10 kGy (SiO_2)). $\mathrm{FWC_{dark}}$ and $\mathrm{FWC_{\Phi}^{acc}}$ are measured with $V_{\mathrm{LOTG}} = -0.6$ V, $\mathrm{FWC_{\Phi}^{dep}}$ is measured with $V_{\mathrm{LOTG}} = +0.1$ V.

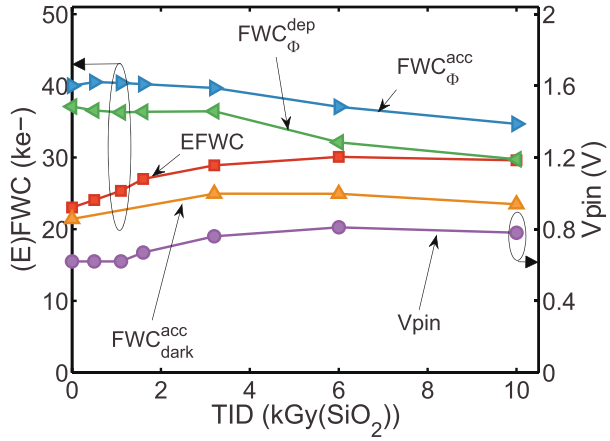

Fig. 9. Evolution of the FWC, the EFWC and the pinning voltage of pixel WideTG with TID.

$\mathrm{FWC_{\Phi}^{dep}}$. $\mathrm{FWC_{\Phi}^{acc}}$ and $\mathrm{FWC_{\Phi}^{dep}}$ are measured under the same illumination condition, respectively with $V_{\mathrm{LOTG}} = -0.6$ V and $V_{\mathrm{LOTG}} = +0.1$ V whereas $\mathrm{FWC_{dark}}$ is measured in the dark and EFWC is extracted from Vpin measurement characteristic (Fig. 4). Table. I depicts values of EFWC, $\mathrm{FWC_{\Phi}^{acc}}$ and $\mathrm{FWC_{\Phi}^{dep}}$ before irradiation. These are represented in the top bar graph of Fig. 8 for the seven studied pixels. One can notice that the different FWCs follow the EFWC on every pixel. The $\mathrm{FWC_{dark}}$ is close to the EFWC, except on pixels having a wide TG (WideTG, $\mathrm{ELTG_{STI}}$ and $\mathrm{ELTG_{Active}}$) because of their high W/L ratio (and thus of their larger subthreshold current).

Fig. 9 presents the evolution with TID of the EFWC, the FWC and the pinning voltage of pixel WideTG. As already noticed in Section III-C, V_{pin} increases with TID, leading to an increase of EFWC. FWCdark and EFWC, initially fairly close, tend to deviate from each other when the TID increases, suggesting an increase of the subthreshold current high enough to compensate the EFWC increase. Regarding the evolution of the WideTG $\mathrm{FWC_{dark}}$ with V_{LOTG} after 10 kGy irradiation (Fig. 10), one can see that it depends quasi linearly on V_{LOTG} suggesting that $\mathrm{I_{subth}}$ is the dominating current (case 3 and 4 in Fig. 7). The same trend is observed on the $\mathrm{FWC_{\Phi}}$ and, as can be seen in Fig. 9, $\mathrm{FWC_{\Phi}^{acc}}$ and $\mathrm{FWC_{\Phi}^{dep}}$ drop with TID. Knowing that the FWC depends logarithmically on the ratio $(\mathrm{I_{phot}} + \mathrm{I_{dark}})/(\mathrm{I_{subth}} + \mathrm{I_{dark}})$ (according to eq. (3) in [15]), an increase of $\mathrm{I_{dark}}$ associated or not to an increase of $\mathrm{I_{subth}}$ explains this behavior. As depicted in Fig. 8, every pixel except the ELTGs presents the same trend with TID as the WideTG pixel (Fig. 5). The ELTG pixels are particular cases. First, after 10 kGy, the difference between the EFWC and the $\mathrm{FWC_{dark}}$ of the $\mathrm{ELTG_{Active}}$ pixel stays unchanged (Fig. 8). Both $\mathrm{FWC_{\Phi}}$ and $\mathrm{FWC_{dark}}$ are still independent of V_{LOTG} in accumulation mode (Fig. 10), demonstrating that there is no creation of a subthreshold leakage path (contrary to the other pixels) and that the I_{dark} increase is the cause of the $\mathrm{FWC_{\Phi}}$ drop in this pixel. The $\mathrm{ELTG_{STI}}$ pixel does not have the same behavior: the FWC variation with V_{LOTG} is rather similar to the WideTG pixel one (Fig. 10). This is most likely due to an interdevice leakage through the inversion of the STI, where the gate overlaps the STI (on the right side of the gate near the contact in Fig. 2(f)).

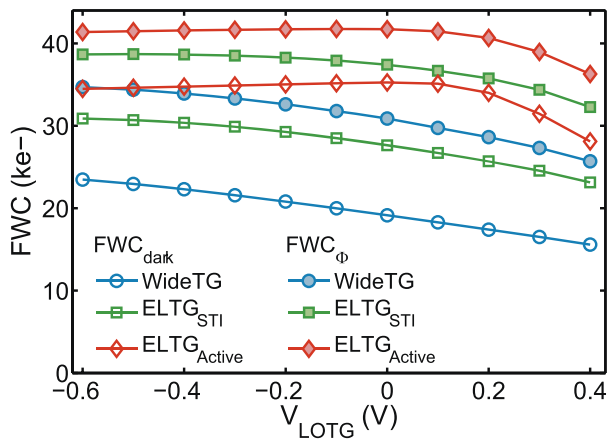

Fig. 10. $\mathrm{FWC_{dark}}$ and $\mathrm{FWC_{\Phi}}$ evolution with V_{LOTG} after 10 kGy(SiO_2) irradiation for the WideTG, $\mathrm{ELTG_{STI}}$ and $\mathrm{ELTG_{Active}}$ pixels.

E. Dark Current

Fig. 11 shows the evolution of the dark signal with integration time with the TG accumulated and depleted during integration after 3 kGy. Both curves reach a saturation level (the $\mathrm{FWC_{dark}}$ as discussed in Section III-D) after a few seconds of integration.[5] It is important to notice that the range in which the dark signal is linear with integration time is much smaller than the $\mathrm{FWC_{\Phi}}$ (less than 20% of $\mathrm{FWC_{\Phi}}$), which is usually the only FWC value measured in literature and in technical reports. As the dark current is by definition the slope of dark signal with integration time, one may easily strongly underestimate the dark current value if this slope is not computed in the first $\approx 20\%$ of the saturation level of the detector (obtained under illumination).[6] This is especially true when only two integration times are used to compute the slope, since in this case there is no way to verify if the measurement is still performed in the linear part

[5]The result would have been the same in a non-irradiated sensor except that the integration time necessary to reach the FWC value would have been much longer (typically several minutes or hours at room temperature).

[6]For instance, the dark current would have been greatly underestimated in the presented study if the extraction range was the same as in [7] where the dark current is computed between 0 and 50% (or even 80% in case of non linearity) of the saturation level determined under illumination and with the TG depleted (worst case).

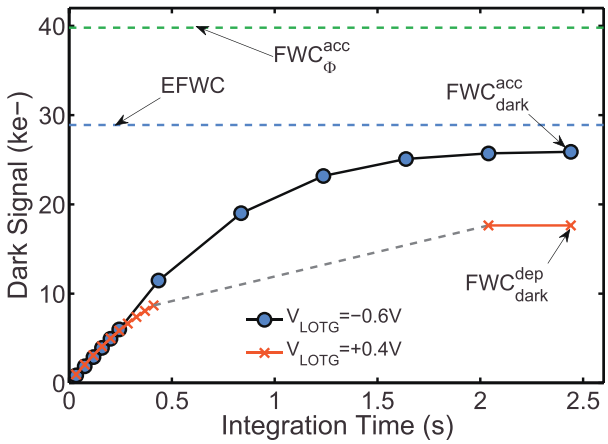

Fig. 11. Evolution of dark signal (Q_{dark}) of WideTG pixels with integration time for two V_{LOTG} bias conditions (accumulated (acc) and depleted (dep)) and comparison with the EFWC and the FWC under illumination (FWC_Φ). The presented data correspond to pixel WideTG after 3 kGy(SiO_2) of TID.

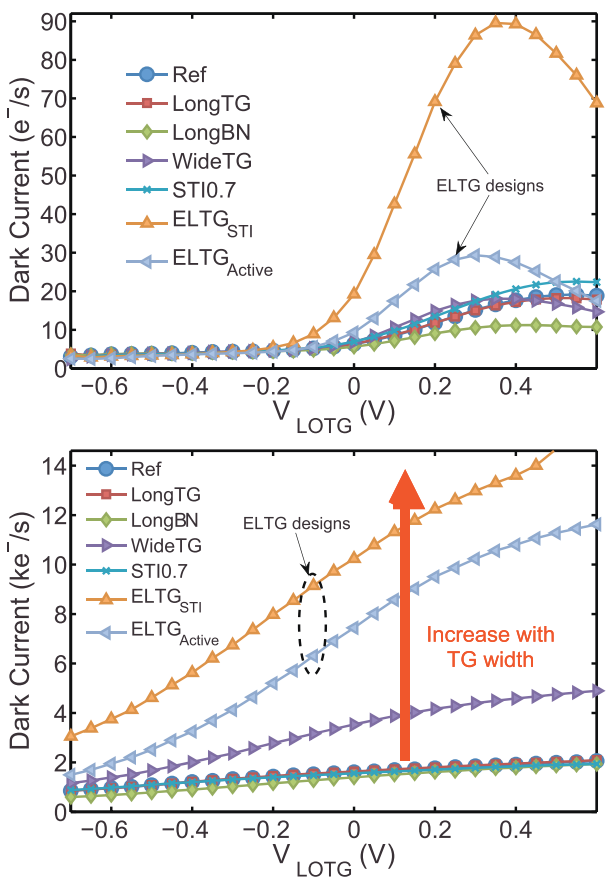

Fig. 12. Dark current evolution with TG OFF voltage (V_{LOTG}) before (top) and after (bottom) 1.1 kGy(SiO_2) for the seven pixel types.

of the dark signal evolution. The issue is even worse when a positive V_{LOTG} is used (or after irradiation) since it reduces further the linear range of dark signal (so does the radiation induced subthreshold leakage). Hence, verifying that the measurement is performed in the linear range of the detector does not provide any guarantee that the dark current evaluation is performed in the linear range of the dark signal which is much smaller than

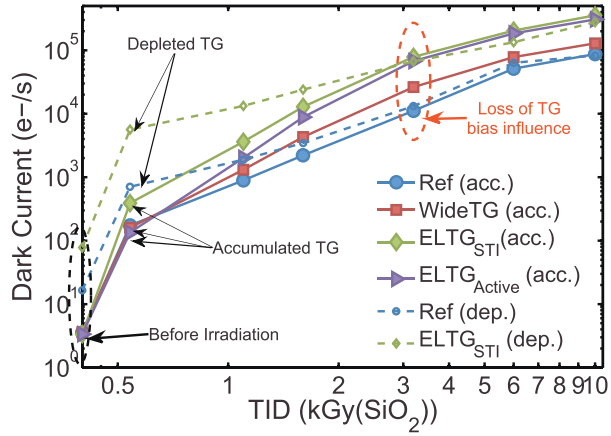

Fig. 13. Dark current evolution with TID, for all the studied pixels and for two selected V_{LOTG} values: −0.6 V (accumulation) and +0.4 V (depletion).

the detector linear range in PPD CIS.[7] To avoid underestimating the dark current values, extreme care has been taken to perform the dark current estimation in the linear range of the dark signal (below 20% of the EFWC value whenever it was possible) and between 10 and 50 different integration times were used after each TID to compute the maximum slope[8] and verify the linearity.

The dark current evolution with V_{LOTG} of the studied pixels before and after irradiation (1.1 kGy) is shown in Fig. 12. Before irradiation, all the pixels exhibit a low dark current ($< 5e^-/s$) when the TG is properly accumulated [5], [25], [26] whereas a much larger value is obtained for positive V_{LOTG}. In this latter regime, the pixels with the widest gates (WideTG and the ELTGs) have the largest dark current values because the area of depleted Si/SiO_2 interface is proportional to the TG width. The STI below the gate of $ELTG_{STI}$ seems to contribute significantly before irradiation to the dark current in the depletion regime according to the large difference between this design and the $ELTG_{Active}$ one. The dark current drop between 0.3 and 0.5 V is due to the compensation of dark current by the TG subthreshold current.

After irradiation (bottom subfigure of Fig. 12), the relative influence of V_{LOTG} on the dark signal becomes weaker (as already observed on the same technology: process B in [6]) and the pixels with the widest gate become the worst pixels (in terms of dark current increase) in both regime (TG accumulation and TG depletion). The same behavior and hierarchy between designs is kept up to the maximum TID, as illustrated in Fig. 13 and Fig. 14. The first figure shows that after 3 kGy, the influence of the TG OFF bias on the dark current value becomes very weak whereas both figures clearly demonstrate that the worst dark current increase is exhibited by the supposed radiation hard ELTG designs. The difference between both ELTG designs is also reduced with TID. Hence, it can be concluded that the STI in the channel is not likely to be a significant contributor to the radiation induced dark current increase. As regards the peripheral STI (source 1 in Fig. 1), recessing the STI away from the

[7]This can be a big issue, especially for displacement damage induced hot pixels characterization.

[8]The maximum slope technique is used to avoid the low level non-linearity sometimes observed on poor CTE PPD pixels.

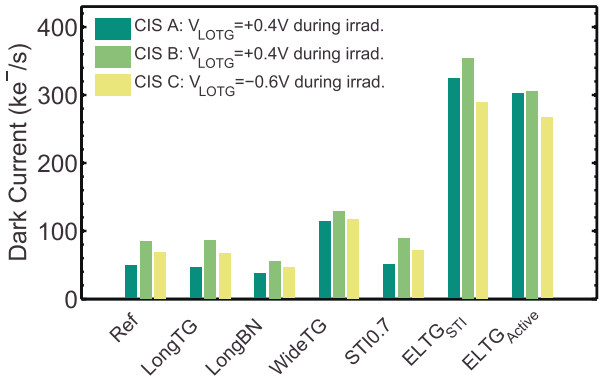

Fig. 14. Studied pixel dark current comparison measured on the three tested image sensors after 10 kGy(SiO_2). The bias conditions during irradiation are indicated in the legend. During the dark current measurement the TG was in accumulation $V_{\mathrm{LOTG}} = -0.6$ V. Very similar dark current values were achieved at this TID level with $V_{\mathrm{LOTG}} = +0.4$ V during the measurement.

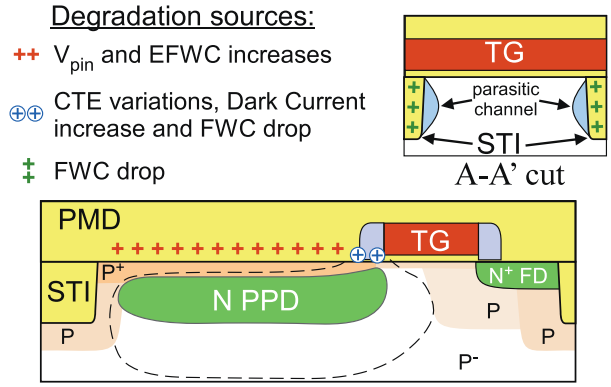

Fig. 15. Summary and localization of the TID induced degradation sources with the TG in accumulation regime. The interface below the TG sidewall spacer is accumulated because of the influence of the TID induced trapped positive charge in the spacer. The PMD interface is not depleted because in this TID range because the P^+ pinning layer doping concentration is much higher below the PMD than below the spacer.

PPD (pixel STI0.7 compared to pixel LongBN) does not mitigate the dark current rise and even enhances it (this enhancement is due to a widest effective TG width in the STI0.7 pixel). It is a clear demonstration that the STI is not responsible for the TID induced dark current degradation. Fig. 14 also compares the dark current values measured on the three devices (with different bias conditions during irradiation).

IV. Analysis and Discussions

A. Degradation Mechanisms

After the study of a single design on two CIS technologies, it has been concluded in [6] that the most probable source of most of the TID induced degradations was the trapped positive charge in the PMD (illustrated in Fig. 15) that raises the pinning voltage, decreases the FWC despite the V_{pin} increase (because of a PPD capacitance rise), enhances the dark current, and leads to the observed CTE variations. At that time, there was no established technique to extract the PPD capacitance, the EFWC concept has not been yet proposed, the FWC dependence on photon flux was not clear and the multiple definitions of FWC were not known.

According to the results of the TG design variations presented here, the proposed role of PMD positive trapped charge in the V_{pin} increase agrees well with the fact that this effect is undergone with the same magnitude by all the tested pixels (independently of their TG design). Indeed, the trapped positive charge in the PMD reduces the effective doping concentration of the P^+ pinning layer and thus increases the uncompensated N PPD doping concentration. The pinning voltage of a PPD is known to grow with the uncompensated N PPD doping concentration [27], and so with the PMD trapped positive charge, whatever the TG layout. Because the EFWC is known to increase with V_{pin}[17], this degradation mechanism also explains the EFWC variation.

By distinguishing the different FWC and especially, by making the difference between the EFWC and the other FWC, it has been possible to progress on the origin of the FWC drop. Contrary to what was suggested in [6], the measured capacitance of the PPD did not change with radiation in this TID range. Thus, the capacitance variation can not be the cause of the FWC decrease observed here. As discussed in III-D, depending on the TID and on the pixel design the drop of FWC is either due to the TG subthreshold leakage (as concluded in [7] and illustrated in Fig. 15), to the magnitude of the dark current or to the combination of both.

It is still possible that at higher TID (or on different technologies where the P^+ pinning layer doping concentration is lower than in the studied technology) this capacitance drop occurs. According to the results presented in Fig. 11 of [6], this effect seems to happen on technology A after 3 kGy and 10 kGy (because of the clear change of slope on the V_{pin} characteristic) but not on technology B (same process as the one studied here).

As regards the other parameters (CTE and dark current), the different behaviors of the studied pixel designs allow to localize more precisely the degradation origin. Up to the highest TID tested here, the dark current remained proportional to the TG width and with little influence of the TG OFF voltage after 3 kGy. It shows that, on this CIS technology, the P^+ pinning layer doping concentration is high enough to prevent the depletion of the PMD interface at 10 kGy and that the main dark current source is not located inside the TG channel. The remaining degradation source that depends on the TG width is the oxide stack in the vicinity of the TG spacer (most likely constituted of several oxides and a nitride), as shown in Fig. 15. A positive trapped charge in this particular region of the PMD influences the PPD channel potential by reducing it locally (as a polysilicon gate would do) and thus it gets the PPD depletion region closer to the PMD interface full of interface states (existing before irradiation but multiplied by the TID) until the full depletion of this part of the PMD interface, even when the TG is accumulated. The reason why the PMD trapped positive charge has a much stronger influence below the spacer than below the rest of the PMD is the fact that in this region, the surface P^+ doping concentration is reduced to let the PPD channel reach the surface and connect to the TG channel (in order to achieve a good CTE), as shown in Fig. 15.

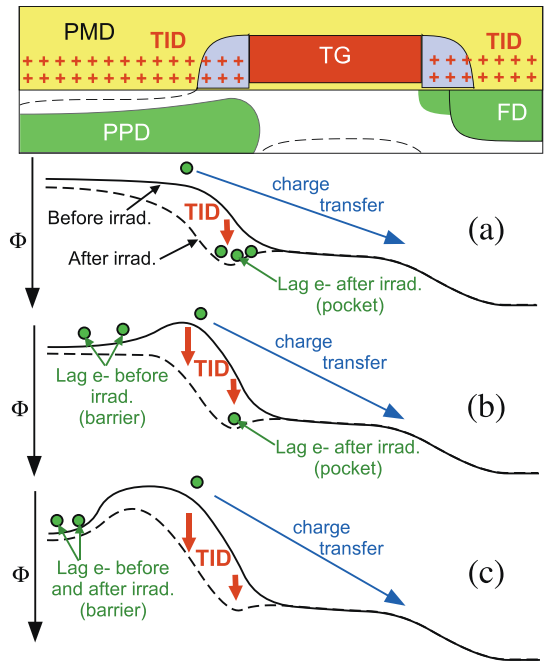

Fig. 16. Illustration of the mechanisms limiting the image lag performance before (plain line) and after (dashed line) irradiation in three cases of interest: (a) when no potential barrier exists before irradiation (pixels WideTG, ELTGs), (b) when a small potential barrier exists before irradiation (Ref and LongTG pixels) and (c) when a large barrier exists before irradiation (LongBN and STI0.7 pixels).

Composite nitride-oxide films are known to trap electrons as well as holes [28], [29] when exposed to ionizing radiation contrary to silicon dioxide that mainly trap holes [30] (as does the PMD [31] despite the fact it is itself constituted by some nitride [32]). The resulting apparent charge in the silicon depends on the different thicknesses (and natures) of the oxide and nitride that constitute the film [28], [29]. Whereas recent work on 1-T floating body random access memory concludes that negative trapped charge dominates in irradiated nitride spacers [33], it seems that in CMOS imagers (at least in the technologies tested here and in [6]) the positive trapped charge dominates the flat-band voltage shift leading to a negative shift (i.e. to an increase of the electrostatic potential in the semiconductor). This conclusion is in good agreement with the positive charge trapping observed in CIS PMD nitride-oxide films exposed to plasma induced radiation [32].

The hypothesis of trapped positive charge in the spacer vicinity is in very good agreement with the dark current evolution with TID on the different designs and also explains very well the CTE variations observed. Fig. 16 shows how this positive trapped charge leads to the reported radiation effects on the different designs (but also on the two different technologies presented in [6]). In pixels with no potential barrier before irradiation (Fig. 16a), the trapped charge in the PMD slightly raises V_{pin} on the whole PPD and induces a much larger potential rise in the spacer vicinity (because of the proximity of the PPD channel to the surface, as discussed previously). In absence of barrier (WideTG and ELTG pixels), this potential intensification generates a potential pocket when the TG electric field overlaps the PMD positive charge electric field leading to a drop of CTE with TID. When a small potential barrier exists in unirradiated devices (Fig. 16(b). and pixels Ref and LongTG), this local potential enhancement first reduces the barrier, leading to a CTE improvement, but at higher TID, the potential pocket becomes significant enough to compensate the barrier lowering and to eventually degrade the CTE. If the barrier is too high (Fig. 16(c). and pixels LongBN and STI0.7), the dominant mechanism is the CTE improvement due to the barrier lowering and the influence of the potential pocket is delayed or hidden by the effect of the large barrier.

It must be emphasized that the three degradation sources presented in Fig. 15 explain all the radiation effects observed on all the pixel designs (and also on the two technologies studied in [6]) and that the following oxides, proposed as possible degradation sources in literature, do not play any obvious role in the TID induced damage reported here:

- the peripheral trench isolation: STI here (source 1 in Fig. 1) proposed in [2], [3], [4] and implicitly proposed in [8], mainly because no significant difference in radiation effects has been observed between pixels LongBN and STI0.7 on one hand and between $\mathrm{ELTG_{Active}}$ and $\mathrm{ELTG_{STI}}$ on the other hand.
- the TG gate oxide (source 4 in Fig. 1) proposed in [4], [16], mostly because pixels Ref and LongTG exhibited the same behavior with TID.

B. Radiation-Hardening Perspectives

According to the summary of the degradation sources presented in Fig. 15, there is little that can be done at the PPD-TG design level to improve the radiation hardness of PPD CIS pixels. One can use an ELTG design (with or without a contact on the STI) as proposed in [8], [9] but it will only mitigate the radiation induced subthreshold leakage, that only plays a secondary role in the FWC drop. The results presented on the $\mathrm{ELTG_{Active}}$ pixel shows that even if the subthreshold leakage is mitigated, the FWC drop still occurs because the dark current is the main contributor to the FWC reduction. As regards the dark current increase, contrary to what is presented in [8], [9], the ELTG geometry does not bring any improvement since the TG channel STI is not the source of TID induced dark current and since the weak point (the nitride spacer vicinity) is not removed in such design. Worse, if the ELTG width is greater than the width of the classical TG design, using an ELTG even boosts the dark current increase (here, a 3 to 10 times enhancement is observed).

Hence, this study demonstrates that the existing PPD-TG radiation tolerant design is not effective on most of the radiation induced degradations and that it can even lead to larger deteriorations. It also shows that the main degradation source (the trapped positive charge in the PMD and especially in the nitride space vicinity) can not be mitigated by design easily. However, the ELTG design should mitigate the radiation induced floating diffusion leakage current (not studied here), as mentioned in [8]. For this reason, this design is recommended in applications where this leakage can be an issue (e.g. global shutter pixels with storage on the FD). If the radiation induced dark current increase is the limiting parameter for a given application, the

TG should be designed as narrow as possible (as far as the CTE stays acceptable) to reduce its contribution.

Since most of the degradation comes from the dielectric layers on top of the PPD, placing a DC biased polysilicon gate (adjacent to the TG, with minimum gap between the gates) on top of the PPD would probably solve the radiation problem in this TID range, because very few defects are generated in thin gate oxides in this TID range and because this additional gate would shield the pinning implant from the PMD trapped charge. Such solution would reduce the external quantum efficiency of a frontside illuminated sensor but it could be a good solution for backside illuminated CIS. The main problem is the fact that pinning and PPD implants are generally performed after polysilicon deposition and a process customization would be required to place a gate on top of the PPD without changing its doping profile. It is also possible to use the first level of metal (M1) to have this electrode on top of the PPD. In this case a significant amount of trapped charge and interface states will be created between the M1 gate and the silicon, but the DC bias applied on the M1 gate could possibly compensate the trapped charge.

Radiation hardening by process is also possible but it has a cost. An increase of the P^+ pinning layer doping concentration would most likely delay the radiation effects discussed here (as discussed in [32], [34]) but extreme care should be taken since increasing the P^+ pinning doping concentration could result in severe CTE loss or to significant electric field enhancement of the dark current. The use of rad-hard oxide for the PMD and spacer formation would improve much the radiation hardness of the CIS but it represents an important process modification that may be difficult to get. Finally, the hole based PPD [35], [36], [16] (also called PMOS PPD process or P-channel PPD) is a promising technology to improve the radiation hardness of PPD CIS and the early results are encouraging [36]. Unfortunately, there are too few published results on the radiation hardness of PMOS PPD pixels to be able to decide whether this technology will exhibit better performances (including CTE, quantum efficiency, FWC etc.) than classical N-channel PPD on a wide TID range or not.

C. Applicability to Other Technologies/Designs

The selected technology being a well-established commercially available CIS process, it is supposed to be representative of mature CIS processes and the presented degradation mechanisms are likely to exist in any irradiated CIS, whatever the manufacturing process. However, other degradation mechanisms may compete and depending on the process, the TID range at which a particular degradation mechanism dominate may differ from what is reported here. For instance, in a CIS process where the dark current is dominated by a parasitic source before irradiation (such as a tunneling current or an unwanted metal contamination [7]), this contribution may hide the dark current degradation mechanisms presented here. The diffusion dark current coming from the top PMD interfaces (source 5 in Fig. 1 [5], [3]) is most likely one important contributor in the tested device between 0 and 0.5 kGy but this contribution is hardly visible because the spacer dark current rises faster here. In a different CIS process with a higher P doping concentration below the spacer, the TID range in which the PMD interface contribution is the main issue can be extended toward higher radiation doses. Peripheral STI interface induced diffusion dark current contribution (source 1 in Fig. 1) can also be visible if the pixel pitch is very small [3], if the distance between the PPD and the STI is not large enough or if the STI is not well passivated [2].

The conclusions on the FWC degradations are mostly based on the analysis of the photodiode I-V curve at saturation (as proposed in [15]) and they should stay valid as far as the saturation level of the sensor is given by the PPD FWC (and not by the ADC or readout chain saturation). The conclusion that the CTE is likely to improve with TID in barrier limited pixel whereas it should be degraded by the irradiation in low lag pixel is also likely to be applicable to any CIS technology. However, a technology where the CTE is limited by charge trapping in the TG channel (as concluded in [16]) may exhibit a different behavior with TID than the ones reported here.

The conclusions of this work should also be transposable to any type of PPD pixel, such as 5T-PPD pixels, as far as the bias dependent contribution of each additional TG is taken into account.[9] These conclusions can also be used for more integrated CIS with on-chip ADC, sequencer and so on, as far as the additional TID effects brought by these additional circuits are taken into account.

V. Summary and Conclusion

Several transfer gate and pinned photodiode designs have been manufactured, characterized and radiation tested up to 10 kGy. For this study, several recently proposed techniques and models to study PPD CIS have been used: an original technique to extract the PPD/TG physical parameters and the associated physical mechanism description [17], an analytical model of the PPD pixel FWC and the concept of equilibrium full well capacity [15]. By combining the use of these recent tools and understanding to the comparison of the different pixel designs, this work confirms the validity of these recent advances: the relevance of the different FWC definitions, the ability of the proposed FWC model to describe the observed radiation effects and the good agreement between the physical mechanisms involved in the V_{pin} characteristic and the achieved experimental results. This combination also demonstrates that three degradation sources are sufficient to describe all the TID induced effects reported on the tested CIS technology:

1) the TID induced trapped positive charge in the PMD leads to pinning voltage and EFWC increases.
2) the TID induced trapped positive charge in the TG spacer vicinity is the main contribution to the radiation induced dark current (which also causes a FWC loss), the origin of CTE enhancement in potential barrier limited pixels (by lowering the potential barrier) and the origin of CTE degradation in other pixels (through the creation of a potential pocket)

[9]For example, in a 5T-PPD sensor, biasing the main TG in accumulation may not have a strong effect on the dark current (even before irradiation) if the other anti-blooming/global shutter TG dominates the dark current because it is biased positively.

3) the TID induced trapped charge in the TG STI sidewalls that generates a TG subthreshold leakage leading to additional FWC reduction.

The first degradation source can not be mitigated by changing the PPD-TG design. The second one, responsible for the dark current rise, is reduced when the TG width is shortened. The third one can be mitigated by using the enclosed layout TG designs proposed in [8], [9] to limits the FWC reduction. Unfortunately the benefit is pretty poor since the dark current enhancement is the main cause of FWC decrease. Moreover, this ELTG design initially proposed to mitigate the radiation induced dark current increase appears to be ineffective on the tested technology and to even enhance the dark current degradation because of a greater TG width. Therefore, it appears that the radiation hardness of PPD CIS is not likely to be significantly improved by changing the PPD-TG design. Alternative solutions to improve the radiation hardness of PPD CIS could be the use a polysilicon or metal electrode on top of the PPD or to modify the manufacturing process (e.g. by increasing the pinning implant doping or by using a PMOS PPD pixel technology).

The effect of TG OFF bias during irradiation has also been studied and no difference has been observed between the two tested conditions (in agreement with [6] but in contradiction with [14]). Contrary to what has been suggested in [6], the PPD capacitance is not influenced by the TID in the tested dose range and it is not the cause of the FWC reduction. PPD capacitance variation may still possibly occur at higher TID or on other CIS technologies which may use P^+ pinning implant with a lower doping concentration.

After the maximum TID (10 kGy), no sign of TG gate oxide degradation has been observed (no TG threshold voltage shift and no significant gate oxide trapping) and the STI had clearly no influence on the observed degradations (except the TG subthreshold leakage that has only a second order effect on the FWC drop compared to the dark current increase).

It must be emphasized that, since the three proposed degradation mechanisms influence differently the FWC (the first source increases the EFWC whereas the other two decreases the FWC), many behavior can be observed on the same technology depending on the device design or depending on how the FWC is measured. Similarly, this study demonstrates that different CTE evolutions with TID can be observed on the same technology depending on the limiting mechanism before exposure.

Acknowledgment

The authors want to thank A. Pelamatti and J.-M. Belloir, ISAE PhD students, and C. Messien, ISAE-SUPAERO graduate student, for their involvement and fruitful discussions about FWC measurements and theory. The authors are grateful to C. Chatry and N. Chatry, Y. Padié and L. Puybusque, all from TRAD, Toulouse, for their great support with irradiation. The authors greatly thank B. Avon (ISAE) for her involvement in characterization.

References

[1] E. R. Fossum and D. B. Hondongwa, "A review of the pinned photodiode for CCD and CMOS image sensors," *IEEE J. Electron Devices Soc.*, 2014.

[2] P. R. Rao, X. Wang, and A. J. P. Theuwissen, "Degradation of CMOS image sensors in deep-submicron technology due to γ-irradiation," *Solid-State Electron.*, vol. 52, no. 9, pp. 1407–1413, Sep. 2008.

[3] S. Place, J. Carrere, S. Allegret, P. Magnan, V. Goiffon, and F. Roy, "Radiation effects on CMOS image sensors with sub-2um pinned photodiodes," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, pp. 909–917, Aug. 2012.

[4] J. Tan, B. Buttgen, and A. J. P. Theuwissen, "Analyzing the radiation degradation of 4-transistor deep submicron technology CMOS image sensors," *IEEE Sensors J.*, vol. 12, no. 6, pp. 2278–2286, Jun. 2012.

[5] V. Goiffon, C. Virmontois, P. Magnan, P. Cervantes, S. Place, M. Gaillardin, S. Girard, P. Paillet, M. Estribeau, and P. Martin-Gonthier, "Identification of radiation induced dark current sources in pinned photodiode CMOS image sensors," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, pp. 918–926, Aug. 2012.

[6] V. Goiffon, M. Estribeau, O. Marcelot, P. Cervantes, P. Magnan, M. Gaillardin, C. Virmontois, P. Martin-Gonthier, R. Molina, F. Corbiere, S. Girard, P. Paillet, and C. Marcandella, "Radiation effects in pinned photodiode CMOS image sensors: Pixel performance degradation due to total ionizing dose," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2878–2887, Dec. 2012.

[7] A. BenMoussa, S. Gissot, B. Giordanengo, G. Meynants, X. Wang, B. Wolfs, J. Bogaerts, U. Schuhle, G. Berger, A. Gottwald, C. Laubis, U. Kroth, F. Scholze, A. Soltani, and T. Saito, "Irradiation damage tests on backside-illuminated CMOS APS prototypes for the extreme ultraviolet imager on-board solar orbiter," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 5, pp. 3907–3914, Oct. 2013.

[8] M. Innocent, "A radiation tolerant 4t pixel for space applications," presented at the IISW, 2009.

[9] M. Innocent, "A radiation tolerant 4t pixel for space applications: Layout and process optimization," presented at the IISW, 2013.

[10] S. Park and H. Uh, "The effect of size on photodiode pinch-off voltage for small pixel CMOS image sensors," *Microelectronics J.*, vol. 40, no. 1, pp. 137–140, Jan. 2009.

[11] L. Bonjour, N. Blanc, and M. Kayal, "Experimental analysis of lag sources in pinned photodiodes," *IEEE Electron. Device Lett.*, vol. 33, no. 12, pp. 1735–1737, 2012.

[12] B. Pain, G. Yang, M. Ortiz, C. Wrigley, B. Hancock, and T. Cunningham, "Analysis and enhancement of low-light-level performance photodiode-type CMOS active pixel imagers operated with sub-threshold reset," presented at the IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, 1999.

[13] V. Goiffon, P. Cervantes, C. Virmontois, F. Corbiere, P. Magnan, and M. Estribeau, "Generic radiation hardened photodiode layouts for deep submicron CMOS image sensor processes," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 3076–3084, Dec. 2011.

[14] E. Martin, T. Nuns, J.-P. David, O. Gilard, J. Vaillant, P. Fereyre, V. Prevost, and M. Boutillier, "Gamma and proton-induced dark current degradation of 5T CMOS pinned photodiode 0.18 μm CMOS image sensors," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 1, pp. 636–645, Feb. 2014.

[15] A. Pelamatti, V. Goiffon, M. Estribeau, P. Cervantes, and P. Magnan, "Estimation and modeling of the full well capacity in pinned photodiode CMOS image sensors," *IEEE Electron Device Lett.*, vol. 34, no. 7, pp. 900–902, Jul. 2013.

[16] J. R. Janesick, T. Elliott, J. Andrews, J. Tower, and J. Pinter, "Fundamental performance differences of CMOS and CCD imagers: Part V," in *Proc. SPIE*, 2013, vol. 8659.

[17] V. Goiffon, M. Estribeau, J. Michelot, P. Cervantes, A. Pelamatti, O. Marcelot, and P. Magnan, "Pixel level characterization of pinned photodiode and transfer gate physical parameters in CMOS image sensors," *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 65–76, Jul. 2014.

[18] N. Teranishi and N. Mutoh, "Partition noise in CCD signal detection," *IEEE Trans. Electron Devices*, vol. 33, no. 11, pp. 1696–1701, 1986.

[19] L. Colquitt, N. Bluzer, Jr., and R. McKee, "Charge partition noise in charge-coupled devices," *Opt. Engrg.*, vol. 26, no. 10, pp. 992–998, 1987.

[20] S.-H. Park, J.-D. Bok, H.-M. Kwon, W.-I. Choi, M.-L. Ha, J.-I. Lee, and H.-D. Lee, "Decrease of dark current by reducing transfer transistor induced partition noise with localized channel implantation," *IEEE Electron Device Lett.*, vol. 31, no. 11, pp. 1278–1280, Nov. 2010.

[21] M. Gaillardin, V. Goiffon, S. Girard, M. Martinez, P. Magnan, and P. Paillet, "Enhanced radiation-induced narrow channel effects in commercial 0.18um bulk technology," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2807–2815, Dec. 2011.

[22] M. R. Shaneyfelt, P. E. Dodd, B. L. Draper, and R. S. Flores, "Challenges in hardening technologies using shallow-trench isolation," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2584–2592, Dec. 1998.

[23] R. Lacoe, "CMOS scaling, design principles and hardening-by-design methodologies," presented at the IEEE NSREC Short Course, 2003.

[24] A. Pelamatti, J. M. Belloir, C. Messien, V. Goiffon, M. Estribeau, P. Magnan, C. Virmontois, O. Saint-Pe, and P. Paillet, "Temperature dependence and dynamic behaviour of full well capacity in pinned photodiode CMOS image sensors," *IEEE Trans. Electron Devices.*, submitted for publication.

[25] H. Han, H. Park, P. Altice, W. Choi, Y. Lim, S. Lee, S. Kang, J. Kim, K. Yoon, and J. Hynecek, "Evaluation of a small negative transfer gate bias on the performance of 4t CMOS image sensor pixels," presented at the Int. Image Sensor Workshop (IISW), 2007.

[26] B. Mheen, Y. J. Song, and A. J. P. Theuwissen, "Negative offset operation of four-transistor CMOS image pixels for increased well capacity and suppressed dark current," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 347–349, 2008.

[27] A. Krymski, N. Bock, N. Tu, D. Blerkom, and E. Fossum, "Estimates for scaling of pinned photodiodes," presented at the IEEE Workshop on CCD and Advanced Image Sensors, 2005.

[28] V. A. K. Raparla, S. C. Lee, R. D. Schrimpf, D. M. Fleetwood, and K. F. Galloway, "A model of radiation effects in nitride–oxide films for power MOSFET applications," *Solid-State Electron.*, vol. 47, no. 5, pp. 775–783, 2003.

[29] Y. Takahashi, K. Ohnishi, T. Fujimaki, and M. Yoshikawa, "Radiation-induced trapped charge in metal-nitride-oxide-semiconductor structure," *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, pp. 1578–1585, 1999.

[30] T. P. Ma and P. V. Dressendorfer, *Ionizing Radiation Effects in MOS Devices and Circuits*. New York, NY, USA: Wiley-Interscience, 1989.

[31] M. Gaillardin, V. Goiffon, C. Marcandella, S. Girard, M. Martinez, P. Paillet, P. Magnan, and M. Estribeau, "Radiation effects in CMOS isolation oxides: Differences and similarities with thermal oxides," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2623–2629, Aug. 2013.

[32] J. P. Carrere, J. P. Oddou, C. Richard, C. Jenny, M. Gatefait, S. Place, C. Aumont, A. Tournier, and F. Roy, "New mechanism of plasma induced damage on CMOS image sensor: Analysis and process optimization," in *Proc. ESSDERC*, Sep. 2010, pp. 106–109.

[33] N. N. Mahatme, E. X. Zhang, R. A. Reed, B. L. Bhuva, R. D. Schrimpf, D. M. Fleetwood, D. Linten, E. Simoen, A. Griffoni, M. Aoulaiche, M. Jurczak, and G. Groeseneken, "Impact of back-gate bias and device geometry on the total ionizing dose response of 1-transistor floating body RAMs," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2966–2973, Dec. 2012.

[34] J. Janesick, J. Pinter, R. Potter, T. Elliott, J. Andrews, J. Tower, J. Cheng, and J. Bishop, "Fundamental performance differences between CMOS and CCD imagers: Part III," in *Proc. SPIE*, 2009, vol. 7439.

[35] E. Stevens, H. Komori, H. Doan, H. Fujita, J. Kyan, C. Parks, G. Shi, C. Tivarus, and J. Wu, "Low-crosstalk and low-dark-current CMOS image-sensor technology using a hole-based detector," in *IEEE Int. Solid-State Circuits Conference (ISSCC) Tech. Dig.*, Feb. 2008, pp. 60–595.

[36] S. Place, J.-P. Carrere, P. Magnan, V. Goiffon, and F. Roy, "Rad tolerant CMOS image sensor based on hole collection 4t pixel pinned photodiode," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2888–2893, 2012.