CMOS Flat-Panel X-ray Detector With Dual-Gain Active Pixel Sensors and Column-Parallel Readout Circuits

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***Abstract*—This paper proposes a CMOS flat-panel X-ray detector (FPXD) with dual-gain active pixel sensors (APSs) and column-parallel readout circuits to reduce the random noise. The proposed dual-gain APS employs the conversion gain control in a pixel sensor array and supports both high and low sensitivity modes for FPXD. The in-pixel conversion gain control suppresses the amplification of the pixel noise, so it improves signal-to-noise characteristics. The column-parallel readout circuits include single-slope analog-to-digital converters (SS-ADCs) and charge-summing circuits for pixel binning and analog double delta sampling (DDS). SS-ADCs support 12-bit resolution and use the driving method of gray-code counters with different initial values to reduce the peak current and the power fluctuation. They also employ a high resolution continuous-type ramp generator to reduce the area. The proposed CMOS FPXD with a pixel size of $100\ \mu\text{m} \times 100\ \mu\text{m}$ was fabricated using a 0.18-μm CMOS process. The conversion gains in high and low sensitivity modes are designed with $0.43\ \mu\text{V}/\text{e}^-$ and $3.00\ \mu\text{V}/\text{e}^-$, respectively. The measured random noises in high and low sensitivity modes are $366\ \mu$V and $400\ \mu$V, respectively, at the resolution of 12 bits and the frame rate of 30 fps. The area of ramp generator and the peak current of the gray-code counter are reduced by 92% and 43%, respectively, compared with the conventional structures.**

***Index Terms*—CMOS X-ray detector, column-parallel readout, dual-gain pixel, medical X-ray imaging, single-slope analog-to-digital converter (SS-ADC).**

I. Introduction

BY THE remarkable development of image sensor and digital video processing technology, medical imaging research has progressed in high resolution and high speed imaging applications such as computed tomography, fluoroscopy, and mammography. For applications that require low noise, high resolution, and high speed operation, the flat-panel X-ray detector (FPXD) using CMOS transistors has become more suitable than those using amorphous silicon (a-Si) thin-film transistors (TFTs) [1], [2].

Conventional FPXD has used a-Si TFT for manufacturing on large-sized substrates [3], [4]. However, the FPXD based on a-Si TFTs suffers from high noise and slow operating speed due to the dangling bond of the amorphous crystal phase [1], [2]. In addition, extra noise is added due to the long signal path between the pixel circuit and off-chip readout integrated circuit, and the operating speed of an a-Si FPXD is limited by a large RC time-constant value, which is determined by the resistance of the TFT and the capacitances of the data line and pixel [1], [2].

The CMOS FPXD has been developed to enhance the signal-to-noise ratio (SNR) and the operating speed using CMOS transistors that are fabricated with single crystalline silicon. CMOS transistors have much higher electron mobility than a-Si TFTs, which enables the integration of active pixel sensors (APSs) and readout circuits, thus reducing the noise sources and increasing operation speed [5]–[9]. However, for medical imaging applications that require a large image acquisition area, the active area of CMOS FPXD is limited by wafer size. To solve the aforementioned problem, a three-side buttable FPXD has been developed by tiling multiple FPXDs into a large-sized panel so that the active area can be easily extended [5]–[7].

As CMOS FPXD technology is developing rapidly, the demands for multi-purpose applications such as radiography/fluoroscopy and interventional medical systems are increasing [10]. In order to implement the multi-purpose FPXD for various applications, multi-gain functions are necessary, because different amounts of X-ray energy and radiation dosage are required according to the medical X-ray applications [11]. For example, the high X-ray dose applications such as radiography and mammography require a FPXD with low sensitivity against X-ray dose; in contrast, low X-ray dose applications such as fluoroscopy require FPXD with high sensitivity. The conventional FPXD adopts the multi-step gain in the readout circuit to control the sensitivity of the pixel output. However, as the pixel output voltage is amplified in the readout circuit, the pixel noise is also amplified along with the gain of the readout circuit.

In this paper, we propose a CMOS FPXD with an in-pixel gain control circuit for multi-purpose applications. The proposed CMOS FPXDs employ dual-gain APS and column-parallel readout circuits. The dual-gain APS provides dual-step conversion gain of pixels by changing the capacitance of the pixels. To enhance the sensitivity and cancel out the pixel noise, the proposed charge-summing circuits adopt pixel binning and the analog double delta sampling (DDS) functions. The analog-to-digital converters (ADCs) in the readout circuits are implemented with single-slope ADCs (SS-ADCs) for good linearity and uniformity. In order to reduce the simultaneous

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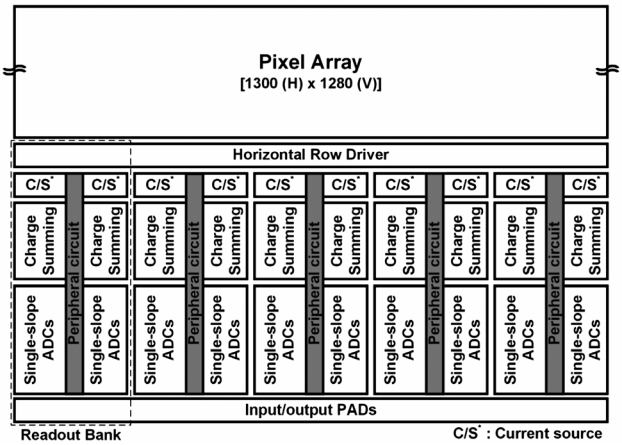


Fig. 1. Block diagram of CMOS FPXD.

switching noise of counters and the area of the ramp generator, we propose a novel driving method involving a gray-code counter and a scheme for a continuous-type ramp generator for 12-bit SS-ADC.

In section II of this paper, we describe the architecture of readout circuits in the proposed CMOS FPXD. The pixel circuit with dual-gain APS is explained in section III. Section IV shows the detailed implementation of the CMOS FPXD, which includes the charge-summing circuit, gray-code counter, and continuous-type ramp generator. In section V, the experimental results of the proposed FPXD are analyzed and compared with previous studies. Finally, the conclusions are given in section VI.

II. Architecture of CMOS Flat-Panel Detector

Fig. 1 shows the block diagram of the wafer-scaled CMOS FPXD, in which the pixel array is $1300(\mathrm{H}) \times 1280(\mathrm{V})$ with a pixel size of $100\ \mu\mathrm{m} \times 100\ \mu\mathrm{m}$. The total active pixel area of the single-wafer FPXD is $130\ \mathrm{mm}(\mathrm{H}) \times 128\ \mathrm{mm}(\mathrm{V})$. The readout circuits of the CMOS FPXD are separated into five readout banks by considering the maximum photolithographic area in wafer fabrication and the signal integrity of FPXD. Each readout bank consists of 260 column-parallel readout circuits, a peripheral circuit, and a horizontal row driver. They operate the individual image capturing process with reference and bias circuits in peripheral circuits.

The block diagram of a single readout bank is shown in Fig. 2. The column-parallel readout circuit is composed of tail current source (I_{TAIL}), charge-summing circuit, and SS-ADC. The tail current sources drive the source followers (M_{SF}) in pixel. The charge-summing circuits perform the analog DDS to cancel pixel noise and the 2×2 pixel binning to enhance the sensitivity and the frame rate. The SS-ADC, which consists of a gray-code counter, memory, and column multiplexer, quantizes the output voltage of the charge-summing circuit. The peripheral circuit is composed of reference buffer, bias circuit, bandgap reference, timing circuit, sense amplifier, and ramp generator for column-parallel readout circuits. The ramp generator in the peripheral circuit generates the ramp signal for SS-ADC operation. The horizontal row driver provides

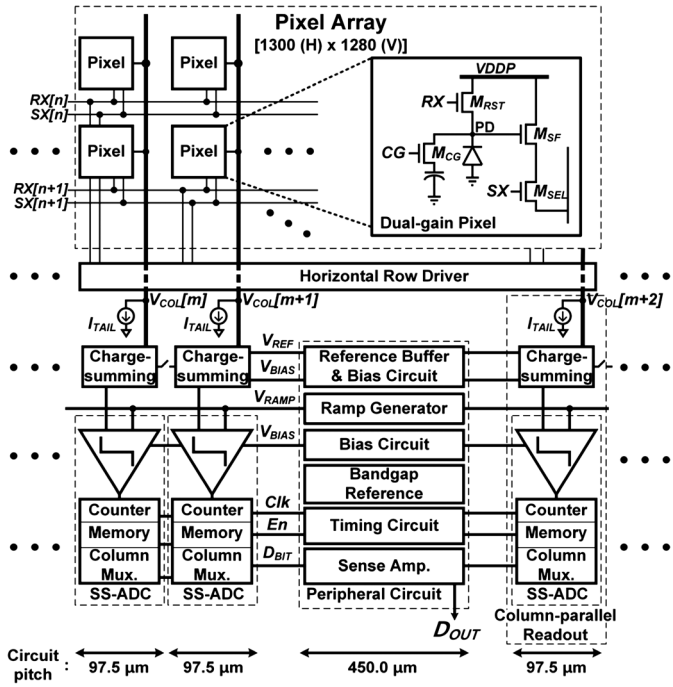


Fig. 2. Block diagram of a readout bank.

the timing signals to the pixel array for the reset and selection operations.

The column-parallel readout circuits are arranged in bilateral symmetry with respect to the peripheral circuit, which is located at the center of the readout bank, as shown in Fig. 1. In order to place the peripheral circuit between the column readout arrays, the column pitch of the readout circuits is designed to be $97.5\ \mu$m, which is less than the pixel pitch of $100\ \mu$m, as shown in Fig. 2. The horizontal row driver is placed in the horizontal direction with the readout circuit to form the three-side buttable CMOS FPXD.

III. Pixel Design

The proposed dual-gain pixel in Fig. 2 consists of four transistors, a photodiode, and a capacitor. It has three control signals, where RX, SX, and CG are the reset, select, and conversion gain control signals for the photodiode, respectively. The sensitivity of the proposed pixel circuits is determined by conversion gain, which is a function of photodiode capacitance at the node, PD. The conversion gain (G_{PD}) of a pixel is expressed as

$$G_{PD} = \frac{q}{C_{PD}} \times G_{SF}, \tag{1}$$

where q is the quantum of electron charge of 1.6×10^{-19} C, C_{PD} is the capacitance at the node of PD with respect to the ground, and G_{SF} is the gain of source follower in pixel [5]. The control signal (CG) of M_{CG} is used to change C_{PD} and to implement the in-pixel dual-gain function for the multi-purpose FPXD. For the low sensitivity mode in which M_{CG} is turned on, C_{PD} is increased and the sensitivity of the pixel circuit is decreased. For the high sensitivity mode in which M_{CG} is turned off, the sensitivity is increased as C_{PD} is decreased.

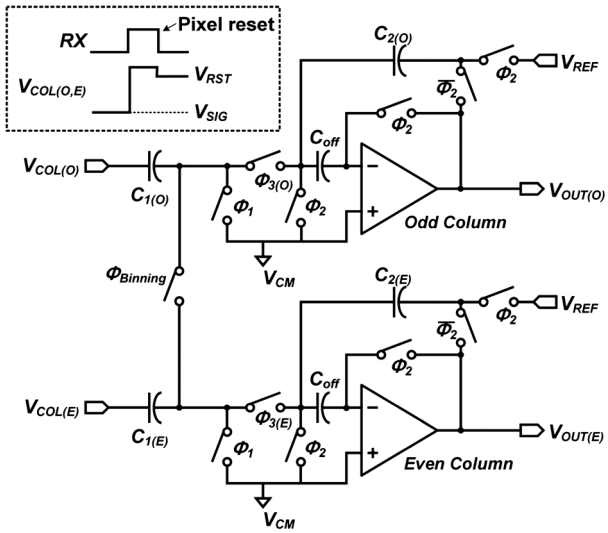


Fig. 3. Schematic diagram of charge-summing circuits for two channels.

The capacitances of the photodiode and the additional capacitor are determined by the required full well capacity for medical X-ray imaging applications. The sensitivity of low-dose fluoroscopy is generally 4-8 times higher than that of high-dose imaging applications such as radiography [11]. The in-pixel gains of $\times 1$ and $\times 7$ are designed with the pixel capacitance (C_{PD}) of 318 fF and 45 fF, respectively. The conversion gains (G_{PD}) are determined to $0.43\ \mu\mathrm{V/e^-}$ and $3.00\ \mu\mathrm{V/e^-}$ by (1) in the low and high sensitivity modes, respectively, with the gain of source follower (G_{SF}) of 0.85 V/V. Accordingly, the photodiode and additional capacitor for conversion gain control are designed with capacitances of 45 fF and 273 fF, respectively.

IV. Implementations of Readout Circuit

A. Charge-summing Circuit

Figs. 3 and 4 show the block and timing diagrams, respectively, of the proposed charge-summing circuit, which performs pixel binning and analog DDS operations. The charge-summing circuit has an input terminal ($V_{COL(E)}$ or $V_{COL(O)}$) which is connected to pixel outputs, four control signals (Φ_1, Φ_2, Φ_3, and $\Phi_{Binning}$), and two reference voltages (V_{CM} and V_{REF}). The pixel binning is selected by $\Phi_{Binning}$ and the analog DDS is operated by Φ_1, Φ_2, and Φ_3, as shown in Fig. 4. In the full resolution mode, the analog DDS operation is separated into two sequences. When Φ_1 and Φ_2 are high, the feedback capacitor (C_2) is initialized and the offset cancellation is performed for the amplifier, and the signal voltage (V_{SIG}) of the pixel at $V_{COL(E,O)}$ is sampled in C_1. After the reset operation of the pixel by RX, the voltage at $V_{COL(E,O)}$ is changed to reset voltage (V_{RST}) of the pixel. When Φ_1 and Φ_2 go low and Φ_3 goes high, the output voltage (V_{OUT}) of the charge-summing circuit is given by

$$V_{OUT} = -\frac{C_1}{C_2} \times (V_{RST} - V_{SIG}) + V_{REF}, \qquad (2)$$

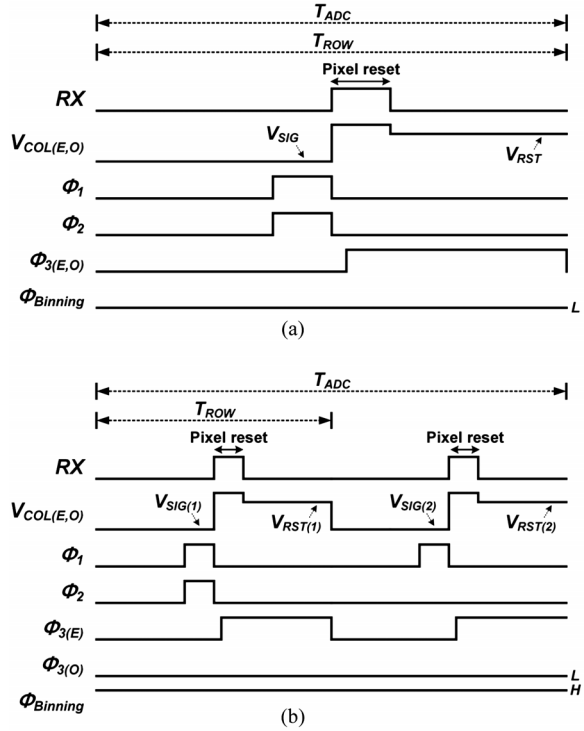


Fig. 4. Timing diagram of charge-summing circuits in (a) full resolution mode and (b) pixel binning mode.

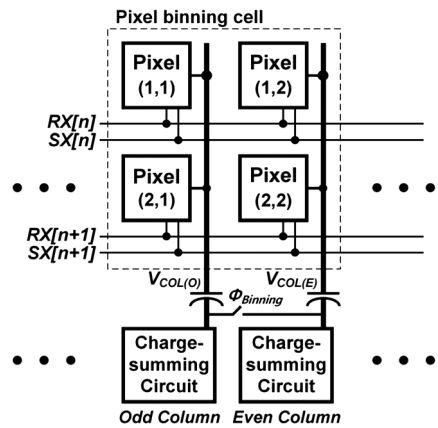


Fig. 5. Block diagram of a 2×2 pixel binning cell.

where V_{REF} is the reference voltage in the charge-summing circuit. The output voltage is sampled at the input stage of the ADC and is quantized to digital data in every row line time (T_{ROW}), which is equal to the ADC conversion time (T_{ADC}).

The pixel binning is done by the charge-summing operation of the adjacent 2×2 pixels, as shown in Fig. 5. The sensitivity and the frame rate are enhanced using the binning signal ($\Phi_{Binning}$). In 2×2 pixel binning, $C_{1(O)}$ and $C_{1(E)}$ are connected together and only even charge-summing circuits are operated. The even charge-summing circuits sum the charges of even and odd column voltages ($V_{COL(E)}$ and $V_{COL(O)}$) in two adjacent rows, and the odd charge-summing circuits are set to power-down mode to reduce the power consumption.

Fig 4(b) shows the timing diagram of the 2×2 pixel binning operation. Firstly, when Φ_1 and Φ_2 are high, the initialization of

$C_{2(E)}$ and the offset cancellation of the amplifier are performed and the even and odd column signal voltages ($V_{SIG(1)}$) of the pixels are sampled in $C_{1(E)}$ and $C_{1(O)}$, respectively. After the reset operation of a pixel by RX, Φ_1 and Φ_2 go low and $\Phi_{3(E)}$ goes high, and the sampled charges in $C_{1(E)}$ and $C_{1(O)}$ are transferred to $C_{2(E)}$ by reset voltages ($V_{RST(1)}$) of pixels. In addition, $\Phi_{3(O)}$ for the odd circuits maintains an off state in order to block the charge transfer into odd circuits. In the charge summing operation for the second row line time, $C_{1(E)}$ and $C_{1(O)}$ capture the even and odd column signal voltages ($V_{SIG(2)}$) of pixels without the initialization of $C_{2(E)}$ by Φ_1. After the pixel output ($V_{COL(E,O)}$) is changed to the reset voltage ($V_{RST(2)}$), Φ_1 goes low and $\Phi_{3(E)}$ goes high, and the charges of $C_{1(E)}$ and $C_{1(O)}$ are also added to $C_{2(E)}$. Finally, the output voltage (V_{OUT}) of the charge-summing circuit is expressed as

$$V_{OUT} = -\frac{C_1}{C_2} \times [(V_{RST(1,1)} + V_{RST(1,2)} + V_{RST(2,1)} + V_{RST(2,2)}) - (V_{SIG(1,1)} + V_{SIG(1,2)} + V_{SIG(2,1)} + V_{SIG(2,2)})] + V_{REF}, \quad (3)$$

where $V_{RST(1,1)}$, $V_{RST(1,2)}$, $V_{RST(2,1)}$, $V_{RST(2,2)}$, $V_{SIG(1,1)}$, $V_{SIG(1,2)}$, $V_{SIG(2,1)}$, and $V_{SIG(2,2)}$ are the reset and signal voltages of pixel (1,1), (1,2), (2,1), and (2,2) in Fig. 5, respectively. In pixel binning mode, the analog DDS operation is performed in the same way as in full resolution mode. After the readout operation for 2×2 pixel, the output voltage is converted to digital data by ADC in the ADC conversion time (T_{ADC}), which is equal to twice the row line time ($2 \times T_{ROW}$).

B. Gray-code Counter

The counters in SS-ADCs count the clock cycles until the ramp signal reaches the input voltage of the SS-ADC. The counting operation occurs in every bit transition at every clock. Moreover, when the most significant bit (MSB) is changed, the binary counter changes every one of its bits and generates the largest peak current. In the case of the column-parallel readout structure, the bit transitions in every bit of all column counters generate a large peak current from the supply voltage to the ground level, which causes a power fluctuation. Specifically, in the readout circuits for CMOS FPXD, which has a width of 2.6 cm, it is crucial to reduce the peak current to make the power supply stable in all readout circuits.

In order to suppress the peak current, the gray-code counter is used in the CMOS FPXD [12]. The gray-code counter has only one-bit transition at one clock cycle. To alleviate the power fluctuation issues, we proposed even and odd counters in column-parallel readout arrays that have different initial values of "0" or "1". Fig. 6 shows the timing diagram of 4-bit gray-code counters with the proposed driving method from two columns. Because the adjacent two column counters have different initial values, the halves of bit streams are transited in opposite direction. The bit transitions in opposite direction are cancelled out, which reduces peak current and power fluctuation.

As shown in Fig. 7, the simulation results of the peak current of a binary counter and that of a gray-code counter without and with different initial values are 7.18 mA, 4.49 mA, and 4.09 mA,

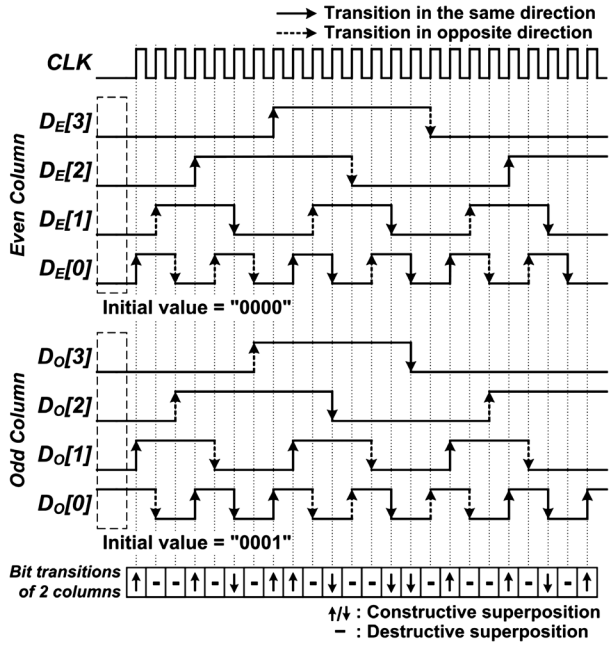


Fig. 6. Timing diagram of the proposed driving method of the 4-bit column counters with different initial values. D_E[3-0] and D_O[3-0] are the outputs of the even and odd counters, respectively. The bit transitions of two columns represent the constructive or destructive superposition of bit stream edges from two column counters at every clock.

respectively. Using the gray-code counter with different initial values reduced the peak current by 43% as compared to that of the binary counter. The simulation results show that the average power consumptions for binary and gray-code counter are 255.8 μW and 334.2 μW, respectively. The gray-code counter requires more logic gates for gray-coding and consumes more power compared with the binary counter. However, because the peak current is considered to be more important than the average power consumption to prevent the power fluctuation in the digital circuit, the gray-code counter is used for SS-ADCs.

C. Continuous-type Ramp Generator

In general, the ramp generator generates the ramp signal to compare the input voltages of SS-ADC; the current steering digital-to-analog converter (DAC) type ramp generator is used for the general SS-ADC in imaging applications [13]. However, the DAC-type ramp generator requires a large area to implement SS-ADCs over 12-bit resolution. For example, the 12-bit DAC-type ramp generator requires 4096 unit cells and occupies at least 0.75 mm^2 [14]. In contrast, the proposed continuous-type ramp generator, which has five transistors, four switches, two capacitors, and one operational transconductance amplifier (OTA), as shown in Fig. 8(a), requires only 0.06 mm^2. Also, the power consumption is reduced by using the proposed continuous ramp generator. The current steering DAC consumes a large load current from 15 to 50 mA [15], whereas the proposed ramp generator consumes the current of only 5 and 85 μA for output load and peripheral control circuit, respectively.

The timing diagram of the continuous-type ramp generator is shown in Fig. 8(b). In the ramp phase, the ramp signal (V_{RAMP}) is decreased from the top voltage (V_{TOP}) to the bottom voltage

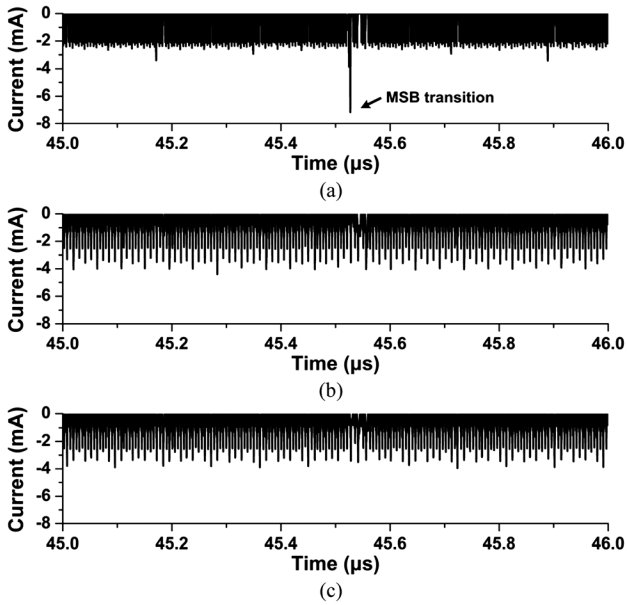


Fig. 7. Simulation results of peak current from two column counters; using (a) binary counter and gray-code counter (b) without and (c) with different initial values.

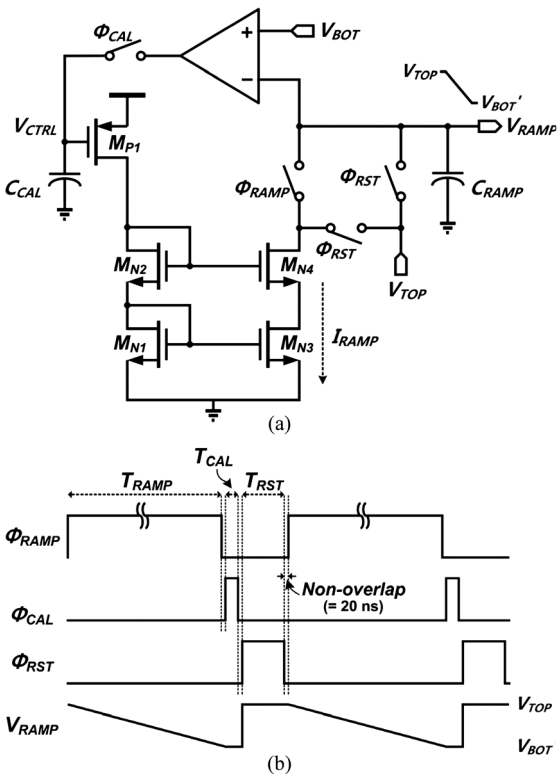


Fig. 8. (a) Schematic and (b) timing diagrams of the proposed continuous-type ramp generator.

(V_{BOT}) during the ramping duration (T_{RAMP}) which has 4096 clock cycles for 12-bit SS-ADC. V_{RAMP} is expressed as

$$V_{RAMP} = V_{TOP} - \frac{I_{RAMP}}{C_{RAMP} + C_{LOAD}} \cdot T_{RAMP}, \qquad (4)$$

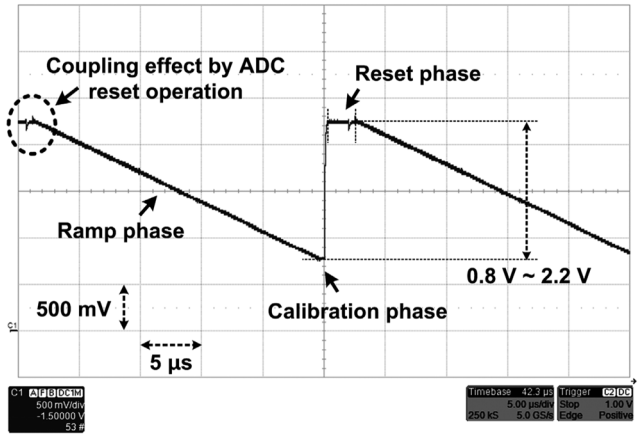


Fig. 9. Measured ramp signal from 2.2 V to 0.8 V at 30 fps.

where I_{RAMP}, C_{RAMP}, and C_{LOAD} are the load current to generate V_{RAMP}, the output capacitance, and the load capacitance of the ramp generator, respectively. Since T_{RAMP} and C_{RAMP} are determined at the early design stage whereas C_{LOAD} is varied by process variation, M_{P1} in Fig. 8(a), which generates the I_{RAMP}, should support the wide range of current driving capabilities. In the calibration phase, the current bottom voltage ($V_{BOT'}$) of V_{RAMP} is calibrated to the desired bottom voltage (V_{BOT}) using a negative feedback system that consists of the OTA, capacitor, and current source. The OTA output voltage is determined by the difference between $V_{BOT'}$ and V_{BOT} and it is integrated into the calibration capacitor (C_{CAL}) during calibration time (T_{CAL}). The control voltage (V_{CTRL}) reaches the voltage level by which I_{RAMP} can swing V_{RAMP} from V_{TOP} to V_{BOT}. The stability of the feedback system is determined by the gain of OTA, the size of C_{CAL}, and the duration of T_{CAL}. To make the ramp generator stable, a single-stage amplifier as an OTA and C_{CAL} of 20 pF are used, and T_{CAL} is controlled by the external timing system. Then, the V_{RAMP} is reset to V_{TOP} in the reset phase and the operation of the ramp generator returns to the ramp phase. The reset phase should be maintained until the coupling noise by ADC reset operation has disappeared.

The simulation results of the ramp generator show a time-to-time variation at the bottom voltage of 85 μV, which is 0.25 least significant bits (LSB) at 12-bit resolution. This variation represents a gain error of SS-ADC and it occurs due to the variations in V_{CTRL} during the calibration phase. The ramp signal is measured from 2.2 V to 0.8 V at 30 fps, as shown in Fig. 9. The error of the ramp generator extracted by the output images is 0.69 LSB at 12-bit resolution and 30 fps.

V. Experimental Results

Fig. 10 shows the photograph of a CMOS FPXD wafer that was fabricated using a 0.18-μm 1-poly 4-metal CMOS process with buried photodiode for the pixel. The active area is 130 mm × 128 mm, with a pixel array of 1300(H) × 1280(V) and a unit pixel size of 100 μm × 100 μm. The readout circuits have five

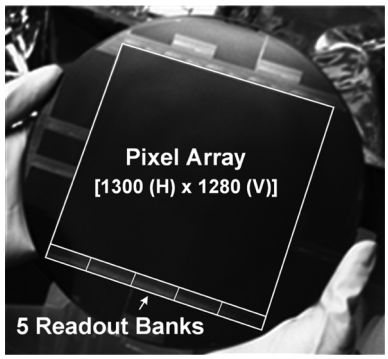


Fig. 10. Photograph of CMOS FPXD wafer.

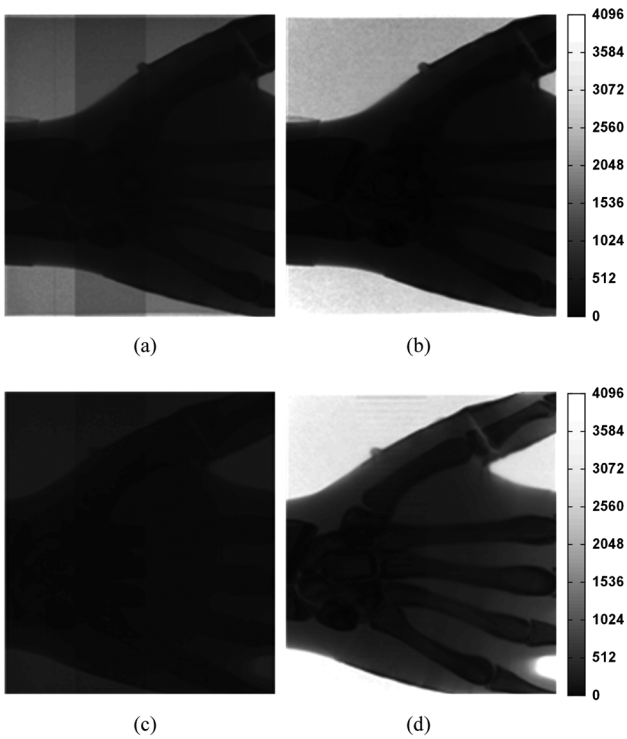


Fig. 11. (a), (c) Captured raw images and (b), (d) processed images of CMOS FPXD with output data from 0 to 4095, frame rate of 30 fps, tube voltage of 50 kV, and tube current of 2.0 mA. (a) and (b) are the images of the high sensitivity mode, while (c) and (d) are the images of the low sensitivity mode.

banks, which consist of 260 readout channels and peripheral circuits and operate at 180 MHz for 30 fps.

CMOS FPXD is packaged with DRZ+(Gd2O2S:Tb) as a scintillator film for converting X-ray to visible light [16]. The scintillator film is attached directly to the pixel array of CMOS FPXD. Fig. 11(a) and (c) show the captured raw images of a hand phantom with the proposed CMOS FPXD when the image depth, frame rate, tube voltage, and tube current are 12-bit, 30 fps, 50 kV, and 2.0 mA, respectively, using a cone-shaped X-ray source. The raw images have bank-to-bank variations of CMOS FPXD due to the shot-to-shot variations of the stitching process. In addition, the scintillator and scintillator-photodiode interface causes the non-uniformity at the raw images. However, the aforementioned errors, bank-to-bank variations and non-uniformity, are cancelled by using the offset and gain map

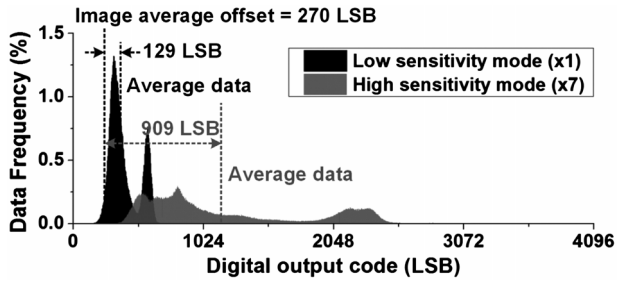


Fig. 12. Histogram of Fig. 11(a) and (c) at low and high sensitivity mode, respectively.

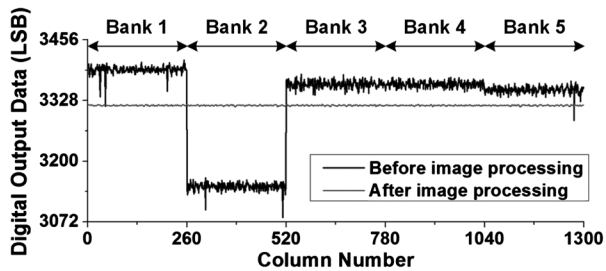


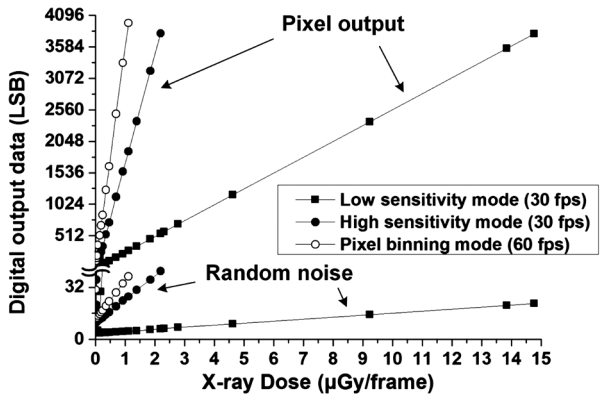
Fig. 13. Output data in the direction of column before and after image processing.

of images at the back-end system. The offset and gain map are extracted from the dark state images and the near-saturation images. Fig. 11(b) and (d) show the processed images at the back-end system after the error cancellation and contrast-ratio enhancement.

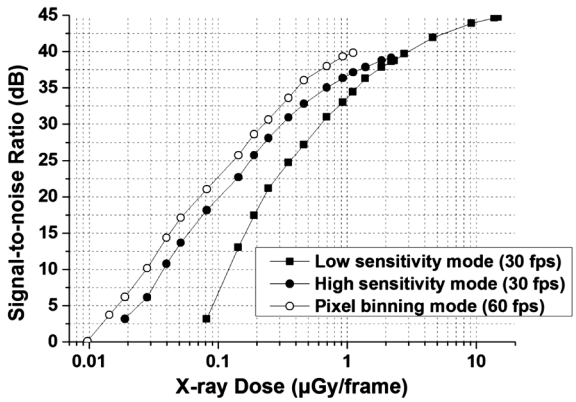
The image performances including random noise, fixed pattern noise (FPN), and SNR are evaluated using the consecutively captured images of 30 frames. The average and standard deviation of the consecutive images represent the signal output and the random noise of the CMOS FPXD. The bank-to-bank variation and the column FPN are extracted from the average image.

To verify the performance of the dual-gain pixel, the image outputs of the high and low sensitivity modes are compared. The histograms of Fig. 11(a) and (c) are shown in Fig. 12. Under the same conditions, the captured images show that the average data, excepting the average offset data of 270 LSB, are 909 LSB and 129 LSB in high and low sensitivity modes, respectively. The average offset data is estimated from averaging the all pixel data of $1300(\mathrm{H}) \times 1280(\mathrm{V})$ for the 30 consecutive frames at dark state. The ratio between the average data of high and low sensitivity modes is 7.0, which is equal to the conversion gain of the pixels. The pixel random noises of the high and low sensitivity mode, which are extracted from output images, are 1.17 LSB ($400\ \mu$V) and 1.07 LSB ($366\ \mu$V), respectively. The noise level is calculated from the standard deviations of consecutive images.

Fig. 13 shows the output data in the direction of columns in order to verify the column variation before and after image processing. After the image processing, the maximum variation of the images is reduced from 246.3 LSB to 1.9 LSB at 12-bit resolution. The column FPNs for a readout bank before and after image processing are 7.96 LSB and 0.59 LSB, respectively.

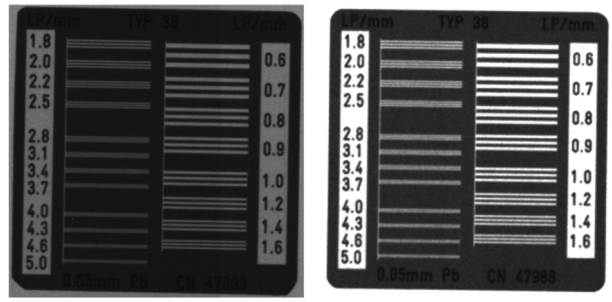


(a)



(b)

Fig. 14. (a) Pixel output data, random noise, and (b) calculated SNR of CMOS FPXD with respect to X-ray dose per frame.



(a) (b)

Fig. 15. Partial view of the captured images (a) in the full resolution mode with 30 fps and spatial resolution of 520×520 and (b) in the binning mode with 60 fps and spatial resolution of 260×260.

TABLE I
PERFORMANCE SUMMARY

Parameter	Value
Process	0.18-μm 1P4M CMOS process
Active area	130 mm (H) × 128 mm (V)
Resolution	1300 (H) × 1280 (V)
Pixel size	100 μm × 100 μm
QE × FF	60 %
MTF	32.45 % at 2 lp/mm (full resolution mode) 20.65 % at 2 lp/mm (2 × 2 pixel binning mode)
Sensitivity	2.94 mV/(μGy·sec) (low sensitivity mode) 20.4 mV/(μGy·sec) (high sensitivity mode)
Pixel conversion gain	0.43 μV/e^- (low sensitivity mode) 3.00 μV/e^- (high sensitivity mode)
Pixel random noise	366 μV (low sensitivity mode) 400 μV (high sensitivity mode)
Column FPN	201 μV
SNR	44.7 dB at 15 μGy (low sensitivity mode, 30 fps) 39.2 dB at 2.2 μGy (high sensitivity mode, 30 fps) 39.8 dB at 1.1 μGy (pixel binning mode, 60 fps)
Dynamic range	70.6 dB (low sensitivity mode, 30 fps) 60.5 dB (high sensitivity mode, 30 fps) 57.3 dB (pixel binning mode,60 fps)
ADC input range	1.4 V
ADC resolution	12-bit
Frame rate	30 fps (full-resolution) 60 fps (2x2 pixel binning)
Power supply	3.3 V (analog) 1.8 V (digital)
Power consumption at 30 fps (1 column)	151.8 μW (analog) 533.9 μW (digital)

The image performances of random noise and dynamic range are evaluated using the captured images without objects. Since the X-ray intensity is linear with respect to tube current, the images are acquired by increasing the tube current with a fixed tube voltage of 50 kV. The pixel output data, random noise, and SNR in the high and low sensitivity modes with respect to the X-ray dose per frame are shown in Fig. 14. The pixel output data are saturated at $2.2\ \mu$Gy and $15\ \mu$Gy with 30 fps in the high and low sensitivity modes, respectively. As the X-ray dose increases, the shot noise of the photodiode becomes dominant noise source. Consequently, the random noise in the high sensitivity mode becomes larger than that in the low sensitivity mode. SNR in the high sensitivity mode is higher than that in the low sensitivity mode in the region of low X-ray dose, which provides better quality images compared with images with digital gain in the low sensitivity mode. Under the saturation conditions, SNRs in the high and low sensitivity modes are 39.2 dB and 44.7 dB, respectively. The dynamic range in low and high sensitivity modes are 70.6 dB and 60.5 dB. The dynamic range in high sensitivity mode is less than that of low sensitivity mode because the high sensitivity mode performs faster saturation of signal than low sensitivity mode, as the X-ray dose is increased.

In pixel binning mode, the image resolution mode is reduced from $1300(\mathrm{H}) \times 1280(\mathrm{V})$ to $650(\mathrm{H}) \times 640(\mathrm{V})$, but the sensitivity of the pixels and the frame rate are increased by two-fold at the same A/D conversion rate. To analyze the performance in pixel binning mode, the full resolution with 30 fps and pixel binning mode with 60 fps is compared at high sensitivity setting. Fig. 14 shows the pixel output, random noise, and SNR of the full resolution mode with 30 fps and pixel binning mode with 60 fps. The pixel random noise is averaged out by charge summing operations in the binning mode and SNR of pixel binning mode is improved by 2.7 dB compared with that of full resolution mode as shown in Fig. 14(b). The dynamic range of pixel binning mode is 57.3 dB which is decreased value by 3.5 dB from that of full resolution mode. Fig. 15 shows the partial view of the captured images for the same size of resolution chart in the full resolution mode with 30 fps and spatial resolution of 520×520, and in the binning mode with 60 fps and spatial resolution of 260×260.

The product of quantum efficiency and fill factor is 60% in the proposed CMOS FPXD. The measured modulation transfer functions (MTFs) at 2 lp/mm are 32.45% and 20.65%, in the

TABLE II
COMPARISON OF CMOS FPXD

Parameter	This work	[6]	[8]	[9]
Pixel pitch	100 μm	150 μm	100 μm	70 μm
ADC	On-chip, 12-bit	On-chip, 12-bit	On-chip, 14.3-bit	External, 14-bit
Gain control	×1 / ×7 (in-pixel)	None	None	None
Random noise				
- at × 1 gain	366 μV,	250 μV,	461 μV,	219 μV,
- at × 7 gain	400 μV	< 1750 μV (estimated)	< 3227 μV (estimated)	1533 μV (estimated)
Row line time	25.6 μs	34.6 μs	13.9 μs	136.5 μs

full resolution mode and pixel binning mode, respectively. The calculated conversion gain is $0.43\ \mu$V/e$^-$ and $3.00\ \mu$V/e$^-$, and the measured sensitivities are $2.94\ \text{mV}/(\mu\text{Gy}\cdot\text{sec})$ and $20.4\ \text{mV}/(\mu\text{Gy}\cdot\text{sec})$, in low and high sensitivity modes, respectively. The measured differential non-linearity (DNL) and integral non-linearity (INL) of ADC are $+0.98/-0.89$ LSB and $+0.13/-7.6$ LSB, respectively. In the imaging applications, DNL is more important than INL, because the human eye cannot detect the non-linearity of INL under 8 LSB at 12-bit resolution [17].

Table I shows the performance summary of the CMOS FPXD. The performance of our proposed CMOS FPXD is compared with previously reported works in Table II. The proposed FPXD is the only detector that can provide an in-pixel gain control function with low noise and high speed performance. Particularly with $\times 7$ in-pixel gain, the pixel random noise of the proposed FPXD is much smaller than those of the other FPXDs.

VI. CONCLUSIONS

A CMOS FPXD with dual-gain APSs and column-parallel readout circuits embedding SS-ADCs is proposed. For multi-purpose medical imaging applications without increasing the noise level, the proposed CMOS FPXD adopts the dual-gain APSs with in-pixel conversion gain control circuit. The dual-gain APS successfully operates in the high and low sensitivity modes with pixel noise levels of 1.78 and 1.07 LSB, respectively. Also, the proposed FPXD uses column-parallel readout circuits with the charge-summing circuit, the area-efficient ramp generator, and the peak current reduction techniques involving a gray-code counter for real-time and high resolution X-ray imaging application. The charge-summing circuit provides the analog DDS and 2×2 pixel binning to suppress random noise. The area of ramp generator and the peak current of the gray-code counter are reduced by 92% and 43%, respectively, compared with the conventional structures. Therefore, the proposed FPXD is suitable for multi-purpose X-ray imaging applications with real-time, high resolution, and low noise.

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