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Single-Event Effects in Heavy-Ion Irradiated 3kV SiC Charge-Balanced Power Devices

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***Abstract*— Experimental heavy-ion responses of 3 kV charge-balanced (CB) SiC power devices are compared to those of 3.3 kV planar SiC devices. The devices are similar, except the epitaxial region of the CB devices is heavily doped compared to the planar devices. The higher doping in the epitaxial region results in lower on-resistance, but typically leads to a lower threshold drain voltage at which single-event burnout occurs. The experimental results demonstrate, however, that the CB devices have a similar SEB threshold to the planar devices due to the improved electric field distribution.**

***Index Terms*— Silicon carbide (SiC), charge-balanced (CB) power devices, superjunction devices, junction-barrier Schottky (JBS) diodes, single-event effects, degradation, heavy ion, MOSFET, single-event burnout (SEB), single-event leakage current (SELC)**

I. Introduction

WIDE bandgap silicon carbide (SiC) power metal-oxide-semiconductor field effect transistors (MOSFETs) and diodes are relatively mature in terms of typical reliability and performance measures [1]. However, single-event effects (SEE) due to heavy-ion irradiation often occur in commercial SiC power devices at voltages 50% or lower than the rated breakdown voltage, which limits usage in space environments [2-5]. This paper examines SEE in SiC CB junction barrier Schottky (JBS) diodes and vertical double diffused MOSFETs (VDMOSFETs) to understand how the device structure affects single-event burnout (SEB) and single-event leakage current (SELC). 3 kV SiC CB devices are fabricated utilizing a novel drift layer architecture that outperforms the 1-D $R_{on,sp}$ versus breakdown voltage limit through buried p-doped regions inside the drift layer [6].

Experimental data from heavy-ion testing, as well as modelling data from Technology Computer Aided Design (TCAD) simulations, indicate that a common mechanism exists for single-event burnout (SEB) as well as single-event leakage current (SELC) degradation in both MOSFETs and diodes [7-14]. Single-event burnout is also a major problem in GaN HEMTs [15-16], and β-Ga_2O_3 Schottky diodes [17-18] when exposed to heavy ions. Previous research has shown that the mechanism of SEB in SiC devices is an electric field collapse that behaves something like a short circuit between the body and the drain contact [12-14].

In this work, we report the SEB boundaries for 3 kV SiC CB diodes and MOSFETs and compare them to the 3.3 kV planar device results for various ions having a wide range of linear energy transfer (LET) values. The results indicate that the SEB boundary is similar for the two types of devices, even though the avalanche breakdown voltage for the CB devices is 3300 V compared to 4000 V for the planar devices. Heavy ion irradiation was performed for 3 kV CB JBS diodes and VDMOSFETs alongside 3.3 kV planar SiC PiN diodes and VDMOSFETs using the Texas A&M University Cyclotron. The diodes and MOSFETs were irradiated up to a bias of 2000 V, and the devices exhibited both catastrophic single-event burnout (SEB), as well as single-event leakage current (SELC) degradation at LETs from 2.8 to 86.9 MeV/(mg/cm^2). The results indicate that the voltage at which the CB devices experience SEB is a somewhat higher fraction of their avalanche breakdown voltage when compared to the planar devices, although they are susceptible to SELC degradation at lower voltages compared to the planar devices at higher LETs.

II. SiC Charge-Balanced Devices

The Charge-Balanced JBS diodes and VDMOSFETs were fabricated by General Electric Research on 100 mm 4°-off 4H-SiC n-type substrates [19]. The drift layer of these diodes and

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MOSFETs consists of three n-type approximately 10 µm thick epitaxial layers with doping concentration of 10^{16} cm^{-3} that were grown in three consecutive runs followed by top P+ JBS and P-Junction Termination Extension (JTE) implantations for the diode as shown in Fig. 1. Shallow implantation was implemented in between growth runs to form two buried P-type CB regions inside the epitaxial layers. In reverse-bias mode, the p-doped CB-regions are depleted and with proper design, they can balance n-doped charges adjacent and below the CB-regions inside the drift layer and act as an electric field divider. The CB MOSFETs have a pitch of 2 mm (both x and y) and have an active area of 0.011 cm^2. Whereas, the CB diodes have a pitch of 1.5 mm (both x and y), with an active area of 0.008 cm^2.

Consequently, this device design allows higher doping concentration of the drift layers for the same breakdown voltage. As reported in earlier literature, CB diodes with floating CB regions exhibit significant turn-on loss due to the slow carrier generation-recombination rate during transition from blocking to conduction [20]. To avoid these floating CB regions, intermittent deep vertical P-type pillars (P-bus) were implemented using high energy implantation [22] to supply holes from the P+ JBS anode to the buried CB-regions throughout the active area of the diode. The purpose of the P-bus pillars was to optimize electric field distribution and simultaneously provide a conductive path for charges during turn-on. CB regions, P-Bus pillars, P+ JBS regions, and JTEs were all formed using Al implantation, followed by an activation anneal, field oxide deposition, and frontside and backside metallization. Ni was selected as the Schottky top contact with Al over-layer metallization. The fabrication of diodes concluded with nitride and polyimide passivation layers for high voltage surface protection.

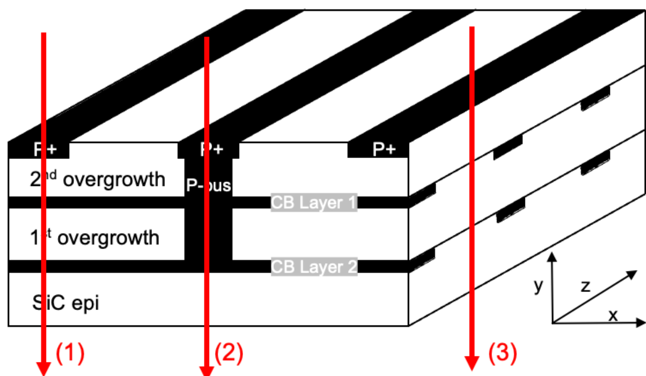

Fig. 1. Perspective view of a 3kV SiC Charge-Balanced (CB) Junction Barrier Schottky (JBS) diode after [19-21] and possible ion-strike locations to determine the worst-case radiation response of the 3 kV SiC CB device, with (1) and (2) being unique to the CB devices and (3) being almost identical to a planar device. The SiC epitaxial and two overgrowth layers (shown in white) are each 10 µm thick, with doping concentration of 10^{16} cm^{-3}.

In Fig. 1, three distinct heavy-ion strike locations are considered to determine their worst-case response. Strike locations 1 and 2 are unique to the CB devices; the dependence on location is further explored in the TCAD modelling section. Strike location 3 is identical to a planar device with only a single additional P+ JBS layer in the ion path. The radiation responses at these three strike locations are expected to be different from one another due to their underlying structural differences.

III. Experimental Heavy-Ion Irradiation Results

A. Experimental Method

The SiC power devices tested are open-cavity packaged charge-balanced SiC JBS diodes and MOSFETs from General Electric. These devices were designed to have 3000 V blocking voltages. Between three and five MOSFETs and diodes were tested with each heavy-ion.

Heavy ion testing was conducted in air with a 3 cm gap from rear foil to the device under test (DUT) at the Texas A&M University Cyclotron facility. The heavy ions used for irradiation of the SiC power diodes and MOSFETs are 15 MeV/u neon (Ne), krypton (Kr), silver (Ag) and praseodymium (Pr) as shown in Table I.

Table I

Details of K500 Heavy-Ion Beams Used for Experiment at Texas A&M University Cyclotron

Ion	MeV/u	LET in SiC after 3 cm air MeV/(mg/cm^2)	Range in SiC after 3 cm air (µm)
^{20}Ne	15	2.8	188.4
^{40}Ar	15	8.6	132.7
^{84}Kr	15	29.8	89.2
^{109}Ag	15	46.8	75.6
^{141}Pr	15	63.9	79.4
^{197}Au	15	86.9	82.4

A fluence of 10^6 ions/cm^2 was used during each bias. The flux was set to 10^4 ions/(cm^2·s) for the experiments which means the devices were irradiated for about 100 s during each run at a particular bias. The LET and range of the heavy ions in SiC were calculated using SRIM [23]. During the irradiations, each JBS diode was reverse biased with a fixed voltage and the reverse leakage current was monitored during each run. For the MOSFET, the high voltage bias was supplied to the drain terminal with the gate terminal grounded, and both the gate and drain leakage currents were monitored during each run. The bias was varied from 200 V to 2000 V with coarse and fine step increments during irradiation. The device current was monitored and recorded during each experiment using high voltage source-measurement units (SMUs). The bond wires and the package edges were inspected to ensure no shadowing effects would occur during irradiation. Each device was characterized before and after the heavy-ion irradiation runs by generating a reverse-bias I-V sweep for the JBS diodes and drain-source I-V sweep for the MOSFETs using an Agilent B1505A parameter analyzer, up to the maximum supported voltage of 3000 V. Also, forward-bias I-V sweep tests were run from the off state to the on state of each device. A thermal camera was present at the TAMU Cyclotron for real-time monitoring of temperature at the ion beam target, which was

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useful to identify whether a catastrophic SEB has occurred.

B. Experimental Results & Discussions

The SEB threshold in the 3 kV DUTs was determined using heavy ions of different LET. Using coarse bias voltage steps of 200 – 400 V, the SEB threshold was identified for these devices and plotted versus LET as shown in Fig. 2. The SEB thresholds for the CB JBS diodes and VDMOSFETs from this experiment are shown in Fig. 2. The observed SEB thresholds for these 3 kV DUTs are compared with the SEB thresholds of 3.3 kV planar PiN diodes and VDMOSFETs from previous work in [24]. The planar devices are made of 4H-SiC with an epitaxial layer approximately 30 µm thick, making the total drift region thickness in both types of devices identical and thus comparing their SEB responses for parts selection and qualification makes sense. The avalanche breakdown occurs for the CB devices at 3300 V whereas it occurs at 4000 V for the planar devices, as described in Table II. Both the planar and CB devices were fabricated by the same manufacturer, General Electric Research, and packaged in open-cavity TO-247-3 packages.

TABLE II

SUMMARY OF TESTED DEVICES

Device Type	Device Class	Rated Voltage (V)	Breakdown Voltage (V)
Diode	Planar	3300	4000
	CB	3000	3300
MOSFET	Planar	3300	4000
	CB	3000	3300

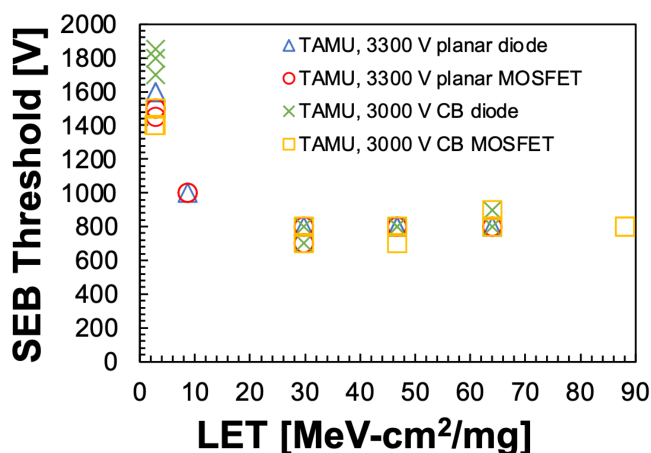

Fig. 2. SEB threshold of 3 kV CB JBS diodes and VDMOSFETs compared with the SEB threshold of 3.3 kV Planar PiN diode and VDMOSFETs after [24]. Both devices were tested at TAMU Cyclotron Facility using the same heavy-ions and total fluence during each run.

The SELC thresholds, on the other hand, from this experiment are shown in Fig. 3. Using fine bias voltage steps of 25 – 50 V, the SELC threshold was identified for these devices and plotted versus LET as shown in Fig. 3. The absolute values of SELC thresholds in the CB devices are observed to be lower than the planar devices when irradiated with high-LET heavy-ions as shown in Fig. 3. This lower SELC tolerance in the CB devices can be potentially due to their higher epitaxial region doping compared to the planar devices, causing the onset of degradation earlier at higher LETs. However, when compared as a percentage of the breakdown voltage, the normalized SELC thresholds in the CB devices are higher as discussed later.

Both the SEB and SELC thresholds are normalized in terms of the avalanche breakdown voltages of the respective devices as shown in Fig. 4 for the diodes and Fig. 7 for the MOSFETs. This shows that the normalized SEB threshold of the CB devices is proportionately higher than the planar devices. SEB occurred at 20-40% of the breakdown voltage for the planar devices, whereas SEB occurred in the CB devices at about 25-50% of the breakdown voltage at the same LET.

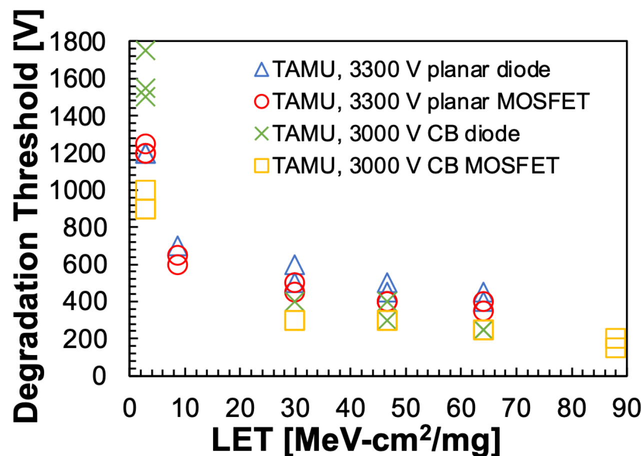

Fig. 3. SELC degradation threshold of 3 kV CB JBS diodes and VDMOSFETs compared with the SELC degradation threshold of 3.3 kV Planar PiN diode and VDMOSFETs after [24]. Both devices were tested at TAMU Cyclotron Facility using the same heavy-ions and total fluence during each run.

Further classification of the safe operating area gives the region of SELC degradation shown in Figs. 4-9 (in yellow and orange). For MOSFETs, the degradation behavior can be further classified into two distinct regions as shown in Figs. 7-9: (i) Degradation I (shown in yellow) where the drain-gate leakage is dominant with $\Delta I_D = \Delta I_G$ and (ii) Degradation II (shown in orange) where the drain-source leakage current is dominant with $\Delta I_D >> \Delta I_G$. Similar findings were reported for 1.2 kV SiC MOSFETs in [25-28]. Except for irradiation with the lightest ion (neon), all planar and CB MOSFETs exhibited these two distinct modes of degradation.

To understand the mechanisms of failure in these devices, it is essential to understand the device response under different bias conditions at a particular LET. In Fig. 4, the lowest observed values of the SEB and SELC thresholds at a given LET are normalized in terms of the avalanche breakdown voltages in the diodes, both CB and planar. Similarly, in Fig. 7, the lowest observed values of the SEB and SELC thresholds at a given LET are normalized in terms of the avalanche breakdown voltages in the MOSFETs, both CB and planar. The epitaxial region in the CB devices has a higher doping compared to the epitaxial region in the planar devices. Having higher epitaxial doping is expected to result in an overall lower SEE thresholds. However, as seen from Figs. 4 and 7, both CB diodes and MOSFETs have a proportionately higher percentage of SEE tolerance compared to the planar devices even though their epitaxial doping is 5× that of the planar devices. This

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improved radiation response is highly likely due to the presence of the buried layers in the CB devices which act as electric field dividers. This distribution of electric field is further explained in the TCAD modelling section.

In Fig. 5, the radiation response of a CB JBS diode is shown, irradiated with 15 MeV/u Ne ions, with an LET of 2.8 MeV/(mg/cm^2) in SiC, using a fluence of 10^6 ions/cm^2 for each ion beam exposure interval. The range of these Ne ions is 188.4 µm in SiC after 3 cm air gap, which means they are capable of penetrating all the way through the epitaxial region in the CB devices. The regions of charge collection, followed by SELC degradation and catastrophic SEB can be clearly seen in Fig. 5.

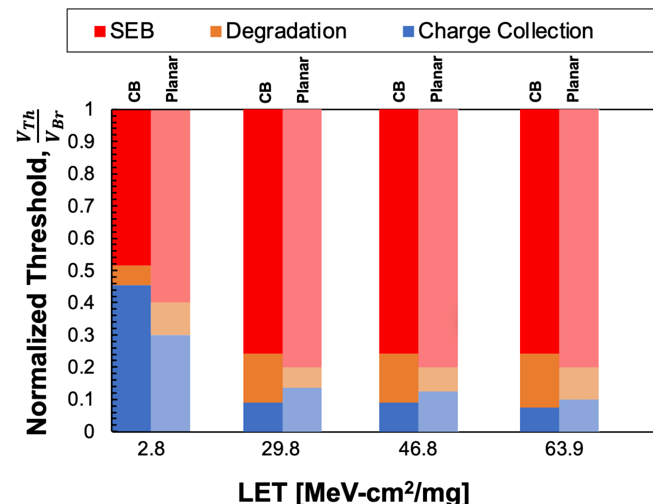

Fig. 4. SEB and SELC thresholds of 3 kV CB JBS diodes compared with the SEB and SELC thresholds of 3.3 kV Planar PiN diodes after [24]. Both devices were tested at TAMU Cyclotron Facility using the same heavy-ions and total fluence during each run. The figures show regions of (I) Charge Collection (in blue), (II) SELC degradation (in orange) and (III) catastrophic SEB (in red) in the diodes.

Coarse voltage steps were used to determine the true SEB threshold in these devices and fine voltage steps were used to understand the device behavior during non-catastrophic SELC degradation mode. The JBS CB diode is reverse-biased at 800 V and irradiated. The reverse-bias current is noted during the entire run which is halted when the fluence reaches 10^6 ions/cm^2. The bias is increased in steps of 200 V until the diode starts showing permanent increase in current, i.e., the mode of operation shifts from the charge collection to SELC degradation region. The reverse-bias is then incremented in steps of 100 V until the diode suffers catastrophic SEB at 1800 V. The SEB thresholds for the 3 kV CB devices were observed to be almost identical to the 3.3 kV planar devices throughout the entire experimental LET range, which is of utmost importance given their distinct structural differences. One of the key structural similarities between the planar and CB devices is that they both have the same epitaxial region thickness of 30 µm and are manufactured by the same vendor. As seen from Figs. 4 and 5, at lower LETs, the CB JBS diodes have higher SEB and SELC thresholds than the planar PiN diodes.

In Fig. 6, the radiation responses of two CB JBS diodes are shown, irradiated with 15 MeV/u Pr ions, with an LET of 63.9 MeV/(mg/cm^2) in SiC, using a fluence of 10^6 ions/cm^2 for each ion beam exposure interval. The range of these Pr ions is 79.4 µm in SiC after 3 cm air gap. The regions of charge collection, followed by SELC degradation and catastrophic SEB can be seen in Fig. 6 (a). The CB JBS diode starts showing SELC degradation at 250 V and had a catastrophic failure at 800 V, with the current reaching compliance value. The current compliance of the HVSMU was set to 4 mA. To verify whether the value of the SEB threshold determined from the first device is accurate, the second pristine diode is biased at the highest value at which the last diode became non-operational, i.e., 800 V and irradiated thereafter. The pristine device did not suffer catastrophic SEB at 800 V as shown in Fig. 6 (b). The current rises immediately to about 5-6 mA when the heavy-ion beam is turned on causing considerable temperature rise as monitored from the thermal camera. However, this does not alter the SEB sensitivity in the device, since this temperature

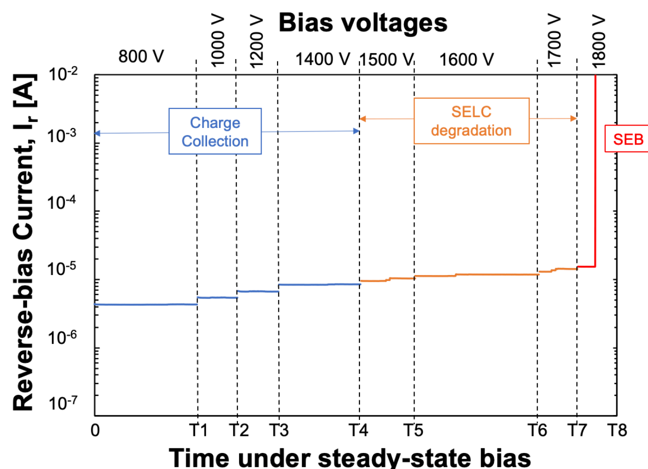

Fig. 5. Reverse-bias current profiles showing regions of (I) Charge Collection (in blue), (II) SELC degradation (in orange) and (III) catastrophic SEB (in red) in a 3 kV CB JBS diode, irradiated using 15 MeV/u Ne ion with an LET of 2.8 MeV/(mg/cm^2) in SiC, using a fluence of 10^6 ions/cm^2 for each ion beam exposure interval. The reverse bias voltage was set to 800 V between 0 to T1, 1000 V between T1 to T2, 1200 V between T2 to T3, 1400 V between T3 to T4, 1500 V between T4 to T5, 1600 V between T5 to T6, 1700 V between T6 to T7 and 1800 V between T7 to T8. Each time interval (0 through T1, and so on) represents an approximately 100 s irradiation run, followed by a finite time interval needed to stop the current run, switch the bias, and start the next run.

rise does not cause any physical damage to the device, and goes back to normal when the beam is turned off. Subsequently, when another identical diode is biased at 900 V (not shown), it suffers catastrophic SEB. Thus 800 V, which is the highest bias at which parametric failure is more likely than catastrophic failure, is considered the SEB threshold for the CB diodes at this LET. This is why multiple devices, at least 3 of each type, are irradiated at a particular LET for generating a reliable dataset.

In Fig. 8, the radiation response of a CB MOSFET is shown, irradiated with 15 MeV/u Ar ions, with an LET of 8.6 MeV/(mg/cm^2) in SiC, using a fluence of 10^6 ions/cm^2 for each ion beam exposure interval. The range of these Pr ions is 132.7 µm in SiC after 3 cm air gap. The regions of charge collection, followed by SELC degradation and catastrophic SEB can be clearly seen in Fig. 8. Both the drain and gate currents were monitored during the experiments to identify the degradation mechanisms in the device. The drain bias was incremented by steps of 200 V from 200 V to 1000 V. As seen in Fig. 8, at 600 V bias, the SELC degradation mode changes from degradation

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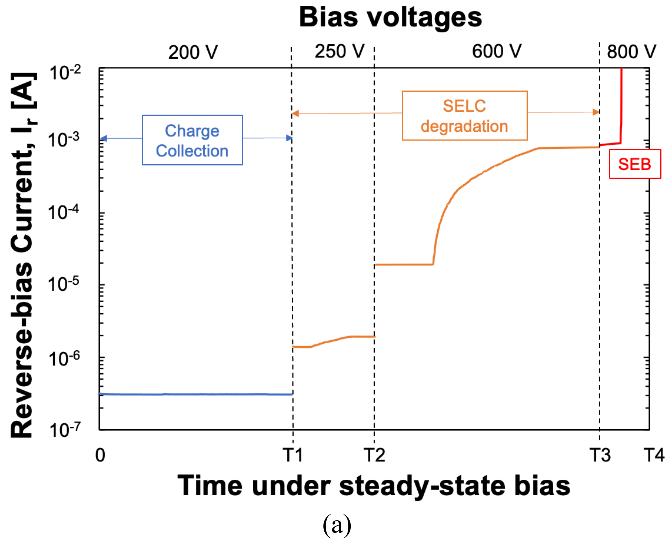
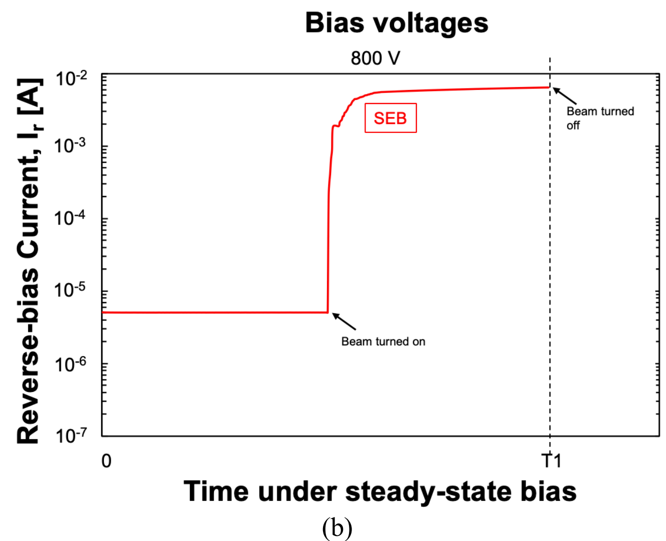
I (in yellow) to degradation II (in orange). Also, to note, the gate current decreases at the instant when the device fails catastrophically. This is most likely due to permanent damage caused to the gate terminal during irradiation. These two types of degradation are distinct from one another and are observed in both CB and planar MOSFETs. The drain-source leakage is more dominant ($\Delta I_D >> \Delta I_G$, shown in orange) at lower LETs as seen in Figs. 7-9 compared to the drain-gate leakage. At very low LETs, the drain-gate leakage dominance ($\Delta I_D = \Delta I_G$, shown in yellow) is inherently absent.



(a)



(b)

Fig. 6. Reverse-bias current profiles showing regions of (I) Charge Collection (in blue), (II) SELC degradation (in orange) and (III) catastrophic SEB (in red) in two 3 kV CB JBS diodes, irradiated using 15 MeV/u Pr ion with an LET of 63.9 MeV/(mg/cm^2) in SiC, using a fluence of 10^6 ions/cm^2 for each ion beam exposure interval. The bias voltage was set to 200 V between 0 to T1, 250 V between T1 to T2, 600 V between T2 to T3 and 800 V between T3 to T4 in (a) whereas the bias was 800 V between 0 to T1 in (b). Each time interval (0 through T1, and so on) represents an approximately 100 s irradiation run, followed by a finite time interval needed to stop the current run, switch the bias, and start the next run.

In Fig. 9, the radiation response of a CB MOSFET is shown, irradiated with 15 MeV/u Ag ions, with an LET of 46.8 MeV/(mg/cm^2) in SiC, using a fluence of 10^6 ions/cm^2 for each ion beam exposure interval. The range of these Ag ions is 75.6 µm in SiC after 3 cm air gap. The regions of charge collection, followed by SELC degradation and catastrophic SEB can be clearly seen in Fig. 9. Both the drain and gate currents were monitored during the experiments to identify the degradation mechanisms in the device. Coarse voltage steps were used to determine the true SEB threshold in these devices and fine voltage steps were used to understand the device behavior during non-catastrophic SELC degradation mode. A pre-degraded device suffers catastrophic SEB at a lower voltage compared to a pristine device, as seen in Fig. 9. A pristine

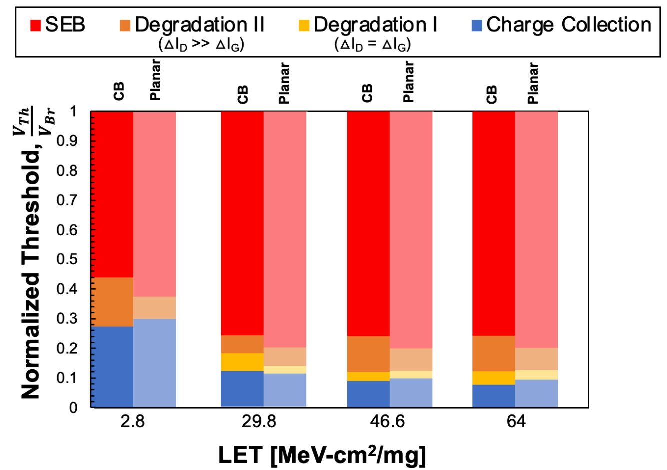


Fig. 7. SEB and SELC thresholds of 3 kV CB VDMOSFETs compared with the SEB and SELC thresholds of 3.3 kV Planar VDMOSFETs after [24]. Both devices were tested at TAMU Cyclotron Facility using the same heavy-ions and total fluence during each run. The figures show regions of (I) Charge Collection (in blue), (II) SELC degradation I (in yellow) where $\Delta I_D = \Delta I_G$, (III) SELC degradation II (in orange) where $\Delta I_D >> \Delta I_G$ and (IV) catastrophic SEB (in red) in the MOSFETs.

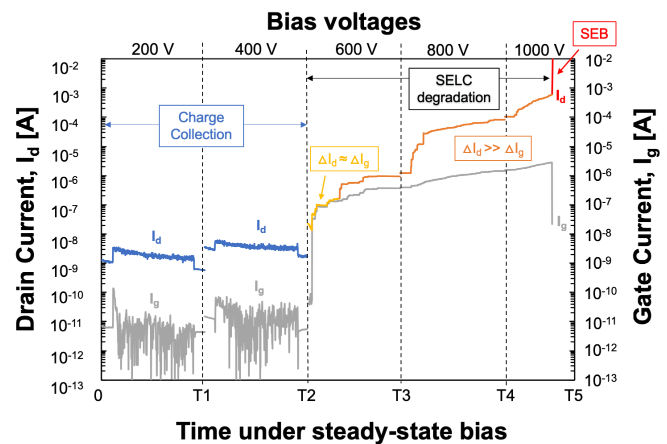


Fig. 8. Drain and gate current profiles showing regions of (I) Charge Collection (in blue), (II) SELC degradation I (in yellow) where $\triangle I_D = \triangle I_G$, (III) SELC degradation II (in orange) where $\triangle I_D >> \triangle I_G$ and (IV) catastrophic SEB (in red) in a 3 kV CB VDMOSFET, irradiated using 15 MeV/u Ar ion with an LET of 8.6 MeV/(mg/cm^2) in SiC, using a fluence of 10^6 ions/cm^2 for each ion beam exposure interval. The bias voltage (drain) was set to 200 V between 0 to T1, 400 V between T1 to T2, 600 V between T2 to T3, 800 V between T3 to T4 and 1000 V between T4 to T5 with the gate voltage at 0 V throughout the entire duration. Each time interval (0 through T1, and so on) represents an approximately 100 s irradiation run, followed by a finite time interval needed to stop the current run, switch the bias, and start the next run.

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device when irradiated using the same heavy-ion succumbs to SEB at 800 V as opposed to 700 V as seen in Fig. 9. The SEB thresholds for the 3 kV CB devices were observed to be almost identical to the 3.3 kV planar devices throughout the entire experimental LET range, which is of utmost importance given their distinct structural differences. One of the key structural similarities between the planar and CB devices is that they both have the same epitaxial region thickness of 30 µm and are manufactured by the same vendor. This means that the underlying mechanism that causes catastrophic SEB in a SiC power device will be mostly dependent on the thickness of this drift region in these devices, irrespective of the rest of the device structure, when irradiated with the same heavy-ion source, having the same LET and total fluence.

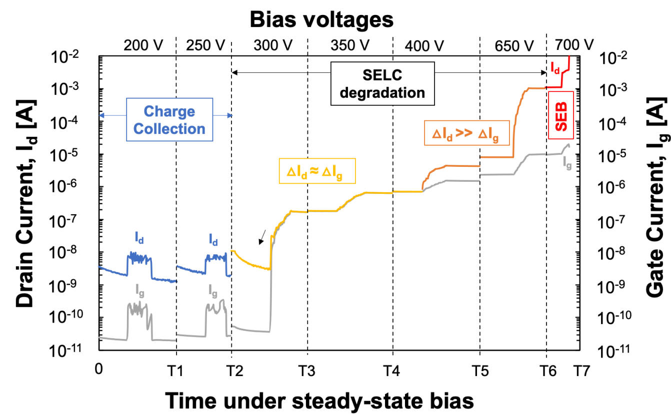

Fig. 9. Drain and gate current profiles showing regions of (I) Charge Collection (in blue), (II) SELC degradation I (in yellow) where $\triangle I_D = \triangle I_G$, (III) SELC degradation II (in orange) where $\triangle I_D >> \triangle I_G$ and (IV) catastrophic SEB (in red) in a 3 kV CB VDMOSFET, irradiated using 15 MeV/u Ag ion with an LET of 46.6 MeV/(mg/cm^2) in SiC, using a fluence of 10^6 ions/cm^2 for each ion beam exposure interval. The bias voltage (drain) was set to 200 V between 0 to T1, 250 V between T1 to T2, 300 V between T2 to T3, 350 V between T3 to T4, 400 V between T4 to T5, 650 V between T5 to T6, and 700 V between T6 to T7 with the gate voltage at 0 V throughout the entire duration. Each time interval (0 through T1, and so on) represents an approximately 10 s irradiation run, followed by a finite time interval needed to stop the current run, switch the bias, and start the next run.

IV. TCAD Modelling

3D TCAD models of 3 kV CB JBS diodes and VDMOSFETs were developed in the Synopsys Sentaurus suite of TCAD tools using version K-2015.06 [12-14, 26]. The 3 kV CB devices have an approximate epitaxial-layer thickness of 30 µm and an epitaxial doping of 10^{16} cm^3 and are based on the devices described in [19-21].

Comparing the two types of devices, the standard device exhibits the traditional triangular electric field profile in the epitaxial region, while the charge-balance layers act as voltage dividers, effectively spreading out, and reducing, the peak electric field at a given bias, as shown in Fig. 10. However, in the presence of the p-type bus pillars, the electric field magnitudes are greater relative to the standard device structure due to the distance between the base of the pillar and the highly-doped drain. Electric fields greater than 1 MV/cm are indicated in Fig. 10 (center) for both devices, and in the charge balanced devices, there is significantly more volume of the device that has an electric field greater than 1 MV/cm, relative to the standard device. High electric fields pre-irradiation typically result in more vulnerability to heavy ion strikes than lower electric fields. From a heavy ion perspective, an ion strike to the pillar would effectively shunt the source to the drain over a distance of 10 µm, which could potentially lead to the failure of the CB device at a lower voltage than the planar device. However, the experimental data show that the CB devices perform marginally better than the planar devices. This may be attributed to statistics, with the data only representing strikes to regions where no pillar is present. However, in contrast, the pillars and charge balance layers may actually serve to protect, or buffer, the device from the full impact of the ion due to the relative slowdown in device operational speed.

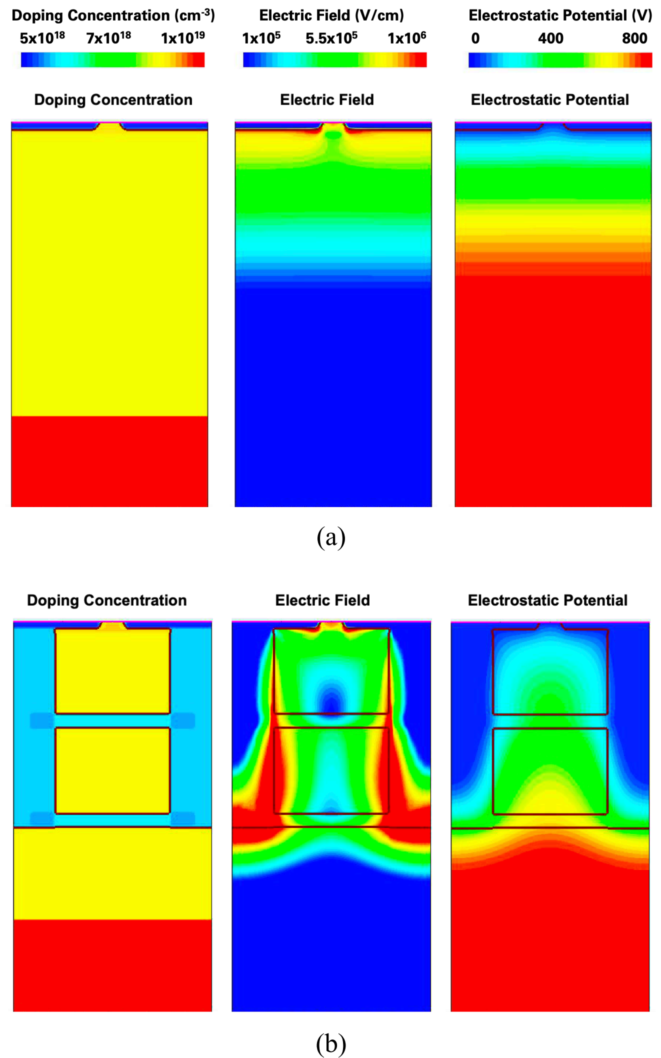

Fig. 10. 2-D contours of 3-D TCAD models of a planar (a) and a CB (b) SiC power devices. In both (a) and (b), the left image represents the doping concentration (cm^{-3}), the central image represents the absolute electric field (V*cm^{-1}) and the right image represents the electrostatic potential (V). Both the devices were at a bias of 800 V.

Increased electric fields do not necessarily indicate damage, and if the ion does hit a pillar, ion-induced current may have dissipated, or spread out, sufficiently that the surface metal is not impacted. In the planar device, much of the ion-induced current is at the top of the device, right near the source contact. In the CB devices, this current is spread out over at least the height of the pillar, which is about 20 µm. It is possible that the

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effects of heavy-ion irradiation happen sufficiently far away from the metal contact that the CB device performs overall better than the planar devices.

V. Discussion

The charge-balanced devices have an expitaxial region that is divided into three n-type 10 µm thick layers with doping concentration of 10^{16} cm^{-3}. The planar devices, on the other hand, contain a contiguous 30 µm thick epitaxial layer with doping concentration of 2×10^{15} cm^{-3}. The epitaxial doping is higher in the CB devices, but the charge balance layers and the pillars maintain the breakdown voltage by smoothing the electric field. To leverage some of their superior electrical performance as well as understand their operational reliability under extreme environment conditions, researchers have recently started investigating commercial SiC device structures such as trench-gate devices [29]. In this paper, the SEE robustness of CB devices is compared with planar devices, and the CB devices are found to be relatively better (as a percentage of their respective breakdown voltage) for both diodes and MOSFETs, as shown in Figs. 4 and 7, respectively.

The CB structure results in a much slower operating device (in the nano to microsecond range). Catastrophic burnout and degradation usually happen within the order of a few hundred picoseconds, so the CB structure does not impact the results significantly from a time perspective. However, the higher epitaxial doping in the CB devices might have lowered the SEB threshold as compared to the planar devices, but the actual values obtained from the experiments are practically the same.

From a radiation perspective, an ion strike to the pillar could potentially lead to the failure of the CB device at a lower voltage than the planar device. However, the experimental data show that the CB devices perform marginally better than the planar devices. This might be because an ion never hit in the pillar region during experiment with the broad beam at TAMU Cyclotron. This is an interesting topic of future experiment with a microbeam study comparing the CB devices with the planar devices. Another possibility is that even if an ion does hit a pillar, high electric fields by themselves do not necessarily lead to failure, and by the time the ion-induced current has made its way all the way up the pillar and out the contact, it may have dissipated, or spread out, sufficiently that the surface metal is not impacted. In the planar device, all that current is in the top few hundred nanometers, right at the contact. In the CB devices, this current is spread out over at least the height of the pillar, which is about 20 µm. It is possible that the effects of heavy-ion irradiation happen sufficiently far away from the metal contact that the CB devices perform overall better than the planar devices.

VI. Conclusions

Heavy-ion induced SEB data indicate that the drift region in SiC power devices is one of the key factors in determining the threshold at which catastrophic SEB will occur [12]. Although the device structures of the planar and charge-balanced devices are different, they have very similar SEB thresholds when irradiated with the same heavy-ion at the same fluence. This indicates that the radiation response in vertical SiC power devices depends strongly on the thickness and composition of their drift region. Structural modifications in the CB devices provide improved electrical performance, but there is no significant difference in terms of radiation hardness. SELC degradation is considered less catastrophic compared to SEB and post-rad I-V sweeps indicate that some of the devices still function as a transistor or diode, even though they are often highly degraded due to SELC. Overall, the CB devices have a higher fractional margin for SEB threshold, along with the improved electrical performance whereas the planar devices are easier to fabricate leading to lower costs. Therefore, depending on the application (space or terrestrial), trade-off between these two types of devices can be made based on the above criteria.

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